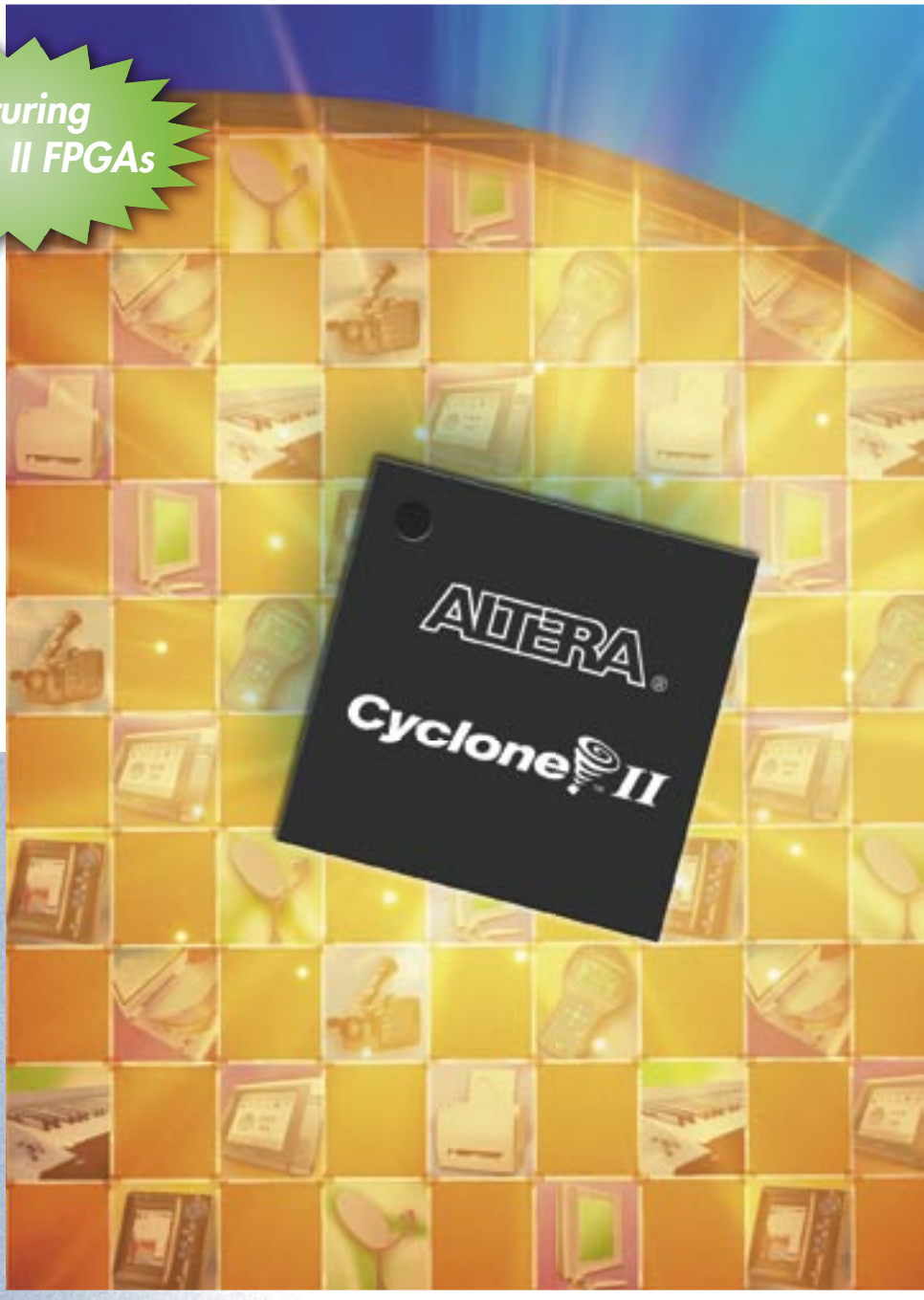
Cyclone Series

The Lowest-Cost FPGAs Ever



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Cyclone Series of FPGAs

Cyclone II Altera's low-cost Cyclone™ series provides the benefits of programmable logic at price points competitive with ASICs and ASSPs. Based on extensive input from hundreds of customers, Cyclone FPGAs were built from the ground up for low cost. These devices provide a high-volume solution with application-focused features such as embedded memory, external memory interfaces, and clock management circuitry.

Cyclone II FPGAs extend the series' logic density to more than 68K logic elements (LEs) at thirty percent lower cost than first-generation Cyclone devices. They also offer additional functionality: embedded multipliers, additional external memory interface support, and new I/O interface capabilities.

Cyclone II devices are manufactured on 300-mm wafers using Taiwan Semiconductor Manufacturing Company's (TSMC's) 90-nm low-k dielectric process, the same process as Altera's Stratix® II devices, thereby assuring rapid availability. By minimizing silicon area, Cyclone II devices can support complex digital systems on a single chip at a cost that rivals ASICs.

An Ideal ASIC Alternative

For applications that currently use low- to mid-density ASICs, Cyclone and Cyclone II FPGAs were designed to provide a perfect mix of density and features to provide a low-cost alternative to ASICs. The Cyclone series provides a flexible, risk-free option without up-front non-recurring engineering charges or minimum order quantities. With its low-cost solution unmatched by any other FPGA, Cyclone II devices offer advanced features such as embedded 18x18 multipliers for high-performance digital signal processing (DSP) applications and support for memory interfaces such as DDR2 (up to 334 Mbps) and QDRII (up to 668 Mbps).

Table 1 summarizes the features of the Cyclone series, and Table 2 details Cyclone II features. Figure 1 shows architectural highlights of the Cyclone II floorplan.

New Applications for FPGAs

With its higher densities, enhanced features, and lower prices, Cyclone II devices extend the use of FPGAs in applications that previously required low- to mid-density ASICs. Thousands of customers have used the first-generation Cyclone devices in the two years since their introduction, and the second generation is an attractive solution for an even wider range of applications.

Low-Cost Nios II Embedded Processors

Nios® II The low-cost Nios® II soft processor family features a general-purpose RISC CPU architecture designed to address a wide range of embedded applications in Altera® FPGAs for as little as $0.35 of logic. By taking advantage of the embedded multipliers in the Cyclone II family, the Nios II processors provide higher performance (more than 100 DMIPs) and greater efficiency than in previous low-cost FPGAs. Additionally, the Cyclone II family can incorporate multiple Nios II processors in a single device for increased system performance, better power efficiency, and greater cost savings. The three Nios II processors share a common 32-bit instruction set architecture and are 100 percent binary code compatible. Cyclone II devices support all members of the Nios II processor family:

- Nios II /f (fast): Highest performance, moderate logic usage
- Nios II /s (standard): High performance, low logic usage
- Nios II /e (economy): Lowest logic usage, lowest cost

Table 1. Cyclone Series Features

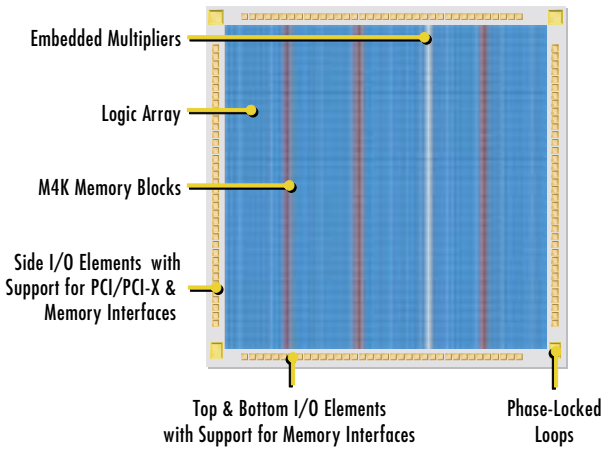
Parameter	Cyclone	Cyclone II
Core Voltage	1.5 V	1.2 V
I/O Voltage	3.3 V, 2.5 V, 1.8 V, 1.5 V	3.3 V, 2.5 V, 1.8 V, 1.5 V
Process Technology	130-nm	90-nm
Logic Elements	2,910 to 20,060	4,608 to 68,416
User I/O Pins	65 to 301	85 to 622
DSP Implementation	Logic Elements	Embedded 18x18 Multipliers[1]
M4K RAM Blocks	13 to 64	26 to 250
Phase-Locked Loops (PLLs)	1 to 2	2 to 4
I/O Standards Support	LVTTL, LVCMOS, PCI, SSTL, LVDS, RSDS	LVTTL, LVCMOS, PCI, PCI-X, SSTL, HSTL, LVDS, mini-LVDS, RSDS, LVPECL
External Memory Interfaces	SDR, DDR	SDR, DDR, DDR2, QDRII
Speed Grades	-6, -7, -8	-6, -7, -8

Note: [1] Each embedded 18x18 multiplier is configurable as two independent 9x9 multipliers.

Low-Cost Configuration Devices

To offer the lowest total solution cost, Altera created a low-cost serial configuration device family for the Cyclone series. On average, these serial configuration devices are priced for volume applications at as low as 10 percent the price of the corresponding Cyclone series device. Four serial configuration devices (1 Mbit, 4 Mbit, 16 Mbit, and 64 Mbit) are offered in space-saving 8-pin and 16-pin small-outline integrated circuit (SOIC) packages for the Cyclone series. To add even more value, any unused memory in these devices can be used for general-purpose storage, such as storing the software code for Nios II embedded processors.

Figure 1. Cyclone II Floorplan



Design Software

Cyclone series designs can be developed from concept to configuration using the free Quartus® II Web Edition software, available from the Altera web site. Cyclone and Cyclone II devices are also supported in Altera's flagship Quartus II software, the industry's most advanced development software. Quartus II software provides a comprehensive suite of synthesis, optimization, and verification tools in a unified design environment. In addition, designers can select, integrate, and evaluate intellectual property in Cyclone series designs in minutes within this easy-to-use software environment.

Table 2. Cyclone II Device Highlights

Feature	Benefit
Embedded Memory	The Cyclone II M4K embedded memory structure consists of 4,608 bits per block supporting multiple configurations, including true dual-port and single-port RAM, ROM, and first-in first-out (FIFO) buffers.
Embedded 18x18 Multipliers	Running at up to 250 MHz, Cyclone II embedded 18x18 multipliers can implement common DSP functions such as finite impulse response (FIR) filters, fast Fourier transforms (FFTs), and correlators. Each 18x18 multiplier can be used as two independent 9x9 multipliers. The multipliers eliminate the performance bottleneck in complex arithmetic calculations and significantly increase overall DSP system throughput.
I/O Standard Support	Cyclone II devices include LVTTL, LVCMOS, PCI, PCI-X, SSTL, and HSTL single-ended I/O standard support. For differential signaling requirements, Cyclone II devices support LVDS (up to 805 Mbps receiving and 622 Mbps transmitting), mini-LVDS, RSDS, LVPECL, SSTL, and HSTL system interfaces.
External Memory Interfaces	Cyclone II devices have dedicated interfaces to support high-speed memory devices including 167 MHz (668 Mbps) QDRII SRAM devices. Cyclone II devices also support SDR, DDR, and DDR2 interfaces.
Clock Management Circuitry	Up to sixteen low-skew, global clock networks span the entire device, fed by sixteen dedicated input clock pins. PLLs, each with three output taps, feature frequency synthesis and phase-shifting capabilities for complete system clock management on- and off-chip.
Nios II Embedded Processors	By supporting all Nios II soft processor cores, Cyclone series devices balance performance needs and device resource use for embedded processing applications.
Intellectual Property (IP)	IP functions that are developed, tested, and licensed by Altera and Altera Megafunction Partners Program (AMPP℠) partners can be implemented on Cyclone series devices. Available functions include PCI, memory controllers, and FFTs.
Serial Configuration Devices	Altera's serial configuration device family is designed to deliver the lowest cost configuration solution in the market. These devices can store configuration data while using remaining resources for general-purpose storage.

Table 3. Cyclone II Family Overview						
Feature	**EP2C5**	**EP2C8**	**EP2C20**	**EP2C35**	**EP2C50**	**EP2C70**
LEs	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM Blocks	26	36	52	105	129	250
Total RAM Bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded 18x18 Multipliers	13	18	26	35	86	150
PLLs	2	2	4	4	4	4
Maximum User I/O Pins	142	182	315	475	450	622
Available Packages	144-pin TQFP[1] 208-pin PQFP[2] 256-pin FBGA[3]	144-pin TQFP 208-pin PQFP 256-pin FBGA	256-pin FBGA 484-pin FBGA	484-pin FBGA 672-pin FBGA	484-pin FBGA 672-pin FBGA	672-pin FBGA 896-pin FBGA

Notes: [1] TQFP: thin quad flat pack, [2] PQFP: plastic quad flat pack, [3] FBGA: FineLine BGA® package

Table 4. Cyclone Family Overview					
Feature	**EP1C3**	**EP1C4**	**EP1C6**	**EP1C12**	**EP1C20**
LEs	2,910	4,000	5,980	12,060	20,060
M4K RAM Blocks	13	17	20	52	64
Total RAM Bits	59,904	78,336	92,160	239,616	294,912
PLLs	1	2	2	2	2
Maximum User I/O Pins	104	301	185	249	301
Available Packages	100-pin TQFP 144-pin TQFP	324-pin FBGA 400-pin FBGA	144-pin TQFP 240-pin PQFP 256-pin FBGA	240-pin PQFP 256-pin FBGA 324-pin FBGA	324-pin FBGA 400-pin FBGA

Contact Altera Today

The Cyclone series of FPGAs is a flexible, cost-effective solution for your low-cost volume-driven system designs. Learn more about Altera's newest low-cost FPGAs, Cyclone II devices, by visiting the Altera web site today at www.altera.com/cyclone2.

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