1. Cyclone III Device Family Overview

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Lowest System-Cost FPGAs

The Cyclone® III device family offered by Altera® is a cost-optimized, memory-rich FPGA family. Cyclone III FPGAs are built on Taiwan Semiconductor Manufacturing Company (TSMC)'s 65-nm low-power (LP) process technology with additional silicon optimizations and software features to minimize power consumption. With this third-generation in the Cyclone series, Altera broadens the number of high volume, cost-sensitive applications that can benefit from FPGAs.

This chapter contains the following sections:

Cyclone III Device Features

Cyclone III devices offer low-power consumption and increased system integration at reduced cost.

Reduced Cost

Cyclone III devices system costs are based on the following facts:

- Staggered I/O ring minimizes die area
- Wide range of low-cost packages
- Support for low-cost serial flash and commodity parallel flash devices for configuration

Lowest-Power 65-nm FPGA

Cyclone III devices are the lowest-power 65-nm FPGAs designed using TSMC's 65-nm LP process and Altera's power aware design flow. Cyclone III devices support hot-socketing operation; therefore, unused I/O banks can be powered down when the devices to which they are connected are turned off. Benefits of the Cyclone III device's low-power operation include:

- Extended battery life for portable and handheld applications
- Enabled operation in thermally challenged environments
- Eliminated or reduced cooling system costs

Increased System Integration

Cyclone III devices provide increased system integration by offering the following features:

- Logic density up to 119,088 logic elements (LEs) and memory up to 3.8 Mbits (for more information about Cyclone III device family features, refer to Table 1–1 on page 1–3)
- High memory-to-logic ratio for computation intensive applications
- Highest multiplier-to-logic ratio in the industry at every density; 340 MHz multiplier performance
- High I/O count, low- and mid-range density devices for user I/O constrained applications
- Up to four phase-locked loops (PLLs) provide robust clock management and synthesis for device clocks, external system clocks, and I/O interfaces
  - Up to five outputs per PLL
  - Cascadable to save I/Os, ease printed circuit board (PCB) routing, and reduce the number of external reference clocks needed
  - Dynamically reconfigurable to change phase shift, frequency multiplication/division, and input frequency in-system without reconfiguring the device
- Support for high-speed external memory interfaces including DDR, DDR2, SDR SDRAM, and QDRII SRAM at up to 400 megabits per second (Mbps)
  - Auto-calibrating physical layer (PHY) feature accelerates timing closure and eliminates variations over process, voltage and temperature (PVT) for DDR, DDR2, SDRAM, and QDRII SRAM interfaces
- Up to 535 user I/O pins arranged in eight I/O banks that support a wide range of industry I/O standards
  - Up to 875 Mbps receive and 840 Mbps transmit LVDS communications
  - Bus LVDS (BLVDS), LVDS, RSDS®, mini-LVDS and PPDS® differential I/O standards
  - Supported I/O standards include LVTTL, LVCMOS, SSTL, HSTL, PCI, PCI-X, LVPECL, LVDS, mini-LVDS, RSDS, and PPDS; PCI Express Base Specification 1.1 and Serial Rapid I/O are supported using external PHY devices
- Multi-value on-chip termination (OCT) support with calibration feature to eliminate variations over PVT
- Adjustable I/O slew rates to improve signal integrity
- Support for low-cost Altera serial flash and commodity parallel flash configuration devices from Intel
- Remote system upgrade feature without requiring an external controller
- Dedicated Cyclic Redundancy Code (CRC) checker circuitry to detect single event upset (SEU) conditions

- Nios® II embedded processors for Cyclone III devices offer low-cost and custom-fit embedded processing solutions
- Broad portfolio of pre-built and verified intellectual property cores from Altera and Altera Megafunction Partners Program (AMPP℠) partners

Table 1–1 displays Cyclone III device family features.

Table 1–1. Cyclone III FPGA Device Family Features

Feature	EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Logic Elements	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
Memory (Kbits)	414	414	504	594	1,134	2,340	2,745	3,888
Multipliers	23	23	56	66	126	156	244	288
PLLs	2	2	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20

All Cyclone III devices support vertical migration in the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. This allows designers to optimize density and cost as the design evolves.

Table 1–2 lists the Cyclone III device package options and user I/O pin counts. The highest I/O count in the family is delivered by the EP3C40.

Table 1–2. Cyclone III FPGA Package Options and I/O Pin Counts *(Note 1), (2), (3)*

Device	144-pin Plastic Enhanced Quad Flat Pack (EQFP) *(5)*	164-pin Micro FineLine Ball-Grid Array (MBGA)	240-pin Plastic Quad Flat Pack (PQFP)	256-pin FineLine Ball-Grid Array (FBGA)	256-pin Ultra FineLine Ball-Grid Array (UBGA) *(6)*	324-pin FineLine Ball-Grid Array (FBGA)	484-pin FineLine Ball-Grid Array (FBGA)	484-pin Ultra FineLine Ball-Grid Array (UBGA) *(6)*	780-pin FineLine Ball-Grid Array (FBGA)
EP3C5	94	106	—	182	182	—	—	—	—
EP3C10	94	106	—	182	182	—	—	—	—
EP3C16	84	92	160	168	168	—	346	346	—
EP3C25	82	—	148	156	156	215	—	—	—
EP3C40	—	—	128	—	—	195	331	331	535 *(4)*
EP3C55	—	—	—	—	—	—	327	327	377
EP3C80	—	—	—	—	—	—	295	295	429
EP3C120	—	—	—	—	—	—	283	—	531

Notes to Table 1–2:

(1) For more information about device packaging specifications, refer to the support section of the Altera website (www.altera.com/support/devices/packaging/specifications/pkg-pin/spe-index.html).

(2) The numbers are the maximum I/O counts (including clock input pins) supported by the device-package combination and can be affected by the configuration scheme selected for the device.

(3) All the packages are available in lead-free and leaded options.

(4) The EP3C40 device in the F780 package supports restricted vertical migration. Maximum user I/O is restricted to 510 I/Os if you enable migration to the EP3C120 and are using voltage referenced I/O standards. If you are not using voltage referenced I/O standards, the maximum number of I/Os can be increased.

(5) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity and not for thermal purposes.

(6) All the UBGA packages are supported by the Quartus® II software version 7.1 SP1 and later, with the exception of the UBGA packages of EP3C16, which is supported by the Quartus II software version 7.2.

Table 1–3 lists the Cyclone III FPGA package sizes.

Table 1–3. Cyclone III FPGA Package Sizes

Dimensions	144-pin EQFP	164-pin MBGA	240-pin PQFP	256-pin FBGA	256-pin UBGA	324-pin FBGA	484-pin FBGA	484-pin UBGA	780-pin FBGA
Pitch (mm)	0.5	0.5	0.5	1.0	0.8	1.0	1.0	0.8	1.0
Nominal Area (mm2)	484	64	1197	289	196	361	529	361	841
Length \ Width (mm \ mm)	22 \ 22	8 \ 8	34.6 \ 34.6	17 \ 17	14 \ 14	19 \ 19	23 \ 23	19 \ 19	29 \ 29
Height (mm)	1.60	1.40	4.10	1.55	2.20	2.20	2.60	2.20	2.60

Cyclone III devices are available in up to three speed grades: –6, –7, and –8 (–6 is the fastest).

Table 1–4 shows Cyclone III device speed grade offerings.

Table 1–4. Cyclone III Devices Speed Grades

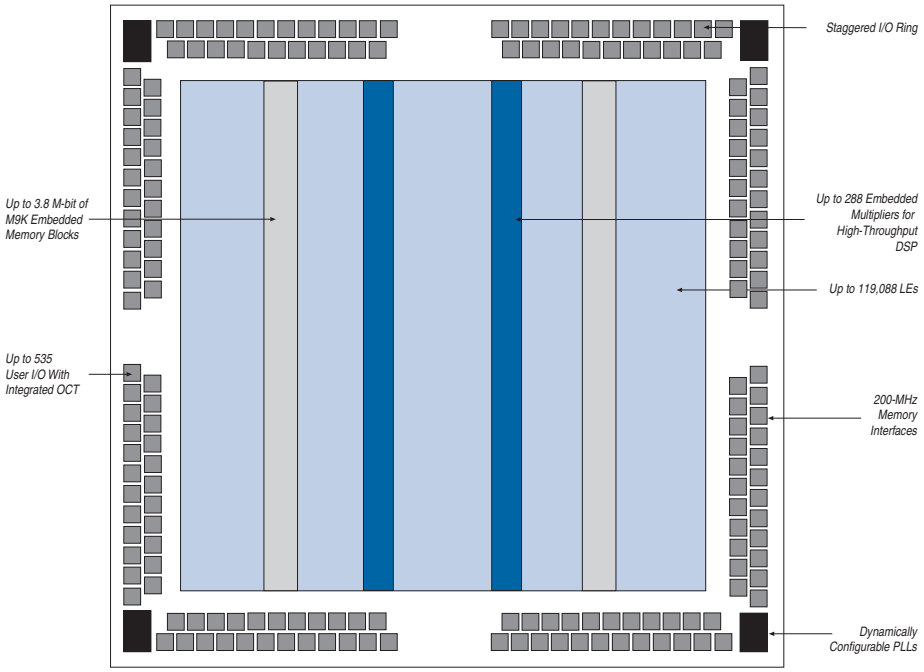
Device	144-pin EQFP	164-pin MBGA	240-pin PQFP	256-pin FBGA	256-pin UBGA	324-pin FBGA	484-pin FBGA	484-pin UBGA	780-pin FBGA
EP3C5	–7, –8	–7, –8	—	–6, –7, –8	–6, –7, –8	—	—	—	—
EP3C10	–7, –8	–7, –8	—	–6, –7, –8	–6, –7, –8	—	—	—	—
EP3C16	–7, –8	–7, –8	–8	–6, –7, –8	–6, –7, –8	—	–6, –7, –8	–6, –7, –8	—
EP3C25	–7, –8	—	–8	–6, –7, –8	–6, –7, –8	–6, –7, –8	—	—	—
EP3C40	—	—	–8	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	–6, –7, –8
EP3C55	—	—	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8
EP3C80	—	—	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8
EP3C120	—	—	—	—	—	—	–7, –8	—	–7, –8

Cyclone III Device Architecture

Cyclone III FPGAs include a customer-defined feature set optimized for cost-sensitive applications, and offer a wide range of density, memory, embedded multiplier, I/O, and packaging options. Cyclone III FPGAs support numerous external memory interfaces and I/O protocols common in high-volume applications.

Figure 1–1 shows a floor plan view of the Cyclone III device architecture.

Figure 1–1. Cyclone III Device Architecture Overview *(Note 1)*



Note to Figure 1–1:

(1) EP3C5 and EP3C10 have only two PLLs.

LEs and LABs

The logic array block (LAB) consists of 16 LEs and a LAB-wide control block. An LE is the smallest unit of logic in the Cyclone III device architecture. Each LE has four inputs, a 4-input look-up-table (LUT), a register, and output logic. The 4-input LUT is a function generator that can provide any function of four variables.

For more information about LEs and LABs, refer to the *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*.

MultiTrack Interconnect

In the Cyclone III device architecture, interconnections between LEs, LABs, M9K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure, which is a fabric of routing wires. The MultiTrack interconnect structure consists of performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II software automatically optimizes designs by placing the critical path on the fastest interconnects.

For more information about MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Memory Blocks

Each Cyclone III FPGA M9K memory block provides up to 9 Kbits of on-chip memory capable of operation up to 315 MHz. The embedded memory structure consists of columns of M9K memory blocks that can be configured as RAM, FIFO buffers, or ROM. Cyclone III memory blocks are optimized for applications, such as high-throughput packet processing, high-definition (HD) line buffers for video processing functions, and embedded processor program and data storage. The Quartus II software allows you to take advantage of M9K memory blocks by instantiating memory using a dedicated megafunction wizard, or by inferring memory directly from VHDL or Verilog source code.

Table 1–5. Cyclone III Memory Modes

Port Mode	Port Width Configuration
Single Port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32 and ×36
Simple Dual Port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32 and ×36
True Dual Port	×1, ×2, ×4, ×8, ×9, ×16 and ×18

For more information about memory blocks, refer to the *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*.

Embedded Multipliers and Digital Signal Processing Support

Cyclone III devices offer up to 288 embedded multiplier blocks and support one individual 18 × 18-bit multiplier per block, or two individual 9 × 9-bit multipliers per block. The Quartus II software includes megafunctions that are used to control the mode of operation of the embedded multiplier blocks based on user parameter settings. Multipliers can also be inferred directly from VHDL or Verilog source code.

In addition to embedded multipliers, Cyclone III FPGAs include a combination of on-chip resources and external interfaces that make them ideal for increasing performance, reducing system cost, and lowering the power consumption of digital signal processing (DSP) systems. Cyclone III FPGAs can be used alone or as DSP device co-processors to improve price-to-performance ratios of DSP systems.

Cyclone III FPGA DSP system design support includes the following features:

- DSP IP cores, which include:
  - Common DSP processing functions, such as finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
  - Suites of common video and image processing functions
- Complete reference designs for end-market applications
- DSP Builder interface tool between The MathWorks Simulink and MATLAB design environment, and the Quartus II software
- DSP development kits

For more information, refer to the *Embedded Multipliers* chapter in volume 1 of the *Cyclone III Device Handbook*.

I/O Features

All Cyclone III devices contain eight I/O banks. All I/O banks support the single-ended and differential I/O standards listed in Table 1–6.

Table 1–6. Cyclone III FPGA I/O Standards Support *(Note 1)*

Type	I/O Standard
Single-Ended I/O	■ LVTTL ■ LVCMOS ■ SSTL ■ HSTL ■ PCI ■ PCI-X
Differential I/O	■ SSTL ■ HSTL ■ LVPECL ■ BLVDS ■ LVDS ■ mini-LVDS ■ RSDS ■ PPDS

Note to Table 1–6:

(1) PCI Express and Serial Rapid I/O can be supported using an external PHY device.

The Cyclone III device I/O also supports programmable bus hold, programmable pull-up resistors, programmable delay, programmable drive strength, programmable slew rate control to optimize signal integrity, and hot socketing. Cyclone III devices support calibrated on-chip series termination (Rs OCT) or driver impedance matching (Rs) for single-ended I/O standards with one OCT calibration block per side.

For more information, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Clock Networks and PLLs

Cyclone III FPGAs include up to 20 global clock networks. Global clock signals can be driven from dedicated clock pins, dual-purpose clock pins, user logic, and PLLs. Cyclone III FPGAs include up to four PLLs with five outputs per PLL to provide robust clock management and synthesis. PLLs can be used for device clock management, external system clock management, and I/O interfaces.

Cyclone III PLLs can be dynamically reconfigured to enable auto-calibration of external memory interfaces while the device is in operation. This feature also enables support of multiple input source frequencies and corresponding multiplication, division, and phase shift requirements. PLLs in Cyclone III devices can be cascaded to generate up to ten internal clocks and two external clocks on output pins from a single external clock source.

For more PLL specifications and information, refer to the *DC and Switching Characteristics* and the *Clock Networks and PLLs* chapters in the *Cyclone III Device Handbook*.

High-Speed Differential Interfaces

Cyclone III FPGAs support high-speed differential interfaces, such as BLVDS, LVDS, mini-LVDS, RSDS, and PPDS. These high-speed I/O standards in Cyclone III FPGAs are ideal for low-cost applications by providing high data throughput using a relatively small number of I/O pins. All device I/O banks contain LVDS receivers that operate up to 875 Mbps data rates. Dedicated differential output drivers on the left and right I/O banks can transmit up to 840 Mbps data rates without the need for any external resistors to save board space and simplify PCB routing. Top and bottom I/O banks support differential transmit functionality with the addition of an external resistor network up to 640 Mbps data rates.

For more information, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

Auto-Calibrating External Memory Interfaces

Cyclone III devices support common memory types including DDR, DDR2, SDR SDRAM, and QDRII SRAM. The DDR2 SDRAM memory interfaces support data rates of up to 400 Mbps. Memory interfaces are supported on all sides of the Cyclone III FPGA. The Cyclone III FPGA contains features such as on-chip termination, DDR output registers, and 8- to 36-bit programmable `DQ` group widths to enable rapid and robust implementation of different memory standards.

An auto-calibrating megafunction is available in the Quartus II software for DDR and QDR memory interface PHYs. The megafunction is optimized to take advantage of the Cyclone III I/O structure, simplify timing closure requirements, and take advantage of the Cyclone III PLL dynamic reconfiguration feature to calibrate over process, voltage, and temperature changes.

For more information, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

Quartus II Software Support

The Quartus II software is the leading design software for performance and productivity. It is the industry's only complete design solution for CPLDs, FPGAs, and structured ASICs. The Quartus II software includes an integrated development environment to accelerate system-level design and seamless integration with leading third-party software tools and flows. Cyclone III FPGAs are supported by both the subscription and free Quartus II Web Edition software.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Nios II Embedded Processor

Cyclone III devices support the Nios® II embedded processor, which allows you to implement custom-fit embedded processing solutions. Cyclone III devices can also expand the peripheral set, memory, I/O, or performance of embedded processors. Single or multiple Nios II embedded processors can be designed into a Cyclone III device to provide additional co-processing power, or even replace existing embedded processors in your system. Using Cyclone III and Nios II together allows for low-cost, high-performance embedded processing solutions, which in turn allows you to extend your product's life cycle and improve time-to-market over standard product solutions.

For more information about the Nios II embedded processor, refer to *Nios II Embedded Processor Design Examples*.

Configuration

Cyclone III devices use SRAM cells to store configuration data. Configuration data is downloaded to Cyclone III devices each time the device powers up. Low-cost configuration options include Altera EPCS family serial flash devices, as well as parallel flash configuration options using commodity Intel devices. These options provide flexibility for general-purpose applications and the ability to meet specific configuration and wake-up time requirements of applications, such as the 100 ms requirement in many automotive applications. Wake-up time can be adjusted by choosing a configuration option and selecting a fast or standard power-on-reset time.

For more information, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

Remote System Upgrades

Cyclone III devices offer remote system upgrades without an external controller. Remote system upgrade capability in Cyclone III devices allows deployment of system upgrades from a remote location. Soft logic (either the Nios II embedded processor or user logic) used in a Cyclone III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting back to a safe configuration image, and provides error status information. This feature supports serial and parallel flash configuration topologies.

For more information, refer to the *Remote System Upgrade* chapter in volume 1 of the *Cyclone III Device Handbook*.

Hot Socketing and Power-On-Reset

Cyclone III devices feature hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of external devices. You can insert or remove a board populated with one or more Cyclone III devices during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature allows you to use FPGAs on PCBs that also contain a mixture of 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V devices. The Cyclone III device's hot socketing feature eliminates power-up sequence requirements for other devices on the board for proper FPGA operation.

For more information, refer to the *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*.

SEU Mitigation

Cyclone III devices offer built-in error detection circuitry to detect data corruption due to soft errors in the configuration random-access memory cells. This feature allows all CRAM contents to be read and verified to match a configuration-computed CRC value. The Quartus II software activates the Cyclone III built-in 32-bit CRC checker.

For more information, refer to the *SEU Mitigation* chapter in volume 1 of the *Cyclone III Device Handbook*.

JTAG Boundary Scan Testing

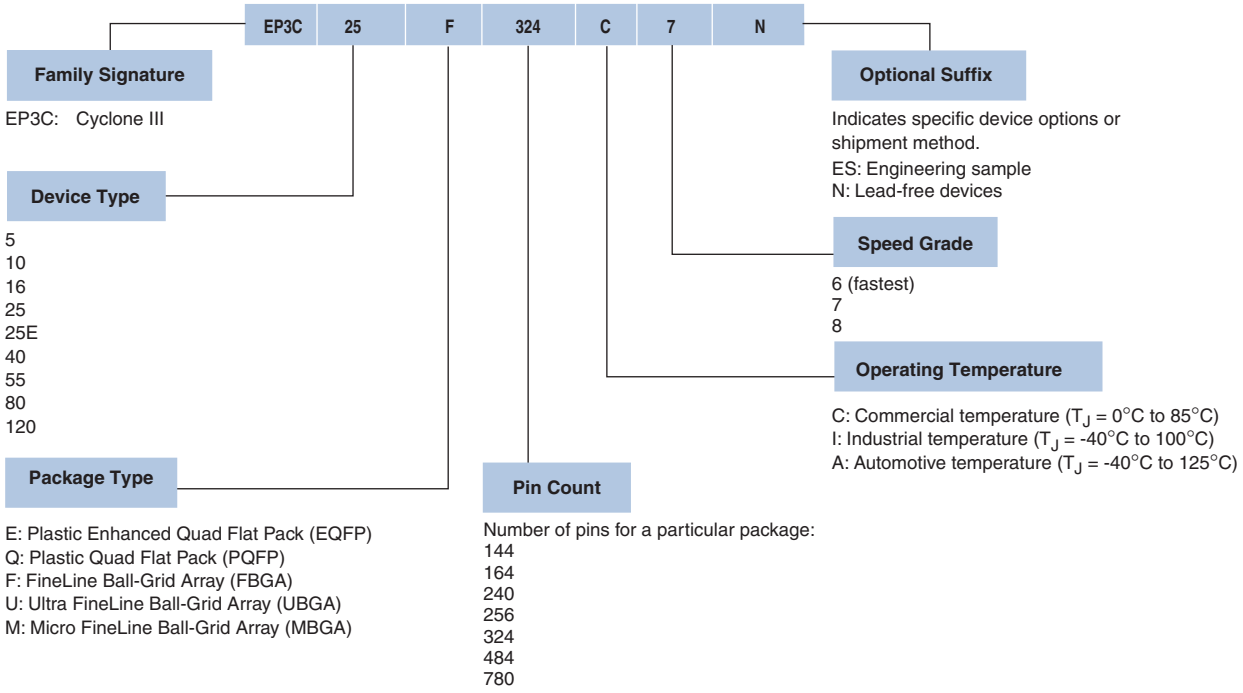
Cyclone III devices support the JTAG IEEE Std. 1149.1 specification. The boundary-scan test (BST) architecture offers the capability to test pin connections without using physical test probes, and captures functional data while a device is operating normally. Boundary-scan cells in the Cyclone III device can force signals onto pins or capture data from pins or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for Cyclone III device in-circuit reconfiguration (ICR).

For more information, refer to *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.

Reference and Ordering Information

Figure 1–2 describes the ordering codes for Cyclone III devices.

Figure 1–2. Cyclone III Device Packaging Ordering Information



For more package information about Cyclone III devices, refer to *Package Information for Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

Referenced Documents

This chapter references the following documents:

- *Clock Networks and PLLs* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Embedded Multipliers* chapter in volume 1 of the *Cyclone III Device Handbook*

- *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Quartus II Handbook*
- *Nios II Embedded Processor Design Examples*
- *Package Information for Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Remote System Upgrade* chapter in volume 1 of the *Cyclone III Device Handbook*
- *SEU Mitigation* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 1–7 shows the revision history for this chapter.

Table 1–7. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
October 2008 v1.3	■ Updated "Increased System Integration" section ■ Updated "Memory Blocks" section ■ Updated chapter to new template	—
May 2008 v1.2	■ Added 164-pin Micro FineLine Ball-Grid Array (MBGA) details to Table 1–2, Table 1–3 and Table 1–4 ■ Updated Figure 1–2 with automotive temperature information ■ Updated "Increased System Integration" section, Table 1–6, and "High-Speed Differential Interfaces" section with BLVDS information	Added 164-pin Micro FineLine Ball-Grid Array (MBGA), automotive temperature, and BLVDS information.

Table 1–7. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	■ Removed the text "Spansion" in "Increased System Integration" and "Configuration" sections ■ Removed trademark symbol from "MultiTrack" in "MultiTrack Interconnect" ■ Removed registered trademark symbol from "Simulink" and "MATLAB" from "Embedded Multipliers and Digital Signal Processing Support" section ■ Added chapter TOC and "Referenced Documents" section	—
March 2007 v1.0	Initial release.	—

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