1. DC and Switching Characteristics

CIII52001-2.2

Electrical Characteristics

Operating Conditions

When Cyclone® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone III devices, system designers must consider the operating requirements in this document. Cyclone III devices are offered in commercial, industrial, and automotive grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades. Industrial and automotive devices are offered only in –7 speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with "C" prefix, industrial with "I" prefix, and automotive with "A" prefix. Commercial devices are therefore indicated as C6, C7, and C8 per respective speed grades. Industrial and automotive devices are indicated as I7 and A7, respectively.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device. All parameters representing voltages are measured with respect to ground.

Table 1–1. Cyclone III Device Absolute Maximum Ratings *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic	–0.5	1.8	V
V_{CCIO}	Supply voltage for output buffers	–0.5	3.9	V
V_{CCA}	Supply (analog) voltage for PLL regulator	–0.5	3.75	V
V_{CCD_PLL}	Supply (digital) voltage for PLL	–0.5	1.8	V
V_I	DC input voltage	–0.5	3.95	V
I_{OUT}	DC output current, per pin	–25	40	mA
V_{ESDHBM}	Electrostatic discharge voltage using the human body model	NA	±2000	V
V_{ESDCDM}	Electrostatic discharge voltage using the charged device model	NA	±500	V
T_{STG}	Storage temperature	–65	150	°C

Table 1–1. Cyclone III Device Absolute Maximum Ratings *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
T_J	Operating junction temperature	–40	125	°C

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 10.74% over the lifetime of the device; for device lifetime of 10 years, this amounts to 10.74/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame *(Note 1)*

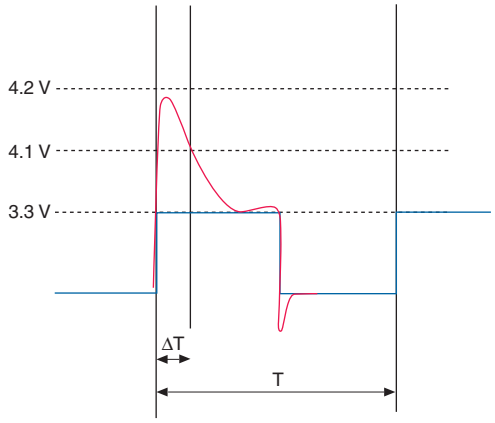
Symbol	Parameter	Condition	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	V_i = 3.95 V	100	%
		V_i = 4.0 V	95.67	%
		V_i = 4.05 V	55.24	%
		V_i = 4.10 V	31.97	%
		V_i = 4.15 V	18.52	%
		V_i = 4.20 V	10.74	%
		V_i = 4.25 V	6.23	%
		V_i = 4.30 V	3.62	%
		V_i = 4.35 V	2.1	%
		V_i = 4.40 V	1.22	%
		V_i = 4.45 V	0.71	%
		V_i = 4.50 V	0.41	%
		V_i = 4.60 V	0.14	%
		V_i = 4.70 V	0.047	%

Note to Table 1–2:

(1) Figure 1–1 shows the methodology to determine the overshoot duration. In the example in Figure 1–1, overshoot voltage is shown in red and is present on the Cyclone III input pin at over 4.1 V but below 4.2 V. From Table 1–1, for an overshoot of 4.1 V, the percentage of high time for the overshoot can be as high as 31.97% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1 shows the way to determine the overshoot duration.

Figure 1–1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone III devices. The steady-state voltage and current values expected from Cyclone III devices are provided in Table 1–3. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions *(Note 1)*, *(2)* (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} *(3)*	Supply voltage for internal logic	—	1.15	1.2	1.25	V
V_{CCIO} *(3)*, *(7)*	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} *(3)*	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} *(3)*	Supply (digital) voltage for PLL	—	1.15	1.2	1.25	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature *(6)*	–40	—	125	°C
		For automotive use	–40	—	125	°C

Table 1–3. Recommended Operating Conditions *(Note 1)*, *(2)* (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramptime	Standard POR *(4)*	50 µs	—	50 ms	—
		Fast POR *(5)*	50 µs	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1–3:

(1) V_{CCIO} for all I/O banks should be powered up during device operation. All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(2) V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead.

(3) The V_{CC} must rise monotonically.

(4) POR time for Standard POR ranges between 50–200 ms. Each individual power supply should reach the recommended operating range within 50 ms.

(5) POR time for Fast POR ranges between 3–9 ms. Each individual power supply should reach the recommended operating range within 3 ms.

(6) The Cyclone III I7 devices support extended operating junction temperature up to 125°C (usual range is –40°C to 100°C). When using I7 devices at the extended junction temperature ranging from –40°C to 125°C, select C8 as the target device when designing in the Quartus® II software. The Cyclone III I7 devices meet all C8 timing specifications when I7 devices operate beyond 100°C and up to 125°C.

(7) All input buffers are powered by the V_{CCIO} supply.

DC Characteristics

This section lists the I/O leakage currents, pin capacitance, on-chip termination tolerance, and bus hold specifications for Cyclone III devices.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Excel-based Early Power Estimator to get the supply current estimates for your design.

Table 1–4 lists I/O pin leakage current for Cyclone III devices.

Table 1–4. Cyclone III I/O Pin Leakage Current *(Note 1)*, *(2)* (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	–10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J= 25°C	EP3C5	1.7	*(3)*	mA
			EP3C10	1.7		mA
			EP3C16	3.0		mA
			EP3C25	3.5		mA
			EP3C40	4.3		mA
			EP3C55	5.2		mA
			EP3C80	6.5		mA
			EP3C120	8.4		mA

Table 1–4. Cyclone III I/O Pin Leakage Current *(Note 1)*, *(2)* (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCA0}	V_{CCA} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25°C	EP3C5	11.3	*(3)*	mA
			EP3C10	11.3		mA
			EP3C16	11.4		mA
			EP3C25	18.4		mA
			EP3C40	18.6		mA
			EP3C55	18.7		mA
			EP3C80	18.9		mA
			EP3C120	19.2		mA
I_{CCD_PLL0}	V_{CCD_PLL} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25°C	EP3C5	4.1	*(3)*	mA
			EP3C10	4.1		mA
			EP3C16	8.2		mA
			EP3C25	8.2		mA
			EP3C40	8.2		mA
			EP3C55	8.2		mA
			EP3C80	8.2		mA
			EP3C120	8.2		mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25°C	EP3C5	0.6	*(3)*	mA
			EP3C10	0.6		mA
			EP3C16	0.9		mA
			EP3C25	0.9		mA
			EP3C40	1.3		mA
			EP3C55	1.3		mA
			EP3C80	1.3		mA
			EP3C120	1.2		mA

Notes to Table 1–4:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

(3) Maximum values depend on the actual T_J and design utilization. Refer to the Excel-based PowerPlay Early Power Estimator (available at www.altera.com/support/devices/estimator/cy3-estimator/cy3-power_estimator.html) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to "Power Consumption" on page 1–13 for more information.

Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–5 lists bus hold specifications for Cyclone III devices. Also listed are input pin capacitances and on-chip termination tolerance specifications.

Table 1–5. Cyclone III Bus Hold Parameter *(Note 1)*

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1–5:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination (OCT) Specifications

Table 1–6 lists variation of uncalibrated OCT across process, temperature, and voltage.

Table 1–6. Uncalibrated On-Chip Series Termination Specifications

Symbol	V_{CCIO} (V)	Resistance Tolerance		Unit
		Commercial Max	Industrial and Automotive Max	
Series Termination without calibration	3.0	±30	±40	%
	2.5	±30	±40	%
	1.8	+40	±50	%
	1.5	+50	±50	%
	1.2	+50	±50	%

OCT calibration is automatically performed at power-up for OCT enabled I/Os.

Table 1–7 lists the OCT calibration accuracy at power-up.

Table 1–7. On-Chip Series Termination Power-Up Calibration Specifications

Symbol	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Max	Industrial and Automotive Max	
Series Termination with power-up calibration	3.0	±10	±10	%
	2.5	±10	±10	%
	1.8	±10	±10	%
	1.5	±10	±10	%
	1.2	±10	±10	%

Table 1–8 lists the percentage change of the OCT resistance with voltage and temperature. Use Table 1–8 and Equation 1–1 to determine OCT variation after power-up calibration.

Table 1–8. On-Chip Termination Variation After Power-Up Calibration *(Note 1)*

Nominal Voltage	dR/dT (%ΔOhm/°C)	dR/dmV (%ΔOhm/mV)
3.0	0.262	–0.026
2.5	0.234	–0.039
1.8	0.219	–0.086
1.5	0.199	–0.136
1.2	0.161	–0.288

Note to Table 1–8:

(1) This table is needed to calculate the final OCT resistance with the variation of temperature and voltage.

Equation 1–1. *(Note 7), (8), (9), (10), (11), (12)*

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dmV \quad \text{——— (1)}$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \quad \text{——— (2)}$$

$$\text{For } \Delta R_x < 0;\ MF_x = 1/\ (|\Delta R_x|\ /100 + 1) \quad \text{——— (3)}$$

$$\text{For } \Delta R_x > 0;\ MF_x = \Delta R_x/100 + 1 \quad \text{——— (4)}$$

$$MF = MF_V \times MF_T \quad \text{——— (5)}$$

$$R_{final} = R_{initial} \times MF \quad \text{——— (6)}$$

Notes to Equation 1–1:

(1) ΔR_V is variation of resistance with voltage.
(2) ΔR_T is variation of resistance with temperature.
(3) dR/dT is the percentage change of resistance with temperature.
(4) dR/dmV is the percentage change of resistance with voltage.
(5) V_2 is final voltage.
(6) $/V_1$ is the initial voltage.
(7) T_2 is the final temperature.
(8) T_1 is the initial temperature.
(9) MF is multiplication factor.
(10) R_{final} is final resistance.
(11) $R_{initial}$ is initial resistance.

(12) Subscript × refers to both V and T.

For example, to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V,

$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$

$\Delta R_T = (85 - 25) \times 0.262 = 15.72$

Because ΔR_V is negative,

$MF_V = 1 / (3.83/100 + 1) = 0.963$

Because ΔR_T is positive,

$MF_T = 15.72/100 + 1 = 1.157$

$MF = 0.963 \times 1.157 = 1.114$

$R_{final} = 50 \times 1.114 = 55.71\ \Omega$

Pin Capacitance

Table 1–9 shows the Cyclone III device family pin capacitance.

Table 1–9. Cyclone III Device Pin Capacitance

Symbol	Parameter	Typical – QFP	Typical – FBGA	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	7	6	pF
C_{IOLR}	Input capacitance on left/right I/O pins	7	5	pF
C_{LVDSLR}	Input capacitance on left/right I/O pins with dedicated LVDS output	8	7	pF
C_{VREFLR} *(2)*	Input capacitance on left/right dual-purpose VREF pin when used as V_{REF} or user I/O pin	21	21	pF
C_{VREFTB} *(2)*	Input capacitance on top/bottom dual-purpose VREF pin when used as V_{REF} or user I/O pin	23 *(1)*	23 *(1)*	pF
C_{CLKTB}	Input capacitance on top/bottom dedicated clock input pins	7	6	pF
C_{CLKLR}	Input capacitance on left/right dedicated clock input pins	6	5	pF

Notes to Table 1–9:

(1) C_{VREFTB} for EP3C25 is 30 pF.

(2) When VREF pin is used as regular input or output, a reduced performance of toggle rate and t_{CO} is expected due to higher pin capacitance.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–10 lists the weak pull-up and pull-down resistor values for Cyclone III devices.

Table 1–10. Cyclone III Internal Weak Pull-Up/Weak Pull-Down Resistor *(Note 1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{_PU}$	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled	V_{CCIO} = 3.3 V ± 5% *(2)*, *(3)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ± 5% *(2)*, *(3)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ± 5% *(2)*, *(3)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ± 5% *(2)*, *(3)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ± 5% *(2)*, *(3)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ± 5% *(2)*, *(3)*	19	143	351	kΩ
$R_{_PD}$	Value of I/O pin pull-down resistor before and during configuration	V_{CCIO} = 3.3 V ± 5% *(4)*	6	19	30	kΩ
		V_{CCIO} = 3.0 V ± 5% *(4)*	6	22	36	kΩ
		V_{CCIO} = 2.5 V ± 5% *(4)*	6	25	43	kΩ
		V_{CCIO} = 1.8 V ± 5% *(4)*	7	35	71	kΩ
		V_{CCIO} = 1.5 V ± 5% *(4)*	8	50	112	kΩ

Notes to Table 1–10:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pin. Weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) $R_{_PU} = (V_{CCIO} – V_I)/I_{R_PU}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, $V_I = V_{CC}$ + 5% – 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, V_I = 0 V;
Maximum condition: 125°C; $V_{CCIO} = V_{CC}$ – 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.

(4) $R_{_PD} = V_I/I_{R_PD}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, V_I = 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = V_{CC}$ – 5%;
Maximum condition: 125°C; $V_{CCIO} = V_{CC}$ – 5%, $V_I = V_{CC}$ – 5%; in which V_I refers to the input voltage at the I/O pin.

Hot Socketing

Table 1–11 lists the hot-socketing specifications for Cyclone III devices.

Table 1–11. Cyclone III Hot-Socketing Specifications

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA ***(1)***

Note to Table 1–11:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

Schmitt Trigger Input

The Cyclone III device supports Schmitt trigger input on `TDI`, `TMS`, `TCK`, `nSTATUS`, `nCONFIG`, `nCE`, `CONF_DONE`, and `DCLK` pins. A Schmitt trigger introduces hysteresis to the input signal for improved noise immunity especially for signal with slow edge rate.

Table 1–12 lists the hysteresis specifications across supported V_{CCIO} range for Schmitt trigger inputs in Cyclone III devices.

Table 1–12. Hysteresis Specifications for Schmitt Trigger Input

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{SCHMITT}$	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3 V	200	—	—	mV
		V_{CCIO} = 2.5 V	200	—	—	mV
		V_{CCIO} = 1.8 V	140	—	—	mV
		V_{CCIO} = 1.5 V	110	—	—	mV

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone III devices.

Table 1–13 through Table 1–18 provide the Cyclone III device family I/O standard specifications.

For voltage referenced receiver input waveform and explanation of terms used in Table 1–13, refer to "Single-ended Voltage referenced I/O Standard" in "Glossary".

Table 1–13. Single-Ended I/O Standard Specifications *(Note 1)*

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} *(3)* (mA)	I_{OH} *(3)* (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL *(2)*	3.135	3.3	3.465	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS *(2)*	3.135	3.3	3.465	—	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL *(2)*	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0-V LVCMOS *(2)*	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5-V LVTTL and LVCMOS *(2)*	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2.0	1	–1
1.8-V LVTTL and LVCMOS	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5-V LVCMOS	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2-V LVCMOS	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
PCI and PCI-X	2.85	3.0	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	V_{CCIO} + 0.3	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	–0.5

Notes to Table 1–13:

(1) AC load CL = 10 pF.

(2) For more detail about interfacing Cyclone III devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL and LVCMOS I/O Systems*.

(3) Specified I_{OL} and I_{OH} are valid with the lowest current strength setting available for respective I/O standards. I_{OL} and I_{OH} values correspond to the selected current strength settings value. For example, current drive characteristics for 3.3-V LVTTL with 8 mA current strength setting are 8 mA (I_{OL}) and –8 mA (I_{OH}) at 0.45 V (V_{OL}) and 2.4 V (V_{OH}), respectively.

For an explanation of terms used in Table 1–14, refer to "Glossary".

Table 1–14. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) *(3)*		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 * V_{CCIO} *(1)*	0.5 * V_{CCIO} *(1)*	0.52 * V_{CCIO} *(1)*	—	0.5 * V_{CCIO}	—
				0.47 * V_{CCIO} *(2)*	0.5 * V_{CCIO} *(2)*	0.53 * V_{CCIO} *(2)*			

Notes to Table 1–14:

(1) Value shown refer to DC input reference voltage, $V_{REF(DC)}$.

(2) Value shown refer to AC input reference voltage, $V_{REF(AC)}$.

(3) V_{TT} of transmitting device must track V_{REF} of the receiving device.

Table 1–15. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

For more illustrations of receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

Table 1–16. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 – 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	$V_{CCIO}/2 – 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2 – 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 – 0.125$	—	$V_{CCIO}/2 + 0.125$

Table 1–17. Differential HSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 * V_{CCIO}	—	0.52 * V_{CCIO}	0.48 * V_{CCIO}	—	0.52 * V_{CCIO}	0.3	0.48 * V_{CCIO}

For an explanation of terms used in Table 1–18, refer to "Transmitter Output Waveform" in "Glossary".

Table 1–18. Differential I/O Standard Specifications (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) *(5)*			V_{OD} (mV) *(1)*			V_{OS} (V) *(1)*		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) *(2)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVPECL (Column I/Os) *(2)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						

Table 1–18. Differential I/O Standard Specifications (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) *(5)*			V_{OD} (mV) *(1)*			V_{OS} (V) *(1)*		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (Column I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) *(3)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
BLVDS (Column I/Os) *(3)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (Row I/Os) *(4)*	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) *(4)*	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os) *(4)*	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) *(4)*	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS® (Row I/Os) *(4)*	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) *(4)*	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–18:

(1) R_L range: 90 $\leq$ $R_L \leq$ 110 Ω.
(2) LVPECL input standard is only supported at clock input. Output standard is not supported.
(3) No fixed V_{IN}, V_{OD}, and V_{OS} specification for BLVDS. They are dependent on the system topology.
(4) Mini-LVDS, RSDS, and PPDS standards are only supported at output pins of Cyclone III devices.
(5) V_{IN} range: 0 V $\leq V_{IN} \leq$ 1.85 V.

Power Consumption

Altera offers two ways to estimate power for a design: the Excel-based Early Power Estimator and the Quartus II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the device to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides better quality estimates based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Cyclone III core and periphery blocks. These characteristics can be designated as **Preliminary** or **Final**, as indicated in the upper-right corner of a table. Each designation is defined as follows:

- **Preliminary:** Preliminary characteristics are created using simulation results, process data, and other known parameters.
- **Final:** Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

Core Performance Specifications

Clock Tree Specifications

Table 1–19 lists clock tree specifications for Cyclone III devices.

Table 1–19. Cyclone III Clock Tree Performance

Device	Performance			Unit
	C6	C7	C8	
EP3C5	500	437.5	402	MHz
EP3C10	500	437.5	402	MHz
EP3C16	500	437.5	402	MHz
EP3C25	500	437.5	402	MHz
EP3C40	500	437.5	402	MHz
EP3C55	500	437.5	402	MHz
EP3C80	500	437.5	402	MHz
EP3C120	*(1)*	437.5	402	MHz

Note to Table 1–19:

(1) EP3C120 offered in C7, C8, and I7 grades only.

PLL Specifications

Table 1–20 describes the Cyclone III PLL specifications when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), and the automotive junction temperature range (–40°Cto 125°C).

For more information about PLL block, refer to "PLL Block" in "Glossary".

Table 1–20. Cyclone III PLL Specifications *(Note 4)* (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} *(1)*	Input clock frequency	5	—	472.5	MHz
f_{INPFD}	PFD input frequency	5	—	325	MHz
f_{VCO} *(6)*	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER_CCJ}$ *(5)*	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	—	—	0.15	UI
	$F_{REF} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} (external clock output) *(1)*	PLL output frequency	—	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	—	—	472.5	MHz
	PLL output frequency (–7 speed grade)	—	—	450	MHz
	PLL output frequency (–8 speed grade)	—	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted)	—	—	1	ms
$t_{OUTJITTER_PERIOD_DEDCLK}$ *(3)*	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}$ *(3)*	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_PERIOD_IO}$ *(3)*	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ *(3)*	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 *(2)*	—	SCANCLK cycles

Table 1–20. Cyclone III PLL Specifications *(Note 4)* (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz

Notes to Table 1–20:

(1) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) With 100 MHz scanclk frequency.

(3) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

(4) V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(6) The V_{CO} frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Embedded Multiplier Specifications

Table 1–21 describes Cyclone III embedded multiplier specifications.

Table 1–21. Cyclone III Embedded Multiplier Specifications

Mode	Resources Used	Performance			Unit
	Number of Multipliers	C6	C7, I7, A7	C8	
9×9-bit multiplier	1	340	300	260	MHz
18×18-bit multiplier	1	287	250	200	MHz

Memory Block Specifications

Table 1–22 describes Cyclone III M9K memory block specifications.

Table 1–22. Cyclone III Memory Block Performance Specifications

Memory	Mode	Resources Used		Performance			
		LEs	M9K Memory	C6	C7, I7, A7	C8	Unit
M9K Block	FIFO 256×36	47	1	315	274	238	MHz
	Single-port 256×36	0	1	315	274	238	MHz
	Simple dual-port 256×36 CLK	0	1	315	274	238	MHz
	True dual port 512×18 single CLK	0	1	315	274	238	MHz

Configuration and JTAG Specifications

Table 1–23 lists Cyclone III configuration mode specifications.

Table 1–23. Cyclone III Configuration Mode Specifications

Programming Mode	DCLK F_{max}	Unit
Passive Serial (PS)	133	MHz
Fast Passive Parallel (FPP) *(1)*	100	MHz

Note to Table 1–23:

(1) EP3C40 and smaller family members support 133 MHz.

Table 1–24 lists the Cyclone III active configuration mode specifications.

Table 1–24. Cyclone III Active Configuration Mode Specifications

Programming Mode	DCLK Range	Unit
Active Parallel (AP)	20 – 40	MHz
Active Serial (AS)	20 – 40	MHz

Table 1–25 shows JTAG timing parameters and values for Cyclone III devices.

For more information, refer to "JTAG Waveform" in "Glossary".

Table 1–25. Cyclone III JTAG Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI *(1)*	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS *(1)*	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(1)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(1)*	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance *(1)*	—	15	ns
t_{JSSU}	Capture register setup time *(1)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Note to Table 1–25:

(1) The specification is shown for 3.3-V, 3.0-V, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port clock to output time is 16 ns.

Periphery Performance

High-Speed I/O Specification

Table 1–26 through Table 1–31 show the high-speed I/O timing for Cyclone III devices.

For definitions of high-speed timing specifications, refer to "Glossary".

Table 1–26. RSDS Transmitter Timing Specification *(Note 1), (2)*

Symbol	Modes	C6			C7, I7			C8, A7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	180	10	—	155.5	10	—	155.5	MHz
	×8	10	—	180	10	—	155.5	10	—	155.5	MHz
	×7	10	—	180	10	—	155.5	10	—	155.5	MHz
	×4	10	—	180	10	—	155.5	10	—	155.5	MHz
	×2	10	—	180	10	—	155.5	10	—	155.5	MHz
	×1	10	—	360	10	—	311	10	—	311	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	Mbps
	×8	80	—	360	80	—	311	80	—	311	Mbps
	×7	70	—	360	70	—	311	70	—	311	Mbps
	×4	40	—	360	40	—	311	40	—	311	Mbps
	×2	20	—	360	20	—	311	20	—	311	Mbps
	×1	10	—	360	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} *(3)*	—	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–26:

(1) Applicable for all dedicated (both denoted with "Adj." and "Sep." pintable location) and three-resistor RSDS transmitters.

(2) Dedicated RSDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6). Three-resistor RSDS transmitter is supported at the output pin of all I/O banks.

(3) t_{LOCK} is the time required for the PLL to lock from the end of device configuration.

Table 1–27. Single-Resistor RSDS Transmitter Timing Specification *(Note 1)*

Symbol	Modes	C6			C7, I7			C8, A7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	85	10	—	85	10	—	85	MHz
	×8	10	—	85	10	—	85	10	—	85	MHz
	×7	10	—	85	10	—	85	10	—	85	MHz
	×4	10	—	85	10	—	85	10	—	85	MHz
	×2	10	—	85	10	—	85	10	—	85	MHz
	×1	10	—	170	10	—	170	10	—	170	MHz
Device operation in Mbps	×10	100	—	170	100	—	170	100	—	170	Mbps
	×8	80	—	170	80	—	170	80	—	170	Mbps
	×7	70	—	170	70	—	170	70	—	170	Mbps
	×4	40	—	170	40	—	170	40	—	170	Mbps
	×2	20	—	170	20	—	170	20	—	170	Mbps
	×1	10	—	170	10	—	170	10	—	170	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} *(2)*	—	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–27:

(1) Single-resistor RSDS transmitter is supported at the output pin of all I/O banks.

(2) t_{LOCK} is the time required for the PLL to lock from the end of device configuration.

Table 1–28. Mini-LVDS Transmitter Timing Specification *(Note 1)*, *(2)* (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	200	10	—	155.5	10	—	155.5	MHz
	×8	10	—	200	10	—	155.5	10	—	155.5	MHz
	×7	10	—	200	10	—	155.5	10	—	155.5	MHz
	×4	10	—	200	10	—	155.5	10	—	155.5	MHz
	×2	10	—	200	10	—	155.5	10	—	155.5	MHz
	×1	10	—	400	10	—	311	10	—	311	MHz

Table 1–28. Mini-LVDS Transmitter Timing Specification *(Note 1)*, *(2)* (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	Mbps
	×8	80	—	400	80	—	311	80	—	311	Mbps
	×7	70	—	400	70	—	311	70	—	311	Mbps
	×4	40	—	400	40	—	311	40	—	311	Mbps
	×2	20	—	400	20	—	311	20	—	311	Mbps
	×1	10	—	400	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} *(3)*	—	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–28:

(1) Applicable for all dedicated (both denoted with "Adj." and "Sep." pintable location) and three-resistor mini-LVDS transmitter.

(2) Dedicated mini-LVDS transmitter is only supported at the output pin of Row I/O (Banks 1, 2, 5, and 6). Three-resistor mini-LVDS transmitter is supported at the output pin of all I/O banks.

(3) t_{LOCK} is the time required for the PLL to lock from the end of device configuration.

Table 1–29. Dedicated LVDS Transmitter Timing Specification *(Note 1)*, *(3)* (Part 1 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		Unit
		Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	10	420	10	370	10	320	MHz
	×8	10	420	10	370	10	320	MHz
	×7	10	420	10	370	10	320	MHz
	×4	10	420	10	370	10	320	MHz
	×2	10	420	10	370	10	320	MHz
	×1	10	420	10	402.5	10	402.5	MHz
HSIODR	×10	100	840	100	740	100	640	Mbps
	×8	80	840	80	740	80	640	Mbps
	×7	70	840	70	740	70	640	Mbps
	×4	40	840	40	740	40	640	Mbps
	×2	20	840	20	740	20	640	Mbps
	×1	10	420	10	402.5	10	402.5	Mbps
t_{DUTY}	—	45	55	45	55	45	55	%

Table 1–29. Dedicated LVDS Transmitter Timing Specification *(Note 1)*, *(3)* (Part 2 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		Unit
		Min	Max	Min	Max	Min	Max	
TCCS	—	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	ps
t_{LOCK} *(2)*	—	—	1	—	1	—	1	ms

Notes to Table 1–29:

(1) Dedicated LVDS transmitter is only supported at the output pin of Row I/O (Banks 1, 2, 5, and 6).

(2) t_{LOCK} is the time required for the PLL to lock from the end of device configuration.

(3) Applicable for all dedicated transmitters (both denoted with "Adj." and "Sep." pintable location).

Table 1–30. Three-Resistor LVDS Transmitter Timing Specification *(Note 1)*

Symbol	Modes	C6		C7, I7		C8, A7		Unit
		Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	10	320	10	320	10	275	MHz
	×8	10	320	10	320	10	275	MHz
	×7	10	320	10	320	10	275	MHz
	×4	10	320	10	320	10	275	MHz
	×2	10	320	10	320	10	275	MHz
	×1	10	402.5	10	402.5	10	402.5	MHz
HSIODR	×10	100	640	100	640	100	550	Mbps
	×8	80	640	80	640	80	550	Mbps
	×7	70	640	70	640	70	550	Mbps
	×4	40	640	40	640	40	550	Mbps
	×2	20	640	20	640	20	550	Mbps
	×1	10	402.5	10	402.5	10	402.5	Mbps
t_{DUTY}	—	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	ps
t_{LOCK} *(2)*	—	—	1	—	1	—	1	ms

Notes to Table 1–30:

(1) Three-resistor LVDS transmitter is supported at the output pin of all I/O banks.

(2) t_{LOCK} is the time required for the PLL to lock from the end of device configuration.

Table 1–31. LVDS Receiver Timing Specification *(Note 1)*

Symbol	Modes	C6		C7, I7		C8, A7		Unit
		Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	MHz
	×8	10	437.5	10	370	10	320	MHz
	×7	10	437.5	10	370	10	320	MHz
	×4	10	437.5	10	370	10	320	MHz
	×2	10	437.5	10	370	10	320	MHz
	×1	10	437.5	10	402.5	10	402.5	MHz
HSIODR	×10	100	875	100	740	100	640	Mbps
	×8	80	875	80	740	80	640	Mbps
	×7	70	875	70	740	70	640	Mbps
	×4	40	875	40	740	40	640	Mbps
	×2	20	875	20	740	20	640	Mbps
	×1	10	437.5	10	402.5	10	402.5	Mbps
SW	—	—	400	—	400	—	400	ps
Input jitter tolerance	—	—	500	—	500	—	550	ps
t_{LOCK} *(2)*	—	—	1	—	1	—	1	ms

Notes to Table 1–31:

(1) Dedicated LVDS receiver is supported at all banks.

(2) t_{LOCK} is the time required for the PLL to lock from the end of device configuration.

External Memory Interface Specifications

Cyclone III devices support external memory interfaces up to 200 MHz. Cyclone III external memory interfaces are auto-calibrating and easy to implement.

Table 1–32 through Table 1–35 list the external memory interface specifications for the Cyclone III device family.

Use Table 1–32 through Table 1–35 for memory interface timing analysis.

Table 1–32. Cyclone III Maximum Clock Rate Support for External Memory Interfaces with Half-Rate Controller *(Note 1)*

Memory Standard	I/O Standard	C6 (MHz)			C7 (MHz)			C8 (MHz)			I7 (MHz)			A7 (MHz)		
		Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode	Column I/O Banks	Row I/O Banks	Hybrid Mode
DDR2 SDRAM *(2)*	SSTL-18 Class I/II	200	167	150	167	150	133	167	133	125	167	150	133	167	133	125
DDR SDRAM *(2)*	SSTL-2 Class I/II	167	150	133	150	133	125	133	125	100	150	133	125	133	125	100
QDRII SRAM *(3)*	1.8-V HSTL Class I/II	167	167	150	150	150	133	133	133	125	150	150	133	133	133	125

Notes to Table 1–32:

(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os. Hybrid mode refers to the combination of Column and Row I/Os.

(2) The values apply to interfaces with both modules and components.

(3) QDRII SRAM also supports the 1.5-V HSTL I/O standard. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O drive strength.

Table 1–33. *C*yclone III Maximum Clock Rate Support for External Memory Interfaces with Full-Rate Controller *(Note 1)*

Memory Standard	I/O Standard	C6 (MHz)		C7 (MHz)		C8 (MHz)		I7 (MHz)		A7 (MHz)	
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks
DDR2 SDRAM *(2)*	SSTL-18 Class I/II	167	167	150	150	133	133	150	150	133	133
DDR SDRAM *(2)*	SSTL-2 Class I/II	167	150	150	133	133	125	150	133	133	125

Notes to Table 1–33:

(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

(2) The values apply for interfaces with both modules and components.

Table 1–34. FPGA Sampling Window (SW) Requirement – Read Side *(Note 1)* (Part 1 of 2)

Memory Standard	Column I/Os		Row I/Os		Hybrid	
	Setup	Hold	Setup	Hold	Setup	Hold
C6						
DDR2 SDRAM	580	550	690	640	850	800

Table 1–34. FPGA Sampling Window (SW) Requirement – Read Side *(Note 1)* (Part 2 of 2)

Memory Standard	Column I/Os		Row I/Os		Hybrid	
	Setup	Hold	Setup	Hold	Setup	Hold
DDR SDRAM	585	535	700	650	870	820
QDRII SRAM	785	735	805	755	905	855
C7						
DDR2 SDRAM	705	650	770	715	985	930
DDR SDRAM	675	620	795	740	970	915
QDRII SRAM	900	845	910	855	1085	1030
C8						
DDR2 SDRAM	785	720	930	870	1115	1055
DDR SDRAM	800	740	915	855	1185	1125
QDRII SRAM	1050	990	1065	1005	1210	1150
I7						
DDR2 SDRAM	765	710	855	800	1040	985
DDR SDRAM	745	690	880	825	1000	945
QDRII SRAM	945	890	955	900	1130	1075
A7						
DDR2 SDRAM	805	745	1020	960	1145	1085
DDR SDRAM	880	820	955	935	1220	1160
QDRII SRAM	1090	1030	1105	1045	1250	1190

Note to Table 1–34:

(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os. Hybrid mode refers to the combination of Column and Row I/Os.

Table 1–35. Transmitter Channel-to-Channel Skew (TCCS) – Write Side *(Note 1)* (Part 1 of 2)

Memory Standard	I/O Standard	Column I/Os (ps)		Row I/Os (ps)		Hybrid (ps)	
		Lead	Lag	Lead	Lag	Lead	Lag
C6							
DDR2 SDRAM	SSTL-18 Class I	790	380	790	380	890	480
	SSTL-18 Class II	870	490	870	490	970	590
DDR SDRAM	SSTL-2 Class I	750	320	750	320	850	420
	SSTL-2 Class II	860	350	860	350	960	450
QDRII SRAM	1.8V HSTL Class I	780	410	780	410	880	510
	1.8V HSTL Class II	830	510	830	510	930	610
C7							
DDR2 SDRAM	SSTL-18 Class I	915	410	915	410	1015	510
	SSTL-18 Class II	1025	545	1025	545	1125	645
DDR SDRAM	SSTL-2 Class I	880	340	880	340	980	440
	SSTL-2 Class II	1010	380	1010	380	1110	480

Table 1–35. Transmitter Channel-to-Channel Skew (TCCS) – Write Side *(Note 1)* (Part 2 of 2)

Memory Standard	I/O Standard	Column I/Os (ps)		Row I/Os (ps)		Hybrid (ps)	
		Lead	Lag	Lead	Lag	Lead	Lag
QDRII SRAM	1.8V HSTL Class I	910	450	910	450	1010	550
	1.8V HSTL Class II	1010	570	1010	570	1110	670
C8							
DDR2 SDRAM	SSTL-18 Class I	1040	440	1040	440	1140	540
	SSTL-18 Class II	1180	600	1180	600	1280	700
DDR SDRAM	SSTL-2 Class I	1010	360	1010	360	1110	460
	SSTL-2 Class II	1160	410	1160	410	1260	510
QDRII SRAM	1.8V HSTL Class I	1040	490	1040	490	1140	590
	1.8V HSTL Class II	1190	630	1190	630	1290	730
I7							
DDR2 SDRAM	SSTL-18 Class I	961	431	961	431	1061	531
	SSTL-18 Class II	1076	572	1076	572	1176	672
DDR SDRAM	SSTL-2 Class I	924	357	924	357	1024	457
	SSTL-2 Class II	1061	399	1061	399	1161	499
QDRII SRAM	1.8V HSTL Class I	956	473	956	473	1056	573
	1.8V HSTL Class II	1061	599	1061	599	1161	699
A7							
DDR2 SDRAM *(2)*	SSTL-18 Class I	1092	462	1092	462	1192	562
	SSTL-18 Class II	1239	630	1239	630	1339	730
DDR SDRAM	SSTL-2 Class I	1061	378	1061	378	1161	478
	SSTL-2 Class II	1218	431	1218	431	1318	531
QDRII SRAM	1.8V HSTL Class I	1092	515	1092	515	1192	615
	1.8V HSTL Class II	1250	662	1250	662	1350	762

Notes to Table 1–35:

(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os. Hybrid mode refers to the combination of Column and Row I/Os.

(2) For DDR2 SDRAM write timing performance on Columns I/O for C8 and A7 devices, 97.5 degree phase offset is required.

DCD Specifications

Table 1–36 lists the worst case duty cycle distortion for Cyclone III devices.

Table 1–36. Duty Cycle Distortion on Cyclone III I/O Pins *(Note 1)*, *(2)*

Symbol	C6		C7, I7		C8, A7		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Notes to Table 1–36:

(1) DCD specification applies to clock outputs from PLLs, global clock tree, and IOE driving dedicated and general purpose I/O pins.

(2) Cyclone III devices meet specified DCD at maximum output toggle rate for each combination of I/O standard and current strength.

OCT Calibration Timing Specification

Table 1–37 lists the duration of calibration for power-up series OCT with calibration for Cyclone III devices.

Table 1–37. Timing Specification for OCT with Calibration *(Note 1)*

Symbol	Description	Maximum	Units
t_{OCTCAL}	Duration of power-up OCT R_s with calibration	20	µs

Notes to Table 1–37:

(1) OCT calibration takes place after device configuration, before entering user mode.

I/O Timing

Timing Model

DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone III device densities and speed grades. This section describes and specifies the performance of I/Os and internal timing.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 8.0 SP 1.

Preliminary, Correlated, and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during design compilation if the timing models are preliminary.

- *Preliminary* status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.
- *Correlated* numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.
- *Final* timing numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Cyclone III family devices have been completely characterized and no further changes to the timing model are expected.

Table 1–38 shows the status of the Cyclone III device timing models.

Table 1–38. Cyclone III Device Timing Model Status

Device	Preliminary	Correlated	Final
EP3C5	—	—	✓
EP3C10	—	—	✓
EP3C16	—	—	✓
EP3C25	—	—	✓
EP3C40	—	—	✓
EP3C55	—	—	✓
EP3C80	—	—	✓
EP3C120	—	—	✓

I/O Timing Measurement Methodology

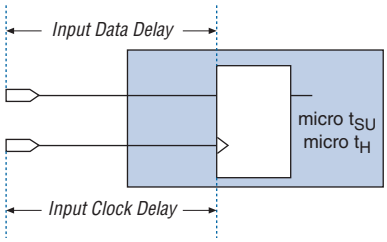
Altera characterizes timing delays at the worst-case process, minimum voltage, and maximum temperature for input register setup time (t_{SU}) and hold time (t_H). The Quartus II software uses the following equations to calculate t_{SU} and t_H timing for Cyclone III devices input signals:

t_{SU} = + data delay from input pin to input register
+ micro setup time of the input register
– clock delay from input pin to input register

t_H = – data delay from input pin to input register
+ micro hold time of the input register
+ clock delay from input pin to input register

Figure 1–2 shows the setup and hold timing diagram for input registers.

Figure 1–2. Input Register Setup and Hold Timing Diagram



For output timing, different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading. The timing is specified up to the output pin of the FPGA device. The Quartus II software calculates I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 1–39.

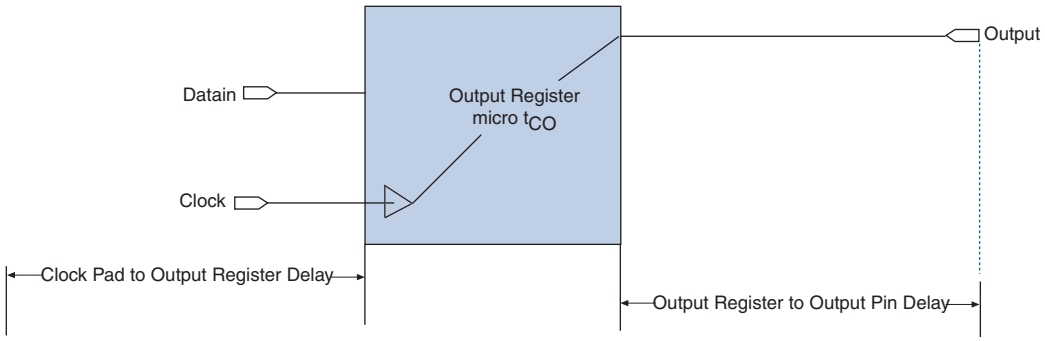
Use the following equations to calculate clock-pin-to-output-pin timing for Cyclone III devices.

t_{CO} from clock pin to I/O pin =

+ delay from clock pad to I/O output register
+ IOE output register clock-to-output delay
+ delay from output register to output pin

Figure 1–3 shows the clock-to-output timing diagram for output registers.

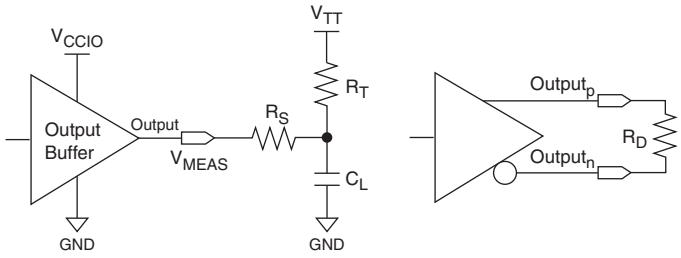
Figure 1–3. Output Register Clock to Output Timing Diagram



The Quartus II software reports the t_{CO} timing with the conditions shown in Table 1–39 using the above equation.

Figure 1–4 shows the model of the circuit that is represented by the output timing of the Quartus II software for single-ended outputs and dedicated differential outputs.

Figure 1–4. Output Delay Timing Reporting Setup Modeled by Quartus II Software for Single-Ended Outputs and Dedicated Differential Outputs *(Note 1)*, *(2)*



Notes to Figure 1–4:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay must be accounted for with IBIS model simulations.

(2) V_{CCINT} is 1.10 V unless otherwise specified.

Figure 1–5 and Figure 1–6 show the model of the circuit that is represented by the output timing of the Quartus II software for differential outputs with single and multiple external resistors.

Figure 1–5. Output Delay Timing Reporting Setup Modeled by Quartus II Software for Differential Outputs with Single External Resistor

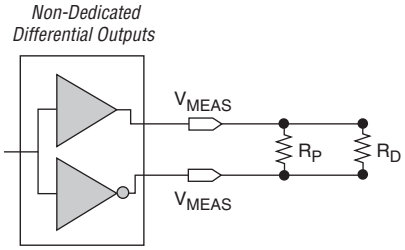
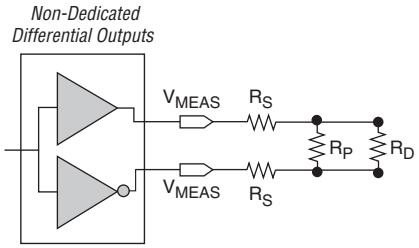


Figure 1–6. Output Delay Timing Reporting Setup Modeled by Quartus II Software for Differential Outputs with Three External Resistor Network



The output timing only accounts for timing delay for the FPGA output.

To account for the timing delay from the FPGA output to the receiving device for system-timing analysis, refer to *AN 366: Understanding I/O Output Timing for Altera Devices*.

Table 1–39. Output Timing Measurement Methodology for Output Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 1 of 2)

I/O Standard	Loading and Termination							Measurement Point
	R_S (Ω)	R_T (Ω)	R_D (Ω)	R_P (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
3.3-V LVTTL	—	—	—	—	3.085	—	0	1.5425
3.3-V LVCMOS	—	—	—	—	3.085	—	0	1.5425
3.0-V LVTTL	—	—	—	—	2.80	—	0	1.40
3.0-V LVCMOS	—	—	—	—	2.80	—	0	1.40
2.5-V LVTTL/LVCMOS	—	—	—	—	2.325	—	0	1.1625
1.8-V LVTTL/LVCMOS	—	—	—	—	1.66	—	0	0.83
1.5-V LVCMOS	—	—	—	—	1.375	—	0	0.6875
1.2-V LVCMOS	—	—	—	—	1.10	—	0	0.55
3.0-V PCI	—	—	—	—	2.80	—	10	1.40
3.0-V PCI-X	—	—	—	—	2.80	—	10	1.40
SSTL-2 Class I *(5)*	25	50	—	—	2.325	1.25	0	1.1625
SSTL-2 Class II *(5)*	25	25	—	—	2.325	1.25	0	1.1625

Table 1–39. Output Timing Measurement Methodology for Output Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 2 of 2)

I/O Standard	Loading and Termination							Measurement Point
	R_S (Ω)	R_T (Ω)	R_D (Ω)	R_P (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
SSTL-18 Class I *(5)*	25	50	—	—	1.66	0.9	0	0.83
SSTL-18 Class II *(5)*	25	25	—	—	1.66	0.9	0	0.83
1.8-V HSTL Class I *(5)*	—	50	—	—	1.66	0.9	0	0.83
1.8-V HSTL Class II *(5)*	—	25	—	—	1.66	0.9	0	0.83
1.5-V HSTL Class I *(5)*	—	50	—	—	1.375	0.75	0	0.6875
1.5-V HSTL Class II *(5)*	—	25	—	—	1.375	0.75	0	0.6875
1.2-V HSTL Class I *(5)*	—	50	—	—	1.10	0.6	0	0.55
1.2-V HSTL Class II *(5)*	—	25	—	—	1.10	0.6	0	0.55
LVDS	—	—	100	—	2.325	—	0	1.1625
LVDS_E_3R	120	—	100	170	2.325	—	0	1.1625
BLVDS	47	—	56	56	2.325	—	0	1.1625
mini-LVDS	—	—	100	—	2.325	—	0	1.1625
mini-LVDS_E_3R	120	—	100	170	2.325	—	0	1.1625
PPDS	—	—	100	—	2.325	—	0	1.1625
PPDS_E_3R	120	—	100	170	2.325	—	0	1.1625
RSDS	—	—	100	—	2.325	—	0	1.1625
RSDS_E_1R	—	—	100	100	2.325	—	0	1.1625
RSDS_E_3R	120	—	100	170	2.325	—	0	1.1625

Notes to Table 1–39:

(1) Input measurement point at internal node is 0.5 × V_{CCINT}.

(2) Output measurement point for V_{MEAS} at the buffer output is 0.5 × V_{CCIO}.

(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO}. V_{CCINT} = 1.10 V with less than 30-mV ripple.

(5) The interface has to use external termination RT. The termination voltage V_{TT} may either be supplied by an independent power supply or created through a Thevenin-equivalent circuit.

I/O Default Capacitive Loading

Refer to Table 1–40 for default capacitive loading of different I/O standards.

Table 1–40. Default Loading of Different I/O Standards for Cyclone III Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
3.3-V LVTTL	0	pF
3.3-V LVCMOS	0	pF
3.0-V LVTTL	0	pF
3.0-V LVCMOS	0	pF
2.5-V LVTTL/LVCMOS	0	pF
1.8-V LVTTL/LVCMOS	0	pF
1.5-V LVCMOS	0	pF
1.2-V LVCMOS	0	pF

Table 1–40. Default Loading of Different I/O Standards for Cyclone III Devices (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
3.0-V PCI	10	pF
3.0-V PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.2-V HSTL Class I	0	pF
1.2-V HSTL Class II	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.2-V Differential HSTL Class I	0	pF
1.2-V Differential HSTL Class II	0	pF
1.5-V Differential HSTL Class I	0	pF
1.5-V Differential HSTL Class II	0	pF
1.8-V Differential HSTL Class I	0	pF
1.8-V Differential HSTL Class II	0	pF
LVDS	0	pF
LVDS_E_3R	0	pF
BLVDS	0	pF
mini-LVDS	0	pF
mini-LVDS_E_3R	0	pF
PPDS	0	pF
PPDS_E_3R	0	pF
RSDS	0	pF
RSDS_E_1R	0	pF
RSDS_E_3R	0	pF

Maximum Input and Output Clock Toggle Rate

The maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 1–41 specifies the maximum input clock toggle rates. Table 1–42 specifies the maximum output clock toggle rates at 0 pF load at Quartus II default (fast) slew rate setting. Table 1–43 specifies the derating factors for the output clock toggle rate for a non 0 pF load at Quartus II default (fast) slew rate setting.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load:

= 1000 / (1000/ toggle rate at 0 pF load + derating factor * load value in pF /1000)

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 16 mA I/O standard is 260 MHz on a C6 device clock output pin. The derating factor is 26 ps/pF. For a 10 pF load, the toggle rate is calculated as:

1000 / (1000/260 + 26 × 10 /1000) = 243 (MHz)

Table 1–41 through Table 1–43 show I/O toggle rates for Cyclone III devices.

Table 1–41. Maximum Input Toggle Rate on Cyclone III Devices *(Note 1)* (Part 1 of 2)

I/O Standard	Column I/O Pins (MHz) C6	Column I/O Pins (MHz) C7, I7	Column I/O Pins (MHz) C8, A7	Row I/O Pins (MHz) C6	Row I/O Pins (MHz) C7, I7	Row I/O Pins (MHz) C8, A7	Dedicated Clock Inputs (MHz) C6	Dedicated Clock Inputs (MHz) C7, I7	Dedicated Clock Inputs (MHz) C8, A7
3.3-V LVTTL	250	250	250	250	250	250	250	250	250
3.3-V LVCMOS	250	250	250	250	250	250	250	250	250
3.0-V LVTTL	250	250	250	250	250	250	250	250	250
3.0-V LVCMOS	250	250	250	250	250	250	250	250	250
2.5V	250	250	250	250	250	250	250	250	250
1.8V	250	250	250	250	250	250	250	250	250
1.5V	250	250	250	250	250	250	250	250	250
1.2V	200	200	200	200	200	200	200	200	200
SSTL-2 Class I	250	250	250	250	250	250	250	250	250
SSTL-2 Class II	250	250	250	250	250	250	250	250	250
SSTL-18 Class I	300	300	300	300	300	300	300	300	300
SSTL-18 Class II	300	300	300	300	300	300	300	300	300
1.8-V HSTL Class I	300	300	300	300	300	300	300	300	300
1.8-V HSTL Class II	300	300	300	300	300	300	300	300	300
1.5-V HSTL Class I	300	300	300	300	300	300	300	300	300
1.5-V HSTL Class II	300	300	300	300	300	300	300	300	300
1.2-V HSTL Class I	125	125	125	125	125	125	125	125	125
1.2-V HSTL Class II	125	125	125	*(2)*	*(2)*	*(2)*	125	125	125
3.0-V PCI	250	250	250	250	250	250	250	250	250
3.0-V PCI-X	250	250	250	250	250	250	250	250	250

Table 1–41. Maximum Input Toggle Rate on Cyclone III Devices *(Note 1)* (Part 2 of 2)

I/O Standard	Column I/O Pins (MHz) C6	Column I/O Pins (MHz) C7, I7	Column I/O Pins (MHz) C8, A7	Row I/O Pins (MHz) C6	Row I/O Pins (MHz) C7, I7	Row I/O Pins (MHz) C8, A7	Dedicated Clock Inputs (MHz) C6	Dedicated Clock Inputs (MHz) C7, I7	Dedicated Clock Inputs (MHz) C8, A7
Differential 2.5-V SSTL Class I	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	250	250	250
Differential 2.5-V SSTL Class II	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	250	250	250
Differential 1.8-V SSTL Class I	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	300	300
Differential 1.8-V SSTL Class II	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	300	300
Differential 1.8-V HSTL Class I	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	300	300
Differential 1.8-V HSTL Class II	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	300	300
Differential 1.5-V HSTL Class I	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	300	300
Differential 1.5-V HSTL Class II	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	300	300
Differential 1.2-V HSTL Class I	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	125	125	125
Differential 1.2-V HSTL Class II	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	125	125	125
LVPECL	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	438	370	320
LVDS	438	370	320	438	370	320	438	370	320
BLVDS	438	370	320	438	370	320	*(5)*	*(5)*	*(5)*

Notes to Table 1–41:

(1) When the VREF pin is used as a regular input pin, a lower maximum input toggle rate performance is expected due to higher pin capacitance.
(2) The 1.2 V_HSTL_CLASS_II is only supported on column I/O pins.
(3) Input differential standard is only supported on the GCLK pin.
(4) Input LVPECL is only supported on the GCLK pin.
(5) BLVDS is a bidirectional I/O standard and is not supported at dedicated clock inputs.

Table 1–42. Maximum Output Toggle Rate on Cyclone III Devices *(Note 1)*, *(6)* (Part 1 of 4)

I/O Standard	Current Strength (mA) or OCT Setting *(8)*	Column I/O Pins (MHz) C6	Column I/O Pins (MHz) C7,I7	Column I/O Pins (MHz) C8,A7	Row I/O Pins (MHz) C6	Row I/O Pins (MHz) C7,I7	Row I/O Pins (MHz) C8,A7	Dedicated Clock Outputs (MHz) C6	Dedicated Clock Outputs (MHz) C7,I7	Dedicated Clock Outputs (MHz) C8,A7
3.3-V LVTTL	4	127	106	85	127	106	85	127	106	85
	8	250	237	223	250	237	223	250	237	223
3.3-V LVCMOS	2	95	74	63	95	74	63	95	74	63
3.0-V LVTTL	4	180	148	116	180	148	116	180	148	116
	8	250	233	191	250	233	191	250	233	191
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
3.0-V LVCMOS	4	233	191	159	233	191	159	233	191	159
	8	250	237	223	250	237	223	250	237	223
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225

Table 1–42. Maximum Output Toggle Rate on Cyclone III Devices *(Note 1)*, *(6)* (Part 2 of 4)

I/O Standard	Current Strength (mA) or OCT Setting *(8)*	Column I/O Pins (MHz)	Column I/O Pins (MHz)	Column I/O Pins (MHz)	Row I/O Pins (MHz)	Row I/O Pins (MHz)	Row I/O Pins (MHz)	Dedicated Clock Outputs (MHz)	Dedicated Clock Outputs (MHz)	Dedicated Clock Outputs (MHz)
		C6	C7,I7	C8,A7	C6	C7,I7	C8,A7	C6	C7,I7	C8,A7
2.5 V	4	170	138	116	170	138	116	170	138	116
	8	250	223	180	250	223	180	250	223	180
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
1.8 V	2	95	74	63	95	74	63	95	74	63
	4	201	170	138	201	170	138	201	170	138
	6	244	201	170	244	201	170	244	201	170
	8	250	237	201	250	237	201	250	237	201
	10	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
1.5 V	2	127	106	85	127	106	85	127	106	85
	4	201	170	138	201	170	138	201	170	138
	6	233	191	159	233	191	159	233	191	159
	8	250	212	170	250	212	170	250	212	170
	10	250	233	191	250	233	191	250	233	191
	12	250	237	223	250	237	223	250	237	223
	16	250	237	225	250	237	225	250	237	225
1.2 V	2	170	138	116	170	138	116	170	138	116
	4	191	159	127	191	159	127	191	159	127
	6	200	180	148	200	180	148	200	180	148
	8	200	180	148	200	180	148	200	180	148
	10	200	190	159	200	190	180	200	190	159
	12	200	190	180	*(2)*	*(2)*	*(2)*	200	190	180
SSTL-2 Class I	8	170	138	116	170	138	116	170	138	116
	12	250	237	225	250	237	225	250	237	225
SSTL-2 Class II	16	250	237	225	250	237	225	250	237	225
SSTL-18 Class I	8	300	285	265	300	285	265	300	285	265
	10	300	285	270	300	285	270	300	285	270
	12	300	285	270	300	285	270	300	285	270
SSTL-18 Class II	12	255	212	170	255	212	170	255	212	170
	16	300	285	270	300	285	270	300	285	270
1.8-V HSTL Class I	8	300	285	265	300	285	265	300	285	265
	10	300	285	265	300	285	265	300	285	265
	12	300	285	270	300	285	270	300	285	270
1.8-V HSTL Class II	16	300	285	270	300	285	270	300	285	270

Table 1–42. Maximum Output Toggle Rate on Cyclone III Devices *(Note 1)*, *(6)* (Part 3 of 4)

I/O Standard	Current Strength (mA) or OCT Setting *(8)*	Column I/O Pins (MHz)	Column I/O Pins (MHz)	Column I/O Pins (MHz)	Row I/O Pins (MHz)	Row I/O Pins (MHz)	Row I/O Pins (MHz)	Dedicated Clock Outputs (MHz)	Dedicated Clock Outputs (MHz)	Dedicated Clock Outputs (MHz)
		C6	C7,I7	C8,A7	C6	C7,I7	C8,A7	C6	C7,I7	C8,A7
1.5-V HSTL Class I	8	300	285	233	300	285	233	300	285	233
	10	300	285	233	300	285	233	300	285	233
	12	300	285	270	300	285	270	300	285	270
1.5-V HSTL Class II	16	300	285	270	300	285	270	300	285	270
1.2-V HSTL Class I	8	125	118	112	125	118	112	125	118	112
	10	125	118	112	125	118	112	125	118	112
	12	125	118	112	*(2)*	*(2)*	*(2)*	125	118	112
1.2-V HSTL Class II	14	125	118	112	*(2)*	*(2)*	*(2)*	125	118	112
3.0-V PCI	—	250	237	225	250	237	225	250	237	225
3.0-V PCI-X	—	250	237	225	250	237	225	250	237	225
Differential 2.5-V SSTL Class I	8	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	170	138	116
	12	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	250	237	225
Differential 2.5-V SSTL Class II	16	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	250	237	225
Differential 1.8-V SSTL Class I	8	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	265
	10	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	270
	12	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	270
Differential 1.8-V HSTL Class I	8	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	265
	10	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	265
	12	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	270
Differential 1.5-V HSTL Class I	8	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	233
	10	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	233
	12	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	285	270
Differential 1.2-V HSTL Class I	8	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	125	118	112
	10	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	125	118	112
	12	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	125	118	112
LVDS	—	*(4)*	*(4)*	*(4)*	420	370	320	*(4)*	*(4)*	*(4)*
LVDS_E_3R	—	320	320	275	320	320	275	320	320	275
BLVDS	8	170	138	116	170	138	116	*(7)*	*(7)*	*(7)*
	12	250	237	225	250	237	225	*(7)*	*(7)*	*(7)*
	16	250	237	225	250	237	225	*(7)*	*(7)*	*(7)*
mini-LVDS	—	*(4)*	*(4)*	*(4)*	200	155	155	*(4)*	*(4)*	*(4)*
mini-LVDS_E_3R	—	155	155	155	200	155	155	155	155	155
PPDS	—	*(4)*	*(4)*	*(4)*	220	155	155	*(4)*	*(4)*	*(4)*
PPDS_E_3R	—	220	155	155	220	155	155	220	155	155
RSDS	—	*(4)*	*(4)*	*(4)*	180	155	155	*(4)*	*(4)*	*(4)*

Table 1–42. Maximum Output Toggle Rate on Cyclone III Devices *(Note 1)*, *(6)* (Part 4 of 4)

I/O Standard	Current Strength (mA) or OCT Setting *(8)*	Column I/O Pins (MHz)	Column I/O Pins (MHz)	Column I/O Pins (MHz)	Row I/O Pins (MHz)	Row I/O Pins (MHz)	Row I/O Pins (MHz)	Dedicated Clock Outputs (MHz)	Dedicated Clock Outputs (MHz)	Dedicated Clock Outputs (MHz)
		C6	C7,I7	C8,A7	C6	C7,I7	C8,A7	C6	C7,I7	C8,A7
RSDS_E_1R	—	85	85	85	85	85	85	85	85	85
RSDS_E_3R	—	180	155	155	180	155	155	180	155	155
3.0-V LVTTL	Series 25 Ω	250	237	225	250	237	225	250	237	225
	Series 50 Ω	250	237	225	250	237	225	250	237	225
2.5 V	Series 25 Ω	250	237	225	250	237	225	250	237	225
	Series 50 Ω	250	237	225	250	237	225	250	237	225
1.8 V	Series 25 Ω	300	285	270	300	285	270	300	285	270
	Series 50 Ω	300	285	270	300	285	270	300	285	270
1.5 V	Series 25 Ω	300	285	270	300	285	270	300	285	270
	Series 50 Ω	300	285	270	300	285	270	300	285	270
1.2 V	Series 25 Ω	200	190	180	*(5)*	*(5)*	*(5)*	200	190	180
	Series 50 Ω	200	190	180	200	190	180	200	190	180

Notes to Table 1–42:

(1) When the VREF pin is used as a regular output pin, a lower maximum output toggle rate performance is expected due to higher pin capacitance.
(2) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I / II (12 mA and 14 mA, respectively) are only supported on column I/O pins.
(3) Output differential standard is only supported on the PLLCLKOUT pin.
(4) Dedicated differential output standards are only supported at row I/O pins. Dedicated LVDS input is supported at both column and row I/O pins.
(5) The 1.2-V output standard with 25-Ω output termination is only supported at column and the PLLCLKOUT pin.
(6) The maximum output toggle rates are specified at 0 pF load at Quartus II default (fast) slew rate setting.
(7) BLVDS is a bidirectional I/O standard and is not supported at dedicated clock outputs.
(8) The OCT settings are applicable for both OCT with and without calibration.

Table 1–43. Maximum Output Toggle Rate Derating Factors on Cyclone III Devices *(Note 4)* (Part 1 of 4)

IO Standard	Current Strength (mA) or OCT Setting *(6)*	Column I/O Pins (ps/pf)	Column I/O Pins (ps/pf)	Column I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Dedicated Clock Outputs (ps/pF)	Dedicated Clock Outputs (ps/pF)	Dedicated Clock Outputs (ps/pF)
		C6	C7,I7	C8,A7	C6	C7,I7	C8,A7	C6	C7,I7	C8,A7
3.3-V LVTTL	4	620	626	627	557	626	709	620	626	627
	8	219	225	231	211	218	225	219	225	231

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Table 1–43. Maximum Output Toggle Rate Derating Factors on Cyclone III Devices *(Note 4)* (Part 2 of 4)

IO Standard	Current Strength (mA) or OCT Setting *(6)*	Column I/O Pins (ps/pf)	Column I/O Pins (ps/pf)	Column I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Dedicated Clock Outputs (ps/pF)	Dedicated Clock Outputs (ps/pF)	Dedicated Clock Outputs (ps/pF)
		C6	C7,I7	C8,A7	C6	C7,I7	C8,A7	C6	C7,I7	C8,A7
3.3-V LVCMOS	2	954	1021	1099	659	995	1582	954	1021	1099
3.0-V LVTTL	4	521	532	534	427	467	514	521	532	534
	8	144	145	145	121	123	126	144	145	145
	12	60	64	68	56	56	56	60	64	68
	16	29	34	39	32	32	32	29	34	39
3.0-V LVCMOS	4	275	312	358	332	352	375	275	312	358
	8	112	119	126	123	126	129	112	119	126
	12	58	59	61	62	63	64	58	59	61
	16	33	34	34	36	36	37	33	34	34
2.5 V	4	394	406	419	379	429	493	394	406	419
	8	206	223	241	150	205	284	206	223	241
	12	138	152	169	86	132	200	138	152	169
	16	103	116	130	58	97	154	103	116	130
1.8 V	2	756	826	908	876	900	919	756	826	908
	4	115	158	221	111	148	197	115	158	221
	6	64	90	127	61	85	117	64	90	127
	8	38	56	80	36	53	76	38	56	80
	10	23	36	54	22	35	53	23	36	54
	12	14	24	38	13	24	39	14	24	38
	16	6	10	15	5	11	19	6	10	15
1.5 V	2	584	624	658	664	684	701	584	624	658
	4	133	137	138	134	138	141	133	137	138
	6	77	81	84	78	80	81	77	81	84
	8	44	48	53	45	47	48	44	48	53
	10	24	28	33	26	26	27	24	28	33
	12	10	14	21	13	13	14	10	14	21
	16	*(1)*	5	12	5	5	6	*(1)*	5	12
1.2 V	2	430	448	450	513	535	540	430	448	450
	4	200	221	245	166	190	223	200	221	245
	6	115	129	148	93	95	95	115	129	148
	8	68	71	73	20	30	45	68	71	73
	10	22	31	46	6	6	7	22	31	46
	12	15	18	22	*(1)*	*(1)*	*(1)*	15	18	22
SSTL-2 Class I	8	256	263	263	305	576	1824	256	263	263
	12	105	105	106	84	98	116	105	105	106
SSTL-2 Class II	16	55	55	56	26	28	31	55	55	56

Table 1–43. Maximum Output Toggle Rate Derating Factors on Cyclone III Devices *(Note 4)* (Part 3 of 4)

IO Standard	Current Strength (mA) or OCT Setting *(6)*	Column I/O Pins (ps/pf)	Column I/O Pins (ps/pf)	Column I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Row I/O Pins (ps/pf)	Dedicated Clock Outputs (ps/pF)	Dedicated Clock Outputs (ps/pF)	Dedicated Clock Outputs (ps/pF)
		C6	C7,I7	C8,A7	C6	C7,I7	C8,A7	C6	C7,I7	C8,A7
SSTL-18 Class I	8	62	63	64	53	70	94	62	63	64
	10	57	58	60	55	63	74	57	58	60
	12	52	54	56	57	57	58	52	54	56
SSTL-18 Class II	12	23	24	26	34	35	37	23	24	26
	16	19	20	21	26	27	27	19	20	21
1.8-V HSTL Class I	8	77	78	80	61	65	68	77	78	80
	10	74	75	77	60	62	64	74	75	77
	12	71	72	74	60	60	61	71	72	74
1.8-V HSTL Class II	16	60	65	71	51	55	59	60	65	71
1.5-V HSTL Class I	8	26	27	28	16	17	17	26	27	28
	10	20	21	22	12	13	15	20	21	22
	12	15	15	16	8	10	14	15	15	16
1.5-V HSTL Class II	16	14	16	18	10	11	11	14	16	18
1.2-V HSTL Class I	8	7	9	13	8	12	19	7	9	13
	10	7	9	11	5	6	8	7	9	11
	12	7	8	9	*(1)*	*(1)*	*(1)*	7	8	9
1.2-V HSTL Class II	14	17	28	44	*(1)*	*(1)*	*(1)*	17	28	44
3.0-V PCI	—	54	55	56	54	54	55	54	55	56
3.0-V PCI-X	—	54	55	56	54	54	55	54	55	56
LVDS	—	*(2)*	*(2)*	*(2)*	10	10	10	*(2)*	*(2)*	*(2)*
LVDS_E_3R	—	11	11	11	10	10	10	11	11	11
BLVDS	8	256	263	263	305	576	1824	*(5)*	*(5)*	*(5)*
	12	105	105	106	84	98	116	*(5)*	*(5)*	*(5)*
	16	55	55	56	26	28	31	*(5)*	*(5)*	*(5)*
mini-LVDS	—	*(2)*	*(2)*	*(2)*	10	10	10	*(2)*	*(2)*	*(2)*
mini-LVDS_E_3R	—	11	11	11	10	10	10	11	11	11
PPDS	—	*(2)*	*(2)*	*(2)*	10	10	10	*(2)*	*(2)*	*(2)*
PPDS_E_3R	—	11	11	11	10	10	10	11	11	11
RSDS	—	*(2)*	*(2)*	*(2)*	10	10	10	*(2)*	*(2)*	*(2)*
RSDS_E_1R	—	11	11	11	10	10	10	11	11	11
RSDS_E_3R	—	11	11	11	10	10	10	11	11	11
3.0-V LVTTL	Series 25 Ω	23	23	24	23	25	27	23	23	24
	Series 50 Ω	155	163	172	136	145	155	155	163	172

Table 1–43. Maximum Output Toggle Rate Derating Factors on Cyclone III Devices *(Note 4)* (Part 4 of 4)

IO Standard	Current Strength (mA) or OCT Setting *(6)*	Column I/O Pins (ps/pf) C6	Column I/O Pins (ps/pf) C7,I7	Column I/O Pins (ps/pf) C8,A7	Row I/O Pins (ps/pf) C6	Row I/O Pins (ps/pf) C7,I7	Row I/O Pins (ps/pf) C8,A7	Dedicated Clock Outputs (ps/pF) C6	Dedicated Clock Outputs (ps/pF) C7,I7	Dedicated Clock Outputs (ps/pF) C8,A7
2.5 V	Series 25 Ω	3	16	34	4	20	41	3	16	34
	Series 50 Ω	235	237	238	247	250	251	235	237	238
1.8 V	Series 25 Ω	3	4	5	5	9	14	3	4	5
	Series 50 Ω	11	20	31	11	19	30	11	20	31
1.5 V	Series 25 Ω	6	7	8	10	17	26	6	7	8
	Series 50 Ω	5	6	8	25	26	26	5	6	8
1.2 V	Series 25 Ω	8	11	15	*(3)*	*(3)*	*(3)*	8	11	15
	Series 50 Ω	11	12	14	33	39	48	11	12	14

Notes to Table 1–43:

(1) The 1.2-V (12 mA) and 1.2-V_HSTL_CLASS_I / II (12 mA and 14 mA respectively) are only supported on column I/O pins.
(2) Dedicated differential output standards are only supported at row I/O pins.
(3) The 1.2-V output standard with 25 Ω output termination is only supported at column and PLLCLKOUT pin.
(4) The maximum output toggle rate derating factors are specified at Quartus II default (fast) slew rate setting.
(5) BLVDS is a bidirectional I/O standard and hence not supported at dedicated clock outputs.
(6) The OCT settings are applicable for both OCT with and without calibration.

IOE Programmable Delay

Table 1–44 and Table 1–45 show IOE programmable delay for Cyclone III devices.

Table 1–44. Cyclone III IOE Programmable Delay on Column Pins *(Note 1), (2)* (Part 1 of 2)

Parameter	Paths Affected	Number of Settings	Min Offset	Fast Corner A7 and I7 Max Offset	Fast Corner C6 Max Offset	C6 Max Offset	C7 Max Offset	C8 Max Offset	I7 Max Offset	A7 Max Offset	Unit
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.211	1.314	2.175	2.32	2.386	2.366	2.49	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.203	1.307	2.19	2.387	2.54	2.43	2.545	ns

Table 1–44. Cyclone III IOE Programmable Delay on Column Pins *(Note 1), (2)* (Part 2 of 2)

Parameter	Paths Affected	Number of Settings	Min Offset	Fast Corner A7 and I7	Fast Corner C6	C6	C7	C8	I7	A7	Unit
				Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	
Delay from output register to output pin	I/O output register to pad	2	0	0.479	0.504	0.915	1.011	1.107	1.018	1.048	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.664	0.694	1.199	1.378	1.532	1.392	1.441	ns

Notes to Table 1–44:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Quartus II software.

Table 1–45. Cyclone III IOE Programmable Delay on Row Pins *(Note 1), (2)*

Parameter	Paths Affected	Number of Settings	Min Offset	Fast Corner A7 and I7	Fast Corner C6	C6	C7	C8	I7	A7	Unit
				Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.209	1.314	2.174	2.335	2.406	2.381	2.505	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.207	1.312	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.51	0.537	0.962	1.072	1.167	1.074	1.101	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.669	0.698	1.207	1.388	1.542	1.403	1.45	ns

Notes to Table 1–45:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Quartus II software

Typical Design Performance

User I/O Pin Timing Parameters

Table 1–46 through Table 1–93 show user I/O pin timing for Cyclone III devices. I/O buffer t_{SU}, t_H and t_{CO} are reported for the cases when clock is driven by global clock and a PLL.

The 12 mA programmable current strength for 1.2-V and 1.2-V HSTL Class I I/O standard is not supported at row I/Os. The 1.2-V HSTL Class II standard is only supported at column I/Os. PCI and PCI-X do not support programmable current strength.

When VREF pin is used as a regular output pin, a larger t_{CO} value is expected due to the higher pin capacitance.

For more information about programmable current strength, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Dedicated LVDS, mini-LVDS, PPDS, and RSDS I/O standards are supported at row I/Os. External resistor networks are required if the differential standards are used as output pins at column banks. LVDS I/O standard is supported at both input and output pins. PPDS, RSDS, and mini-LVDS standards are only supported at output pins.

For more information about the differential I/O interface, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

EP3C5 I/O Timing Parameters

Table 1–46 through Table 1–51 show the maximum I/O timing parameters for EP3C5 devices.

Table 1–46. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.034	–1.157	–1.267	–1.171	–1.189	ns
		t_{H}	1.259	1.418	1.560	1.431	1.452	ns
	GCLK PLL	t_{SU}	1.159	1.262	1.333	1.289	1.396	ns
		t_{H}	–0.667	–0.697	–0.709	–0.723	–0.814	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.034	–1.157	–1.267	–1.171	–1.189	ns
		t_{H}	1.259	1.418	1.560	1.431	1.452	ns
	GCLK PLL	t_{SU}	1.159	1.262	1.333	1.289	1.396	ns
		t_{H}	–0.667	–0.697	–0.709	–0.723	–0.814	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.026	–1.154	–1.270	–1.169	–1.187	ns
		t_{H}	1.251	1.415	1.563	1.429	1.450	ns
	GCLK PLL	t_{SU}	1.167	1.265	1.330	1.291	1.398	ns
		t_{H}	–0.675	–0.700	–0.706	–0.725	–0.816	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.026	–1.154	–1.270	–1.169	–1.187	ns
		t_{H}	1.251	1.415	1.563	1.429	1.450	ns
	GCLK PLL	t_{SU}	1.167	1.265	1.330	1.291	1.398	ns
		t_{H}	–0.675	–0.700	–0.706	–0.725	–0.816	ns
2.5 V	GCLK	t_{SU}	–0.995	–1.127	–1.245	–1.143	–1.162	ns
		t_{H}	1.220	1.388	1.538	1.403	1.425	ns
	GCLK PLL	t_{SU}	1.198	1.292	1.355	1.317	1.423	ns
		t_{H}	–0.706	–0.727	–0.731	–0.751	–0.841	ns

Table 1–46. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8 V	GCLK	t_{SU}	–0.892	–1.060	–1.208	–1.073	–1.091	ns
		t_{H}	1.117	1.321	1.501	1.333	1.354	ns
	GCLK PLL	t_{SU}	1.301	1.359	1.392	1.387	1.494	ns
		t_{H}	–0.809	–0.794	–0.768	–0.821	–0.912	ns
1.5 V	GCLK	t_{SU}	–0.828	–0.973	–1.096	–0.989	–1.011	ns
		t_{H}	1.053	1.234	1.389	1.249	1.274	ns
	GCLK PLL	t_{SU}	1.365	1.446	1.504	1.471	1.574	ns
		t_{H}	–0.873	–0.881	–0.880	–0.905	–0.992	ns
1.2 V	GCLK	t_{SU}	–0.695	–0.795	–0.892	–0.816	–0.846	ns
		t_{H}	0.920	1.056	1.185	1.076	1.109	ns
	GCLK PLL	t_{SU}	1.498	1.624	1.708	1.644	1.739	ns
		t_{H}	–1.006	–1.059	–1.084	–1.078	–1.157	ns
SSTL-2 Class I	GCLK	t_{SU}	–0.916	–1.091	–1.251	–1.103	–1.117	ns
		t_{H}	1.141	1.352	1.544	1.363	1.380	ns
	GCLK PLL	t_{SU}	1.284	1.334	1.356	1.363	1.476	ns
		t_{H}	–0.791	–0.770	–0.733	–0.797	–0.894	ns
SSTL-2 Class II	GCLK	t_{SU}	–0.916	–1.091	–1.251	–1.103	–1.117	ns
		t_{H}	1.141	1.352	1.544	1.363	1.380	ns
	GCLK PLL	t_{SU}	1.284	1.334	1.356	1.363	1.476	ns
		t_{H}	–0.791	–0.770	–0.733	–0.797	–0.894	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.746	–0.870	–0.968	–0.887	–0.910	ns
		t_{H}	0.971	1.131	1.261	1.147	1.173	ns
	GCLK PLL	t_{SU}	1.454	1.555	1.639	1.579	1.683	ns
		t_{H}	–0.961	–0.991	–1.016	–1.013	–1.101	ns
SSTL-18 Class II	GCLK	t_{SU}	–0.746	–0.870	–0.968	–0.887	–0.910	ns
		t_{H}	0.971	1.131	1.261	1.147	1.173	ns
	GCLK PLL	t_{SU}	1.454	1.555	1.639	1.579	1.683	ns
		t_{H}	–0.961	–0.991	–1.016	–1.013	–1.101	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–0.746	–0.870	–0.968	–0.887	–0.910	ns
		t_{H}	0.971	1.131	1.261	1.147	1.173	ns
	GCLK PLL	t_{SU}	1.454	1.555	1.639	1.579	1.683	ns
		t_{H}	–0.961	–0.991	–1.016	–1.013	–1.101	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.746	–0.870	–0.968	–0.887	–0.910	ns
		t_{H}	0.971	1.131	1.261	1.147	1.173	ns
	GCLK PLL	t_{SU}	1.454	1.555	1.639	1.579	1.683	ns
		t_{H}	–0.961	–0.991	–1.016	–1.013	–1.101	ns

Table 1–46. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5-V HSTL Class I	GCLK	t_{SU}	–0.837	–0.978	–1.096	–0.995	–1.015	ns
		t_H	1.062	1.239	1.389	1.255	1.278	ns
	GCLK PLL	t_{SU}	1.363	1.447	1.511	1.471	1.578	ns
		t_H	–0.870	–0.883	–0.888	–0.905	–0.996	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–0.837	–0.978	–1.096	–0.995	–1.015	ns
		t_H	1.062	1.239	1.389	1.255	1.278	ns
	GCLK PLL	t_{SU}	1.363	1.447	1.511	1.471	1.578	ns
		t_H	–0.870	–0.883	–0.888	–0.905	–0.996	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.649	–0.733	–0.814	–0.760	–0.800	ns
		t_H	0.874	0.994	1.107	1.020	1.063	ns
	GCLK PLL	t_{SU}	1.551	1.692	1.793	1.706	1.793	ns
		t_H	–1.058	–1.128	–1.170	–1.140	–1.211	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–0.649	–0.733	–0.814	–0.760	–0.800	ns
		t_H	0.874	0.994	1.107	1.020	1.063	ns
	GCLK PLL	t_{SU}	1.551	1.692	1.793	1.706	1.793	ns
		t_H	–1.058	–1.128	–1.170	–1.140	–1.211	ns
3.0-V PCI	GCLK	t_{SU}	–1.026	–1.154	–1.270	–1.169	–1.187	ns
		t_H	1.251	1.415	1.563	1.429	1.450	ns
	GCLK PLL	t_{SU}	1.167	1.265	1.330	1.291	1.398	ns
		t_H	–0.675	–0.700	–0.706	–0.725	–0.816	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.026	–1.154	–1.270	–1.169	–1.187	ns
		t_H	1.251	1.415	1.563	1.429	1.450	ns
	GCLK PLL	t_{SU}	1.167	1.265	1.330	1.291	1.398	ns
		t_H	–0.675	–0.700	–0.706	–0.725	–0.816	ns

Table 1–47. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–0.991	–1.103	–1.202	–1.117	–1.133	ns
		t_H	1.214	1.363	1.493	1.376	1.395	ns
	GCLK PLL	t_{SU}	1.176	1.289	1.372	1.315	1.427	ns
		t_H	–0.685	–0.726	–0.750	–0.750	–0.847	ns
3.3-V LVCMOS	GCLK	t_{SU}	–0.991	–1.103	–1.202	–1.117	–1.133	ns
		t_H	1.214	1.363	1.493	1.376	1.395	ns
	GCLK PLL	t_{SU}	1.176	1.289	1.372	1.315	1.427	ns
		t_H	–0.685	–0.726	–0.750	–0.750	–0.847	ns

Table 1–47. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVTTL	GCLK	t_{SU}	–0.986	–1.099	–1.204	–1.114	–1.131	ns
		t_{H}	1.209	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.181	1.293	1.370	1.318	1.429	ns
		t_{H}	–0.690	–0.730	–0.748	–0.753	–0.849	ns
3.0-V LVCMOS	GCLK	t_{SU}	–0.986	–1.099	–1.204	–1.114	–1.131	ns
		t_{H}	1.209	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.181	1.293	1.370	1.318	1.429	ns
		t_{H}	–0.690	–0.730	–0.748	–0.753	–0.849	ns
2.5 V	GCLK	t_{SU}	–0.953	–1.072	–1.184	–1.087	–1.107	ns
		t_{H}	1.176	1.332	1.475	1.346	1.369	ns
	GCLK PLL	t_{SU}	1.214	1.320	1.390	1.345	1.453	ns
		t_{H}	–0.723	–0.757	–0.768	–0.780	–0.873	ns
1.8 V	GCLK	t_{SU}	–0.851	–1.005	–1.147	–1.018	–1.033	ns
		t_{H}	1.074	1.265	1.438	1.277	1.295	ns
	GCLK PLL	t_{SU}	1.306	1.377	1.417	1.404	1.517	ns
		t_{H}	–0.815	–0.814	–0.795	–0.839	–0.937	ns
1.5 V	GCLK	t_{SU}	–0.786	–0.918	–1.036	–0.934	–0.954	ns
		t_{H}	1.009	1.178	1.327	1.193	1.216	ns
	GCLK PLL	t_{SU}	1.371	1.464	1.528	1.488	1.596	ns
		t_{H}	–0.880	–0.901	–0.906	–0.923	–1.016	ns
1.2 V	GCLK	t_{SU}	–0.649	–0.739	–0.831	–0.760	–0.788	ns
		t_{H}	0.872	0.999	1.122	1.019	1.050	ns
	GCLK PLL	t_{SU}	1.508	1.643	1.733	1.662	1.762	ns
		t_{H}	–1.017	–1.080	–1.111	–1.097	–1.182	ns
SSTL-2 Class I	GCLK	t_{SU}	–0.901	–1.058	–1.210	–1.067	–1.080	ns
		t_{H}	1.124	1.317	1.501	1.326	1.341	ns
	GCLK PLL	t_{SU}	1.296	1.366	1.392	1.397	1.512	ns
		t_{H}	–0.805	–0.802	–0.770	–0.832	–0.931	ns
SSTL-2 Class II	GCLK	t_{SU}	–0.901	–1.058	–1.210	–1.067	–1.080	ns
		t_{H}	1.124	1.317	1.501	1.326	1.341	ns
	GCLK PLL	t_{SU}	1.296	1.366	1.392	1.397	1.512	ns
		t_{H}	–0.805	–0.802	–0.770	–0.832	–0.931	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.724	–0.837	–0.928	–0.853	–0.875	ns
		t_{H}	0.947	1.096	1.219	1.112	1.136	ns
	GCLK PLL	t_{SU}	1.463	1.577	1.664	1.601	1.707	ns
		t_{H}	–0.972	–1.013	–1.042	–1.036	–1.126	ns

Table 1–47. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	GCLK	t_{SU}	–0.724	–0.837	–0.928	–0.853	–0.875	ns
		t_H	0.947	1.096	1.219	1.112	1.136	ns
	GCLK PLL	t_{SU}	1.463	1.577	1.664	1.601	1.707	ns
		t_H	–0.972	–1.013	–1.042	–1.036	–1.126	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–0.724	–0.837	–0.928	–0.853	–0.875	ns
		t_H	0.947	1.096	1.219	1.112	1.136	ns
	GCLK PLL	t_{SU}	1.463	1.577	1.664	1.601	1.707	ns
		t_H	–0.972	–1.013	–1.042	–1.036	–1.126	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.724	–0.837	–0.928	–0.853	–0.875	ns
		t_H	0.947	1.096	1.219	1.112	1.136	ns
	GCLK PLL	t_{SU}	1.463	1.577	1.664	1.601	1.707	ns
		t_H	–0.972	–1.013	–1.042	–1.036	–1.126	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–0.822	–0.943	–1.047	–0.960	–0.979	ns
		t_H	1.045	1.202	1.338	1.219	1.240	ns
	GCLK PLL	t_{SU}	1.365	1.471	1.545	1.494	1.603	ns
		t_H	–0.874	–0.907	–0.923	–0.929	–1.022	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–0.822	–0.943	–1.047	–0.960	–0.979	ns
		t_H	1.045	1.202	1.338	1.219	1.240	ns
	GCLK PLL	t_{SU}	1.365	1.471	1.545	1.494	1.603	ns
		t_H	–0.874	–0.907	–0.923	–0.929	–1.022	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.623	–0.699	–0.776	–0.725	–0.763	ns
		t_H	0.846	0.958	1.067	0.984	1.024	ns
	GCLK PLL	t_{SU}	1.564	1.715	1.816	1.729	1.819	ns
		t_H	–1.073	–1.151	–1.194	–1.164	–1.238	ns
3.0-V PCI	GCLK	t_{SU}	–0.986	–1.099	–1.204	–1.114	–1.131	ns
		t_H	1.209	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.181	1.293	1.370	1.318	1.429	ns
		t_H	–0.690	–0.730	–0.748	–0.753	–0.849	ns
3.0-V PCI-X	GCLK	t_{SU}	–0.986	–1.099	–1.204	–1.114	–1.131	ns
		t_H	1.209	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.181	1.293	1.370	1.318	1.429	ns
		t_H	–0.690	–0.730	–0.748	–0.753	–0.849	ns

Table 1–48. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	4.765	5.294	5.814	5.368	5.495	ns
		GCLK PLL	t_{CO}	2.854	3.192	3.558	3.228	3.241	ns
	8 mA	GCLK	t_{CO}	4.449	4.961	5.466	5.024	5.131	ns
		GCLK PLL	t_{CO}	2.538	2.859	3.210	2.884	2.877	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.514	5.034	5.541	5.103	5.219	ns
		GCLK PLL	t_{CO}	2.603	2.932	3.285	2.963	2.965	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	4.576	5.099	5.615	5.171	5.292	ns
		GCLK PLL	t_{CO}	2.665	2.997	3.359	3.031	3.038	ns
	8 mA	GCLK	t_{CO}	4.385	4.900	5.406	4.965	5.075	ns
		GCLK PLL	t_{CO}	2.474	2.798	3.150	2.825	2.821	ns
	12 mA	GCLK	t_{CO}	4.328	4.832	5.327	4.891	4.997	ns
		GCLK PLL	t_{CO}	2.417	2.730	3.071	2.751	2.743	ns
	16 mA	GCLK	t_{CO}	4.299	4.799	5.289	4.858	4.961	ns
		GCLK PLL	t_{CO}	2.388	2.697	3.033	2.718	2.707	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.392	4.907	5.413	4.972	5.082	ns
		GCLK PLL	t_{CO}	2.481	2.805	3.157	2.832	2.828	ns
	8 mA	GCLK	t_{CO}	4.298	4.800	5.293	4.859	4.963	ns
		GCLK PLL	t_{CO}	2.387	2.698	3.037	2.719	2.709	ns
	12 mA	GCLK	t_{CO}	4.266	4.768	5.260	4.827	4.930	ns
		GCLK PLL	t_{CO}	2.355	2.666	3.004	2.687	2.676	ns
	16 mA	GCLK	t_{CO}	4.252	4.755	5.248	4.814	4.917	ns
		GCLK PLL	t_{CO}	2.341	2.653	2.992	2.674	2.663	ns
2.5 V	4 mA	GCLK	t_{CO}	4.679	5.205	5.733	5.287	5.432	ns
		GCLK PLL	t_{CO}	2.768	3.103	3.477	3.147	3.178	ns
	8 mA	GCLK	t_{CO}	4.498	5.025	5.548	5.095	5.216	ns
		GCLK PLL	t_{CO}	2.587	2.923	3.292	2.955	2.962	ns
	12 mA	GCLK	t_{CO}	4.426	4.942	5.453	5.007	5.120	ns
		GCLK PLL	t_{CO}	2.515	2.840	3.197	2.867	2.866	ns
	16 mA	GCLK	t_{CO}	4.396	4.913	5.424	4.976	5.087	ns
		GCLK PLL	t_{CO}	2.485	2.811	3.168	2.836	2.833	ns

Table 1–48. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8 V	2 mA	GCLK	t_{CO}	5.633	6.290	6.954	6.380	6.550	ns
		GCLK PLL	t_{CO}	3.722	4.188	4.698	4.240	4.296	ns
	4 mA	GCLK	t_{CO}	5.262	5.897	6.541	5.981	6.120	ns
		GCLK PLL	t_{CO}	3.351	3.795	4.285	3.841	3.866	ns
	6 mA	GCLK	t_{CO}	5.069	5.681	6.301	5.757	5.887	ns
		GCLK PLL	t_{CO}	3.158	3.579	4.045	3.617	3.633	ns
	8 mA	GCLK	t_{CO}	5.008	5.610	6.215	5.683	5.809	ns
		GCLK PLL	t_{CO}	3.097	3.508	3.959	3.543	3.555	ns
	10 mA	GCLK	t_{CO}	4.949	5.548	6.155	5.621	5.747	ns
		GCLK PLL	t_{CO}	3.038	3.446	3.899	3.481	3.493	ns
	12 mA	GCLK	t_{CO}	4.902	5.498	6.091	5.567	5.689	ns
		GCLK PLL	t_{CO}	2.991	3.396	3.835	3.427	3.435	ns
	16 mA	GCLK	t_{CO}	4.860	5.456	6.053	5.526	5.646	ns
		GCLK PLL	t_{CO}	2.949	3.354	3.797	3.386	3.392	ns
1.5 V	2 mA	GCLK	t_{CO}	6.120	6.905	7.739	6.992	7.136	ns
		GCLK PLL	t_{CO}	4.209	4.803	5.483	4.852	4.882	ns
	4 mA	GCLK	t_{CO}	5.714	6.433	7.191	6.517	6.647	ns
		GCLK PLL	t_{CO}	3.803	4.331	4.935	4.377	4.393	ns
	6 mA	GCLK	t_{CO}	5.573	6.290	7.034	6.369	6.492	ns
		GCLK PLL	t_{CO}	3.662	4.188	4.778	4.229	4.238	ns
	8 mA	GCLK	t_{CO}	5.487	6.176	6.900	6.257	6.378	ns
		GCLK PLL	t_{CO}	3.576	4.074	4.644	4.117	4.124	ns
	10 mA	GCLK	t_{CO}	5.449	6.138	6.851	6.209	6.326	ns
		GCLK PLL	t_{CO}	3.538	4.036	4.595	4.069	4.072	ns
	12mA	GCLK	t_{CO}	5.416	6.103	6.809	6.175	6.292	ns
		GCLK PLL	t_{CO}	3.505	4.001	4.553	4.035	4.038	ns
	16 mA	GCLK	t_{CO}	5.308	5.985	6.676	6.055	6.168	ns
		GCLK PLL	t_{CO}	3.397	3.883	4.420	3.915	3.914	ns

Table 1–48. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.2 V	2 mA	GCLK	t_{CO}	7.251	8.323	9.514	8.370	8.447	ns
		GCLK PLL	t_{CO}	5.340	6.221	7.258	6.230	6.193	ns
	4 mA	GCLK	t_{CO}	6.893	7.909	9.032	7.953	8.026	ns
		GCLK PLL	t_{CO}	4.982	5.807	6.776	5.813	5.772	ns
	6 mA	GCLK	t_{CO}	6.757	7.746	8.835	7.791	7.863	ns
		GCLK PLL	t_{CO}	4.846	5.644	6.579	5.651	5.609	ns
	8 mA	GCLK	t_{CO}	6.697	7.678	8.759	7.722	7.793	ns
		GCLK PLL	t_{CO}	4.786	5.576	6.503	5.582	5.539	ns
	10 mA	GCLK	t_{CO}	6.566	7.509	8.536	7.550	7.618	ns
		GCLK PLL	t_{CO}	4.655	5.407	6.280	5.410	5.364	ns
	12 mA	GCLK	t_{CO}	6.549	7.492	8.521	7.532	7.600	ns
		GCLK PLL	t_{CO}	4.638	5.390	6.265	5.392	5.346	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.441	4.956	5.464	5.017	5.125	ns
		GCLK PLL	t_{CO}	2.530	2.854	3.208	2.877	2.871	ns
	12 mA	GCLK	t_{CO}	4.421	4.934	5.441	4.995	5.103	ns
		GCLK PLL	t_{CO}	2.510	2.832	3.185	2.855	2.849	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.386	4.895	5.398	4.955	5.061	ns
		GCLK PLL	t_{CO}	2.475	2.793	3.142	2.815	2.807	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	4.858	5.440	6.025	5.507	5.624	ns
		GCLK PLL	t_{CO}	2.947	3.338	3.769	3.367	3.370	ns
	10 mA	GCLK	t_{CO}	4.834	5.409	5.986	5.477	5.594	ns
		GCLK PLL	t_{CO}	2.923	3.307	3.730	3.337	3.340	ns
	12 mA	GCLK	t_{CO}	4.831	5.408	5.982	5.475	5.589	ns
		GCLK PLL	t_{CO}	2.920	3.306	3.726	3.335	3.335	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.816	5.390	5.967	5.457	5.573	ns
		GCLK PLL	t_{CO}	2.905	3.288	3.711	3.317	3.319	ns
	16 mA	GCLK	t_{CO}	4.803	5.378	5.953	5.444	5.559	ns
		GCLK PLL	t_{CO}	2.892	3.276	3.697	3.304	3.305	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	4.842	5.416	5.992	5.483	5.600	ns
		GCLK PLL	t_{CO}	2.931	3.314	3.736	3.343	3.346	ns
	10 mA	GCLK	t_{CO}	4.835	5.412	5.990	5.478	5.593	ns
		GCLK PLL	t_{CO}	2.924	3.310	3.734	3.338	3.339	ns
	12 mA	GCLK	t_{CO}	4.821	5.393	5.967	5.460	5.575	ns
		GCLK PLL	t_{CO}	2.910	3.291	3.711	3.320	3.321	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.802	5.371	5.941	5.437	5.550	ns
		GCLK PLL	t_{CO}	2.891	3.269	3.685	3.297	3.296	ns

Table 1–48. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.340	6.003	6.689	6.073	6.185	ns
		GCLK PLL	t_{CO}	3.429	3.901	4.433	3.933	3.931	ns
	10 mA	GCLK	t_{CO}	5.336	5.993	6.674	6.065	6.176	ns
		GCLK PLL	t_{CO}	3.425	3.891	4.418	3.925	3.922	ns
	12 mA	GCLK	t_{CO}	5.329	5.990	6.672	6.061	6.171	ns
		GCLK PLL	t_{CO}	3.418	3.888	4.416	3.921	3.917	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.294	5.944	6.616	6.015	6.125	ns
		GCLK PLL	t_{CO}	3.383	3.842	4.360	3.875	3.871	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.519	7.456	8.484	7.496	7.563	ns
		GCLK PLL	t_{CO}	4.608	5.354	6.228	5.356	5.309	ns
	10 mA	GCLK	t_{CO}	6.442	7.346	8.325	7.385	7.452	ns
		GCLK PLL	t_{CO}	4.531	5.244	6.069	5.245	5.198	ns
	12 mA	GCLK	t_{CO}	6.444	7.348	8.329	7.388	7.455	ns
		GCLK PLL	t_{CO}	4.533	5.246	6.073	5.248	5.201	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.382	7.275	8.257	7.317	7.388	ns
		GCLK PLL	t_{CO}	4.471	5.173	6.001	5.177	5.134	ns
3.0-V PCI	—	GCLK	t_{CO}	4.561	5.070	5.570	5.133	5.242	ns
		GCLK PLL	t_{CO}	2.650	2.968	3.314	2.993	2.988	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.561	5.070	5.570	5.133	5.242	ns
		GCLK PLL	t_{CO}	2.650	2.968	3.314	2.993	2.988	ns

Table 1–49. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	8.807	9.564	10.320	9.743	10.043	ns
		GCLK PLL	t_{CO}	3.054	3.403	3.771	3.446	3.463	ns
	8 mA	GCLK	t_{CO}	6.397	6.981	7.593	7.082	7.269	ns
		GCLK PLL	t_{CO}	2.607	2.940	3.290	2.972	2.967	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	7.180	7.798	8.379	7.935	8.216	ns
		GCLK PLL	t_{CO}	2.701	3.027	3.381	3.063	3.069	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	7.611	8.243	8.867	8.414	8.718	ns
		GCLK PLL	t_{CO}	2.806	3.126	3.471	3.161	3.175	ns
	8 mA	GCLK	t_{CO}	6.055	6.630	7.221	6.745	6.948	ns
		GCLK PLL	t_{CO}	2.550	2.871	3.211	2.899	2.896	ns
	12 mA	GCLK	t_{CO}	5.407	5.979	6.525	6.070	6.219	ns
		GCLK PLL	t_{CO}	2.434	2.745	3.084	2.768	2.761	ns
	16 mA	GCLK	t_{CO}	5.053	5.579	6.103	5.658	5.809	ns
		GCLK PLL	t_{CO}	2.385	2.690	3.017	2.712	2.700	ns

Table 1–49. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.054	6.628	7.219	6.742	6.945	ns
		GCLK PLL	t_{CO}	2.548	2.870	3.209	2.897	2.895	ns
	8 mA	GCLK	t_{CO}	5.082	5.613	6.147	5.696	5.852	ns
		GCLK PLL	t_{CO}	2.386	2.693	3.021	2.714	2.702	ns
	12 mA	GCLK	t_{CO}	4.773	5.291	5.798	5.359	5.482	ns
		GCLK PLL	t_{CO}	2.346	2.653	2.981	2.674	2.662	ns
	16 mA	GCLK	t_{CO}	4.597	5.111	5.618	5.178	5.302	ns
		GCLK PLL	t_{CO}	2.325	2.633	2.962	2.654	2.641	ns
2.5 V	4 mA	GCLK	t_{CO}	7.790	8.488	9.191	8.685	9.009	ns
		GCLK PLL	t_{CO}	2.932	3.266	3.629	3.309	3.343	ns
	8 mA	GCLK	t_{CO}	6.184	6.799	7.419	6.920	7.120	ns
		GCLK PLL	t_{CO}	2.663	2.996	3.352	3.027	3.033	ns
	12 mA	GCLK	t_{CO}	5.535	6.124	6.697	6.219	6.380	ns
		GCLK PLL	t_{CO}	2.548	2.876	3.229	2.904	2.905	ns
	16 mA	GCLK	t_{CO}	5.229	5.797	6.363	5.887	6.041	ns
		GCLK PLL	t_{CO}	2.495	2.820	3.170	2.847	2.843	ns
1.8 V	2 mA	GCLK	t_{CO}	12.035	13.209	14.450	13.527	14.058	ns
		GCLK PLL	t_{CO}	4.093	4.563	5.086	4.640	4.720	ns
	4 mA	GCLK	t_{CO}	8.644	9.561	10.524	9.725	10.005	ns
		GCLK PLL	t_{CO}	3.537	3.993	4.494	4.045	4.076	ns
	6 mA	GCLK	t_{CO}	7.322	8.117	8.940	8.258	8.494	ns
		GCLK PLL	t_{CO}	3.275	3.699	4.162	3.744	3.767	ns
	8 mA	GCLK	t_{CO}	6.662	7.398	8.152	7.516	7.711	ns
		GCLK PLL	t_{CO}	3.159	3.570	4.017	3.610	3.625	ns
	10 mA	GCLK	t_{CO}	6.313	7.029	7.767	7.133	7.317	ns
		GCLK PLL	t_{CO}	3.098	3.516	3.970	3.555	3.568	ns
	12 mA	GCLK	t_{CO}	6.010	6.701	7.396	6.799	6.969	ns
		GCLK PLL	t_{CO}	3.037	3.440	3.881	3.477	3.487	ns
	16 mA	GCLK	t_{CO}	5.704	6.365	7.040	6.459	6.617	ns
		GCLK PLL	t_{CO}	2.993	3.391	3.825	3.426	3.432	ns

Table 1–49. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	2 mA	GCLK	t_{CO}	11.401	12.761	14.246	12.948	13.259	ns
		GCLK PLL	t_{CO}	4.506	5.134	5.839	5.189	5.225	ns
	4 mA	GCLK	t_{CO}	8.342	9.354	10.423	9.481	9.693	ns
		GCLK PLL	t_{CO}	3.946	4.491	5.095	4.535	4.550	ns
	6 mA	GCLK	t_{CO}	7.327	8.232	9.189	8.343	8.524	ns
		GCLK PLL	t_{CO}	3.756	4.286	4.879	4.326	4.336	ns
	8 mA	GCLK	t_{CO}	6.819	7.661	8.540	7.759	7.927	ns
		GCLK PLL	t_{CO}	3.658	4.176	4.741	4.214	4.223	ns
	10 mA	GCLK	t_{CO}	6.501	7.316	8.157	7.408	7.562	ns
		GCLK PLL	t_{CO}	3.591	4.104	4.671	4.141	4.149	ns
	12 mA	GCLK	t_{CO}	6.298	7.087	7.899	7.175	7.323	ns
		GCLK PLL	t_{CO}	3.552	4.053	4.607	4.089	4.093	ns
	16 mA	GCLK	t_{CO}	5.956	6.699	7.451	6.782	6.915	ns
		GCLK PLL	t_{CO}	3.479	3.970	4.516	4.005	4.003	ns
1.2 V	2 mA	GCLK	t_{CO}	11.610	13.339	15.330	13.421	13.556	ns
		GCLK PLL	t_{CO}	5.595	6.513	7.588	6.524	6.488	ns
	4 mA	GCLK	t_{CO}	8.993	10.323	11.824	10.383	10.485	ns
		GCLK PLL	t_{CO}	5.103	5.945	6.927	5.952	5.910	ns
	6 mA	GCLK	t_{CO}	8.199	9.404	10.754	9.459	9.553	ns
		GCLK PLL	t_{CO}	4.949	5.762	6.712	5.769	5.727	ns
	8 mA	GCLK	t_{CO}	7.786	8.930	10.205	8.982	9.070	ns
		GCLK PLL	t_{CO}	4.861	5.664	6.599	5.670	5.626	ns
	10 mA	GCLK	t_{CO}	7.445	8.519	9.703	8.567	8.648	ns
		GCLK PLL	t_{CO}	4.738	5.515	6.413	5.522	5.475	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.481	4.992	5.490	5.054	5.162	ns
		GCLK PLL	t_{CO}	2.551	2.872	3.218	2.895	2.888	ns
	12 mA	GCLK	t_{CO}	4.448	4.958	5.454	5.020	5.126	ns
		GCLK PLL	t_{CO}	2.518	2.838	3.182	2.861	2.852	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.398	4.904	5.397	4.965	5.069	ns
		GCLK PLL	t_{CO}	2.468	2.784	3.125	2.806	2.795	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	4.888	5.466	6.043	5.535	5.651	ns
		GCLK PLL	t_{CO}	2.958	3.346	3.771	3.376	3.377	ns
	10 mA	GCLK	t_{CO}	4.869	5.443	6.013	5.512	5.628	ns
		GCLK PLL	t_{CO}	2.939	3.323	3.741	3.353	3.354	ns
	12 mA	GCLK	t_{CO}	4.846	5.418	5.986	5.487	5.603	ns
		GCLK PLL	t_{CO}	2.916	3.298	3.714	3.328	3.329	ns

Table 1–49. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.839	5.411	5.979	5.478	5.593	ns
		GCLK PLL	t_{CO}	2.909	3.291	3.707	3.319	3.319	ns
	16 mA	GCLK	t_{CO}	4.823	5.396	5.965	5.464	5.578	ns
		GCLK PLL	t_{CO}	2.893	3.276	3.693	3.305	3.304	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	4.868	5.438	6.004	5.506	5.620	ns
		GCLK PLL	t_{CO}	2.938	3.318	3.732	3.347	3.346	ns
	10 mA	GCLK	t_{CO}	4.861	5.434	6.003	5.501	5.615	ns
		GCLK PLL	t_{CO}	2.931	3.314	3.731	3.342	3.341	ns
	12 mA	GCLK	t_{CO}	4.850	5.420	5.985	5.488	5.602	ns
		GCLK PLL	t_{CO}	2.920	3.300	3.713	3.329	3.328	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.817	5.382	5.943	5.449	5.561	ns
		GCLK PLL	t_{CO}	2.887	3.262	3.671	3.290	3.287	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.373	6.037	6.712	6.105	6.216	ns
		GCLK PLL	t_{CO}	3.443	3.917	4.440	3.946	3.942	ns
	10 mA	GCLK	t_{CO}	5.371	6.033	6.704	6.102	6.213	ns
		GCLK PLL	t_{CO}	3.441	3.913	4.432	3.943	3.939	ns
	12 mA	GCLK	t_{CO}	5.361	6.026	6.700	6.094	6.205	ns
		GCLK PLL	t_{CO}	3.431	3.906	4.428	3.935	3.931	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.323	5.980	6.646	6.047	6.156	ns
		GCLK PLL	t_{CO}	3.393	3.860	4.374	3.888	3.882	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.566	7.505	8.527	7.545	7.612	ns
		GCLK PLL	t_{CO}	4.636	5.385	6.255	5.386	5.338	ns
	10 mA	GCLK	t_{CO}	6.481	7.389	8.366	7.429	7.494	ns
		GCLK PLL	t_{CO}	4.551	5.269	6.094	5.270	5.220	ns
3.0-V PCI	—	GCLK	t_{CO}	4.959	5.502	6.048	5.578	5.714	ns
		GCLK PLL	t_{CO}	2.643	2.957	3.293	2.982	2.974	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.959	5.502	6.048	5.578	5.714	ns
		GCLK PLL	t_{CO}	2.643	2.957	3.293	2.982	2.974	ns

Table 1–50. EP3C5 Column Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–0.993	–1.124	–1.255	–1.153	–1.170	ns
	—		t_{H}	1.243	1.414	1.580	1.441	1.461	ns
	—	GCLK PLL	t_{SU}	1.195	1.289	1.339	1.301	1.411	ns
	—		t_{H}	–0.677	–0.695	–0.683	–0.706	–0.801	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns

Table 1–50. EP3C5 Column Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
BLVDS	—	GCLK	t_{SU}	–0.964	–1.092	–1.214	–1.117	–1.133	ns
	—		t_{H}	1.212	1.380	1.537	1.404	1.422	ns
	—	GCLK PLL	t_{SU}	1.221	1.319	1.376	1.333	1.445	ns
	—		t_{H}	–0.704	–0.727	–0.722	–0.740	–0.837	ns
	8 mA	GCLK	t_{CO}	4.688	5.207	5.710	5.271	5.379	ns
		GCLK PLL	t_{CO}	2.768	3.096	3.448	3.123	3.116	ns
	12 mA	GCLK	t_{CO}	4.688	5.207	5.710	5.271	5.379	ns
		GCLK PLL	t_{CO}	2.768	3.096	3.448	3.123	3.116	ns
	16 mA	GCLK	t_{CO}	4.688	5.207	5.710	5.271	5.379	ns
		GCLK PLL	t_{CO}	2.768	3.096	3.448	3.123	3.116	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.310	4.800	5.280	4.858	4.961	ns
	—	GCLK PLL	t_{CO}	2.395	2.695	3.020	2.714	2.703	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns

Table 1–51. EP3C5 Row Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–0.966	–1.094	–1.217	–1.120	–1.136	ns
	—		t_{H}	1.215	1.382	1.540	1.407	1.425	ns
	—		t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{SU}	1.223	1.321	1.379	1.336	1.448	ns
	—		t_{H}	–0.707	–0.729	–0.725	–0.743	–0.840	ns
	—		t_{CO}	1.715	1.980	2.226	1.899	1.837	ns
BLVDS	—	GCLK	t_{SU}	–0.966	–1.094	–1.217	–1.120	–1.136	ns
	—		t_{H}	1.215	1.382	1.540	1.407	1.425	ns
	—	GCLK PLL	t_{SU}	1.223	1.321	1.379	1.336	1.448	ns
	—		t_{H}	–0.707	–0.729	–0.725	–0.743	–0.840	ns
	8 mA	GCLK	t_{CO}	4.687	5.205	5.710	5.270	5.378	ns
		GCLK PLL	t_{CO}	2.769	3.098	3.448	3.124	3.117	ns
	12 mA	GCLK	t_{CO}	4.687	5.205	5.710	5.270	5.378	ns
		GCLK PLL	t_{CO}	2.769	3.098	3.448	3.124	3.117	ns
	16 mA	GCLK	t_{CO}	4.687	5.205	5.710	5.270	5.378	ns
		GCLK PLL	t_{CO}	2.769	3.098	3.448	3.124	3.117	ns

Table 1–51. EP3C5 Row Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
mini-LVDS	—	GCLK	t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{CO}	1.715	1.980	2.226	1.899	1.837	ns
PPDS	—	GCLK	t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{CO}	1.715	1.980	2.226	1.899	1.837	ns
RSDS	—	GCLK	t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{CO}	1.715	1.980	2.226	1.899	1.837	ns

EP3C10 I/O Timing Parameters

Table 1–52 through Table 1–57 show the maximum I/O timing parameters for EP3C10 devices.

Table 1–52. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.023	–1.147	–1.256	–1.160	–1.179	ns
		t_{H}	1.248	1.408	1.549	1.421	1.442	ns
	GCLK PLL	t_{SU}	1.149	1.251	1.323	1.279	1.387	ns
		t_{H}	–0.656	–0.687	–0.700	–0.713	–0.806	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.023	–1.147	–1.256	–1.160	–1.179	ns
		t_{H}	1.248	1.408	1.549	1.421	1.442	ns
	GCLK PLL	t_{SU}	1.149	1.251	1.323	1.279	1.387	ns
		t_{H}	–0.656	–0.687	–0.700	–0.713	–0.806	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.015	–1.144	–1.259	–1.158	–1.177	ns
		t_{H}	1.240	1.405	1.552	1.419	1.440	ns
	GCLK PLL	t_{SU}	1.157	1.254	1.320	1.281	1.389	ns
		t_{H}	–0.664	–0.690	–0.697	–0.715	–0.808	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.015	–1.144	–1.259	–1.158	–1.177	ns
		t_{H}	1.240	1.405	1.552	1.419	1.440	ns
	GCLK PLL	t_{SU}	1.157	1.254	1.320	1.281	1.389	ns
		t_{H}	–0.664	–0.690	–0.697	–0.715	–0.808	ns
2.5 V	GCLK	t_{SU}	–0.984	–1.117	–1.234	–1.132	–1.152	ns
		t_{H}	1.209	1.378	1.527	1.393	1.415	ns
	GCLK PLL	t_{SU}	1.188	1.281	1.345	1.307	1.414	ns
		t_{H}	–0.695	–0.717	–0.722	–0.741	–0.833	ns
1.8 V	GCLK	t_{SU}	–0.881	–1.050	–1.197	–1.062	–1.081	ns
		t_{H}	1.106	1.311	1.490	1.323	1.344	ns
	GCLK PLL	t_{SU}	1.291	1.348	1.382	1.377	1.485	ns
		t_{H}	–0.798	–0.784	–0.759	–0.811	–0.904	ns

Table 1–52. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	GCLK	t_{SU}	–0.817	–0.963	–1.085	–0.978	–1.001	ns
		t_{H}	1.042	1.224	1.378	1.239	1.264	ns
	GCLK PLL	t_{SU}	1.355	1.435	1.494	1.461	1.565	ns
		t_{H}	–0.862	–0.871	–0.871	–0.895	–0.984	ns
1.2 V	GCLK	t_{SU}	–0.684	–0.785	–0.881	–0.805	–0.836	ns
		t_{H}	0.909	1.046	1.174	1.066	1.099	ns
	GCLK PLL	t_{SU}	1.488	1.613	1.698	1.634	1.730	ns
		t_{H}	–0.995	–1.049	–1.075	–1.068	–1.149	ns
SSTL-2 Class I	GCLK	t_{SU}	–0.905	–1.081	–1.240	–1.092	–1.107	ns
		t_{H}	1.130	1.342	1.533	1.353	1.370	ns
	GCLK PLL	t_{SU}	1.267	1.317	1.339	1.347	1.459	ns
		t_{H}	–0.774	–0.753	–0.716	–0.781	–0.878	ns
SSTL-2 Class II	GCLK	t_{SU}	–0.905	–1.081	–1.240	–1.092	–1.107	ns
		t_{H}	1.130	1.342	1.533	1.353	1.370	ns
	GCLK PLL	t_{SU}	1.267	1.317	1.339	1.347	1.459	ns
		t_{H}	–0.774	–0.753	–0.716	–0.781	–0.878	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.735	–0.860	–0.957	–0.876	–0.900	ns
		t_{H}	0.960	1.121	1.250	1.137	1.163	ns
	GCLK PLL	t_{SU}	1.437	1.538	1.622	1.563	1.666	ns
		t_{H}	–0.944	–0.974	–0.999	–0.997	–1.085	ns
SSTL-18 Class II	GCLK	t_{SU}	–0.735	–0.860	–0.957	–0.876	–0.900	ns
		t_{H}	0.960	1.121	1.250	1.137	1.163	ns
	GCLK PLL	t_{SU}	1.437	1.538	1.622	1.563	1.666	ns
		t_{H}	–0.944	–0.974	–0.999	–0.997	–1.085	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–0.735	–0.860	–0.957	–0.876	–0.900	ns
		t_{H}	0.960	1.121	1.250	1.137	1.163	ns
	GCLK PLL	t_{SU}	1.437	1.538	1.622	1.563	1.666	ns
		t_{H}	–0.944	–0.974	–0.999	–0.997	–1.085	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.735	–0.860	–0.957	–0.876	–0.900	ns
		t_{H}	0.960	1.121	1.250	1.137	1.163	ns
	GCLK PLL	t_{SU}	1.437	1.538	1.622	1.563	1.666	ns
		t_{H}	–0.944	–0.974	–0.999	–0.997	–1.085	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–0.826	–0.968	–1.085	–0.984	–1.005	ns
		t_{H}	1.051	1.229	1.378	1.245	1.268	ns
	GCLK PLL	t_{SU}	1.346	1.430	1.494	1.455	1.561	ns
		t_{H}	–0.853	–0.866	–0.871	–0.889	–0.980	ns

Table 1–52. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5-V HSTL Class II	GCLK	t_{SU}	–0.826	–0.968	–1.085	–0.984	–1.005	ns
		t_H	1.051	1.229	1.378	1.245	1.268	ns
	GCLK PLL	t_{SU}	1.346	1.430	1.494	1.455	1.561	ns
		t_H	–0.853	–0.866	–0.871	–0.889	–0.980	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.638	–0.723	–0.803	–0.749	–0.790	ns
		t_H	0.863	0.984	1.096	1.010	1.053	ns
	GCLK PLL	t_{SU}	1.534	1.675	1.776	1.690	1.776	ns
		t_H	–1.041	–1.111	–1.153	–1.124	–1.195	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–0.638	–0.723	–0.803	–0.749	–0.790	ns
		t_H	0.863	0.984	1.096	1.010	1.053	ns
	GCLK PLL	t_{SU}	1.534	1.675	1.776	1.690	1.776	ns
		t_H	–1.041	–1.111	–1.153	–1.124	–1.195	ns
3.0-V PCI	GCLK	t_{SU}	–1.015	–1.144	–1.259	–1.158	–1.177	ns
		t_H	1.240	1.405	1.552	1.419	1.440	ns
	GCLK PLL	t_{SU}	1.157	1.254	1.320	1.281	1.389	ns
		t_H	–0.664	–0.690	–0.697	–0.715	–0.808	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.015	–1.144	–1.259	–1.158	–1.177	ns
		t_H	1.240	1.405	1.552	1.419	1.440	ns
	GCLK PLL	t_{SU}	1.157	1.254	1.320	1.281	1.389	ns
		t_H	–0.664	–0.690	–0.697	–0.715	–0.808	ns

Table 1–53. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–0.993	–1.104	–1.202	–1.118	–1.135	ns
		t_H	1.215	1.363	1.493	1.376	1.395	ns
	GCLK PLL	t_{SU}	1.166	1.280	1.361	1.306	1.417	ns
		t_H	–0.674	–0.716	–0.738	–0.741	–0.837	ns
3.3-V LVCMOS	GCLK	t_{SU}	–0.993	–1.104	–1.202	–1.118	–1.135	ns
		t_H	1.215	1.363	1.493	1.376	1.395	ns
	GCLK PLL	t_{SU}	1.166	1.280	1.361	1.306	1.417	ns
		t_H	–0.674	–0.716	–0.738	–0.741	–0.837	ns
3.0-V LVTTL	GCLK	t_{SU}	–0.988	–1.100	–1.204	–1.115	–1.133	ns
		t_H	1.210	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.171	1.284	1.359	1.309	1.419	ns
		t_H	–0.679	–0.720	–0.736	–0.744	–0.839	ns

Table 1–53. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVCMOS	GCLK	t_{SU}	–0.988	–1.100	–1.204	–1.115	–1.133	ns
		t_{H}	1.210	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.171	1.284	1.359	1.309	1.419	ns
		t_{H}	–0.679	–0.720	–0.736	–0.744	–0.839	ns
2.5 V	GCLK	t_{SU}	–0.955	–1.073	–1.184	–1.088	–1.109	ns
		t_{H}	1.177	1.332	1.475	1.346	1.369	ns
	GCLK PLL	t_{SU}	1.204	1.311	1.379	1.336	1.443	ns
		t_{H}	–0.712	–0.747	–0.756	–0.771	–0.863	ns
1.8 V	GCLK	t_{SU}	–0.853	–1.006	–1.147	–1.019	–1.035	ns
		t_{H}	1.075	1.265	1.438	1.277	1.295	ns
	GCLK PLL	t_{SU}	1.296	1.368	1.406	1.395	1.507	ns
		t_{H}	–0.804	–0.804	–0.783	–0.830	–0.927	ns
1.5 V	GCLK	t_{SU}	–0.788	–0.919	–1.036	–0.935	–0.956	ns
		t_{H}	1.010	1.178	1.327	1.193	1.216	ns
	GCLK PLL	t_{SU}	1.361	1.455	1.517	1.479	1.586	ns
		t_{H}	–0.869	–0.891	–0.894	–0.914	–1.006	ns
1.2 V	GCLK	t_{SU}	–0.651	–0.740	–0.831	–0.761	–0.790	ns
		t_{H}	0.873	0.999	1.122	1.019	1.050	ns
	GCLK PLL	t_{SU}	1.498	1.634	1.722	1.653	1.752	ns
		t_{H}	–1.006	–1.070	–1.099	–1.088	–1.172	ns
SSTL-2 Class I	GCLK	t_{SU}	–0.883	–1.038	–1.191	–1.047	–1.061	ns
		t_{H}	1.105	1.297	1.482	1.305	1.321	ns
	GCLK PLL	t_{SU}	1.276	1.346	1.372	1.377	1.491	ns
		t_{H}	–0.784	–0.782	–0.749	–0.812	–0.911	ns
SSTL-2 Class II	GCLK	t_{SU}	–0.883	–1.038	–1.191	–1.047	–1.061	ns
		t_{H}	1.105	1.297	1.482	1.305	1.321	ns
	GCLK PLL	t_{SU}	1.276	1.346	1.372	1.377	1.491	ns
		t_{H}	–0.784	–0.782	–0.749	–0.812	–0.911	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.706	–0.817	–0.909	–0.833	–0.856	ns
		t_{H}	0.928	1.076	1.200	1.091	1.116	ns
	GCLK PLL	t_{SU}	1.443	1.557	1.644	1.581	1.686	ns
		t_{H}	–0.951	–0.993	–1.021	–1.016	–1.106	ns
SSTL-18 Class II	GCLK	t_{SU}	–0.706	–0.817	–0.909	–0.833	–0.856	ns
		t_{H}	0.928	1.076	1.200	1.091	1.116	ns
	GCLK PLL	t_{SU}	1.443	1.557	1.644	1.581	1.686	ns
		t_{H}	–0.951	–0.993	–1.021	–1.016	–1.106	ns

Table 1–53. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8-V HSTL Class I	GCLK	t_{SU}	–0.706	–0.817	–0.909	–0.833	–0.856	ns
		t_{H}	0.928	1.076	1.200	1.091	1.116	ns
	GCLK PLL	t_{SU}	1.443	1.557	1.644	1.581	1.686	ns
		t_{H}	–0.951	–0.993	–1.021	–1.016	–1.106	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.706	–0.817	–0.909	–0.833	–0.856	ns
		t_{H}	0.928	1.076	1.200	1.091	1.116	ns
	GCLK PLL	t_{SU}	1.443	1.557	1.644	1.581	1.686	ns
		t_{H}	–0.951	–0.993	–1.021	–1.016	–1.106	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–0.804	–0.923	–1.028	–0.940	–0.960	ns
		t_{H}	1.026	1.182	1.319	1.198	1.220	ns
	GCLK PLL	t_{SU}	1.345	1.451	1.525	1.474	1.582	ns
		t_{H}	–0.853	–0.887	–0.902	–0.909	–1.002	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–0.804	–0.923	–1.028	–0.940	–0.960	ns
		t_{H}	1.026	1.182	1.319	1.198	1.220	ns
	GCLK PLL	t_{SU}	1.345	1.451	1.525	1.474	1.582	ns
		t_{H}	–0.853	–0.887	–0.902	–0.909	–1.002	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.605	–0.679	–0.757	–0.705	–0.744	ns
		t_{H}	0.827	0.938	1.048	0.963	1.004	ns
	GCLK PLL	t_{SU}	1.544	1.695	1.796	1.709	1.798	ns
		t_{H}	–1.052	–1.131	–1.173	–1.144	–1.218	ns
3.0-V PCI	GCLK	t_{SU}	–0.988	–1.100	–1.204	–1.115	–1.133	ns
		t_{H}	1.210	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.171	1.284	1.359	1.309	1.419	ns
		t_{H}	–0.679	–0.720	–0.736	–0.744	–0.839	ns
3.0-V PCI-X	GCLK	t_{SU}	–0.988	–1.100	–1.204	–1.115	–1.133	ns
		t_{H}	1.210	1.359	1.495	1.373	1.393	ns
	GCLK PLL	t_{SU}	1.171	1.284	1.359	1.309	1.419	ns
		t_{H}	–0.679	–0.720	–0.736	–0.744	–0.839	ns

Table 1–54. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	4.770	5.298	5.817	5.371	5.499	ns
		GCLK PLL	t_{CO}	2.847	3.185	3.553	3.221	3.233	ns
	8 mA	GCLK	t_{CO}	4.454	4.965	5.469	5.027	5.135	ns
		GCLK PLL	t_{CO}	2.531	2.852	3.205	2.877	2.869	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.519	5.038	5.544	5.106	5.223	ns
		GCLK PLL	t_{CO}	2.596	2.925	3.280	2.956	2.957	ns

Table 1–54. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVTTL	4 mA	GCLK	t_{CO}	4.581	5.103	5.618	5.174	5.296	ns
		GCLK PLL	t_{CO}	2.658	2.990	3.354	3.024	3.030	ns
	8 mA	GCLK	t_{CO}	4.390	4.904	5.409	4.968	5.079	ns
		GCLK PLL	t_{CO}	2.467	2.791	3.145	2.818	2.813	ns
	12 mA	GCLK	t_{CO}	4.333	4.836	5.330	4.894	5.001	ns
		GCLK PLL	t_{CO}	2.410	2.723	3.066	2.744	2.735	ns
	16 mA	GCLK	t_{CO}	4.304	4.803	5.292	4.861	4.965	ns
		GCLK PLL	t_{CO}	2.381	2.690	3.028	2.711	2.699	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.397	4.911	5.416	4.975	5.086	ns
		GCLK PLL	t_{CO}	2.474	2.798	3.152	2.825	2.820	ns
	8 mA	GCLK	t_{CO}	4.303	4.804	5.296	4.862	4.967	ns
		GCLK PLL	t_{CO}	2.380	2.691	3.032	2.712	2.701	ns
	12 mA	GCLK	t_{CO}	4.271	4.772	5.263	4.830	4.934	ns
		GCLK PLL	t_{CO}	2.348	2.659	2.999	2.680	2.668	ns
	16 mA	GCLK	t_{CO}	4.257	4.759	5.251	4.817	4.921	ns
		GCLK PLL	t_{CO}	2.334	2.646	2.987	2.667	2.655	ns
2.5 V	4 mA	GCLK	t_{CO}	4.684	5.209	5.736	5.290	5.436	ns
		GCLK PLL	t_{CO}	2.761	3.096	3.472	3.140	3.170	ns
	8 mA	GCLK	t_{CO}	4.503	5.029	5.551	5.098	5.220	ns
		GCLK PLL	t_{CO}	2.580	2.916	3.287	2.948	2.954	ns
	12 mA	GCLK	t_{CO}	4.431	4.946	5.456	5.010	5.124	ns
		GCLK PLL	t_{CO}	2.508	2.833	3.192	2.860	2.858	ns
	16 mA	GCLK	t_{CO}	4.401	4.917	5.427	4.979	5.091	ns
		GCLK PLL	t_{CO}	2.478	2.804	3.163	2.829	2.825	ns
1.8 V	2 mA	GCLK	t_{CO}	5.638	6.294	6.957	6.383	6.554	ns
		GCLK PLL	t_{CO}	3.715	4.181	4.693	4.233	4.288	ns
	4 mA	GCLK	t_{CO}	5.267	5.901	6.544	5.984	6.124	ns
		GCLK PLL	t_{CO}	3.344	3.788	4.280	3.834	3.858	ns
	6 mA	GCLK	t_{CO}	5.074	5.685	6.304	5.760	5.891	ns
		GCLK PLL	t_{CO}	3.151	3.572	4.040	3.610	3.625	ns
	8 mA	GCLK	t_{CO}	5.013	5.614	6.218	5.686	5.813	ns
		GCLK PLL	t_{CO}	3.090	3.501	3.954	3.536	3.547	ns
	10 mA	GCLK	t_{CO}	4.954	5.552	6.158	5.624	5.751	ns
		GCLK PLL	t_{CO}	3.031	3.439	3.894	3.474	3.485	ns
	12 mA	GCLK	t_{CO}	4.907	5.502	6.094	5.570	5.693	ns
		GCLK PLL	t_{CO}	2.984	3.389	3.830	3.420	3.427	ns
	16 mA	GCLK	t_{CO}	4.865	5.460	6.056	5.529	5.650	ns
		GCLK PLL	t_{CO}	2.942	3.347	3.792	3.379	3.384	ns

Table 1–54. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	2 mA	GCLK	t_{CO}	6.125	6.909	7.742	6.995	7.140	ns
		GCLK PLL	t_{CO}	4.202	4.796	5.478	4.845	4.874	ns
	4 mA	GCLK	t_{CO}	5.719	6.437	7.194	6.520	6.651	ns
		GCLK PLL	t_{CO}	3.796	4.324	4.930	4.370	4.385	ns
	6 mA	GCLK	t_{CO}	5.578	6.294	7.037	6.372	6.496	ns
		GCLK PLL	t_{CO}	3.655	4.181	4.773	4.222	4.230	ns
	8 mA	GCLK	t_{CO}	5.492	6.180	6.903	6.260	6.382	ns
		GCLK PLL	t_{CO}	3.569	4.067	4.639	4.110	4.116	ns
	10 mA	GCLK	t_{CO}	5.454	6.142	6.854	6.212	6.330	ns
		GCLK PLL	t_{CO}	3.531	4.029	4.590	4.062	4.064	ns
	12 mA	GCLK	t_{CO}	5.421	6.107	6.812	6.178	6.296	ns
		GCLK PLL	t_{CO}	3.498	3.994	4.548	4.028	4.030	ns
	16 mA	GCLK	t_{CO}	5.313	5.989	6.679	6.058	6.172	ns
		GCLK PLL	t_{CO}	3.390	3.876	4.415	3.908	3.906	ns
1.2 V	2 mA	GCLK	t_{CO}	7.256	8.327	9.517	8.373	8.451	ns
		GCLK PLL	t_{CO}	5.333	6.214	7.253	6.223	6.185	ns
	4 mA	GCLK	t_{CO}	6.898	7.913	9.035	7.956	8.030	ns
		GCLK PLL	t_{CO}	4.975	5.800	6.771	5.806	5.764	ns
	6 mA	GCLK	t_{CO}	6.762	7.750	8.838	7.794	7.867	ns
		GCLK PLL	t_{CO}	4.839	5.637	6.574	5.644	5.601	ns
	8 mA	GCLK	t_{CO}	6.702	7.682	8.762	7.725	7.797	ns
		GCLK PLL	t_{CO}	4.779	5.569	6.498	5.575	5.531	ns
	10 mA	GCLK	t_{CO}	6.571	7.513	8.539	7.553	7.622	ns
		GCLK PLL	t_{CO}	4.648	5.400	6.275	5.403	5.356	ns
	12 mA	GCLK	t_{CO}	6.554	7.496	8.524	7.535	7.604	ns
		GCLK PLL	t_{CO}	4.631	5.383	6.260	5.385	5.338	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.446	4.960	5.467	5.020	5.129	ns
		GCLK PLL	t_{CO}	2.523	2.847	3.203	2.870	2.863	ns
	12 mA	GCLK	t_{CO}	4.426	4.938	5.444	4.998	5.107	ns
		GCLK PLL	t_{CO}	2.503	2.825	3.180	2.848	2.841	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.391	4.899	5.401	4.958	5.065	ns
		GCLK PLL	t_{CO}	2.468	2.786	3.137	2.808	2.799	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	4.863	5.444	6.028	5.510	5.628	ns
		GCLK PLL	t_{CO}	2.940	3.331	3.764	3.360	3.362	ns
	10 mA	GCLK	t_{CO}	4.839	5.413	5.989	5.480	5.598	ns
		GCLK PLL	t_{CO}	2.916	3.300	3.725	3.330	3.332	ns
	12 mA	GCLK	t_{CO}	4.836	5.412	5.985	5.478	5.593	ns
		GCLK PLL	t_{CO}	2.913	3.299	3.721	3.328	3.327	ns

Table 1–54. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.821	5.394	5.970	5.460	5.577	ns
		GCLK PLL	t_{CO}	2.898	3.281	3.706	3.310	3.311	ns
	16 mA	GCLK	t_{CO}	4.808	5.382	5.956	5.447	5.563	ns
		GCLK PLL	t_{CO}	2.885	3.269	3.692	3.297	3.297	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	4.847	5.420	5.995	5.486	5.604	ns
		GCLK PLL	t_{CO}	2.924	3.307	3.731	3.336	3.338	ns
	10 mA	GCLK	t_{CO}	4.840	5.416	5.993	5.481	5.597	ns
		GCLK PLL	t_{CO}	2.917	3.303	3.729	3.331	3.331	ns
	12 mA	GCLK	t_{CO}	4.826	5.397	5.970	5.463	5.579	ns
		GCLK PLL	t_{CO}	2.903	3.284	3.706	3.313	3.313	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.807	5.375	5.944	5.440	5.554	ns
		GCLK PLL	t_{CO}	2.884	3.262	3.680	3.290	3.288	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.345	6.007	6.692	6.076	6.189	ns
		GCLK PLL	t_{CO}	3.422	3.894	4.428	3.926	3.923	ns
	10 mA	GCLK	t_{CO}	5.341	5.997	6.677	6.068	6.180	ns
		GCLK PLL	t_{CO}	3.418	3.884	4.413	3.918	3.914	ns
	12 mA	GCLK	t_{CO}	5.334	5.994	6.675	6.064	6.175	ns
		GCLK PLL	t_{CO}	3.411	3.881	4.411	3.914	3.909	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.299	5.948	6.619	6.018	6.129	ns
		GCLK PLL	t_{CO}	3.376	3.835	4.355	3.868	3.863	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.524	7.460	8.487	7.499	7.567	ns
		GCLK PLL	t_{CO}	4.601	5.347	6.223	5.349	5.301	ns
	10 mA	GCLK	t_{CO}	6.447	7.350	8.328	7.388	7.456	ns
		GCLK PLL	t_{CO}	4.524	5.237	6.064	5.238	5.190	ns
	12 mA	GCLK	t_{CO}	6.449	7.352	8.332	7.391	7.459	ns
		GCLK PLL	t_{CO}	4.526	5.239	6.068	5.241	5.193	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.387	7.279	8.260	7.320	7.392	ns
		GCLK PLL	t_{CO}	4.464	5.166	5.996	5.170	5.126	ns
3.0-V PCI	—	GCLK	t_{CO}	4.566	5.074	5.573	5.136	5.246	ns
		GCLK PLL	t_{CO}	2.643	2.961	3.309	2.986	2.980	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.566	5.074	5.573	5.136	5.246	ns
		GCLK PLL	t_{CO}	2.643	2.961	3.309	2.986	2.980	ns

Table 1–55. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	4.962	5.501	6.023	5.581	5.713	ns
		GCLK PLL	t_{CO}	3.034	3.382	3.752	3.424	3.441	ns
	8 mA	GCLK	t_{CO}	4.515	5.038	5.542	5.107	5.217	ns
		GCLK PLL	t_{CO}	2.587	2.919	3.271	2.950	2.945	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.609	5.125	5.633	5.198	5.319	ns
		GCLK PLL	t_{CO}	2.681	3.006	3.362	3.041	3.047	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	4.714	5.224	5.723	5.296	5.425	ns
		GCLK PLL	t_{CO}	2.786	3.105	3.452	3.139	3.153	ns
	8 mA	GCLK	t_{CO}	4.458	4.969	5.463	5.034	5.146	ns
		GCLK PLL	t_{CO}	2.530	2.850	3.192	2.877	2.874	ns
	12 mA	GCLK	t_{CO}	4.342	4.843	5.336	4.903	5.011	ns
		GCLK PLL	t_{CO}	2.414	2.724	3.065	2.746	2.739	ns
	16 mA	GCLK	t_{CO}	4.293	4.788	5.269	4.847	4.950	ns
		GCLK PLL	t_{CO}	2.365	2.669	2.998	2.690	2.678	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.456	4.968	5.461	5.032	5.145	ns
		GCLK PLL	t_{CO}	2.528	2.849	3.190	2.875	2.873	ns
	8 mA	GCLK	t_{CO}	4.294	4.791	5.273	4.849	4.952	ns
		GCLK PLL	t_{CO}	2.366	2.672	3.002	2.692	2.680	ns
	12 mA	GCLK	t_{CO}	4.254	4.751	5.233	4.809	4.912	ns
		GCLK PLL	t_{CO}	2.326	2.632	2.962	2.652	2.640	ns
	16 mA	GCLK	t_{CO}	4.233	4.731	5.214	4.789	4.891	ns
		GCLK PLL	t_{CO}	2.305	2.612	2.943	2.632	2.619	ns
2.5 V	4 mA	GCLK	t_{CO}	4.840	5.364	5.881	5.444	5.593	ns
		GCLK PLL	t_{CO}	2.912	3.245	3.610	3.287	3.321	ns
	8 mA	GCLK	t_{CO}	4.571	5.094	5.604	5.162	5.283	ns
		GCLK PLL	t_{CO}	2.643	2.975	3.333	3.005	3.011	ns
	12 mA	GCLK	t_{CO}	4.456	4.974	5.481	5.039	5.155	ns
		GCLK PLL	t_{CO}	2.528	2.855	3.210	2.882	2.883	ns
	16 mA	GCLK	t_{CO}	4.403	4.918	5.422	4.982	5.093	ns
		GCLK PLL	t_{CO}	2.475	2.799	3.151	2.825	2.821	ns

Table 1–55. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8 V	2 mA	GCLK	t_{CO}	5.991	6.651	7.328	6.765	6.960	ns
		GCLK PLL	t_{CO}	4.063	4.532	5.057	4.608	4.688	ns
	4 mA	GCLK	t_{CO}	5.435	6.081	6.736	6.170	6.316	ns
		GCLK PLL	t_{CO}	3.507	3.962	4.465	4.013	4.044	ns
	6 mA	GCLK	t_{CO}	5.173	5.787	6.404	5.869	6.007	ns
		GCLK PLL	t_{CO}	3.245	3.668	4.133	3.712	3.735	ns
	8 mA	GCLK	t_{CO}	5.057	5.658	6.259	5.735	5.865	ns
		GCLK PLL	t_{CO}	3.129	3.539	3.988	3.578	3.593	ns
	10 mA	GCLK	t_{CO}	4.996	5.604	6.212	5.680	5.808	ns
		GCLK PLL	t_{CO}	3.068	3.485	3.941	3.523	3.536	ns
	12 mA	GCLK	t_{CO}	4.935	5.528	6.123	5.602	5.727	ns
		GCLK PLL	t_{CO}	3.007	3.409	3.852	3.445	3.455	ns
	16 mA	GCLK	t_{CO}	4.891	5.479	6.067	5.551	5.672	ns
		GCLK PLL	t_{CO}	2.963	3.360	3.796	3.394	3.400	ns
1.5 V	2 mA	GCLK	t_{CO}	6.404	7.222	8.081	7.314	7.465	ns
		GCLK PLL	t_{CO}	4.476	5.103	5.810	5.157	5.193	ns
	4 mA	GCLK	t_{CO}	5.844	6.579	7.337	6.660	6.790	ns
		GCLK PLL	t_{CO}	3.916	4.460	5.066	4.503	4.518	ns
	6 mA	GCLK	t_{CO}	5.654	6.374	7.121	6.451	6.576	ns
		GCLK PLL	t_{CO}	3.726	4.255	4.850	4.294	4.304	ns
	8 mA	GCLK	t_{CO}	5.556	6.264	6.983	6.339	6.463	ns
		GCLK PLL	t_{CO}	3.628	4.145	4.712	4.182	4.191	ns
	10 mA	GCLK	t_{CO}	5.489	6.192	6.913	6.266	6.389	ns
		GCLK PLL	t_{CO}	3.561	4.073	4.642	4.109	4.117	ns
	12 mA	GCLK	t_{CO}	5.450	6.141	6.849	6.214	6.333	ns
		GCLK PLL	t_{CO}	3.522	4.022	4.578	4.057	4.061	ns
	16 mA	GCLK	t_{CO}	5.377	6.058	6.758	6.130	6.243	ns
		GCLK PLL	t_{CO}	3.449	3.939	4.487	3.973	3.971	ns
1.2 V	2 mA	GCLK	t_{CO}	7.493	8.601	9.830	8.649	8.728	ns
		GCLK PLL	t_{CO}	5.565	6.482	7.559	6.492	6.456	ns
	4 mA	GCLK	t_{CO}	7.001	8.033	9.169	8.077	8.150	ns
		GCLK PLL	t_{CO}	5.073	5.914	6.898	5.920	5.878	ns
	6 mA	GCLK	t_{CO}	6.847	7.850	8.954	7.894	7.967	ns
		GCLK PLL	t_{CO}	4.919	5.731	6.683	5.737	5.695	ns
	8 mA	GCLK	t_{CO}	6.759	7.752	8.841	7.795	7.866	ns
		GCLK PLL	t_{CO}	4.831	5.633	6.570	5.638	5.594	ns
	10 mA	GCLK	t_{CO}	6.636	7.603	8.655	7.647	7.715	ns
		GCLK PLL	t_{CO}	4.708	5.484	6.384	5.490	5.443	ns

Table 1–55. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.470	4.981	5.480	5.042	5.150	ns
		GCLK PLL	t_{CO}	2.542	2.862	3.209	2.885	2.878	ns
	12 mA	GCLK	t_{CO}	4.437	4.947	5.444	5.008	5.114	ns
		GCLK PLL	t_{CO}	2.509	2.828	3.173	2.851	2.842	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.387	4.893	5.387	4.953	5.057	ns
		GCLK PLL	t_{CO}	2.459	2.774	3.116	2.796	2.785	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	4.877	5.455	6.033	5.523	5.639	ns
		GCLK PLL	t_{CO}	2.949	3.336	3.762	3.366	3.367	ns
	10 mA	GCLK	t_{CO}	4.858	5.432	6.003	5.500	5.616	ns
		GCLK PLL	t_{CO}	2.930	3.313	3.732	3.343	3.344	ns
	12 mA	GCLK	t_{CO}	4.835	5.407	5.976	5.475	5.591	ns
		GCLK PLL	t_{CO}	2.907	3.288	3.705	3.318	3.319	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.828	5.400	5.969	5.466	5.581	ns
		GCLK PLL	t_{CO}	2.900	3.281	3.698	3.309	3.309	ns
	16 mA	GCLK	t_{CO}	4.812	5.385	5.955	5.452	5.566	ns
		GCLK PLL	t_{CO}	2.884	3.266	3.684	3.295	3.294	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	4.857	5.427	5.994	5.494	5.608	ns
		GCLK PLL	t_{CO}	2.929	3.308	3.723	3.337	3.336	ns
	10 mA	GCLK	t_{CO}	4.850	5.423	5.993	5.489	5.603	ns
		GCLK PLL	t_{CO}	2.922	3.304	3.722	3.332	3.331	ns
	12 mA	GCLK	t_{CO}	4.839	5.409	5.975	5.476	5.590	ns
		GCLK PLL	t_{CO}	2.911	3.290	3.704	3.319	3.318	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.806	5.371	5.933	5.437	5.549	ns
		GCLK PLL	t_{CO}	2.878	3.252	3.662	3.280	3.277	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.362	6.026	6.702	6.093	6.204	ns
		GCLK PLL	t_{CO}	3.434	3.907	4.431	3.936	3.932	ns
	10 mA	GCLK	t_{CO}	5.360	6.022	6.694	6.090	6.201	ns
		GCLK PLL	t_{CO}	3.432	3.903	4.423	3.933	3.929	ns
	12 mA	GCLK	t_{CO}	5.350	6.015	6.690	6.082	6.193	ns
		GCLK PLL	t_{CO}	3.422	3.896	4.419	3.925	3.921	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.312	5.969	6.636	6.035	6.144	ns
		GCLK PLL	t_{CO}	3.384	3.850	4.365	3.878	3.872	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.555	7.494	8.517	7.533	7.600	ns
		GCLK PLL	t_{CO}	4.627	5.375	6.246	5.376	5.328	ns
	10 mA	GCLK	t_{CO}	6.470	7.378	8.356	7.417	7.482	ns
		GCLK PLL	t_{CO}	4.542	5.259	6.085	5.260	5.210	ns
3.0-V PCI	—	GCLK	t_{CO}	4.551	5.055	5.545	5.117	5.224	ns
		GCLK PLL	t_{CO}	2.623	2.936	3.274	2.960	2.952	ns

Table 1–55. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V PCI-X	—	GCLK	t_{CO}	4.551	5.055	5.545	5.117	5.224	ns
		GCLK PLL	t_{CO}	2.623	2.936	3.274	2.960	2.952	ns

Table 1–56. EP3C10 Column Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–0.993	–1.124	–1.255	–1.153	–1.170	ns
	—		t_{H}	1.243	1.414	1.580	1.441	1.461	ns
	—	GCLK PLL	t_{SU}	1.195	1.289	1.339	1.301	1.411	ns
	—		t_{H}	–0.677	–0.695	–0.683	–0.706	–0.801	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns
BLVDS	—	GCLK	t_{SU}	–0.964	–1.092	–1.214	–1.117	–1.133	ns
	—		t_{H}	1.212	1.380	1.537	1.404	1.422	ns
	—	GCLK PLL	t_{SU}	1.221	1.319	1.376	1.333	1.445	ns
	—		t_{H}	–0.704	–0.727	–0.722	–0.740	–0.837	ns
	8 mA	GCLK	t_{CO}	4.688	5.207	5.710	5.271	5.379	ns
		GCLK PLL	t_{CO}	2.768	3.096	3.448	3.123	3.116	ns
	12 mA	GCLK	t_{CO}	4.688	5.207	5.710	5.271	5.379	ns
		GCLK PLL	t_{CO}	2.768	3.096	3.448	3.123	3.116	ns
	16 mA	GCLK	t_{CO}	4.688	5.207	5.710	5.271	5.379	ns
		GCLK PLL	t_{CO}	2.768	3.096	3.448	3.123	3.116	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.310	4.800	5.280	4.858	4.961	ns
	—	GCLK PLL	t_{CO}	2.395	2.695	3.020	2.714	2.703	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.385	4.899	5.406	4.962	5.069	ns
	—	GCLK PLL	t_{CO}	2.470	2.794	3.146	2.818	2.811	ns

Table 1–57. EP3C10 Row Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–0.966	–1.094	–1.217	–1.120	–1.136	ns
	—		t_{H}	1.215	1.382	1.540	1.407	1.425	ns
	—		t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{SU}	1.223	1.321	1.379	1.336	1.448	ns
	—		t_{H}	–0.707	–0.729	–0.725	–0.743	–0.840	ns
	—		t_{CO}	1.715	1.980	2.226	1.899	1.837	ns
BLVDS	—	GCLK	t_{SU}	–0.966	–1.094	–1.217	–1.120	–1.136	ns
	—		t_{H}	1.215	1.382	1.540	1.407	1.425	ns
	—	GCLK PLL	t_{SU}	1.223	1.321	1.379	1.336	1.448	ns
	—		t_{H}	–0.707	–0.729	–0.725	–0.743	–0.840	ns
	8 mA	GCLK	t_{CO}	4.687	5.205	5.710	5.270	5.378	ns
		GCLK PLL	t_{CO}	2.769	3.098	3.448	3.124	3.117	ns
	12 mA	GCLK	t_{CO}	4.687	5.205	5.710	5.270	5.378	ns
		GCLK PLL	t_{CO}	2.769	3.098	3.448	3.124	3.117	ns
	16 mA	GCLK	t_{CO}	4.687	5.205	5.710	5.270	5.378	ns
		GCLK PLL	t_{CO}	2.769	3.098	3.448	3.124	3.117	ns
mini-LVDS	—	GCLK	t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{CO}	1.715	1.980	2.226	1.899	1.837	ns
PPDS	—	GCLK	t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{CO}	1.715	1.980	2.226	1.899	1.837	ns
RSDS	—	GCLK	t_{CO}	3.644	4.099	4.499	4.055	4.109	ns
	—	GCLK PLL	t_{CO}	1.715	1.980	2.226	1.899	1.837	ns

EP3C16 I/O Timing Parameters

Table 1–58 through Table 1–63 show the maximum I/O timing parameters for EP3C16 devices.

Table 1–58. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.266	–1.409	–1.539	–1.426	–1.454	ns
		t_{H}	1.499	1.677	1.840	1.695	1.725	ns
	GCLK PLL	t_{SU}	1.112	1.222	1.290	1.246	1.358	ns
		t_{H}	–0.563	–0.593	–0.595	–0.616	–0.710	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.266	–1.409	–1.539	–1.426	–1.454	ns
		t_{H}	1.499	1.677	1.840	1.695	1.725	ns
	GCLK PLL	t_{SU}	1.112	1.222	1.290	1.246	1.358	ns
		t_{H}	–0.563	–0.593	–0.595	–0.616	–0.710	ns

Table 1–58. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVTTL	GCLK	t_{SU}	–1.259	–1.406	–1.541	–1.422	–1.451	ns
		t_{H}	1.492	1.674	1.842	1.691	1.722	ns
	GCLK PLL	t_{SU}	1.119	1.225	1.288	1.250	1.361	ns
		t_{H}	–0.570	–0.596	–0.593	–0.620	–0.713	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.259	–1.406	–1.541	–1.422	–1.451	ns
		t_{H}	1.492	1.674	1.842	1.691	1.722	ns
	GCLK PLL	t_{SU}	1.119	1.225	1.288	1.250	1.361	ns
		t_{H}	–0.570	–0.596	–0.593	–0.620	–0.713	ns
2.5 V	GCLK	t_{SU}	–1.226	–1.378	–1.519	–1.396	–1.426	ns
		t_{H}	1.459	1.646	1.820	1.665	1.697	ns
	GCLK PLL	t_{SU}	1.152	1.253	1.310	1.276	1.386	ns
		t_{H}	–0.603	–0.624	–0.615	–0.646	–0.738	ns
1.8 V	GCLK	t_{SU}	–1.123	–1.310	–1.487	–1.325	–1.353	ns
		t_{H}	1.356	1.578	1.788	1.594	1.624	ns
	GCLK PLL	t_{SU}	1.255	1.321	1.342	1.347	1.459	ns
		t_{H}	–0.706	–0.692	–0.647	–0.717	–0.811	ns
1.5 V	GCLK	t_{SU}	–1.059	–1.223	–1.373	–1.241	–1.273	ns
		t_{H}	1.292	1.491	1.674	1.510	1.544	ns
	GCLK PLL	t_{SU}	1.319	1.408	1.456	1.431	1.539	ns
		t_{H}	–0.770	–0.779	–0.761	–0.801	–0.891	ns
1.2 V	GCLK	t_{SU}	–0.919	–1.045	–1.153	–1.069	–1.110	ns
		t_{H}	1.152	1.313	1.454	1.338	1.381	ns
	GCLK PLL	t_{SU}	1.459	1.586	1.676	1.603	1.702	ns
		t_{H}	–0.910	–0.957	–0.981	–0.973	–1.054	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.136	–1.324	–1.510	–1.346	–1.363	ns
		t_{H}	1.369	1.593	1.811	1.614	1.635	ns
	GCLK PLL	t_{SU}	1.232	1.297	1.319	1.324	1.439	ns
		t_{H}	–0.683	–0.669	–0.624	–0.695	–0.792	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.136	–1.324	–1.510	–1.346	–1.363	ns
		t_{H}	1.369	1.593	1.811	1.614	1.635	ns
	GCLK PLL	t_{SU}	1.232	1.297	1.319	1.324	1.439	ns
		t_{H}	–0.683	–0.669	–0.624	–0.695	–0.792	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.968	–1.112	–1.243	–1.139	–1.167	ns
		t_{H}	1.201	1.381	1.544	1.407	1.439	ns
	GCLK PLL	t_{SU}	1.400	1.509	1.586	1.531	1.635	ns
		t_{H}	–0.851	–0.881	–0.891	–0.902	–0.988	ns

Table 1–58. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	GCLK	t_{SU}	–0.968	–1.112	–1.243	–1.139	–1.167	ns
		t_{H}	1.201	1.381	1.544	1.407	1.439	ns
	GCLK PLL	t_{SU}	1.400	1.509	1.586	1.531	1.635	ns
		t_{H}	–0.851	–0.881	–0.891	–0.902	–0.988	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–0.968	–1.112	–1.243	–1.139	–1.167	ns
		t_{H}	1.201	1.381	1.544	1.407	1.439	ns
	GCLK PLL	t_{SU}	1.400	1.509	1.586	1.531	1.635	ns
		t_{H}	–0.851	–0.881	–0.891	–0.902	–0.988	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.968	–1.112	–1.243	–1.139	–1.167	ns
		t_{H}	1.201	1.381	1.544	1.407	1.439	ns
	GCLK PLL	t_{SU}	1.400	1.509	1.586	1.531	1.635	ns
		t_{H}	–0.851	–0.881	–0.891	–0.902	–0.988	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.058	–1.211	–1.355	–1.238	–1.263	ns
		t_{H}	1.291	1.480	1.656	1.506	1.535	ns
	GCLK PLL	t_{SU}	1.310	1.410	1.474	1.432	1.539	ns
		t_{H}	–0.761	–0.782	–0.779	–0.803	–0.892	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.058	–1.211	–1.355	–1.238	–1.263	ns
		t_{H}	1.291	1.480	1.656	1.506	1.535	ns
	GCLK PLL	t_{SU}	1.310	1.410	1.474	1.432	1.539	ns
		t_{H}	–0.761	–0.782	–0.779	–0.803	–0.892	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.861	–0.973	–1.076	–1.009	–1.053	ns
		t_{H}	1.094	1.242	1.377	1.277	1.325	ns
	GCLK PLL	t_{SU}	1.507	1.648	1.753	1.661	1.749	ns
		t_{H}	–0.958	–1.020	–1.058	–1.032	–1.102	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–0.861	–0.973	–1.076	–1.009	–1.053	ns
		t_{H}	1.094	1.242	1.377	1.277	1.325	ns
	GCLK PLL	t_{SU}	1.507	1.648	1.753	1.661	1.749	ns
		t_{H}	–0.958	–1.020	–1.058	–1.032	–1.102	ns
3.0-V PCI	GCLK	t_{SU}	–1.259	–1.406	–1.541	–1.422	–1.451	ns
		t_{H}	1.492	1.674	1.842	1.691	1.722	ns
	GCLK PLL	t_{SU}	1.119	1.225	1.288	1.250	1.361	ns
		t_{H}	–0.570	–0.596	–0.593	–0.620	–0.713	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.259	–1.406	–1.541	–1.422	–1.451	ns
		t_{H}	1.492	1.674	1.842	1.691	1.722	ns
	GCLK PLL	t_{SU}	1.119	1.225	1.288	1.250	1.361	ns
		t_{H}	–0.570	–0.596	–0.593	–0.620	–0.713	ns

Table 1–59. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.215	–1.346	–1.465	–1.365	–1.393	ns
		t_{H}	1.447	1.613	1.765	1.631	1.663	ns
	GCLK PLL	t_{SU}	1.183	1.304	1.384	1.327	1.438	ns
		t_{H}	–0.635	–0.677	–0.692	–0.699	–0.792	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.215	–1.346	–1.465	–1.365	–1.393	ns
		t_{H}	1.447	1.613	1.765	1.631	1.663	ns
	GCLK PLL	t_{SU}	1.183	1.304	1.384	1.327	1.438	ns
		t_{H}	–0.635	–0.677	–0.692	–0.699	–0.792	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.208	–1.343	–1.466	–1.361	–1.390	ns
		t_{H}	1.440	1.610	1.766	1.627	1.660	ns
	GCLK PLL	t_{SU}	1.190	1.307	1.383	1.331	1.441	ns
		t_{H}	–0.642	–0.680	–0.691	–0.703	–0.795	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.208	–1.343	–1.466	–1.361	–1.390	ns
		t_{H}	1.440	1.610	1.766	1.627	1.660	ns
	GCLK PLL	t_{SU}	1.190	1.307	1.383	1.331	1.441	ns
		t_{H}	–0.642	–0.680	–0.691	–0.703	–0.795	ns
2.5 V	GCLK	t_{SU}	–1.176	–1.315	–1.443	–1.333	–1.364	ns
		t_{H}	1.408	1.582	1.743	1.599	1.634	ns
	GCLK PLL	t_{SU}	1.222	1.335	1.406	1.359	1.467	ns
		t_{H}	–0.674	–0.708	–0.714	–0.731	–0.821	ns
1.8 V	GCLK	t_{SU}	–1.075	–1.250	–1.417	–1.266	–1.294	ns
		t_{H}	1.307	1.517	1.717	1.532	1.564	ns
	GCLK PLL	t_{SU}	1.323	1.400	1.432	1.426	1.537	ns
		t_{H}	–0.775	–0.773	–0.740	–0.798	–0.891	ns
1.5 V	GCLK	t_{SU}	–1.011	–1.164	–1.303	–1.182	–1.214	ns
		t_{H}	1.243	1.431	1.603	1.448	1.484	ns
	GCLK PLL	t_{SU}	1.387	1.486	1.546	1.510	1.617	ns
		t_{H}	–0.839	–0.859	–0.854	–0.882	–0.971	ns
1.2 V	GCLK	t_{SU}	–0.867	–0.983	–1.083	–1.007	–1.049	ns
		t_{H}	1.099	1.250	1.383	1.273	1.319	ns
	GCLK PLL	t_{SU}	1.531	1.667	1.766	1.685	1.782	ns
		t_{H}	–0.983	–1.040	–1.074	–1.057	–1.136	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.094	–1.273	–1.441	–1.288	–1.312	ns
		t_{H}	1.326	1.540	1.741	1.554	1.582	ns
	GCLK PLL	t_{SU}	1.295	1.368	1.399	1.395	1.510	ns
		t_{H}	–0.747	–0.741	–0.707	–0.767	–0.864	ns

Table 1–59. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-2 Class II	GCLK	t_{SU}	–1.094	–1.273	–1.441	–1.288	–1.312	ns
		t_{H}	1.326	1.540	1.741	1.554	1.582	ns
	GCLK PLL	t_{SU}	1.295	1.368	1.399	1.395	1.510	ns
		t_{H}	–0.747	–0.741	–0.707	–0.767	–0.864	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.927	–1.062	–1.177	–1.082	–1.115	ns
		t_{H}	1.159	1.329	1.477	1.348	1.385	ns
	GCLK PLL	t_{SU}	1.462	1.579	1.663	1.601	1.707	ns
		t_{H}	–0.914	–0.952	–0.971	–0.973	–1.061	ns
SSTL-18 Class II	GCLK	t_{SU}	–0.927	–1.062	–1.177	–1.082	–1.115	ns
		t_{H}	1.159	1.329	1.477	1.348	1.385	ns
	GCLK PLL	t_{SU}	1.462	1.579	1.663	1.601	1.707	ns
		t_{H}	–0.914	–0.952	–0.971	–0.973	–1.061	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–0.927	–1.062	–1.177	–1.082	–1.115	ns
		t_{H}	1.159	1.329	1.477	1.348	1.385	ns
	GCLK PLL	t_{SU}	1.462	1.579	1.663	1.601	1.707	ns
		t_{H}	–0.914	–0.952	–0.971	–0.973	–1.061	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.927	–1.062	–1.177	–1.082	–1.115	ns
		t_{H}	1.159	1.329	1.477	1.348	1.385	ns
	GCLK PLL	t_{SU}	1.462	1.579	1.663	1.601	1.707	ns
		t_{H}	–0.914	–0.952	–0.971	–0.973	–1.061	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.015	–1.160	–1.285	–1.179	–1.210	ns
		t_{H}	1.247	1.427	1.585	1.445	1.480	ns
	GCLK PLL	t_{SU}	1.374	1.481	1.555	1.504	1.612	ns
		t_{H}	–0.826	–0.854	–0.863	–0.876	–0.966	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.015	–1.160	–1.285	–1.179	–1.210	ns
		t_{H}	1.247	1.427	1.585	1.445	1.480	ns
	GCLK PLL	t_{SU}	1.374	1.481	1.555	1.504	1.612	ns
		t_{H}	–0.826	–0.854	–0.863	–0.876	–0.966	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.821	–0.924	–1.011	–0.953	–1.004	ns
		t_{H}	1.053	1.191	1.311	1.219	1.274	ns
	GCLK PLL	t_{SU}	1.568	1.717	1.829	1.730	1.818	ns
		t_{H}	–1.020	–1.090	–1.137	–1.102	–1.172	ns
3.0-V PCI	GCLK	t_{SU}	–1.208	–1.343	–1.466	–1.361	–1.390	ns
		t_{H}	1.440	1.610	1.766	1.627	1.660	ns
	GCLK PLL	t_{SU}	1.190	1.307	1.383	1.331	1.441	ns
		t_{H}	–0.642	–0.680	–0.691	–0.703	–0.795	ns

Table 1–59. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V PCI-X	GCLK	t_{SU}	–1.208	–1.343	–1.466	–1.361	–1.390	ns
		t_{H}	1.440	1.610	1.766	1.627	1.660	ns
	GCLK PLL	t_{SU}	1.190	1.307	1.383	1.331	1.441	ns
		t_{H}	–0.642	–0.680	–0.691	–0.703	–0.795	ns

Table 1–60. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.167	5.752	6.326	5.835	5.958	ns
		GCLK PLL	t_{CO}	7.214	7.803	8.463	7.956	8.146	ns
	8 mA	GCLK	t_{CO}	4.802	5.362	5.911	5.428	5.527	ns
		GCLK PLL	t_{CO}	4.741	5.154	5.674	5.228	5.305	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.911	5.483	6.043	5.558	5.670	ns
		GCLK PLL	t_{CO}	5.690	6.143	6.615	6.251	6.425	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	4.974	5.553	6.115	5.628	5.742	ns
		GCLK PLL	t_{CO}	5.916	6.386	6.892	6.512	6.703	ns
	8 mA	GCLK	t_{CO}	4.756	5.320	5.870	5.387	5.488	ns
		GCLK PLL	t_{CO}	4.408	4.831	5.302	4.913	4.982	ns
	12 mA	GCLK	t_{CO}	4.680	5.241	5.793	5.308	5.410	ns
		GCLK PLL	t_{CO}	3.708	4.102	4.537	4.158	4.192	ns
	16 mA	GCLK	t_{CO}	4.643	5.199	5.744	5.264	5.362	ns
		GCLK PLL	t_{CO}	3.357	3.713	4.136	3.762	3.801	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.761	5.325	5.875	5.392	5.493	ns
		GCLK PLL	t_{CO}	4.405	4.826	5.299	4.910	4.978	ns
	8 mA	GCLK	t_{CO}	4.642	5.199	5.745	5.264	5.362	ns
		GCLK PLL	t_{CO}	3.373	3.732	4.156	3.783	3.820	ns
	12 mA	GCLK	t_{CO}	4.616	5.168	5.709	5.232	5.328	ns
		GCLK PLL	t_{CO}	3.054	3.395	3.788	3.428	3.432	ns
	16 mA	GCLK	t_{CO}	4.604	5.155	5.695	5.218	5.313	ns
		GCLK PLL	t_{CO}	2.883	3.222	3.620	3.254	3.263	ns
2.5 V	4 mA	GCLK	t_{CO}	5.034	5.610	6.181	5.696	5.823	ns
		GCLK PLL	t_{CO}	6.310	6.843	7.444	7.011	7.231	ns
	8 mA	GCLK	t_{CO}	4.844	5.426	5.995	5.497	5.603	ns
		GCLK PLL	t_{CO}	4.471	4.911	5.419	4.999	5.079	ns
	12 mA	GCLK	t_{CO}	4.756	5.327	5.891	5.397	5.501	ns
		GCLK PLL	t_{CO}	3.834	4.248	4.709	4.306	4.352	ns
	16 mA	GCLK	t_{CO}	4.722	5.289	5.847	5.357	5.457	ns
		GCLK PLL	t_{CO}	3.537	3.936	4.387	3.990	4.023	ns

Table 1–60. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8 V	2 mA	GCLK	t_{CO}	6.077	6.798	7.520	6.899	7.047	ns
		GCLK PLL	t_{CO}	10.963	12.004	13.186	12.308	12.761	ns
	4 mA	GCLK	t_{CO}	5.574	6.252	6.934	6.338	6.465	ns
		GCLK PLL	t_{CO}	6.939	7.678	8.530	7.809	7.970	ns
	6 mA	GCLK	t_{CO}	5.442	6.108	6.779	6.190	6.312	ns
		GCLK PLL	t_{CO}	5.685	6.310	7.025	6.414	6.539	ns
	8 mA	GCLK	t_{CO}	5.388	6.043	6.701	6.122	6.241	ns
		GCLK PLL	t_{CO}	4.973	5.539	6.183	5.620	5.700	ns
	10 mA	GCLK	t_{CO}	5.314	5.963	6.614	6.040	6.154	ns
		GCLK PLL	t_{CO}	4.644	5.183	5.811	5.255	5.324	ns
	12 mA	GCLK	t_{CO}	5.293	5.941	6.587	6.017	6.129	ns
		GCLK PLL	t_{CO}	4.305	4.819	5.404	4.882	4.936	ns
	16 mA	GCLK	t_{CO}	5.235	5.883	6.532	5.959	6.072	ns
		GCLK PLL	t_{CO}	3.974	4.459	5.018	4.517	4.557	ns
1.5 V	2 mA	GCLK	t_{CO}	6.435	7.260	8.128	7.351	7.481	ns
		GCLK PLL	t_{CO}	9.715	10.894	12.268	11.051	11.243	ns
	4 mA	GCLK	t_{CO}	6.087	6.862	7.660	6.943	7.059	ns
		GCLK PLL	t_{CO}	6.677	7.512	8.477	7.604	7.706	ns
	6 mA	GCLK	t_{CO}	5.935	6.696	7.480	6.775	6.889	ns
		GCLK PLL	t_{CO}	5.639	6.367	7.212	6.442	6.506	ns
	8 mA	GCLK	t_{CO}	5.894	6.643	7.414	6.719	6.828	ns
		GCLK PLL	t_{CO}	5.092	5.750	6.512	5.813	5.864	ns
	10 mA	GCLK	t_{CO}	5.843	6.591	7.357	6.666	6.773	ns
		GCLK PLL	t_{CO}	4.770	5.402	6.125	5.458	5.495	ns
	12 mA	GCLK	t_{CO}	5.801	6.547	7.309	6.622	6.729	ns
		GCLK PLL	t_{CO}	4.582	5.189	5.887	5.241	5.274	ns
	16 mA	GCLK	t_{CO}	5.730	6.466	7.219	6.540	6.647	ns
		GCLK PLL	t_{CO}	4.267	4.837	5.503	4.879	4.894	ns

Table 1–60. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.2 V	2 mA	GCLK	t_{CO}	7.618	8.732	9.954	8.785	8.851	ns
		GCLK PLL	t_{CO}	10.015	11.580	13.472	11.628	11.642	ns
	4 mA	GCLK	t_{CO}	7.297	8.358	9.514	8.405	8.463	ns
		GCLK PLL	t_{CO}	7.304	8.458	9.846	8.483	8.463	ns
	6 mA	GCLK	t_{CO}	7.182	8.231	9.373	8.278	8.337	ns
		GCLK PLL	t_{CO}	6.460	7.481	8.708	7.501	7.474	ns
	8 mA	GCLK	t_{CO}	7.066	8.087	9.194	8.131	8.187	ns
		GCLK PLL	t_{CO}	6.067	7.030	8.187	7.047	7.015	ns
	10 mA	GCLK	t_{CO}	7.042	8.062	9.168	8.106	8.162	ns
		GCLK PLL	t_{CO}	5.786	6.702	7.786	6.711	6.668	ns
	12 mA	GCLK	t_{CO}	7.018	8.034	9.136	8.078	8.133	ns
		GCLK PLL	t_{CO}	5.638	6.533	7.591	6.541	6.496	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.760	5.297	5.847	5.362	5.476	ns
		GCLK PLL	t_{CO}	2.718	3.047	3.422	3.062	3.061	ns
	12 mA	GCLK	t_{CO}	4.778	5.320	5.870	5.385	5.501	ns
		GCLK PLL	t_{CO}	2.736	3.070	3.445	3.085	3.086	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.751	5.290	5.838	5.355	5.471	ns
		GCLK PLL	t_{CO}	2.709	3.040	3.413	3.055	3.056	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.205	5.810	6.433	5.882	6.006	ns
		GCLK PLL	t_{CO}	3.163	3.560	4.008	3.582	3.591	ns
	10 mA	GCLK	t_{CO}	5.220	5.827	6.451	5.899	6.023	ns
		GCLK PLL	t_{CO}	3.178	3.577	4.026	3.599	3.608	ns
	12 mA	GCLK	t_{CO}	5.208	5.816	6.443	5.888	6.013	ns
		GCLK PLL	t_{CO}	3.166	3.566	4.018	3.588	3.598	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.191	5.793	6.412	5.865	5.989	ns
		GCLK PLL	t_{CO}	3.149	3.543	3.987	3.565	3.574	ns
	16 mA	GCLK	t_{CO}	5.169	5.769	6.386	5.840	5.964	ns
		GCLK PLL	t_{CO}	3.127	3.519	3.961	3.540	3.549	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.161	5.758	6.374	5.828	5.952	ns
		GCLK PLL	t_{CO}	3.119	3.508	3.949	3.528	3.537	ns
	10 mA	GCLK	t_{CO}	5.172	5.768	6.389	5.838	5.961	ns
		GCLK PLL	t_{CO}	3.130	3.518	3.964	3.538	3.546	ns
	12 mA	GCLK	t_{CO}	5.197	5.797	6.414	5.868	5.992	ns
		GCLK PLL	t_{CO}	3.155	3.547	3.989	3.568	3.577	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.144	5.732	6.331	5.803	5.928	ns
		GCLK PLL	t_{CO}	3.102	3.482	3.906	3.503	3.513	ns

Table 1–60. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.672	6.361	7.087	6.432	6.553	ns
		GCLK PLL	t_{CO}	3.630	4.111	4.662	4.132	4.138	ns
	10 mA	GCLK	t_{CO}	5.688	6.370	7.080	6.442	6.565	ns
		GCLK PLL	t_{CO}	3.646	4.120	4.655	4.142	4.150	ns
	12 mA	GCLK	t_{CO}	5.702	6.386	7.098	6.458	6.581	ns
		GCLK PLL	t_{CO}	3.660	4.136	4.673	4.158	4.166	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.632	6.311	7.024	6.382	6.502	ns
		GCLK PLL	t_{CO}	3.590	4.061	4.599	4.082	4.087	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.851	7.810	8.877	7.854	7.928	ns
		GCLK PLL	t_{CO}	4.809	5.560	6.452	5.554	5.513	ns
	10 mA	GCLK	t_{CO}	6.798	7.734	8.767	7.778	7.852	ns
		GCLK PLL	t_{CO}	4.756	5.484	6.342	5.478	5.437	ns
	12 mA	GCLK	t_{CO}	6.800	7.737	8.771	7.781	7.855	ns
		GCLK PLL	t_{CO}	4.758	5.487	6.346	5.481	5.440	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.726	7.648	8.689	7.694	7.774	ns
		GCLK PLL	t_{CO}	4.684	5.398	6.264	5.394	5.359	ns
3.0-V PCI	—	GCLK	t_{CO}	4.913	5.472	6.020	5.539	5.640	ns
		GCLK PLL	t_{CO}	3.295	3.671	4.115	3.713	3.738	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.913	5.472	6.020	5.539	5.640	ns
		GCLK PLL	t_{CO}	3.295	3.671	4.115	3.713	3.738	ns

Table 1–61. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.648	6.239	6.839	6.333	6.494	ns
		GCLK PLL	t_{CO}	3.597	3.978	4.413	4.031	4.067	ns
	8 mA	GCLK	t_{CO}	5.031	5.577	6.133	5.646	5.772	ns
		GCLK PLL	t_{CO}	2.980	3.316	3.707	3.344	3.345	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.191	5.754	6.322	5.832	5.971	ns
		GCLK PLL	t_{CO}	3.140	3.493	3.896	3.530	3.544	ns

Table 1–61. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVTTL	4 mA	GCLK	t_{co}	5.272	5.837	6.415	5.919	6.065	ns
		GCLK PLL	t_{co}	3.221	3.576	3.989	3.617	3.638	ns
	8 mA	GCLK	t_{co}	4.918	5.457	6.011	5.529	5.664	ns
		GCLK PLL	t_{co}	2.867	3.196	3.585	3.227	3.237	ns
	12 mA	GCLK	t_{co}	4.799	5.340	5.890	5.407	5.527	ns
		GCLK PLL	t_{co}	2.748	3.079	3.464	3.105	3.100	ns
	16 mA	GCLK	t_{co}	4.724	5.268	5.820	5.335	5.455	ns
		GCLK PLL	t_{co}	2.673	3.007	3.394	3.033	3.028	ns
3.0-V LVCMOS	4 mA	GCLK	t_{co}	4.917	5.455	6.022	5.527	5.661	ns
		GCLK PLL	t_{co}	2.866	3.194	3.596	3.225	3.234	ns
	8 mA	GCLK	t_{co}	4.721	5.269	5.823	5.337	5.457	ns
		GCLK PLL	t_{co}	2.670	3.008	3.397	3.035	3.030	ns
	12 mA	GCLK	t_{co}	4.648	5.182	5.726	5.247	5.365	ns
		GCLK PLL	t_{co}	2.597	2.921	3.300	2.945	2.938	ns
	16 mA	GCLK	t_{co}	4.624	5.156	5.697	5.219	5.335	ns
		GCLK PLL	t_{co}	2.573	2.895	3.271	2.917	2.908	ns
2.5 V	4 mA	GCLK	t_{co}	5.447	6.014	6.597	6.108	6.283	ns
		GCLK PLL	t_{co}	3.396	3.753	4.171	3.806	3.856	ns
	8 mA	GCLK	t_{co}	5.019	5.577	6.150	5.655	5.792	ns
		GCLK PLL	t_{co}	2.968	3.316	3.724	3.353	3.365	ns
	12 mA	GCLK	t_{co}	4.887	5.438	5.999	5.510	5.638	ns
		GCLK PLL	t_{co}	2.836	3.177	3.573	3.208	3.211	ns
	16 mA	GCLK	t_{co}	4.815	5.363	5.924	5.433	5.557	ns
		GCLK PLL	t_{co}	2.764	3.102	3.498	3.131	3.130	ns
1.8 V	2 mA	GCLK	t_{co}	6.912	7.648	8.416	7.787	8.015	ns
		GCLK PLL	t_{co}	4.868	5.396	5.995	5.495	5.597	ns
	4 mA	GCLK	t_{co}	6.004	6.692	7.419	6.791	6.956	ns
		GCLK PLL	t_{co}	3.960	4.440	4.998	4.499	4.538	ns
	6 mA	GCLK	t_{co}	5.691	6.342	7.035	6.432	6.586	ns
		GCLK PLL	t_{co}	3.647	4.090	4.614	4.140	4.168	ns
	8 mA	GCLK	t_{co}	5.556	6.206	6.877	6.287	6.429	ns
		GCLK PLL	t_{co}	3.512	3.954	4.456	3.995	4.011	ns
	10 mA	GCLK	t_{co}	5.462	6.098	6.762	6.180	6.319	ns
		GCLK PLL	t_{co}	3.418	3.846	4.341	3.888	3.901	ns
	1 2mA	GCLK	t_{co}	5.397	6.033	6.693	6.111	6.250	ns
		GCLK PLL	t_{co}	3.353	3.781	4.272	3.819	3.832	ns
	16 mA	GCLK	t_{co}	5.332	5.960	6.609	6.035	6.168	ns
		GCLK PLL	t_{co}	3.288	3.708	4.188	3.743	3.750	ns

Table 1–61. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	2 mA	GCLK	t_{CO}	7.100	7.979	8.930	8.081	8.251	ns
		GCLK PLL	t_{CO}	5.056	5.727	6.509	5.789	5.833	ns
	4 mA	GCLK	t_{CO}	6.396	7.182	8.013	7.270	7.418	ns
		GCLK PLL	t_{CO}	4.352	4.930	5.592	4.978	5.000	ns
	6 mA	GCLK	t_{CO}	6.137	6.902	7.710	6.984	7.123	ns
		GCLK PLL	t_{CO}	4.093	4.650	5.289	4.692	4.705	ns
	8 mA	GCLK	t_{CO}	6.025	6.772	7.555	6.849	6.981	ns
		GCLK PLL	t_{CO}	3.981	4.520	5.134	4.557	4.563	ns
	10 mA	GCLK	t_{CO}	5.948	6.690	7.472	6.766	6.898	ns
		GCLK PLL	t_{CO}	3.904	4.438	5.051	4.474	4.480	ns
	12 mA	GCLK	t_{CO}	5.888	6.620	7.393	6.695	6.824	ns
		GCLK PLL	t_{CO}	3.844	4.368	4.972	4.403	4.406	ns
	16 mA	GCLK	t_{CO}	5.853	6.582	7.347	6.656	6.782	ns
		GCLK PLL	t_{CO}	3.809	4.330	4.926	4.364	4.364	ns
1.2 V	2 mA	GCLK	t_{CO}	8.157	9.335	10.667	9.390	9.476	ns
		GCLK PLL	t_{CO}	6.113	7.083	8.246	7.098	7.058	ns
	4 mA	GCLK	t_{CO}	7.520	8.595	9.806	8.645	8.725	ns
		GCLK PLL	t_{CO}	5.476	6.343	7.385	6.353	6.307	ns
	6 mA	GCLK	t_{CO}	7.340	8.386	9.551	8.434	8.512	ns
		GCLK PLL	t_{CO}	5.296	6.134	7.130	6.142	6.094	ns
	8 mA	GCLK	t_{CO}	7.236	8.271	9.420	8.317	8.393	ns
		GCLK PLL	t_{CO}	5.192	6.019	6.999	6.025	5.975	ns
	10 mA	GCLK	t_{CO}	7.177	8.204	9.344	8.251	8.327	ns
		GCLK PLL	t_{CO}	5.133	5.952	6.923	5.959	5.909	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.896	5.436	5.986	5.502	5.620	ns
		GCLK PLL	t_{CO}	2.844	3.174	3.559	3.199	3.192	ns
	12 mA	GCLK	t_{CO}	4.855	5.394	5.944	5.459	5.577	ns
		GCLK PLL	t_{CO}	2.803	3.132	3.517	3.156	3.149	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.793	5.331	5.879	5.396	5.512	ns
		GCLK PLL	t_{CO}	2.741	3.069	3.452	3.093	3.084	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.286	5.894	6.524	5.968	6.094	ns
		GCLK PLL	t_{CO}	3.241	3.641	4.102	3.675	3.675	ns
	10 mA	GCLK	t_{CO}	5.280	5.888	6.512	5.959	6.087	ns
		GCLK PLL	t_{CO}	3.235	3.635	4.090	3.666	3.668	ns
	12 mA	GCLK	t_{CO}	5.253	5.861	6.486	5.932	6.060	ns
		GCLK PLL	t_{CO}	3.208	3.608	4.064	3.639	3.641	ns

Table 1–61. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.243	5.848	6.468	5.918	6.045	ns
		GCLK PLL	t_{CO}	3.198	3.595	4.046	3.625	3.626	ns
	16 mA	GCLK	t_{CO}	5.223	5.829	6.450	5.899	6.025	ns
		GCLK PLL	t_{CO}	3.178	3.576	4.028	3.606	3.606	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.262	5.861	6.479	5.933	6.058	ns
		GCLK PLL	t_{CO}	3.217	3.608	4.057	3.640	3.639	ns
	10 mA	GCLK	t_{CO}	5.260	5.863	6.487	5.935	6.060	ns
		GCLK PLL	t_{CO}	3.215	3.610	4.065	3.642	3.641	ns
	12 mA	GCLK	t_{CO}	5.254	5.856	6.474	5.927	6.053	ns
		GCLK PLL	t_{CO}	3.209	3.603	4.052	3.634	3.634	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.199	5.790	6.394	5.859	5.984	ns
		GCLK PLL	t_{CO}	3.154	3.537	3.972	3.566	3.565	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.780	6.473	7.203	6.545	6.667	ns
		GCLK PLL	t_{CO}	3.735	4.220	4.781	4.252	4.248	ns
	10 mA	GCLK	t_{CO}	5.758	6.446	7.164	6.516	6.638	ns
		GCLK PLL	t_{CO}	3.713	4.193	4.742	4.223	4.219	ns
	12 mA	GCLK	t_{CO}	5.775	6.466	7.189	6.537	6.660	ns
		GCLK PLL	t_{CO}	3.730	4.213	4.767	4.244	4.241	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.696	6.378	7.094	6.448	6.568	ns
		GCLK PLL	t_{CO}	3.651	4.125	4.672	4.155	4.149	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.946	7.909	8.974	7.953	8.028	ns
		GCLK PLL	t_{CO}	4.901	5.656	6.552	5.660	5.609	ns
	10 mA	GCLK	t_{CO}	6.940	7.873	8.888	7.919	7.998	ns
		GCLK PLL	t_{CO}	4.895	5.620	6.466	5.626	5.579	ns
3.0-V PCI	—	GCLK	t_{CO}	4.969	5.509	6.058	5.575	5.695	ns
		GCLK PLL	t_{CO}	2.918	3.248	3.632	3.273	3.268	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.969	5.509	6.058	5.575	5.695	ns
		GCLK PLL	t_{CO}	2.918	3.248	3.632	3.273	3.268	ns

Table 1–62. EP3C16 Column Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–1.239	–1.394	–1.564	–1.426	–1.454	ns
	—		t_{H}	1.497	1.692	1.898	1.723	1.754	ns
	—	GCLK PLL	t_{SU}	1.169	1.267	1.296	1.276	1.388	ns
	—		t_{H}	–0.595	–0.609	–0.569	–0.618	–0.713	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.721	5.264	5.818	5.330	5.447	ns
	—	GCLK PLL	t_{CO}	2.658	2.992	3.380	3.018	3.010	ns

Table 1–62. EP3C16 Column Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
BLVDS	—	GCLK	t_{SU}	–1.198	–1.349	–1.512	–1.378	–1.406	ns
	—		t_{H}	1.455	1.645	1.843	1.673	1.704	ns
	—	GCLK PLL	t_{SU}	1.181	1.283	1.319	1.295	1.407	ns
	—		t_{H}	–0.608	–0.627	–0.595	–0.639	–0.733	ns
	8 mA	GCLK	t_{CO}	5.191	5.750	6.317	5.819	5.938	ns
		GCLK PLL	t_{CO}	3.141	3.489	3.891	3.517	3.512	ns
	12 mA	GCLK	t_{CO}	5.191	5.750	6.317	5.819	5.938	ns
		GCLK PLL	t_{CO}	3.141	3.489	3.891	3.517	3.512	ns
	16 mA	GCLK	t_{CO}	5.191	5.750	6.317	5.819	5.938	ns
		GCLK PLL	t_{CO}	3.141	3.489	3.891	3.517	3.512	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.721	5.264	5.818	5.330	5.447	ns
	—	GCLK PLL	t_{CO}	2.658	2.992	3.380	3.018	3.010	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.721	5.264	5.818	5.330	5.447	ns
	—	GCLK PLL	t_{CO}	2.658	2.992	3.380	3.018	3.010	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.645	5.161	5.683	5.223	5.333	ns
	—	GCLK PLL	t_{CO}	2.582	2.889	3.245	2.911	2.896	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.721	5.264	5.818	5.330	5.447	ns
	—	GCLK PLL	t_{CO}	2.658	2.992	3.380	3.018	3.010	ns

Table 1–63. EP3C16 Row Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–1.208	–1.358	–1.521	–1.388	–1.415	ns
	—		t_{H}	1.465	1.654	1.853	1.682	1.713	ns
	—		t_{CO}	3.940	4.417	4.857	4.377	4.442	ns
	—	GCLK PLL	t_{SU}	1.191	1.294	1.330	1.305	1.418	ns
	—		t_{H}	–0.618	–0.638	–0.605	–0.650	–0.744	ns
	—		t_{CO}	1.847	2.115	2.392	2.035	1.975	ns
BLVDS	—	GCLK	t_{SU}	–1.208	–1.359	–1.522	–1.388	–1.416	ns
	—		t_{H}	1.465	1.655	1.853	1.683	1.714	ns
	—	GCLK PLL	t_{SU}	1.191	1.293	1.329	1.305	1.417	ns
	—		t_{H}	–0.618	–0.637	–0.605	–0.649	–0.743	ns
	8 mA	GCLK	t_{CO}	5.214	5.771	6.339	5.839	5.959	ns
		GCLK PLL	t_{CO}	3.118	3.468	3.869	3.497	3.491	ns
	12 mA	GCLK	t_{CO}	5.214	5.771	6.339	5.839	5.959	ns
		GCLK PLL	t_{CO}	3.118	3.468	3.869	3.497	3.491	ns
	16 mA	GCLK	t_{CO}	5.214	5.771	6.339	5.839	5.959	ns
		GCLK PLL	t_{CO}	3.118	3.468	3.869	3.497	3.491	ns

Table 1–63. EP3C16 Row Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
mini-LVDS	—	GCLK	t_{CO}	3.940	4.417	4.857	4.377	4.442	ns
	—	GCLK PLL	t_{CO}	1.847	2.115	2.392	2.035	1.975	ns
PPDS	—	GCLK	t_{CO}	3.940	4.417	4.857	4.377	4.442	ns
	—	GCLK PLL	t_{CO}	1.847	2.115	2.392	2.035	1.975	ns
RSDS	—	GCLK	t_{CO}	3.940	4.417	4.857	4.377	4.442	ns
	—	GCLK PLL	t_{CO}	1.847	2.115	2.392	2.035	1.975	ns

EP3C25 I/O Timing Parameters

Table 1–64 through Table 1–69 show the maximum I/O timing parameters for EP3C25 devices.

Table 1–64. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.266	–1.428	–1.556	–1.445	–1.475	ns
		t_{H}	1.501	1.699	1.861	1.716	1.748	ns
	GCLK PLL	t_{SU}	1.059	1.154	1.237	1.196	1.291	ns
		t_{H}	–0.389	–0.392	–0.396	–0.430	–0.501	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.266	–1.428	–1.556	–1.445	–1.475	ns
		t_{H}	1.501	1.699	1.861	1.716	1.748	ns
	GCLK PLL	t_{SU}	1.059	1.154	1.237	1.196	1.291	ns
		t_{H}	–0.389	–0.392	–0.396	–0.430	–0.501	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.258	–1.425	–1.559	–1.443	–1.473	ns
		t_{H}	1.493	1.696	1.864	1.714	1.746	ns
	GCLK PLL	t_{SU}	1.067	1.157	1.234	1.198	1.293	ns
		t_{H}	–0.397	–0.395	–0.393	–0.432	–0.503	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.258	–1.425	–1.559	–1.443	–1.473	ns
		t_{H}	1.493	1.696	1.864	1.714	1.746	ns
	GCLK PLL	t_{SU}	1.067	1.157	1.234	1.198	1.293	ns
		t_{H}	–0.397	–0.395	–0.393	–0.432	–0.503	ns
2.5 V	GCLK	t_{SU}	–1.227	–1.398	–1.534	–1.417	–1.448	ns
		t_{H}	1.462	1.669	1.839	1.688	1.721	ns
	GCLK PLL	t_{SU}	1.098	1.184	1.259	1.224	1.318	ns
		t_{H}	–0.428	–0.422	–0.418	–0.458	–0.528	ns
1.8 V	GCLK	t_{SU}	–1.124	–1.331	–1.497	–1.347	–1.377	ns
		t_{H}	1.359	1.602	1.802	1.618	1.650	ns
	GCLK PLL	t_{SU}	1.201	1.251	1.296	1.294	1.389	ns
		t_{H}	–0.531	–0.489	–0.455	–0.528	–0.599	ns

Table 1–64. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	GCLK	t_{SU}	–1.060	–1.244	–1.385	–1.263	–1.297	ns
		t_{H}	1.295	1.515	1.690	1.534	1.570	ns
	GCLK PLL	t_{SU}	1.265	1.338	1.408	1.378	1.469	ns
		t_{H}	–0.595	–0.576	–0.567	–0.612	–0.679	ns
1.2 V	GCLK	t_{SU}	–0.927	–1.066	–1.181	–1.090	–1.132	ns
		t_{H}	1.162	1.337	1.486	1.361	1.405	ns
	GCLK PLL	t_{SU}	1.398	1.516	1.612	1.551	1.634	ns
		t_{H}	–0.728	–0.754	–0.771	–0.785	–0.844	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.163	–1.362	–1.525	–1.377	–1.403	ns
		t_{H}	1.398	1.633	1.829	1.648	1.676	ns
	GCLK PLL	t_{SU}	1.177	1.220	1.238	1.264	1.363	ns
		t_{H}	–0.507	–0.458	–0.396	–0.498	–0.573	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.163	–1.362	–1.525	–1.377	–1.403	ns
		t_{H}	1.398	1.633	1.829	1.648	1.676	ns
	GCLK PLL	t_{SU}	1.177	1.220	1.238	1.264	1.363	ns
		t_{H}	–0.507	–0.458	–0.396	–0.498	–0.573	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.993	–1.141	–1.242	–1.161	–1.196	ns
		t_{H}	1.228	1.412	1.546	1.432	1.469	ns
	GCLK PLL	t_{SU}	1.347	1.441	1.521	1.480	1.570	ns
		t_{H}	–0.677	–0.679	–0.679	–0.714	–0.780	ns
SSTL-18 Class II	GCLK	t_{SU}	–0.993	–1.141	–1.242	–1.161	–1.196	ns
		t_{H}	1.228	1.412	1.546	1.432	1.469	ns
	GCLK PLL	t_{SU}	1.347	1.441	1.521	1.480	1.570	ns
		t_{H}	–0.677	–0.679	–0.679	–0.714	–0.780	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–0.993	–1.141	–1.242	–1.161	–1.196	ns
		t_{H}	1.228	1.412	1.546	1.432	1.469	ns
	GCLK PLL	t_{SU}	1.347	1.441	1.521	1.480	1.570	ns
		t_{H}	–0.677	–0.679	–0.679	–0.714	–0.780	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.993	–1.141	–1.242	–1.161	–1.196	ns
		t_{H}	1.228	1.412	1.546	1.432	1.469	ns
	GCLK PLL	t_{SU}	1.347	1.441	1.521	1.480	1.570	ns
		t_{H}	–0.677	–0.679	–0.679	–0.714	–0.780	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.084	–1.249	–1.370	–1.269	–1.301	ns
		t_{H}	1.319	1.520	1.674	1.540	1.574	ns
	GCLK PLL	t_{SU}	1.256	1.333	1.393	1.372	1.465	ns
		t_{H}	–0.586	–0.571	–0.551	–0.606	–0.675	ns

Table 1–64. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5-V HSTL Class II	GCLK	t_{SU}	–1.084	–1.249	–1.370	–1.269	–1.301	ns
		t_{H}	1.319	1.520	1.674	1.540	1.574	ns
	GCLK PLL	t_{SU}	1.256	1.333	1.393	1.372	1.465	ns
		t_{H}	–0.586	–0.571	–0.551	–0.606	–0.675	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.896	–1.004	–1.088	–1.034	–1.086	ns
		t_{H}	1.131	1.275	1.392	1.305	1.359	ns
	GCLK PLL	t_{SU}	1.444	1.578	1.675	1.607	1.680	ns
		t_{H}	–0.774	–0.816	–0.833	–0.841	–0.890	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–0.896	–1.004	–1.088	–1.034	–1.086	ns
		t_{H}	1.131	1.275	1.392	1.305	1.359	ns
	GCLK PLL	t_{SU}	1.444	1.578	1.675	1.607	1.680	ns
		t_{H}	–0.774	–0.816	–0.833	–0.841	–0.890	ns
3.0-V PCI	GCLK	t_{SU}	–1.258	–1.425	–1.559	–1.443	–1.473	ns
		t_{H}	1.493	1.696	1.864	1.714	1.746	ns
	GCLK PLL	t_{SU}	1.067	1.157	1.234	1.198	1.293	ns
		t_{H}	–0.397	–0.395	–0.393	–0.432	–0.503	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.258	–1.425	–1.559	–1.443	–1.473	ns
		t_{H}	1.493	1.696	1.864	1.714	1.746	ns
	GCLK PLL	t_{SU}	1.067	1.157	1.234	1.198	1.293	ns
		t_{H}	–0.397	–0.395	–0.393	–0.432	–0.503	ns

Table 1–65. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.232	–1.367	–1.488	–1.385	–1.413	ns
		t_{H}	1.464	1.637	1.790	1.654	1.684	ns
	GCLK PLL	t_{SU}	1.098	1.205	1.280	1.230	1.343	ns
		t_{H}	–0.431	–0.446	–0.441	–0.466	–0.554	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.232	–1.367	–1.488	–1.385	–1.413	ns
		t_{H}	1.464	1.637	1.790	1.654	1.684	ns
	GCLK PLL	t_{SU}	1.098	1.205	1.280	1.230	1.343	ns
		t_{H}	–0.431	–0.446	–0.441	–0.466	–0.554	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.227	–1.363	–1.490	–1.382	–1.411	ns
		t_{H}	1.459	1.633	1.792	1.651	1.682	ns
	GCLK PLL	t_{SU}	1.103	1.209	1.278	1.233	1.345	ns
		t_{H}	–0.436	–0.450	–0.439	–0.469	–0.556	ns

Table 1–65. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVCMOS	GCLK	t_{SU}	–1.227	–1.363	–1.490	–1.382	–1.411	ns
		t_{H}	1.459	1.633	1.792	1.651	1.682	ns
	GCLK PLL	t_{SU}	1.103	1.209	1.278	1.233	1.345	ns
		t_{H}	–0.436	–0.450	–0.439	–0.469	–0.556	ns
2.5 V	GCLK	t_{SU}	–1.194	–1.336	–1.470	–1.355	–1.387	ns
		t_{H}	1.426	1.606	1.772	1.624	1.658	ns
	GCLK PLL	t_{SU}	1.136	1.236	1.298	1.260	1.369	ns
		t_{H}	–0.469	–0.477	–0.459	–0.496	–0.580	ns
1.8 V	GCLK	t_{SU}	–1.092	–1.269	–1.433	–1.286	–1.313	ns
		t_{H}	1.324	1.539	1.735	1.555	1.584	ns
	GCLK PLL	t_{SU}	1.238	1.303	1.335	1.329	1.443	ns
		t_{H}	–0.571	–0.544	–0.496	–0.565	–0.654	ns
1.5 V	GCLK	t_{SU}	–1.027	–1.182	–1.322	–1.202	–1.234	ns
		t_{H}	1.259	1.452	1.624	1.471	1.505	ns
	GCLK PLL	t_{SU}	1.303	1.390	1.446	1.413	1.522	ns
		t_{H}	–0.636	–0.631	–0.607	–0.649	–0.733	ns
1.2 V	GCLK	t_{SU}	–0.890	–1.003	–1.117	–1.028	–1.068	ns
		t_{H}	1.122	1.273	1.419	1.297	1.339	ns
	GCLK PLL	t_{SU}	1.440	1.569	1.651	1.587	1.688	ns
		t_{H}	–0.773	–0.810	–0.812	–0.823	–0.899	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.122	–1.301	–1.477	–1.314	–1.339	ns
		t_{H}	1.354	1.571	1.779	1.583	1.610	ns
	GCLK PLL	t_{SU}	1.208	1.271	1.291	1.301	1.417	ns
		t_{H}	–0.541	–0.512	–0.452	–0.537	–0.628	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.122	–1.301	–1.477	–1.314	–1.339	ns
		t_{H}	1.354	1.571	1.779	1.583	1.610	ns
	GCLK PLL	t_{SU}	1.208	1.271	1.291	1.301	1.417	ns
		t_{H}	–0.541	–0.512	–0.452	–0.537	–0.628	ns
SSTL-18 Class I	GCLK	t_{SU}	–0.945	–1.080	–1.195	–1.100	–1.134	ns
		t_{H}	1.177	1.350	1.497	1.369	1.405	ns
	GCLK PLL	t_{SU}	1.385	1.492	1.573	1.515	1.622	ns
		t_{H}	–0.718	–0.733	–0.734	–0.751	–0.833	ns
SSTL-18 Class II	GCLK	t_{SU}	–0.945	–1.080	–1.195	–1.100	–1.134	ns
		t_{H}	1.177	1.350	1.497	1.369	1.405	ns
	GCLK PLL	t_{SU}	1.385	1.492	1.573	1.515	1.622	ns
		t_{H}	–0.718	–0.733	–0.734	–0.751	–0.833	ns

Table 1–65. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8-V HSTL Class I	GCLK	t_{SU}	–0.945	–1.080	–1.195	–1.100	–1.134	ns
		t_{H}	1.177	1.350	1.497	1.369	1.405	ns
	GCLK PLL	t_{SU}	1.385	1.492	1.573	1.515	1.622	ns
		t_{H}	–0.718	–0.733	–0.734	–0.751	–0.833	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–0.945	–1.080	–1.195	–1.100	–1.134	ns
		t_{H}	1.177	1.350	1.497	1.369	1.405	ns
	GCLK PLL	t_{SU}	1.385	1.492	1.573	1.515	1.622	ns
		t_{H}	–0.718	–0.733	–0.734	–0.751	–0.833	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.043	–1.186	–1.314	–1.207	–1.238	ns
		t_{H}	1.275	1.456	1.616	1.476	1.509	ns
	GCLK PLL	t_{SU}	1.287	1.386	1.454	1.408	1.518	ns
		t_{H}	–0.620	–0.627	–0.615	–0.644	–0.729	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.043	–1.186	–1.314	–1.207	–1.238	ns
		t_{H}	1.275	1.456	1.616	1.476	1.509	ns
	GCLK PLL	t_{SU}	1.287	1.386	1.454	1.408	1.518	ns
		t_{H}	–0.620	–0.627	–0.615	–0.644	–0.729	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.844	–0.942	–1.043	–0.972	–1.022	ns
		t_{H}	1.076	1.212	1.345	1.241	1.293	ns
	GCLK PLL	t_{SU}	1.486	1.630	1.725	1.643	1.734	ns
		t_{H}	–0.819	–0.871	–0.886	–0.879	–0.945	ns
3.0-V PCI	GCLK	t_{SU}	–1.227	–1.363	–1.490	–1.382	–1.411	ns
		t_{H}	1.459	1.633	1.792	1.651	1.682	ns
	GCLK PLL	t_{SU}	1.103	1.209	1.278	1.233	1.345	ns
		t_{H}	–0.436	–0.450	–0.439	–0.469	–0.556	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.227	–1.363	–1.490	–1.382	–1.411	ns
		t_{H}	1.459	1.633	1.792	1.651	1.682	ns
	GCLK PLL	t_{SU}	1.103	1.209	1.278	1.233	1.345	ns
		t_{H}	–0.436	–0.450	–0.439	–0.469	–0.556	ns

Table 1–66. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.033	5.586	6.120	5.657	5.801	ns
		GCLK PLL	t_{CO}	3.123	3.487	3.886	3.534	3.546	ns
	8 mA	GCLK	t_{CO}	4.717	5.253	5.772	5.313	5.437	ns
		GCLK PLL	t_{CO}	2.807	3.154	3.538	3.190	3.182	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.782	5.326	5.847	5.392	5.525	ns
		GCLK PLL	t_{CO}	2.872	3.227	3.613	3.269	3.270	ns

Table 1–66. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVTTL	4 mA	GCLK	t_{CO}	4.844	5.391	5.921	5.460	5.598	ns
		GCLK PLL	t_{CO}	2.934	3.292	3.687	3.337	3.343	ns
	8 mA	GCLK	t_{CO}	4.653	5.192	5.712	5.254	5.381	ns
		GCLK PLL	t_{CO}	2.743	3.093	3.478	3.131	3.126	ns
	12 mA	GCLK	t_{CO}	4.596	5.124	5.633	5.180	5.303	ns
		GCLK PLL	t_{CO}	2.686	3.025	3.399	3.057	3.048	ns
	16 mA	GCLK	t_{CO}	4.567	5.091	5.595	5.147	5.267	ns
		GCLK PLL	t_{CO}	2.657	2.992	3.361	3.024	3.012	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.660	5.199	5.719	5.261	5.388	ns
		GCLK PLL	t_{CO}	2.750	3.100	3.485	3.138	3.133	ns
	8 mA	GCLK	t_{CO}	4.566	5.092	5.599	5.148	5.269	ns
		GCLK PLL	t_{CO}	2.656	2.993	3.365	3.025	3.014	ns
	12 mA	GCLK	t_{CO}	4.534	5.060	5.566	5.116	5.236	ns
		GCLK PLL	t_{CO}	2.624	2.961	3.332	2.993	2.981	ns
	16 mA	GCLK	t_{CO}	4.520	5.047	5.554	5.103	5.223	ns
		GCLK PLL	t_{CO}	2.610	2.948	3.320	2.980	2.968	ns
2.5 V	4 mA	GCLK	t_{CO}	4.947	5.497	6.039	5.576	5.738	ns
		GCLK PLL	t_{CO}	3.037	3.398	3.805	3.453	3.483	ns
	8 mA	GCLK	t_{CO}	4.766	5.317	5.854	5.384	5.522	ns
		GCLK PLL	t_{CO}	2.856	3.218	3.620	3.261	3.267	ns
	12 mA	GCLK	t_{CO}	4.694	5.234	5.759	5.296	5.426	ns
		GCLK PLL	t_{CO}	2.784	3.135	3.525	3.173	3.171	ns
	16 mA	GCLK	t_{CO}	4.664	5.205	5.730	5.265	5.393	ns
		GCLK PLL	t_{CO}	2.754	3.106	3.496	3.142	3.138	ns
1.8 V	2 mA	GCLK	t_{CO}	5.901	6.582	7.260	6.669	6.856	ns
		GCLK PLL	t_{CO}	3.991	4.483	5.026	4.546	4.601	ns
	4 mA	GCLK	t_{CO}	5.530	6.189	6.847	6.270	6.426	ns
		GCLK PLL	t_{CO}	3.620	4.090	4.613	4.147	4.171	ns
	6 mA	GCLK	t_{CO}	5.337	5.973	6.607	6.046	6.193	ns
		GCLK PLL	t_{CO}	3.427	3.874	4.373	3.923	3.938	ns
	8 mA	GCLK	t_{CO}	5.276	5.902	6.521	5.972	6.115	ns
		GCLK PLL	t_{CO}	3.366	3.803	4.287	3.849	3.860	ns
	10 mA	GCLK	t_{CO}	5.217	5.840	6.461	5.910	6.053	ns
		GCLK PLL	t_{CO}	3.307	3.741	4.227	3.787	3.798	ns
	12 mA	GCLK	t_{CO}	5.170	5.790	6.397	5.856	5.995	ns
		GCLK PLL	t_{CO}	3.260	3.691	4.163	3.733	3.740	ns
	16 mA	GCLK	t_{CO}	5.128	5.748	6.359	5.815	5.952	ns
		GCLK PLL	t_{CO}	3.218	3.649	4.125	3.692	3.697	ns

Table 1–66. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	2 mA	GCLK	t_{CO}	6.388	7.197	8.045	7.281	7.442	ns
		GCLK PLL	t_{CO}	4.478	5.098	5.811	5.158	5.187	ns
	4 mA	GCLK	t_{CO}	5.982	6.725	7.497	6.806	6.953	ns
		GCLK PLL	t_{CO}	4.072	4.626	5.263	4.683	4.698	ns
	6 mA	GCLK	t_{CO}	5.841	6.582	7.340	6.658	6.798	ns
		GCLK PLL	t_{CO}	3.931	4.483	5.106	4.535	4.543	ns
	8 mA	GCLK	t_{CO}	5.755	6.468	7.206	6.546	6.684	ns
		GCLK PLL	t_{CO}	3.845	4.369	4.972	4.423	4.429	ns
	10 mA	GCLK	t_{CO}	5.717	6.430	7.157	6.498	6.632	ns
		GCLK PLL	t_{CO}	3.807	4.331	4.923	4.375	4.377	ns
	12 mA	GCLK	t_{CO}	5.684	6.395	7.115	6.464	6.598	ns
		GCLK PLL	t_{CO}	3.774	4.296	4.881	4.341	4.343	ns
	16 mA	GCLK	t_{CO}	5.576	6.277	6.982	6.344	6.474	ns
		GCLK PLL	t_{CO}	3.666	4.178	4.748	4.221	4.219	ns
1.2 V	2 mA	GCLK	t_{CO}	7.519	8.615	9.820	8.659	8.753	ns
		GCLK PLL	t_{CO}	5.609	6.516	7.586	6.536	6.498	ns
	4 mA	GCLK	t_{CO}	7.161	8.201	9.338	8.242	8.332	ns
		GCLK PLL	t_{CO}	5.251	6.102	7.104	6.119	6.077	ns
	6 mA	GCLK	t_{CO}	7.025	8.038	9.141	8.080	8.169	ns
		GCLK PLL	t_{CO}	5.115	5.939	6.907	5.957	5.914	ns
	8 mA	GCLK	t_{CO}	6.965	7.970	9.065	8.011	8.099	ns
		GCLK PLL	t_{CO}	5.055	5.871	6.831	5.888	5.844	ns
	10 mA	GCLK	t_{CO}	6.834	7.801	8.842	7.839	7.924	ns
		GCLK PLL	t_{CO}	4.924	5.702	6.608	5.716	5.669	ns
	12 mA	GCLK	t_{CO}	6.817	7.784	8.827	7.821	7.906	ns
		GCLK PLL	t_{CO}	4.907	5.685	6.593	5.698	5.651	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.709	5.248	5.770	5.306	5.431	ns
		GCLK PLL	t_{CO}	2.799	3.149	3.536	3.183	3.176	ns
	12 mA	GCLK	t_{CO}	4.689	5.226	5.747	5.284	5.409	ns
		GCLK PLL	t_{CO}	2.779	3.127	3.513	3.161	3.154	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.654	5.187	5.704	5.244	5.367	ns
		GCLK PLL	t_{CO}	2.744	3.088	3.470	3.121	3.112	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.126	5.732	6.331	5.796	5.930	ns
		GCLK PLL	t_{CO}	3.216	3.633	4.097	3.673	3.675	ns
	10 mA	GCLK	t_{CO}	5.102	5.701	6.292	5.766	5.900	ns
		GCLK PLL	t_{CO}	3.192	3.602	4.058	3.643	3.645	ns
	12 mA	GCLK	t_{CO}	5.099	5.700	6.288	5.764	5.895	ns
		GCLK PLL	t_{CO}	3.189	3.601	4.054	3.641	3.640	ns

Table 1–66. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.084	5.682	6.273	5.746	5.879	ns
		GCLK PLL	t_{CO}	3.174	3.583	4.039	3.623	3.624	ns
	16 mA	GCLK	t_{CO}	5.071	5.670	6.259	5.733	5.865	ns
		GCLK PLL	t_{CO}	3.161	3.571	4.025	3.610	3.610	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.110	5.708	6.298	5.772	5.906	ns
		GCLK PLL	t_{CO}	3.200	3.609	4.064	3.649	3.651	ns
	10 mA	GCLK	t_{CO}	5.103	5.704	6.296	5.767	5.899	ns
		GCLK PLL	t_{CO}	3.193	3.605	4.062	3.644	3.644	ns
	12 mA	GCLK	t_{CO}	5.089	5.685	6.273	5.749	5.881	ns
		GCLK PLL	t_{CO}	3.179	3.586	4.039	3.626	3.626	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.070	5.663	6.247	5.726	5.856	ns
		GCLK PLL	t_{CO}	3.160	3.564	4.013	3.603	3.601	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.608	6.295	6.995	6.362	6.491	ns
		GCLK PLL	t_{CO}	3.698	4.196	4.761	4.239	4.236	ns
	10 mA	GCLK	t_{CO}	5.604	6.285	6.980	6.354	6.482	ns
		GCLK PLL	t_{CO}	3.694	4.186	4.746	4.231	4.227	ns
	12 mA	GCLK	t_{CO}	5.597	6.282	6.978	6.350	6.477	ns
		GCLK PLL	t_{CO}	3.687	4.183	4.744	4.227	4.222	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.562	6.236	6.922	6.304	6.431	ns
		GCLK PLL	t_{CO}	3.652	4.137	4.688	4.181	4.176	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.787	7.748	8.790	7.785	7.869	ns
		GCLK PLL	t_{CO}	4.877	5.649	6.556	5.662	5.614	ns
	10 mA	GCLK	t_{CO}	6.710	7.638	8.631	7.674	7.758	ns
		GCLK PLL	t_{CO}	4.800	5.539	6.397	5.551	5.503	ns
	12 mA	GCLK	t_{CO}	6.712	7.640	8.635	7.677	7.761	ns
		GCLK PLL	t_{CO}	4.802	5.541	6.401	5.554	5.506	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.650	7.567	8.563	7.606	7.694	ns
		GCLK PLL	t_{CO}	4.740	5.468	6.329	5.483	5.439	ns
3.0-V PCI	—	GCLK	t_{CO}	4.829	5.362	5.876	5.422	5.548	ns
		GCLK PLL	t_{CO}	2.919	3.263	3.642	3.299	3.293	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.829	5.362	5.876	5.422	5.548	ns
		GCLK PLL	t_{CO}	2.919	3.263	3.642	3.299	3.293	ns

Table 1–67. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.223	5.786	6.331	5.870	6.012	ns
		GCLK PLL	t_{CO}	3.306	3.682	4.078	3.727	3.754	ns
	8 mA	GCLK	t_{CO}	4.776	5.323	5.850	5.396	5.516	ns
		GCLK PLL	t_{CO}	2.859	3.219	3.597	3.253	3.258	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.870	5.410	5.941	5.487	5.618	ns
		GCLK PLL	t_{CO}	2.953	3.306	3.688	3.344	3.360	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	4.975	5.509	6.031	5.585	5.724	ns
		GCLK PLL	t_{CO}	3.058	3.405	3.778	3.442	3.466	ns
	8 mA	GCLK	t_{CO}	4.719	5.254	5.771	5.323	5.445	ns
		GCLK PLL	t_{CO}	2.802	3.150	3.518	3.180	3.187	ns
	12 mA	GCLK	t_{CO}	4.603	5.128	5.644	5.192	5.310	ns
		GCLK PLL	t_{CO}	2.686	3.024	3.391	3.049	3.052	ns
	16 mA	GCLK	t_{CO}	4.554	5.073	5.577	5.136	5.249	ns
		GCLK PLL	t_{CO}	2.637	2.969	3.324	2.993	2.991	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.717	5.253	5.769	5.321	5.444	ns
		GCLK PLL	t_{CO}	2.800	3.149	3.516	3.178	3.186	ns
	8 mA	GCLK	t_{CO}	4.555	5.076	5.581	5.138	5.251	ns
		GCLK PLL	t_{CO}	2.638	2.972	3.328	2.995	2.993	ns
	12 mA	GCLK	t_{CO}	4.515	5.036	5.541	5.098	5.211	ns
		GCLK PLL	t_{CO}	2.598	2.932	3.288	2.955	2.953	ns
	16 mA	GCLK	t_{CO}	4.494	5.016	5.522	5.078	5.190	ns
		GCLK PLL	t_{CO}	2.577	2.912	3.269	2.935	2.932	ns
2.5 V	4 mA	GCLK	t_{CO}	5.101	5.649	6.189	5.733	5.892	ns
		GCLK PLL	t_{CO}	3.184	3.545	3.936	3.590	3.634	ns
	8 mA	GCLK	t_{CO}	4.832	5.379	5.912	5.451	5.582	ns
		GCLK PLL	t_{CO}	2.915	3.275	3.659	3.308	3.324	ns
	12 mA	GCLK	t_{CO}	4.717	5.259	5.789	5.328	5.454	ns
		GCLK PLL	t_{CO}	2.800	3.155	3.536	3.185	3.196	ns
	16 mA	GCLK	t_{CO}	4.664	5.203	5.730	5.271	5.392	ns
		GCLK PLL	t_{CO}	2.747	3.099	3.477	3.128	3.134	ns

Table 1–67. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8 V	2 mA	GCLK	t_{CO}	6.252	6.936	7.636	7.054	7.259	ns
		GCLK PLL	t_{CO}	4.335	4.832	5.383	4.911	5.001	ns
	4 mA	GCLK	t_{CO}	5.696	6.366	7.044	6.459	6.615	ns
		GCLK PLL	t_{CO}	3.779	4.262	4.791	4.316	4.357	ns
	6 mA	GCLK	t_{CO}	5.434	6.072	6.712	6.158	6.306	ns
		GCLK PLL	t_{CO}	3.517	3.968	4.459	4.015	4.048	ns
	8 mA	GCLK	t_{CO}	5.318	5.943	6.567	6.024	6.164	ns
		GCLK PLL	t_{CO}	3.401	3.839	4.314	3.881	3.906	ns
	10 mA	GCLK	t_{CO}	5.257	5.889	6.520	5.969	6.107	ns
		GCLK PLL	t_{CO}	3.340	3.785	4.267	3.826	3.849	ns
	12 mA	GCLK	t_{CO}	5.196	5.813	6.431	5.891	6.026	ns
		GCLK PLL	t_{CO}	3.279	3.709	4.178	3.748	3.768	ns
	16 mA	GCLK	t_{CO}	5.152	5.764	6.375	5.840	5.971	ns
		GCLK PLL	t_{CO}	3.235	3.660	4.122	3.697	3.713	ns
1.5 V	2 mA	GCLK	t_{CO}	6.665	7.507	8.389	7.603	7.764	ns
		GCLK PLL	t_{CO}	4.748	5.403	6.136	5.460	5.506	ns
	4 mA	GCLK	t_{CO}	6.105	6.864	7.645	6.949	7.089	ns
		GCLK PLL	t_{CO}	4.188	4.760	5.392	4.806	4.831	ns
	6 mA	GCLK	t_{CO}	5.915	6.659	7.429	6.740	6.875	ns
		GCLK PLL	t_{CO}	3.998	4.555	5.176	4.597	4.617	ns
	8 mA	GCLK	t_{CO}	5.817	6.549	7.291	6.628	6.762	ns
		GCLK PLL	t_{CO}	3.900	4.445	5.038	4.485	4.504	ns
	10 mA	GCLK	t_{CO}	5.750	6.477	7.221	6.555	6.688	ns
		GCLK PLL	t_{CO}	3.833	4.373	4.968	4.412	4.430	ns
	12 mA	GCLK	t_{CO}	5.711	6.426	7.157	6.503	6.632	ns
		GCLK PLL	t_{CO}	3.794	4.322	4.904	4.360	4.374	ns
	16 mA	GCLK	t_{CO}	5.638	6.343	7.066	6.419	6.542	ns
		GCLK PLL	t_{CO}	3.721	4.239	4.813	4.276	4.284	ns
1.2 V	2 mA	GCLK	t_{CO}	7.754	8.886	10.138	8.938	9.027	ns
		GCLK PLL	t_{CO}	5.837	6.782	7.885	6.795	6.769	ns
	4 mA	GCLK	t_{CO}	7.262	8.318	9.477	8.366	8.449	ns
		GCLK PLL	t_{CO}	5.345	6.214	7.224	6.223	6.191	ns
	6 mA	GCLK	t_{CO}	7.108	8.135	9.262	8.183	8.266	ns
		GCLK PLL	t_{CO}	5.191	6.031	7.009	6.040	6.008	ns
	8 mA	GCLK	t_{CO}	7.020	8.037	9.149	8.084	8.165	ns
		GCLK PLL	t_{CO}	5.103	5.933	6.896	5.941	5.907	ns
	10 mA	GCLK	t_{CO}	6.897	7.888	8.963	7.936	8.014	ns
		GCLK PLL	t_{CO}	4.980	5.784	6.710	5.793	5.756	ns

Table 1–67. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.731	5.266	5.788	5.331	5.449	ns
		GCLK PLL	t_{CO}	2.814	3.162	3.535	3.188	3.191	ns
	12 mA	GCLK	t_{CO}	4.698	5.232	5.752	5.297	5.413	ns
		GCLK PLL	t_{CO}	2.781	3.128	3.499	3.154	3.155	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.648	5.178	5.695	5.242	5.356	ns
		GCLK PLL	t_{CO}	2.731	3.074	3.442	3.099	3.098	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.138	5.740	6.341	5.812	5.938	ns
		GCLK PLL	t_{CO}	3.221	3.636	4.088	3.669	3.680	ns
	10 mA	GCLK	t_{CO}	5.119	5.717	6.311	5.789	5.915	ns
		GCLK PLL	t_{CO}	3.202	3.613	4.058	3.646	3.657	ns
	12 mA	GCLK	t_{CO}	5.096	5.692	6.284	5.764	5.890	ns
		GCLK PLL	t_{CO}	3.179	3.588	4.031	3.621	3.632	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.089	5.685	6.277	5.755	5.880	ns
		GCLK PLL	t_{CO}	3.172	3.581	4.024	3.612	3.622	ns
	16 mA	GCLK	t_{CO}	5.073	5.670	6.263	5.741	5.865	ns
		GCLK PLL	t_{CO}	3.156	3.566	4.010	3.598	3.607	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.118	5.712	6.302	5.783	5.907	ns
		GCLK PLL	t_{CO}	3.201	3.608	4.049	3.640	3.649	ns
	10 mA	GCLK	t_{CO}	5.111	5.708	6.301	5.778	5.902	ns
		GCLK PLL	t_{CO}	3.194	3.604	4.048	3.635	3.644	ns
	12 mA	GCLK	t_{CO}	5.100	5.694	6.283	5.765	5.889	ns
		GCLK PLL	t_{CO}	3.183	3.590	4.030	3.622	3.631	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.067	5.656	6.241	5.726	5.848	ns
		GCLK PLL	t_{CO}	3.150	3.552	3.988	3.583	3.590	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.623	6.311	7.010	6.382	6.503	ns
		GCLK PLL	t_{CO}	3.706	4.207	4.757	4.239	4.245	ns
	10 mA	GCLK	t_{CO}	5.621	6.307	7.002	6.379	6.500	ns
		GCLK PLL	t_{CO}	3.704	4.203	4.749	4.236	4.242	ns
	12 mA	GCLK	t_{CO}	5.611	6.300	6.998	6.371	6.492	ns
		GCLK PLL	t_{CO}	3.694	4.196	4.745	4.228	4.234	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.573	6.254	6.944	6.324	6.443	ns
		GCLK PLL	t_{CO}	3.656	4.150	4.691	4.181	4.185	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.816	7.779	8.825	7.822	7.899	ns
		GCLK PLL	t_{CO}	4.899	5.675	6.572	5.679	5.641	ns
	10 mA	GCLK	t_{CO}	6.731	7.663	8.664	7.706	7.781	ns
		GCLK PLL	t_{CO}	4.814	5.559	6.411	5.563	5.523	ns
3.0-V PCI	—	GCLK	t_{CO}	4.812	5.340	5.853	5.406	5.523	ns
		GCLK PLL	t_{CO}	2.895	3.236	3.600	3.263	3.265	ns

Table 1–67. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V PCI-X	—	GCLK	t_{CO}	4.812	5.340	5.853	5.406	5.523	ns
		GCLK PLL	t_{CO}	2.895	3.236	3.600	3.263	3.265	ns

Table 1–68. EP3C25 Column Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–1.240	–1.395	–1.544	–1.427	–1.456	ns
	—		t_{H}	1.500	1.695	1.881	1.726	1.757	ns
	—	GCLK PLL	t_{SU}	1.112	1.199	1.246	1.210	1.322	ns
	—		t_{H}	–0.418	–0.409	–0.373	–0.416	–0.503	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.647	5.184	5.711	5.251	5.368	ns
	—	GCLK PLL	t_{CO}	2.738	3.089	3.467	3.118	3.117	ns
BLVDS	—	GCLK	t_{SU}	–1.200	–1.350	–1.494	–1.380	–1.408	ns
	—		t_{H}	1.457	1.648	1.828	1.677	1.707	ns
	—	GCLK PLL	t_{SU}	1.150	1.242	1.294	1.255	1.368	ns
	—		t_{H}	–0.571	–0.581	–0.562	–0.592	–0.686	ns
	8 mA	GCLK	t_{CO}	4.937	5.480	6.006	5.547	5.668	ns
		GCLK PLL	t_{CO}	2.931	3.272	3.638	3.301	3.295	ns
	12 mA	GCLK	t_{CO}	4.937	5.480	6.006	5.547	5.668	ns
		GCLK PLL	t_{CO}	2.931	3.272	3.638	3.301	3.295	ns
	16 mA	GCLK	t_{CO}	4.937	5.480	6.006	5.547	5.668	ns
		GCLK PLL	t_{CO}	2.931	3.272	3.638	3.301	3.295	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.647	5.184	5.711	5.251	5.368	ns
	—	GCLK PLL	t_{CO}	2.738	3.089	3.467	3.118	3.117	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.647	5.184	5.711	5.251	5.368	ns
	—	GCLK PLL	t_{CO}	2.738	3.089	3.467	3.118	3.117	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.572	5.085	5.585	5.147	5.260	ns
	—	GCLK PLL	t_{CO}	2.663	2.990	3.341	3.014	3.009	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.647	5.184	5.711	5.251	5.368	ns
	—	GCLK PLL	t_{CO}	2.738	3.089	3.467	3.118	3.117	ns

Table 1–69. EP3C25 Row Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–1.188	–1.338	–1.483	–1.368	–1.397	ns
	—		t_{H}	1.446	1.636	1.817	1.665	1.696	ns
	—		t_{CO}	3.894	4.373	4.796	4.333	4.396	ns
	—	GCLK PLL	t_{SU}	1.143	1.235	1.288	1.248	1.360	ns
	—		t_{H}	–0.450	–0.447	–0.417	–0.456	–0.543	ns
	—		t_{CO}	1.977	2.269	2.543	2.190	2.138	ns
BLVDS	—	GCLK	t_{SU}	–1.190	–1.340	–1.484	–1.370	–1.398	ns
	—		t_{H}	1.447	1.639	1.818	1.667	1.697	ns
	—	GCLK PLL	t_{SU}	1.140	1.232	1.284	1.245	1.358	ns
	—		t_{H}	–0.561	–0.572	–0.552	–0.582	–0.676	ns
	8 mA	GCLK	t_{CO}	4.949	5.492	6.018	5.560	5.678	ns
		GCLK PLL	t_{CO}	2.919	3.260	3.626	3.288	3.285	ns
	12 mA	GCLK	t_{CO}	4.949	5.492	6.018	5.560	5.678	ns
		GCLK PLL	t_{CO}	2.919	3.260	3.626	3.288	3.285	ns
	16 mA	GCLK	t_{CO}	4.949	5.492	6.018	5.560	5.678	ns
		GCLK PLL	t_{CO}	2.919	3.260	3.626	3.288	3.285	ns
mini-LVDS	—	GCLK	t_{CO}	3.894	4.373	4.796	4.333	4.396	ns
	—	GCLK PLL	t_{CO}	1.977	2.269	2.543	2.190	2.138	ns
PPDS	—	GCLK	t_{CO}	3.894	4.373	4.796	4.333	4.396	ns
	—	GCLK PLL	t_{CO}	1.977	2.269	2.543	2.190	2.138	ns
RSDS	—	GCLK	t_{CO}	3.894	4.373	4.796	4.333	4.396	ns
	—	GCLK PLL	t_{CO}	1.977	2.269	2.543	2.190	2.138	ns

EP3C40 I/O Timing Parameters

Table 1–70 through Table 1–75 show the maximum I/O timing parameters for EP3C40 devices.

Table 1–70. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.417	–1.559	–1.711	–1.588	–1.609	ns
		t_{H}	1.655	1.833	2.019	1.862	1.886	ns
	GCLK PLL	t_{SU}	1.128	1.257	1.319	1.278	1.397	ns
		t_{H}	–0.450	–0.483	–0.464	–0.500	–0.594	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.417	–1.559	–1.711	–1.588	–1.609	ns
		t_{H}	1.655	1.833	2.019	1.862	1.886	ns
	GCLK PLL	t_{SU}	1.128	1.257	1.319	1.278	1.397	ns
		t_{H}	–0.450	–0.483	–0.464	–0.500	–0.594	ns

Table 1–70. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVTTL	GCLK	t_{SU}	–1.410	–1.556	–1.713	–1.584	–1.606	ns
		t_{H}	1.648	1.830	2.021	1.858	1.883	ns
	GCLK PLL	t_{SU}	1.135	1.260	1.317	1.282	1.400	ns
		t_{H}	–0.457	–0.486	–0.462	–0.504	–0.597	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.410	–1.556	–1.713	–1.584	–1.606	ns
		t_{H}	1.648	1.830	2.021	1.858	1.883	ns
	GCLK PLL	t_{SU}	1.135	1.260	1.317	1.282	1.400	ns
		t_{H}	–0.457	–0.486	–0.462	–0.504	–0.597	ns
2.5 V	GCLK	t_{SU}	–1.377	–1.528	–1.691	–1.558	–1.581	ns
		t_{H}	1.615	1.802	1.999	1.832	1.858	ns
	GCLK PLL	t_{SU}	1.168	1.288	1.339	1.308	1.425	ns
		t_{H}	–0.490	–0.514	–0.484	–0.530	–0.622	ns
1.8 V	GCLK	t_{SU}	–1.274	–1.460	–1.659	–1.487	–1.508	ns
		t_{H}	1.512	1.734	1.967	1.761	1.785	ns
	GCLK PLL	t_{SU}	1.271	1.356	1.371	1.379	1.498	ns
		t_{H}	–0.593	–0.582	–0.516	–0.601	–0.695	ns
1.5 V	GCLK	t_{SU}	–1.210	–1.373	–1.545	–1.403	–1.428	ns
		t_{H}	1.448	1.647	1.853	1.677	1.705	ns
	GCLK PLL	t_{SU}	1.335	1.443	1.485	1.463	1.578	ns
		t_{H}	–0.657	–0.669	–0.630	–0.685	–0.775	ns
1.2 V	GCLK	t_{SU}	–1.070	–1.195	–1.325	–1.231	–1.265	ns
		t_{H}	1.308	1.469	1.633	1.505	1.542	ns
	GCLK PLL	t_{SU}	1.475	1.621	1.705	1.635	1.741	ns
		t_{H}	–0.797	–0.847	–0.850	–0.857	–0.938	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.283	–1.482	–1.678	–1.504	–1.525	ns
		t_{H}	1.520	1.757	1.986	1.779	1.803	ns
	GCLK PLL	t_{SU}	1.255	1.315	1.332	1.339	1.462	ns
		t_{H}	–0.577	–0.541	–0.477	–0.561	–0.658	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.283	–1.482	–1.678	–1.504	–1.525	ns
		t_{H}	1.520	1.757	1.986	1.779	1.803	ns
	GCLK PLL	t_{SU}	1.255	1.315	1.332	1.339	1.462	ns
		t_{H}	–0.577	–0.541	–0.477	–0.561	–0.658	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.115	–1.270	–1.411	–1.297	–1.329	ns
		t_{H}	1.352	1.545	1.719	1.572	1.607	ns
	GCLK PLL	t_{SU}	1.423	1.527	1.599	1.546	1.658	ns
		t_{H}	–0.745	–0.753	–0.744	–0.768	–0.854	ns

Table 1–70. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	GCLK	t_{SU}	–1.115	–1.270	–1.411	–1.297	–1.329	ns
		t_{H}	1.352	1.545	1.719	1.572	1.607	ns
	GCLK PLL	t_{SU}	1.423	1.527	1.599	1.546	1.658	ns
		t_{H}	–0.745	–0.753	–0.744	–0.768	–0.854	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.115	–1.270	–1.411	–1.297	–1.329	ns
		t_{H}	1.352	1.545	1.719	1.572	1.607	ns
	GCLK PLL	t_{SU}	1.423	1.527	1.599	1.546	1.658	ns
		t_{H}	–0.745	–0.753	–0.744	–0.768	–0.854	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.115	–1.270	–1.411	–1.297	–1.329	ns
		t_{H}	1.352	1.545	1.719	1.572	1.607	ns
	GCLK PLL	t_{SU}	1.423	1.527	1.599	1.546	1.658	ns
		t_{H}	–0.745	–0.753	–0.744	–0.768	–0.854	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.205	–1.369	–1.523	–1.396	–1.425	ns
		t_{H}	1.442	1.644	1.831	1.671	1.703	ns
	GCLK PLL	t_{SU}	1.333	1.428	1.487	1.447	1.562	ns
		t_{H}	–0.655	–0.654	–0.632	–0.669	–0.758	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.205	–1.369	–1.523	–1.396	–1.425	ns
		t_{H}	1.442	1.644	1.831	1.671	1.703	ns
	GCLK PLL	t_{SU}	1.333	1.428	1.487	1.447	1.562	ns
		t_{H}	–0.655	–0.654	–0.632	–0.669	–0.758	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.008	–1.131	–1.244	–1.167	–1.215	ns
		t_{H}	1.245	1.406	1.552	1.442	1.493	ns
	GCLK PLL	t_{SU}	1.530	1.666	1.766	1.676	1.772	ns
		t_{H}	–0.852	–0.892	–0.911	–0.898	–0.968	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–1.008	–1.131	–1.244	–1.167	–1.215	ns
		t_{H}	1.245	1.406	1.552	1.442	1.493	ns
	GCLK PLL	t_{SU}	1.530	1.666	1.766	1.676	1.772	ns
		t_{H}	–0.852	–0.892	–0.911	–0.898	–0.968	ns
3.0-V PCI	GCLK	t_{SU}	–1.410	–1.556	–1.713	–1.584	–1.606	ns
		t_{H}	1.648	1.830	2.021	1.858	1.883	ns
	GCLK PLL	t_{SU}	1.135	1.260	1.317	1.282	1.400	ns
		t_{H}	–0.457	–0.486	–0.462	–0.504	–0.597	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.410	–1.556	–1.713	–1.584	–1.606	ns
		t_{H}	1.648	1.830	2.021	1.858	1.883	ns
	GCLK PLL	t_{SU}	1.135	1.260	1.317	1.282	1.400	ns
		t_{H}	–0.457	–0.486	–0.462	–0.504	–0.597	ns

Table 1–71. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.334	–1.478	–1.612	–1.501	–1.531	ns
		t_{H}	1.570	1.752	1.918	1.774	1.807	ns
	GCLK PLL	t_{SU}	1.211	1.334	1.412	1.354	1.473	ns
		t_{H}	–0.534	–0.562	–0.559	–0.578	–0.672	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.334	–1.478	–1.612	–1.501	–1.531	ns
		t_{H}	1.570	1.752	1.918	1.774	1.807	ns
	GCLK PLL	t_{SU}	1.211	1.334	1.412	1.354	1.473	ns
		t_{H}	–0.534	–0.562	–0.559	–0.578	–0.672	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.327	–1.475	–1.613	–1.497	–1.528	ns
		t_{H}	1.563	1.749	1.919	1.770	1.804	ns
	GCLK PLL	t_{SU}	1.218	1.337	1.411	1.358	1.476	ns
		t_{H}	–0.541	–0.565	–0.558	–0.582	–0.675	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.327	–1.475	–1.613	–1.497	–1.528	ns
		t_{H}	1.563	1.749	1.919	1.770	1.804	ns
	GCLK PLL	t_{SU}	1.218	1.337	1.411	1.358	1.476	ns
		t_{H}	–0.541	–0.565	–0.558	–0.582	–0.675	ns
2.5 V	GCLK	t_{SU}	–1.295	–1.447	–1.590	–1.469	–1.502	ns
		t_{H}	1.531	1.721	1.896	1.742	1.778	ns
	GCLK PLL	t_{SU}	1.250	1.365	1.434	1.386	1.502	ns
		t_{H}	–0.573	–0.593	–0.581	–0.610	–0.701	ns
1.8 V	GCLK	t_{SU}	–1.194	–1.382	–1.564	–1.402	–1.432	ns
		t_{H}	1.430	1.656	1.870	1.675	1.708	ns
	GCLK PLL	t_{SU}	1.351	1.430	1.460	1.453	1.572	ns
		t_{H}	–0.674	–0.658	–0.607	–0.677	–0.771	ns
1.5 V	GCLK	t_{SU}	–1.130	–1.296	–1.450	–1.318	–1.352	ns
		t_{H}	1.366	1.570	1.756	1.591	1.628	ns
	GCLK PLL	t_{SU}	1.415	1.516	1.574	1.537	1.652	ns
		t_{H}	–0.738	–0.744	–0.721	–0.761	–0.851	ns
1.2 V	GCLK	t_{SU}	–0.986	–1.115	–1.230	–1.143	–1.187	ns
		t_{H}	1.222	1.389	1.536	1.416	1.463	ns
	GCLK PLL	t_{SU}	1.559	1.697	1.794	1.712	1.817	ns
		t_{H}	–0.882	–0.925	–0.941	–0.936	–1.016	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.222	–1.414	–1.597	–1.433	–1.459	ns
		t_{H}	1.458	1.688	1.903	1.706	1.735	ns
	GCLK PLL	t_{SU}	1.323	1.398	1.427	1.422	1.545	ns
		t_{H}	–0.646	–0.626	–0.574	–0.646	–0.743	ns

Table 1–71. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-2 Class II	GCLK	t_{SU}	–1.222	–1.414	–1.597	–1.433	–1.459	ns
		t_H	1.458	1.688	1.903	1.706	1.735	ns
	GCLK PLL	t_{SU}	1.323	1.398	1.427	1.422	1.545	ns
		t_H	–0.646	–0.626	–0.574	–0.646	–0.743	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.055	–1.203	–1.333	–1.227	–1.262	ns
		t_H	1.291	1.477	1.639	1.500	1.538	ns
	GCLK PLL	t_{SU}	1.490	1.609	1.691	1.628	1.742	ns
		t_H	–0.813	–0.837	–0.838	–0.852	–0.940	ns
SSTL-18 Class II	GCLK	t_{SU}	–1.055	–1.203	–1.333	–1.227	–1.262	ns
		t_H	1.291	1.477	1.639	1.500	1.538	ns
	GCLK PLL	t_{SU}	1.490	1.609	1.691	1.628	1.742	ns
		t_H	–0.813	–0.837	–0.838	–0.852	–0.940	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.055	–1.203	–1.333	–1.227	–1.262	ns
		t_H	1.291	1.477	1.639	1.500	1.538	ns
	GCLK PLL	t_{SU}	1.490	1.609	1.691	1.628	1.742	ns
		t_H	–0.813	–0.837	–0.838	–0.852	–0.940	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.055	–1.203	–1.333	–1.227	–1.262	ns
		t_H	1.291	1.477	1.639	1.500	1.538	ns
	GCLK PLL	t_{SU}	1.490	1.609	1.691	1.628	1.742	ns
		t_H	–0.813	–0.837	–0.838	–0.852	–0.940	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.143	–1.301	–1.441	–1.324	–1.357	ns
		t_H	1.379	1.575	1.747	1.597	1.633	ns
	GCLK PLL	t_{SU}	1.402	1.511	1.583	1.531	1.647	ns
		t_H	–0.725	–0.739	–0.730	–0.755	–0.845	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.143	–1.301	–1.441	–1.324	–1.357	ns
		t_H	1.379	1.575	1.747	1.597	1.633	ns
	GCLK PLL	t_{SU}	1.402	1.511	1.583	1.531	1.647	ns
		t_H	–0.725	–0.739	–0.730	–0.755	–0.845	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–0.949	–1.065	–1.167	–1.098	–1.151	ns
		t_H	1.185	1.339	1.473	1.371	1.427	ns
	GCLK PLL	t_{SU}	1.596	1.747	1.857	1.757	1.853	ns
		t_H	–0.919	–0.975	–1.004	–0.981	–1.051	ns
3.0-V PCI	GCLK	t_{SU}	–1.327	–1.475	–1.613	–1.497	–1.528	ns
		t_H	1.563	1.749	1.919	1.770	1.804	ns
	GCLK PLL	t_{SU}	1.218	1.337	1.411	1.358	1.476	ns
		t_H	–0.541	–0.565	–0.558	–0.582	–0.675	ns

Table 1–71. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V PCI-X	GCLK	t_{SU}	–1.327	–1.475	–1.613	–1.497	–1.528	ns
		t_{H}	1.563	1.749	1.919	1.770	1.804	ns
	GCLK PLL	t_{SU}	1.218	1.337	1.411	1.358	1.476	ns
		t_{H}	–0.541	–0.565	–0.558	–0.582	–0.675	ns

Table 1–72. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.310	5.891	6.479	5.978	6.119	ns
		GCLK PLL	t_{CO}	3.216	7.941	8.618	8.099	8.290	ns
	8 mA	GCLK	t_{CO}	4.945	5.501	6.064	5.571	5.688	ns
		GCLK PLL	t_{CO}	2.851	5.292	5.829	5.371	5.449	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.054	5.622	6.196	5.701	5.831	ns
		GCLK PLL	t_{CO}	2.960	6.281	6.770	6.394	6.569	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.117	5.692	6.268	5.771	5.903	ns
		GCLK PLL	t_{CO}	3.023	6.524	7.047	6.655	6.847	ns
	8 mA	GCLK	t_{CO}	4.899	5.459	6.023	5.530	5.649	ns
		GCLK PLL	t_{CO}	2.805	4.969	5.457	5.056	5.126	ns
	12 mA	GCLK	t_{CO}	4.823	5.380	5.946	5.451	5.571	ns
		GCLK PLL	t_{CO}	2.729	4.240	4.692	4.301	4.336	ns
	16 mA	GCLK	t_{CO}	4.786	5.338	5.897	5.407	5.523	ns
		GCLK PLL	t_{CO}	2.692	3.851	4.291	3.905	3.945	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.904	5.464	6.028	5.535	5.654	ns
		GCLK PLL	t_{CO}	2.810	4.964	5.454	5.053	5.122	ns
	8 mA	GCLK	t_{CO}	4.785	5.338	5.898	5.407	5.523	ns
		GCLK PLL	t_{CO}	2.691	3.870	4.311	3.926	3.964	ns
	12 mA	GCLK	t_{CO}	4.759	5.307	5.862	5.375	5.489	ns
		GCLK PLL	t_{CO}	2.665	3.533	3.943	3.571	3.576	ns
	16 mA	GCLK	t_{CO}	4.747	5.294	5.848	5.361	5.474	ns
		GCLK PLL	t_{CO}	2.653	3.360	3.775	3.397	3.407	ns
2.5 V	4 mA	GCLK	t_{CO}	5.177	5.749	6.334	5.839	5.984	ns
		GCLK PLL	t_{CO}	3.083	6.981	7.599	7.154	7.375	ns
	8 mA	GCLK	t_{CO}	4.987	5.565	6.148	5.640	5.764	ns
		GCLK PLL	t_{CO}	2.893	5.049	5.574	5.142	5.223	ns
	12 mA	GCLK	t_{CO}	4.899	5.466	6.044	5.540	5.662	ns
		GCLK PLL	t_{CO}	2.805	4.386	4.864	4.449	4.496	ns
	16 mA	GCLK	t_{CO}	4.865	5.428	6.000	5.500	5.618	ns
		GCLK PLL	t_{CO}	2.771	4.074	4.542	4.133	4.167	ns

Table 1–72. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.8 V	2 mA	GCLK	t_{CO}	6.220	6.937	7.673	7.042	7.208	ns
		GCLK PLL	t_{CO}	4.126	12.142	13.341	12.451	12.905	ns
	4 mA	GCLK	t_{CO}	5.717	6.391	7.087	6.481	6.626	ns
		GCLK PLL	t_{CO}	3.623	7.816	8.685	7.952	8.114	ns
	6 mA	GCLK	t_{CO}	5.585	6.247	6.932	6.333	6.473	ns
		GCLK PLL	t_{CO}	3.491	6.448	7.180	6.557	6.683	ns
	8 mA	GCLK	t_{CO}	5.531	6.182	6.854	6.265	6.402	ns
		GCLK PLL	t_{CO}	3.437	5.677	6.338	5.763	5.844	ns
	10 mA	GCLK	t_{CO}	5.457	6.102	6.767	6.183	6.315	ns
		GCLK PLL	t_{CO}	3.363	5.321	5.966	5.398	5.468	ns
	12 mA	GCLK	t_{CO}	5.436	6.080	6.740	6.160	6.290	ns
		GCLK PLL	t_{CO}	3.342	4.957	5.559	5.025	5.080	ns
	16 mA	GCLK	t_{CO}	5.378	6.022	6.685	6.102	6.233	ns
		GCLK PLL	t_{CO}	3.284	4.597	5.173	4.660	4.701	ns
1.5 V	2 mA	GCLK	t_{CO}	6.578	7.399	8.281	7.494	7.642	ns
		GCLK PLL	t_{CO}	4.484	11.032	12.423	11.194	11.387	ns
	4 mA	GCLK	t_{CO}	6.230	7.001	7.813	7.086	7.220	ns
		GCLK PLL	t_{CO}	4.136	7.650	8.632	7.747	7.850	ns
	6 mA	GCLK	t_{CO}	6.078	6.835	7.633	6.918	7.050	ns
		GCLK PLL	t_{CO}	3.984	6.505	7.367	6.585	6.650	ns
	8 mA	GCLK	t_{CO}	6.037	6.782	7.567	6.862	6.989	ns
		GCLK PLL	t_{CO}	3.943	5.888	6.667	5.956	6.008	ns
	10 mA	GCLK	t_{CO}	5.986	6.730	7.510	6.809	6.934	ns
		GCLK PLL	t_{CO}	3.892	5.540	6.280	5.601	5.639	ns
	12 mA	GCLK	t_{CO}	5.944	6.686	7.462	6.765	6.890	ns
		GCLK PLL	t_{CO}	3.850	5.327	6.042	5.384	5.418	ns
	16 mA	GCLK	t_{CO}	5.873	6.605	7.372	6.683	6.808	ns
		GCLK PLL	t_{CO}	3.779	4.975	5.658	5.022	5.038	ns

Table 1–72. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.2 V	2 mA	GCLK	t_{CO}	7.761	8.871	10.107	8.928	9.012	ns
		GCLK PLL	t_{CO}	5.667	11.718	13.627	11.771	11.786	ns
	4 mA	GCLK	t_{CO}	7.440	8.497	9.667	8.548	8.624	ns
		GCLK PLL	t_{CO}	5.346	8.596	10.001	8.626	8.607	ns
	6 mA	GCLK	t_{CO}	7.325	8.370	9.526	8.421	8.498	ns
		GCLK PLL	t_{CO}	5.231	7.619	8.863	7.644	7.618	ns
	8 mA	GCLK	t_{CO}	7.209	8.226	9.347	8.274	8.348	ns
		GCLK PLL	t_{CO}	5.115	7.168	8.342	7.190	7.159	ns
	10 mA	GCLK	t_{CO}	7.185	8.201	9.321	8.249	8.323	ns
		GCLK PLL	t_{CO}	5.091	6.840	7.941	6.854	6.812	ns
	12 mA	GCLK	t_{CO}	7.161	8.173	9.289	8.221	8.294	ns
		GCLK PLL	t_{CO}	5.067	6.671	7.746	6.684	6.640	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.895	5.448	6.013	5.517	5.631	ns
		GCLK PLL	t_{CO}	2.793	3.146	3.548	3.176	3.166	ns
	12 mA	GCLK	t_{CO}	4.913	5.471	6.036	5.540	5.656	ns
		GCLK PLL	t_{CO}	2.811	3.169	3.571	3.199	3.191	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.886	5.441	6.004	5.510	5.626	ns
		GCLK PLL	t_{CO}	2.784	3.139	3.539	3.169	3.161	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.340	5.961	6.599	6.037	6.161	ns
		GCLK PLL	t_{CO}	3.238	3.659	4.134	3.696	3.696	ns
	10 mA	GCLK	t_{CO}	5.355	5.978	6.617	6.054	6.178	ns
		GCLK PLL	t_{CO}	3.253	3.676	4.152	3.713	3.713	ns
	12 mA	GCLK	t_{CO}	5.343	5.967	6.609	6.043	6.168	ns
		GCLK PLL	t_{CO}	3.241	3.665	4.144	3.702	3.703	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.326	5.944	6.578	6.020	6.144	ns
		GCLK PLL	t_{CO}	3.224	3.642	4.113	3.679	3.679	ns
	16 mA	GCLK	t_{CO}	5.304	5.920	6.552	5.995	6.119	ns
		GCLK PLL	t_{CO}	3.202	3.618	4.087	3.654	3.654	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.296	5.909	6.540	5.983	6.107	ns
		GCLK PLL	t_{CO}	3.194	3.607	4.075	3.642	3.642	ns
	10 mA	GCLK	t_{CO}	5.307	5.919	6.555	5.993	6.116	ns
		GCLK PLL	t_{CO}	3.205	3.617	4.090	3.652	3.651	ns
	12 mA	GCLK	t_{CO}	5.332	5.948	6.580	6.023	6.147	ns
		GCLK PLL	t_{CO}	3.230	3.646	4.115	3.682	3.682	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.279	5.883	6.497	5.958	6.083	ns
		GCLK PLL	t_{CO}	3.177	3.581	4.032	3.617	3.618	ns

Table 1–72. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.807	6.512	7.253	6.587	6.708	ns
		GCLK PLL	t_{CO}	3.705	4.210	4.788	4.246	4.243	ns
	10 mA	GCLK	t_{CO}	5.823	6.521	7.246	6.597	6.720	ns
		GCLK PLL	t_{CO}	3.721	4.219	4.781	4.256	4.255	ns
	12 mA	GCLK	t_{CO}	5.837	6.537	7.264	6.613	6.736	ns
		GCLK PLL	t_{CO}	3.735	4.235	4.799	4.272	4.271	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.767	6.462	7.190	6.537	6.657	ns
		GCLK PLL	t_{CO}	3.665	4.160	4.725	4.196	4.192	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.986	7.961	9.043	8.009	8.083	ns
		GCLK PLL	t_{CO}	4.884	5.659	6.578	5.668	5.618	ns
	10 mA	GCLK	t_{CO}	6.933	7.885	8.933	7.933	8.007	ns
		GCLK PLL	t_{CO}	4.831	5.583	6.468	5.592	5.542	ns
	12 mA	GCLK	t_{CO}	6.935	7.888	8.937	7.936	8.010	ns
		GCLK PLL	t_{CO}	4.833	5.586	6.472	5.595	5.545	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.861	7.799	8.855	7.849	7.929	ns
		GCLK PLL	t_{CO}	4.759	5.497	6.390	5.508	5.464	ns
3.0-V PCI	—	GCLK	t_{CO}	5.056	5.611	6.173	5.682	5.801	ns
		GCLK PLL	t_{CO}	2.962	3.809	4.270	3.856	3.882	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.056	5.611	6.173	5.682	5.801	ns
		GCLK PLL	t_{CO}	2.962	3.809	4.270	3.856	3.882	ns

Table 1–73. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.780	6.385	6.999	6.484	6.645	ns
		GCLK PLL	t_{CO}	7.495	8.108	8.794	8.271	8.470	ns
	8 mA	GCLK	t_{CO}	5.163	5.723	6.293	5.797	5.923	ns
		GCLK PLL	t_{CO}	4.888	5.371	5.853	5.436	5.478	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.323	5.900	6.482	5.983	6.122	ns
		GCLK PLL	t_{CO}	5.942	6.379	6.896	6.528	6.702	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.404	5.983	6.575	6.070	6.216	ns
		GCLK PLL	t_{CO}	6.168	6.633	7.183	6.796	6.990	ns
	8 mA	GCLK	t_{CO}	5.050	5.603	6.171	5.680	5.815	ns
		GCLK PLL	t_{CO}	4.580	5.014	5.500	5.091	5.190	ns
	12 mA	GCLK	t_{CO}	4.931	5.486	6.050	5.558	5.678	ns
		GCLK PLL	t_{CO}	3.850	4.245	4.691	4.300	4.344	ns
	16 mA	GCLK	t_{CO}	4.856	5.414	5.980	5.486	5.606	ns
		GCLK PLL	t_{CO}	3.465	3.846	4.285	3.905	3.938	ns

Table 1–73. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.049	5.601	6.182	5.678	5.812	ns
		GCLK PLL	t_{CO}	4.575	5.011	5.497	5.088	5.187	ns
	8 mA	GCLK	t_{CO}	4.853	5.415	5.983	5.488	5.608	ns
		GCLK PLL	t_{CO}	3.483	3.866	4.303	3.924	3.955	ns
	12 mA	GCLK	t_{CO}	4.780	5.328	5.886	5.398	5.516	ns
		GCLK PLL	t_{CO}	3.144	3.498	3.908	3.537	3.549	ns
	16 mA	GCLK	t_{CO}	4.756	5.302	5.857	5.370	5.486	ns
		GCLK PLL	t_{CO}	2.968	3.323	3.739	3.365	3.377	ns
2.5 V	4 mA	GCLK	t_{CO}	5.579	6.160	6.757	6.259	6.434	ns
		GCLK PLL	t_{CO}	6.576	7.132	7.755	7.300	7.532	ns
	8 mA	GCLK	t_{CO}	5.151	5.723	6.310	5.806	5.943	ns
		GCLK PLL	t_{CO}	4.631	5.101	5.621	5.186	5.281	ns
	12 mA	GCLK	t_{CO}	5.019	5.584	6.159	5.661	5.789	ns
		GCLK PLL	t_{CO}	3.973	4.392	4.875	4.456	4.512	ns
	16 mA	GCLK	t_{CO}	4.947	5.509	6.084	5.584	5.708	ns
		GCLK PLL	t_{CO}	3.656	4.069	4.532	4.126	4.158	ns
1.8 V	2 mA	GCLK	t_{CO}	7.044	7.794	8.576	7.938	8.166	ns
		GCLK PLL	t_{CO}	11.424	12.515	13.745	12.836	13.311	ns
	4 mA	GCLK	t_{CO}	6.136	6.838	7.579	6.942	7.107	ns
		GCLK PLL	t_{CO}	7.206	7.980	8.863	8.119	8.290	ns
	6 mA	GCLK	t_{CO}	5.823	6.488	7.195	6.583	6.737	ns
		GCLK PLL	t_{CO}	5.888	6.537	7.281	6.655	6.782	ns
	8 mA	GCLK	t_{CO}	5.688	6.352	7.037	6.438	6.580	ns
		GCLK PLL	t_{CO}	5.130	5.717	6.389	5.806	5.896	ns
	10 mA	GCLK	t_{CO}	5.594	6.244	6.922	6.331	6.470	ns
		GCLK PLL	t_{CO}	4.788	5.354	5.997	5.433	5.496	ns
	12 mA	GCLK	t_{CO}	5.529	6.179	6.853	6.262	6.401	ns
		GCLK PLL	t_{CO}	4.441	4.966	5.576	5.038	5.098	ns
	16 mA	GCLK	t_{CO}	5.464	6.106	6.769	6.186	6.319	ns
		GCLK PLL	t_{CO}	4.085	4.594	5.161	4.655	4.692	ns

Table 1–73. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
1.5 V	2 mA	GCLK	t_{CO}	7.232	8.125	9.090	8.232	8.402	ns
		GCLK PLL	t_{CO}	10.101	11.327	12.753	11.490	11.694	ns
	4 mA	GCLK	t_{CO}	6.528	7.328	8.173	7.421	7.569	ns
		GCLK PLL	t_{CO}	6.895	7.759	8.755	7.862	7.963	ns
	6 mA	GCLK	t_{CO}	6.269	7.048	7.870	7.135	7.274	ns
		GCLK PLL	t_{CO}	5.810	6.561	7.430	6.640	6.709	ns
	8 mA	GCLK	t_{CO}	6.157	6.918	7.715	7.000	7.132	ns
		GCLK PLL	t_{CO}	5.234	5.907	6.689	5.979	6.031	ns
	10 mA	GCLK	t_{CO}	6.080	6.836	7.632	6.917	7.049	ns
		GCLK PLL	t_{CO}	4.895	5.542	6.292	5.604	5.646	ns
	12 mA	GCLK	t_{CO}	6.020	6.766	7.553	6.846	6.975	ns
		GCLK PLL	t_{CO}	4.699	5.316	6.038	5.376	5.412	ns
	16 mA	GCLK	t_{CO}	5.985	6.728	7.507	6.807	6.933	ns
		GCLK PLL	t_{CO}	4.397	4.994	5.688	5.044	5.061	ns
1.2 V	2 mA	GCLK	t_{CO}	8.289	9.481	10.827	9.541	9.627	ns
		GCLK PLL	t_{CO}	10.352	11.971	13.928	12.027	12.045	ns
	4 mA	GCLK	t_{CO}	7.652	8.741	9.966	8.796	8.876	ns
		GCLK PLL	t_{CO}	7.495	8.680	10.106	8.712	8.694	ns
	6 mA	GCLK	t_{CO}	7.472	8.532	9.711	8.585	8.663	ns
		GCLK PLL	t_{CO}	6.605	7.650	8.903	7.676	7.650	ns
	8 mA	GCLK	t_{CO}	7.368	8.417	9.580	8.468	8.544	ns
		GCLK PLL	t_{CO}	6.194	7.179	8.358	7.201	7.169	ns
	10 mA	GCLK	t_{CO}	7.309	8.350	9.504	8.402	8.478	ns
		GCLK PLL	t_{CO}	5.916	6.860	7.980	6.876	6.833	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.027	5.581	6.145	5.652	5.770	ns
		GCLK PLL	t_{CO}	2.944	3.292	3.693	3.323	3.316	ns
	12 mA	GCLK	t_{CO}	4.986	5.539	6.103	5.609	5.727	ns
		GCLK PLL	t_{CO}	2.903	3.250	3.651	3.280	3.273	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.924	5.476	6.038	5.546	5.662	ns
		GCLK PLL	t_{CO}	2.841	3.187	3.586	3.217	3.208	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.417	6.039	6.683	6.118	6.244	ns
		GCLK PLL	t_{CO}	3.334	3.750	4.231	3.789	3.790	ns
	10 mA	GCLK	t_{CO}	5.411	6.033	6.671	6.109	6.237	ns
		GCLK PLL	t_{CO}	3.328	3.744	4.219	3.780	3.783	ns
	12 mA	GCLK	t_{CO}	5.384	6.006	6.645	6.082	6.210	ns
		GCLK PLL	t_{CO}	3.301	3.717	4.193	3.753	3.756	ns

Table 1–73. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.374	5.993	6.627	6.068	6.195	ns
		GCLK PLL	t_{CO}	3.291	3.704	4.175	3.739	3.741	ns
	16 mA	GCLK	t_{CO}	5.354	5.974	6.609	6.049	6.175	ns
		GCLK PLL	t_{CO}	3.271	3.685	4.157	3.720	3.721	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.393	6.006	6.638	6.083	6.208	ns
		GCLK PLL	t_{CO}	3.310	3.717	4.186	3.754	3.754	ns
	10 mA	GCLK	t_{CO}	5.391	6.008	6.646	6.085	6.210	ns
		GCLK PLL	t_{CO}	3.308	3.719	4.194	3.756	3.756	ns
	12 mA	GCLK	t_{CO}	5.385	6.001	6.633	6.077	6.203	ns
		GCLK PLL	t_{CO}	3.302	3.712	4.181	3.748	3.749	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.330	5.935	6.553	6.009	6.134	ns
		GCLK PLL	t_{CO}	3.247	3.646	4.101	3.680	3.680	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.911	6.618	7.362	6.695	6.817	ns
		GCLK PLL	t_{CO}	3.828	4.329	4.910	4.366	4.363	ns
	10 mA	GCLK	t_{CO}	5.889	6.591	7.323	6.666	6.788	ns
		GCLK PLL	t_{CO}	3.806	4.302	4.871	4.337	4.334	ns
	12 mA	GCLK	t_{CO}	5.906	6.611	7.348	6.687	6.810	ns
		GCLK PLL	t_{CO}	3.823	4.322	4.896	4.358	4.356	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.827	6.523	7.253	6.598	6.718	ns
		GCLK PLL	t_{CO}	3.744	4.234	4.801	4.269	4.264	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.077	8.054	9.133	8.103	8.178	ns
		GCLK PLL	t_{CO}	4.994	5.765	6.681	5.774	5.724	ns
	10 mA	GCLK	t_{CO}	7.071	8.018	9.047	8.069	8.148	ns
		GCLK PLL	t_{CO}	4.988	5.729	6.595	5.740	5.694	ns
3.0-V PCI	—	GCLK	t_{CO}	5.101	5.655	6.218	5.726	5.846	ns
		GCLK PLL	t_{CO}	3.381	3.777	4.264	3.830	3.874	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.101	5.655	6.218	5.726	5.846	ns
		GCLK PLL	t_{CO}	3.381	3.777	4.264	3.830	3.874	ns

Table 1–74. EP3C40 Column Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–1.378	–1.547	–1.731	–1.583	–1.610	ns
	—		t_{H}	1.641	1.851	2.071	1.886	1.916	ns
	—	GCLK PLL	t_{SU}	1.176	1.274	1.301	1.280	1.400	ns
	—		t_{H}	–0.473	–0.471	–0.414	–0.475	–0.568	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.852	5.410	5.978	5.480	5.598	ns
	—	GCLK PLL	t_{CO}	2.753	3.103	3.508	3.134	3.127	ns

Table 1–74. EP3C40 Column Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
BLVDS	—	GCLK	t_{SU}	–1.337	–1.500	–1.678	–1.534	–1.562	ns
	—		t_{H}	1.598	1.802	2.016	1.835	1.866	ns
	—	GCLK PLL	t_{SU}	1.208	1.310	1.344	1.320	1.439	ns
	—		t_{H}	–0.624	–0.642	–0.604	–0.651	–0.750	ns
	8 mA	GCLK	t_{CO}	5.344	5.918	6.499	5.991	6.112	ns
		GCLK PLL	t_{CO}	3.104	3.453	3.859	3.486	3.475	ns
	12 mA	GCLK	t_{CO}	5.344	5.918	6.499	5.991	6.112	ns
		GCLK PLL	t_{CO}	3.104	3.453	3.859	3.486	3.475	ns
	16 mA	GCLK	t_{CO}	5.344	5.918	6.499	5.991	6.112	ns
		GCLK PLL	t_{CO}	3.104	3.453	3.859	3.486	3.475	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.852	5.410	5.978	5.480	5.598	ns
	—	GCLK PLL	t_{CO}	2.753	3.103	3.508	3.134	3.127	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.852	5.410	5.978	5.480	5.598	ns
	—	GCLK PLL	t_{CO}	2.753	3.103	3.508	3.134	3.127	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.776	5.307	5.843	5.373	5.484	ns
	—	GCLK PLL	t_{CO}	2.677	3.000	3.373	3.027	3.013	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.852	5.410	5.978	5.480	5.598	ns
	—	GCLK PLL	t_{CO}	2.753	3.103	3.508	3.134	3.127	ns

Table 1–75. EP3C40 Row Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
LVDS	—	GCLK	t_{SU}	–1.336	–1.499	–1.677	–1.533	–1.562	ns
	—		t_{H}	1.597	1.802	2.015	1.834	1.866	ns
	—		t_{CO}	4.053	4.543	5.000	4.508	4.574	ns
	—	GCLK PLL	t_{SU}	1.207	1.310	1.343	1.319	1.438	ns
	—		t_{H}	–0.505	–0.508	–0.458	–0.515	–0.608	ns
	—		t_{CO}	1.971	2.255	2.549	2.180	2.122	ns
BLVDS	—	GCLK	t_{SU}	–1.335	–1.499	–1.676	–1.532	–1.561	ns
	—		t_{H}	1.596	1.801	2.014	1.833	1.865	ns
	—	GCLK PLL	t_{SU}	1.206	1.309	1.342	1.318	1.438	ns
	—		t_{H}	–0.622	–0.641	–0.602	–0.649	–0.749	ns
	8 mA	GCLK	t_{CO}	5.324	5.896	6.477	5.970	6.090	ns
		GCLK PLL	t_{CO}	3.124	3.475	3.881	3.507	3.497	ns
	12 mA	GCLK	t_{CO}	5.324	5.896	6.477	5.970	6.090	ns
		GCLK PLL	t_{CO}	3.124	3.475	3.881	3.507	3.497	ns
	16 mA	GCLK	t_{CO}	5.324	5.896	6.477	5.970	6.090	ns
		GCLK PLL	t_{CO}	3.124	3.475	3.881	3.507	3.497	ns

Table 1–75. EP3C40 Row Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	A7	Unit
mini-LVDS	—	GCLK	t_{CO}	4.053	4.543	5.000	4.508	4.574	ns
	—	GCLK PLL	t_{CO}	1.971	2.255	2.549	2.180	2.122	ns
PPDS	—	GCLK	t_{CO}	4.053	4.543	5.000	4.508	4.574	ns
	—	GCLK PLL	t_{CO}	1.971	2.255	2.549	2.180	2.122	ns
RSDS	—	GCLK	t_{CO}	4.053	4.543	5.000	4.508	4.574	ns
	—	GCLK PLL	t_{CO}	1.971	2.255	2.549	2.180	2.122	ns

EP3C55 I/O Timing Parameters

Table 1–76 through Table 1–81 show the maximum I/O timing parameters for EP3C55 devices.

Table 1–76. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.447	–1.611	–1.764	–1.631	ns
		t_{H}	1.688	1.890	2.076	1.910	ns
	GCLK PLL	t_{SU}	1.083	1.227	1.280	1.251	ns
		t_{H}	–0.412	–0.461	–0.433	–0.479	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.447	–1.611	–1.764	–1.631	ns
		t_{H}	1.688	1.890	2.076	1.910	ns
	GCLK PLL	t_{SU}	1.083	1.227	1.280	1.251	ns
		t_{H}	–0.412	–0.461	–0.433	–0.479	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.439	–1.608	–1.767	–1.629	ns
		t_{H}	1.680	1.887	2.079	1.908	ns
	GCLK PLL	t_{SU}	1.091	1.230	1.277	1.253	ns
		t_{H}	–0.420	–0.464	–0.430	–0.481	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.439	–1.608	–1.767	–1.629	ns
		t_{H}	1.680	1.887	2.079	1.908	ns
	GCLK PLL	t_{SU}	1.091	1.230	1.277	1.253	ns
		t_{H}	–0.420	–0.464	–0.430	–0.481	ns
2.5 V	GCLK	t_{SU}	–1.408	–1.581	–1.742	–1.603	ns
		t_{H}	1.649	1.860	2.054	1.882	ns
	GCLK PLL	t_{SU}	1.122	1.257	1.302	1.279	ns
		t_{H}	–0.451	–0.491	–0.455	–0.507	ns
1.8 V	GCLK	t_{SU}	–1.305	–1.514	–1.705	–1.533	ns
		t_{H}	1.546	1.793	2.017	1.812	ns
	GCLK PLL	t_{SU}	1.225	1.324	1.339	1.349	ns
		t_{H}	–0.554	–0.558	–0.492	–0.577	ns

Table 1–76. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
1.5 V	GCLK	t_{SU}	–1.241	–1.427	–1.593	–1.449	ns
		t_H	1.482	1.706	1.905	1.728	ns
	GCLK PLL	t_{SU}	1.289	1.411	1.451	1.433	ns
		t_H	–0.618	–0.645	–0.604	–0.661	ns
1.2 V	GCLK	t_{SU}	–1.108	–1.249	–1.389	–1.276	ns
		t_H	1.349	1.528	1.701	1.555	ns
	GCLK PLL	t_{SU}	1.422	1.589	1.655	1.606	ns
		t_H	–0.751	–0.823	–0.808	–0.834	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.331	–1.548	–1.744	–1.563	ns
		t_H	1.572	1.826	2.055	1.842	ns
	GCLK PLL	t_{SU}	1.230	1.283	1.300	1.309	ns
		t_H	–0.559	–0.517	–0.453	–0.537	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.331	–1.548	–1.744	–1.563	ns
		t_H	1.572	1.826	2.055	1.842	ns
	GCLK PLL	t_{SU}	1.230	1.283	1.300	1.309	ns
		t_H	–0.559	–0.517	–0.453	–0.537	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.161	–1.327	–1.461	–1.347	ns
		t_H	1.402	1.605	1.772	1.626	ns
	GCLK PLL	t_{SU}	1.400	1.504	1.583	1.525	ns
		t_H	–0.729	–0.738	–0.736	–0.753	ns
SSTL-18 Class II	GCLK	t_{SU}	–1.161	–1.327	–1.461	–1.347	ns
		t_H	1.402	1.605	1.772	1.626	ns
	GCLK PLL	t_{SU}	1.400	1.504	1.583	1.525	ns
		t_H	–0.729	–0.738	–0.736	–0.753	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.161	–1.327	–1.461	–1.347	ns
		t_H	1.402	1.605	1.772	1.626	ns
	GCLK PLL	t_{SU}	1.400	1.504	1.583	1.525	ns
		t_H	–0.729	–0.738	–0.736	–0.753	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.161	–1.327	–1.461	–1.347	ns
		t_H	1.402	1.605	1.772	1.626	ns
	GCLK PLL	t_{SU}	1.400	1.504	1.583	1.525	ns
		t_H	–0.729	–0.738	–0.736	–0.753	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.252	–1.435	–1.589	–1.455	ns
		t_H	1.493	1.713	1.900	1.734	ns
	GCLK PLL	t_{SU}	1.309	1.396	1.455	1.417	ns
		t_H	–0.638	–0.630	–0.608	–0.645	ns

Table 1–76. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
1.5-V HSTL Class II	GCLK	t_{SU}	–1.252	–1.435	–1.589	–1.455	ns
		t_{H}	1.493	1.713	1.900	1.734	ns
	GCLK PLL	t_{SU}	1.309	1.396	1.455	1.417	ns
		t_{H}	–0.638	–0.630	–0.608	–0.645	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.064	–1.190	–1.307	–1.220	ns
		t_{H}	1.305	1.468	1.618	1.499	ns
	GCLK PLL	t_{SU}	1.497	1.641	1.737	1.652	ns
		t_{H}	–0.826	–0.875	–0.890	–0.880	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–1.064	–1.190	–1.307	–1.220	ns
		t_{H}	1.305	1.468	1.618	1.499	ns
	GCLK PLL	t_{SU}	1.497	1.641	1.737	1.652	ns
		t_{H}	–0.826	–0.875	–0.890	–0.880	ns
3.0-V PCI	GCLK	t_{SU}	–1.439	–1.608	–1.767	–1.629	ns
		t_{H}	1.680	1.887	2.079	1.908	ns
	GCLK PLL	t_{SU}	1.091	1.230	1.277	1.253	ns
		t_{H}	–0.420	–0.464	–0.430	–0.481	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.439	–1.608	–1.767	–1.629	ns
		t_{H}	1.680	1.887	2.079	1.908	ns
	GCLK PLL	t_{SU}	1.091	1.230	1.277	1.253	ns
		t_{H}	–0.420	–0.464	–0.430	–0.481	ns

Table 1–77. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.412	–1.565	–1.702	–1.585	ns
		t_{H}	1.653	1.843	2.012	1.863	ns
	GCLK PLL	t_{SU}	1.134	1.251	1.329	1.276	ns
		t_{H}	–0.464	–0.486	–0.484	–0.506	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.412	–1.565	–1.702	–1.585	ns
		t_{H}	1.653	1.843	2.012	1.863	ns
	GCLK PLL	t_{SU}	1.134	1.251	1.329	1.276	ns
		t_{H}	–0.464	–0.486	–0.484	–0.506	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.407	–1.561	–1.704	–1.582	ns
		t_{H}	1.648	1.839	2.014	1.860	ns
	GCLK PLL	t_{SU}	1.139	1.255	1.327	1.279	ns
		t_{H}	–0.469	–0.490	–0.482	–0.509	ns

Table 1–77. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.0-V LVCMOS	GCLK	t_{SU}	–1.407	–1.561	–1.704	–1.582	ns
		t_{H}	1.648	1.839	2.014	1.860	ns
	GCLK PLL	t_{SU}	1.139	1.255	1.327	1.279	ns
		t_{H}	–0.469	–0.490	–0.482	–0.509	ns
2.5 V	GCLK	t_{SU}	–1.374	–1.534	–1.684	–1.555	ns
		t_{H}	1.615	1.812	1.994	1.833	ns
	GCLK PLL	t_{SU}	1.172	1.282	1.347	1.306	ns
		t_{H}	–0.502	–0.517	–0.502	–0.536	ns
1.8 V	GCLK	t_{SU}	–1.272	–1.467	–1.647	–1.486	ns
		t_{H}	1.513	1.745	1.957	1.764	ns
	GCLK PLL	t_{SU}	1.274	1.349	1.384	1.375	ns
		t_{H}	–0.604	–0.584	–0.539	–0.605	ns
1.5 V	GCLK	t_{SU}	–1.207	–1.380	–1.536	–1.402	ns
		t_{H}	1.448	1.658	1.846	1.680	ns
	GCLK PLL	t_{SU}	1.339	1.436	1.495	1.459	ns
		t_{H}	–0.669	–0.671	–0.650	–0.689	ns
1.2 V	GCLK	t_{SU}	–1.070	–1.201	–1.331	–1.228	ns
		t_{H}	1.311	1.479	1.641	1.506	ns
	GCLK PLL	t_{SU}	1.476	1.615	1.700	1.633	ns
		t_{H}	–0.806	–0.850	–0.855	–0.863	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.302	–1.499	–1.691	–1.514	ns
		t_{H}	1.543	1.777	2.001	1.792	ns
	GCLK PLL	t_{SU}	1.244	1.317	1.340	1.347	ns
		t_{H}	–0.574	–0.552	–0.495	–0.577	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.302	–1.499	–1.691	–1.514	ns
		t_{H}	1.543	1.777	2.001	1.792	ns
	GCLK PLL	t_{SU}	1.244	1.317	1.340	1.347	ns
		t_{H}	–0.574	–0.552	–0.495	–0.577	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.125	–1.278	–1.409	–1.300	ns
		t_{H}	1.366	1.556	1.719	1.578	ns
	GCLK PLL	t_{SU}	1.421	1.538	1.622	1.561	ns
		t_{H}	–0.751	–0.773	–0.777	–0.791	ns
SSTL-18 Class II	GCLK	t_{SU}	–1.125	–1.278	–1.409	–1.300	ns
		t_{H}	1.366	1.556	1.719	1.578	ns
	GCLK PLL	t_{SU}	1.421	1.538	1.622	1.561	ns
		t_{H}	–0.751	–0.773	–0.777	–0.791	ns

Table 1–77. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
1.8-V HSTL Class I	GCLK	t_{SU}	–1.125	–1.278	–1.409	–1.300	ns
		t_{H}	1.366	1.556	1.719	1.578	ns
	GCLK PLL	t_{SU}	1.421	1.538	1.622	1.561	ns
		t_{H}	–0.751	–0.773	–0.777	–0.791	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.125	–1.278	–1.409	–1.300	ns
		t_{H}	1.366	1.556	1.719	1.578	ns
	GCLK PLL	t_{SU}	1.421	1.538	1.622	1.561	ns
		t_{H}	–0.751	–0.773	–0.777	–0.791	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.223	–1.384	–1.528	–1.407	ns
		t_{H}	1.464	1.662	1.838	1.685	ns
	GCLK PLL	t_{SU}	1.323	1.432	1.503	1.454	ns
		t_{H}	–0.653	–0.667	–0.658	–0.684	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.223	–1.384	–1.528	–1.407	ns
		t_{H}	1.464	1.662	1.838	1.685	ns
	GCLK PLL	t_{SU}	1.323	1.432	1.503	1.454	ns
		t_{H}	–0.653	–0.667	–0.658	–0.684	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.024	–1.140	–1.257	–1.172	ns
		t_{H}	1.265	1.418	1.567	1.450	ns
	GCLK PLL	t_{SU}	1.522	1.676	1.774	1.689	ns
		t_{H}	–0.852	–0.911	–0.929	–0.919	ns
3.0-V PCI	GCLK	t_{SU}	–1.407	–1.561	–1.704	–1.582	ns
		t_{H}	1.648	1.839	2.014	1.860	ns
	GCLK PLL	t_{SU}	1.139	1.255	1.327	1.279	ns
		t_{H}	–0.469	–0.490	–0.482	–0.509	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.407	–1.561	–1.704	–1.582	ns
		t_{H}	1.648	1.839	2.014	1.860	ns
	GCLK PLL	t_{SU}	1.139	1.255	1.327	1.279	ns
		t_{H}	–0.469	–0.490	–0.482	–0.509	ns

Table 1–78. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.252	10.139	10.940	10.322	ns
		GCLK PLL	t_{CO}	7.206	3.484	3.879	3.527	ns
	8 mA	GCLK	t_{CO}	4.936	7.546	8.207	7.659	ns
		GCLK PLL	t_{CO}	4.780	3.151	3.531	3.183	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.001	8.344	8.984	8.495	ns
		GCLK PLL	t_{CO}	5.560	3.224	3.606	3.262	ns

Table 1–78. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.063	8.801	9.468	8.970	ns
		GCLK PLL	t_{CO}	5.983	3.289	3.680	3.330	ns
	8 mA	GCLK	t_{CO}	4.872	7.175	7.816	7.301	ns
		GCLK PLL	t_{CO}	4.423	3.090	3.471	3.124	ns
	12 mA	GCLK	t_{CO}	4.815	6.522	7.114	6.619	ns
		GCLK PLL	t_{CO}	3.773	3.022	3.392	3.050	ns
	16 mA	GCLK	t_{CO}	4.786	6.118	6.692	6.204	ns
		GCLK PLL	t_{CO}	3.415	2.989	3.354	3.017	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.879	7.172	7.813	7.297	ns
		GCLK PLL	t_{CO}	4.421	3.097	3.478	3.131	ns
	8 mA	GCLK	t_{CO}	4.785	6.154	6.738	6.245	ns
		GCLK PLL	t_{CO}	3.444	2.990	3.358	3.018	ns
	12 mA	GCLK	t_{CO}	4.753	5.822	6.376	5.896	ns
		GCLK PLL	t_{CO}	3.131	2.958	3.325	2.986	ns
	16 mA	GCLK	t_{CO}	4.739	5.643	6.200	5.718	ns
		GCLK PLL	t_{CO}	2.955	2.945	3.313	2.973	ns
2.5 V	4 mA	GCLK	t_{CO}	5.166	9.038	9.787	9.246	ns
		GCLK PLL	t_{CO}	6.167	3.395	3.798	3.446	ns
	8 mA	GCLK	t_{CO}	4.985	7.343	8.008	7.471	ns
		GCLK PLL	t_{CO}	4.549	3.215	3.613	3.254	ns
	12 mA	GCLK	t_{CO}	4.913	6.666	7.285	6.765	ns
		GCLK PLL	t_{CO}	3.900	3.132	3.518	3.166	ns
	16 mA	GCLK	t_{CO}	4.883	6.339	6.951	6.435	ns
		GCLK PLL	t_{CO}	3.593	3.103	3.489	3.135	ns
1.8 V	2 mA	GCLK	t_{CO}	6.120	13.785	15.077	14.113	ns
		GCLK PLL	t_{CO}	10.427	4.480	5.019	4.539	ns
	4 mA	GCLK	t_{CO}	5.749	10.114	11.128	10.288	ns
		GCLK PLL	t_{CO}	7.021	4.087	4.606	4.140	ns
	6 mA	GCLK	t_{CO}	5.556	8.663	9.533	8.811	ns
		GCLK PLL	t_{CO}	5.691	3.871	4.366	3.916	ns
	8 mA	GCLK	t_{CO}	5.495	7.945	8.747	8.068	ns
		GCLK PLL	t_{CO}	5.030	3.800	4.280	3.842	ns
	10 mA	GCLK	t_{CO}	5.436	7.572	8.359	7.683	ns
		GCLK PLL	t_{CO}	4.681	3.738	4.220	3.780	ns
	12 mA	GCLK	t_{CO}	5.389	7.241	7.984	7.346	ns
		GCLK PLL	t_{CO}	4.373	3.688	4.156	3.726	ns
	16 mA	GCLK	t_{CO}	5.347	6.894	7.613	6.993	ns
		GCLK PLL	t_{CO}	4.055	3.646	4.118	3.685	ns

Table 1–78. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
1.5 V	2 mA	GCLK	t_{CO}	6.607	13.329	14.868	13.527	ns
		GCLK PLL	t_{CO}	9.793	5.095	5.804	5.151	ns
	4 mA	GCLK	t_{CO}	6.201	9.904	11.027	10.040	ns
		GCLK PLL	t_{CO}	6.720	4.623	5.256	4.676	ns
	6 mA	GCLK	t_{CO}	6.060	8.776	9.786	8.897	ns
		GCLK PLL	t_{CO}	5.699	4.480	5.099	4.528	ns
	8 mA	GCLK	t_{CO}	5.974	8.179	9.107	8.289	ns
		GCLK PLL	t_{CO}	5.170	4.366	4.965	4.416	ns
	10 mA	GCLK	t_{CO}	5.936	7.836	8.727	7.939	ns
		GCLK PLL	t_{CO}	4.852	4.328	4.916	4.368	ns
	12 mA	GCLK	t_{CO}	5.903	7.610	8.472	7.709	ns
		GCLK PLL	t_{CO}	4.652	4.293	4.874	4.334	ns
	16 mA	GCLK	t_{CO}	5.795	7.223	8.027	7.317	ns
		GCLK PLL	t_{CO}	4.312	4.175	4.741	4.214	ns
1.2 V	2 mA	GCLK	t_{CO}	7.738	13.898	15.940	13.986	ns
		GCLK PLL	t_{CO}	9.990	6.513	7.579	6.529	ns
	4 mA	GCLK	t_{CO}	7.380	10.869	12.420	10.936	ns
		GCLK PLL	t_{CO}	7.362	6.099	7.097	6.112	ns
	6 mA	GCLK	t_{CO}	7.244	9.920	11.312	9.983	ns
		GCLK PLL	t_{CO}	6.543	5.936	6.900	5.950	ns
	8 mA	GCLK	t_{CO}	7.184	9.451	10.769	9.509	ns
		GCLK PLL	t_{CO}	6.134	5.868	6.824	5.881	ns
	10 mA	GCLK	t_{CO}	7.053	9.045	10.275	9.099	ns
		GCLK PLL	t_{CO}	5.797	5.699	6.601	5.709	ns
	12 mA	GCLK	t_{CO}	7.036	8.869	10.074	8.922	ns
		GCLK PLL	t_{CO}	5.641	5.682	6.586	5.691	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.911	5.475	6.018	5.542	ns
		GCLK PLL	t_{CO}	2.805	3.146	3.529	3.176	ns
	12 mA	GCLK	t_{CO}	4.891	5.453	5.995	5.520	ns
		GCLK PLL	t_{CO}	2.785	3.124	3.506	3.154	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.856	5.414	5.952	5.480	ns
		GCLK PLL	t_{CO}	2.750	3.085	3.463	3.114	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.328	5.959	6.579	6.032	ns
		GCLK PLL	t_{CO}	3.222	3.630	4.090	3.666	ns
	10 mA	GCLK	t_{CO}	5.304	5.928	6.540	6.002	ns
		GCLK PLL	t_{CO}	3.198	3.599	4.051	3.636	ns
	12 mA	GCLK	t_{CO}	5.301	5.927	6.536	6.000	ns
		GCLK PLL	t_{CO}	3.195	3.598	4.047	3.634	ns

Table 1–78. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.286	5.909	6.521	5.982	ns
		GCLK PLL	t_{CO}	3.180	3.580	4.032	3.616	ns
	16 mA	GCLK	t_{CO}	5.273	5.897	6.507	5.969	ns
		GCLK PLL	t_{CO}	3.167	3.568	4.018	3.603	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.312	5.935	6.546	6.008	ns
		GCLK PLL	t_{CO}	3.206	3.606	4.057	3.642	ns
	10 mA	GCLK	t_{CO}	5.305	5.931	6.544	6.003	ns
		GCLK PLL	t_{CO}	3.199	3.602	4.055	3.637	ns
	12 mA	GCLK	t_{CO}	5.291	5.912	6.521	5.985	ns
		GCLK PLL	t_{CO}	3.185	3.583	4.032	3.619	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.272	5.890	6.495	5.962	ns
		GCLK PLL	t_{CO}	3.166	3.561	4.006	3.596	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.810	6.522	7.243	6.598	ns
		GCLK PLL	t_{CO}	3.704	4.193	4.754	4.232	ns
	10 mA	GCLK	t_{CO}	5.806	6.512	7.228	6.590	ns
		GCLK PLL	t_{CO}	3.700	4.183	4.739	4.224	ns
	12 mA	GCLK	t_{CO}	5.799	6.509	7.226	6.586	ns
		GCLK PLL	t_{CO}	3.693	4.180	4.737	4.220	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.764	6.463	7.170	6.540	ns
		GCLK PLL	t_{CO}	3.658	4.134	4.681	4.174	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.989	7.975	9.038	8.021	ns
		GCLK PLL	t_{CO}	4.883	5.646	6.549	5.655	ns
	10 mA	GCLK	t_{CO}	6.912	7.865	8.879	7.910	ns
		GCLK PLL	t_{CO}	4.806	5.536	6.390	5.544	ns
	12 mA	GCLK	t_{CO}	6.914	7.867	8.883	7.913	ns
		GCLK PLL	t_{CO}	4.808	5.538	6.394	5.547	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.852	7.794	8.811	7.842	ns
		GCLK PLL	t_{CO}	4.746	5.465	6.322	5.476	ns
3.0-V PCI	—	GCLK	t_{CO}	5.048	6.054	6.651	6.137	ns
		GCLK PLL	t_{CO}	3.333	3.260	3.635	3.292	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.048	6.054	6.651	6.137	ns
		GCLK PLL	t_{CO}	3.333	3.260	3.635	3.292	ns

Table 1–79. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.444	6.023	6.576	6.110	ns
		GCLK PLL	t_{CO}	3.315	3.683	4.077	3.730	ns
	8 mA	GCLK	t_{CO}	4.997	5.560	6.095	5.636	ns
		GCLK PLL	t_{CO}	2.868	3.220	3.596	3.256	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.091	5.647	6.186	5.727	ns
		GCLK PLL	t_{CO}	2.962	3.307	3.687	3.347	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.196	5.746	6.276	5.825	ns
		GCLK PLL	t_{CO}	3.067	3.406	3.777	3.445	ns
	8 mA	GCLK	t_{CO}	4.940	5.491	6.016	5.563	ns
		GCLK PLL	t_{CO}	2.811	3.151	3.517	3.183	ns
	12 mA	GCLK	t_{CO}	4.824	5.365	5.889	5.432	ns
		GCLK PLL	t_{CO}	2.695	3.025	3.390	3.052	ns
	16 mA	GCLK	t_{CO}	4.775	5.310	5.822	5.376	ns
		GCLK PLL	t_{CO}	2.646	2.970	3.323	2.996	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.938	5.490	6.014	5.561	ns
		GCLK PLL	t_{CO}	2.809	3.150	3.515	3.181	ns
	8 mA	GCLK	t_{CO}	4.776	5.313	5.826	5.378	ns
		GCLK PLL	t_{CO}	2.647	2.973	3.327	2.998	ns
	12 mA	GCLK	t_{CO}	4.736	5.273	5.786	5.338	ns
		GCLK PLL	t_{CO}	2.607	2.933	3.287	2.958	ns
	16 mA	GCLK	t_{CO}	4.715	5.253	5.767	5.318	ns
		GCLK PLL	t_{CO}	2.586	2.913	3.268	2.938	ns
2.5 V	4 mA	GCLK	t_{CO}	5.322	5.886	6.434	5.973	ns
		GCLK PLL	t_{CO}	3.193	3.546	3.935	3.593	ns
	8 mA	GCLK	t_{CO}	5.053	5.616	6.157	5.691	ns
		GCLK PLL	t_{CO}	2.924	3.276	3.658	3.311	ns
	12 mA	GCLK	t_{CO}	4.938	5.496	6.034	5.568	ns
		GCLK PLL	t_{CO}	2.809	3.156	3.535	3.188	ns
	16 mA	GCLK	t_{CO}	4.885	5.440	5.975	5.511	ns
		GCLK PLL	t_{CO}	2.756	3.100	3.476	3.131	ns

Table 1–79. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
1.8 V	2 mA	GCLK	t_{CO}	6.474	7.176	7.891	7.297	ns
		GCLK PLL	t_{CO}	4.344	4.833	5.382	4.914	ns
	4 mA	GCLK	t_{CO}	5.918	6.606	7.299	6.702	ns
		GCLK PLL	t_{CO}	3.788	4.263	4.790	4.319	ns
	6 mA	GCLK	t_{CO}	5.656	6.312	6.967	6.401	ns
		GCLK PLL	t_{CO}	3.526	3.969	4.458	4.018	ns
	8 mA	GCLK	t_{CO}	5.540	6.183	6.822	6.267	ns
		GCLK PLL	t_{CO}	3.410	3.840	4.313	3.884	ns
	10 mA	GCLK	t_{CO}	5.479	6.129	6.775	6.212	ns
		GCLK PLL	t_{CO}	3.349	3.786	4.266	3.829	ns
	12 mA	GCLK	t_{CO}	5.418	6.053	6.686	6.134	ns
		GCLK PLL	t_{CO}	3.288	3.710	4.177	3.751	ns
	16 mA	GCLK	t_{CO}	5.374	6.004	6.630	6.083	ns
		GCLK PLL	t_{CO}	3.244	3.661	4.121	3.700	ns
1.5 V	2 mA	GCLK	t_{CO}	6.887	7.747	8.644	7.846	ns
		GCLK PLL	t_{CO}	4.757	5.404	6.135	5.463	ns
	4 mA	GCLK	t_{CO}	6.327	7.104	7.900	7.192	ns
		GCLK PLL	t_{CO}	4.197	4.761	5.391	4.809	ns
	6 mA	GCLK	t_{CO}	6.137	6.899	7.684	6.983	ns
		GCLK PLL	t_{CO}	4.007	4.556	5.175	4.600	ns
	8 mA	GCLK	t_{CO}	6.039	6.789	7.546	6.871	ns
		GCLK PLL	t_{CO}	3.909	4.446	5.037	4.488	ns
	10 mA	GCLK	t_{CO}	5.972	6.717	7.476	6.798	ns
		GCLK PLL	t_{CO}	3.842	4.374	4.967	4.415	ns
	12 mA	GCLK	t_{CO}	5.933	6.666	7.412	6.746	ns
		GCLK PLL	t_{CO}	3.803	4.323	4.903	4.363	ns
	16 mA	GCLK	t_{CO}	5.860	6.583	7.321	6.662	ns
		GCLK PLL	t_{CO}	3.730	4.240	4.812	4.279	ns
1.2 V	2 mA	GCLK	t_{CO}	7.976	9.126	10.393	9.181	ns
		GCLK PLL	t_{CO}	5.846	6.783	7.884	6.798	ns
	4 mA	GCLK	t_{CO}	7.484	8.558	9.732	8.609	ns
		GCLK PLL	t_{CO}	5.354	6.215	7.223	6.226	ns
	6 mA	GCLK	t_{CO}	7.330	8.375	9.517	8.426	ns
		GCLK PLL	t_{CO}	5.200	6.032	7.008	6.043	ns
	8 mA	GCLK	t_{CO}	7.242	8.277	9.404	8.327	ns
		GCLK PLL	t_{CO}	5.112	5.934	6.895	5.944	ns
	10 mA	GCLK	t_{CO}	7.119	8.128	9.218	8.179	ns
		GCLK PLL	t_{CO}	4.989	5.785	6.709	5.796	ns

Table 1–79. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.945	5.498	6.034	5.565	ns
		GCLK PLL	t_{CO}	2.823	3.163	3.534	3.191	ns
	12 mA	GCLK	t_{CO}	4.912	5.464	5.998	5.531	ns
		GCLK PLL	t_{CO}	2.790	3.129	3.498	3.157	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.862	5.410	5.941	5.476	ns
		GCLK PLL	t_{CO}	2.740	3.075	3.441	3.102	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.362	5.982	6.597	6.056	ns
		GCLK PLL	t_{CO}	3.230	3.637	4.087	3.672	ns
	10 mA	GCLK	t_{CO}	5.343	5.959	6.567	6.033	ns
		GCLK PLL	t_{CO}	3.211	3.614	4.057	3.649	ns
	12 mA	GCLK	t_{CO}	5.320	5.934	6.540	6.008	ns
		GCLK PLL	t_{CO}	3.188	3.589	4.030	3.624	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.313	5.927	6.533	5.999	ns
		GCLK PLL	t_{CO}	3.181	3.582	4.023	3.615	ns
	16 mA	GCLK	t_{CO}	5.297	5.912	6.519	5.985	ns
		GCLK PLL	t_{CO}	3.165	3.567	4.009	3.601	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.342	5.954	6.558	6.027	ns
		GCLK PLL	t_{CO}	3.210	3.609	4.048	3.643	ns
	10 mA	GCLK	t_{CO}	5.335	5.950	6.557	6.022	ns
		GCLK PLL	t_{CO}	3.203	3.605	4.047	3.638	ns
	12 mA	GCLK	t_{CO}	5.324	5.936	6.539	6.009	ns
		GCLK PLL	t_{CO}	3.192	3.591	4.029	3.625	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.291	5.898	6.497	5.970	ns
		GCLK PLL	t_{CO}	3.159	3.553	3.987	3.586	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.847	6.553	7.266	6.626	ns
		GCLK PLL	t_{CO}	3.715	4.208	4.756	4.242	ns
	10 mA	GCLK	t_{CO}	5.845	6.549	7.258	6.623	ns
		GCLK PLL	t_{CO}	3.713	4.204	4.748	4.239	ns
	12 mA	GCLK	t_{CO}	5.835	6.542	7.254	6.615	ns
		GCLK PLL	t_{CO}	3.703	4.197	4.744	4.231	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.797	6.496	7.200	6.568	ns
		GCLK PLL	t_{CO}	3.665	4.151	4.690	4.184	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.040	8.021	9.081	8.066	ns
		GCLK PLL	t_{CO}	4.908	5.676	6.571	5.682	ns
	10 mA	GCLK	t_{CO}	6.955	7.905	8.920	7.950	ns
		GCLK PLL	t_{CO}	4.823	5.560	6.410	5.566	ns
3.0-V PCI	—	GCLK	t_{CO}	5.033	5.577	6.098	5.646	ns
		GCLK PLL	t_{CO}	2.904	3.237	3.599	3.266	ns

Table 1–79. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.0-V PCI-X	—	GCLK	t_{CO}	5.033	5.577	6.098	5.646	ns
		GCLK PLL	t_{CO}	2.904	3.237	3.599	3.266	ns

Table 1–80. EP3C55 Column Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
LVDS	—	GCLK	t_{SU}	–1.413	–1.586	–1.752	–1.621	ns
	—		t_{H}	1.680	1.894	2.096	1.928	ns
	—	GCLK PLL	t_{SU}	1.145	1.242	1.289	1.251	ns
	—		t_{H}	–0.448	–0.447	–0.410	–0.451	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.864	5.421	5.967	5.491	ns
	—	GCLK PLL	t_{CO}	2.735	3.080	3.459	3.112	ns
BLVDS	—	GCLK	t_{SU}	–1.370	–1.538	–1.698	–1.570	ns
	—		t_{H}	1.636	1.845	2.040	1.876	ns
	—	GCLK PLL	t_{SU}	1.176	1.278	1.333	1.291	ns
	—		t_{H}	–0.601	–0.618	–0.602	–0.630	ns
	8 mA	GCLK	t_{CO}	5.171	5.732	6.273	5.803	ns
		GCLK PLL	t_{CO}	2.921	3.255	3.618	3.283	ns
	12 mA	GCLK	t_{CO}	5.171	5.732	6.273	5.803	ns
		GCLK PLL	t_{CO}	2.921	3.255	3.618	3.283	ns
	16 mA	GCLK	t_{CO}	5.171	5.732	6.273	5.803	ns
		GCLK PLL	t_{CO}	2.921	3.255	3.618	3.283	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.864	5.421	5.967	5.491	ns
	—	GCLK PLL	t_{CO}	2.735	3.080	3.459	3.112	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.864	5.421	5.967	5.491	ns
	—	GCLK PLL	t_{CO}	2.735	3.080	3.459	3.112	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.789	5.322	5.841	5.387	ns
	—	GCLK PLL	t_{CO}	2.660	2.981	3.333	3.008	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.864	5.421	5.967	5.491	ns
	—	GCLK PLL	t_{CO}	2.735	3.080	3.459	3.112	ns

Table 1–81. EP3C55 Row Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
LVDS	—	GCLK	t_{SU}	–1.390	–1.558	–1.718	–1.590	ns
	—		t_{H}	1.656	1.865	2.060	1.896	ns
	—		t_{CO}	4.108	4.605	5.042	4.567	ns
	—	GCLK PLL	t_{SU}	1.169	1.271	1.324	1.283	ns
	—		t_{H}	–0.474	–0.477	–0.447	–0.484	ns
	—		t_{CO}	1.985	2.268	2.542	2.193	ns
BLVDS	—	GCLK	t_{SU}	–1.382	–1.550	–1.708	–1.581	ns
	—		t_{H}	1.647	1.857	2.050	1.886	ns
	—	GCLK PLL	t_{SU}	1.188	1.290	1.343	1.302	ns
	—		t_{H}	–0.612	–0.630	–0.612	–0.640	ns
	8 mA	GCLK	t_{CO}	5.169	5.730	6.270	5.799	ns
		GCLK PLL	t_{CO}	2.923	3.257	3.621	3.287	ns
	12 mA	GCLK	t_{CO}	5.169	5.730	6.270	5.799	ns
		GCLK PLL	t_{CO}	2.923	3.257	3.621	3.287	ns
	16 mA	GCLK	t_{CO}	5.169	5.730	6.270	5.799	ns
		GCLK PLL	t_{CO}	2.923	3.257	3.621	3.287	ns
mini-LVDS	—	GCLK	t_{CO}	4.108	4.605	5.042	4.567	ns
	—	GCLK PLL	t_{CO}	1.985	2.268	2.542	2.193	ns
PPDS	—	GCLK	t_{CO}	4.108	4.605	5.042	4.567	ns
	—	GCLK PLL	t_{CO}	1.985	2.268	2.542	2.193	ns
RSDS	—	GCLK	t_{CO}	4.108	4.605	5.042	4.567	ns
	—	GCLK PLL	t_{CO}	1.985	2.268	2.542	2.193	ns

EP3C80 I/O Timing Parameters

Table 1–82 through Table 1–87 show the maximum I/O timing parameters for EP3C80 devices.

Table 1–82. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.567	–1.744	–1.910	–1.765	ns
		t_{H}	1.813	2.028	2.226	2.048	ns
	GCLK PLL	t_{SU}	1.139	1.258	1.331	1.288	ns
		t_{H}	–0.435	–0.456	–0.448	–0.482	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.567	–1.744	–1.910	–1.765	ns
		t_{H}	1.813	2.028	2.226	2.048	ns
	GCLK PLL	t_{SU}	1.139	1.258	1.331	1.288	ns
		t_{H}	–0.435	–0.456	–0.448	–0.482	ns

Table 1–82. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.0-V LVTTL	GCLK	t_{SU}	–1.559	–1.741	–1.913	–1.763	ns
		t_H	1.805	2.025	2.229	2.046	ns
	GCLK PLL	t_{SU}	1.147	1.261	1.328	1.290	ns
		t_H	–0.443	–0.459	–0.445	–0.484	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.559	–1.741	–1.913	–1.763	ns
		t_H	1.805	2.025	2.229	2.046	ns
	GCLK PLL	t_{SU}	1.147	1.261	1.328	1.290	ns
		t_H	–0.443	–0.459	–0.445	–0.484	ns
2.5 V	GCLK	t_{SU}	–1.528	–1.714	–1.888	–1.737	ns
		t_H	1.774	1.998	2.204	2.020	ns
	GCLK PLL	t_{SU}	1.178	1.288	1.353	1.316	ns
		t_H	–0.474	–0.486	–0.470	–0.510	ns
1.8 V	GCLK	t_{SU}	–1.425	–1.647	–1.851	–1.667	ns
		t_H	1.671	1.931	2.167	1.950	ns
	GCLK PLL	t_{SU}	1.281	1.355	1.390	1.386	ns
		t_H	–0.577	–0.553	–0.507	–0.580	ns
1.5 V	GCLK	t_{SU}	–1.361	–1.560	–1.739	–1.583	ns
		t_H	1.607	1.844	2.055	1.866	ns
	GCLK PLL	t_{SU}	1.345	1.442	1.502	1.470	ns
		t_H	–0.641	–0.640	–0.619	–0.664	ns
1.2 V	GCLK	t_{SU}	–1.228	–1.382	–1.535	–1.410	ns
		t_H	1.474	1.666	1.851	1.693	ns
	GCLK PLL	t_{SU}	1.478	1.620	1.706	1.643	ns
		t_H	–0.774	–0.818	–0.823	–0.837	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.454	–1.676	–1.897	–1.694	ns
		t_H	1.699	1.960	2.214	1.978	ns
	GCLK PLL	t_{SU}	1.277	1.352	1.347	1.381	ns
		t_H	–0.572	–0.549	–0.463	–0.575	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.454	–1.676	–1.897	–1.694	ns
		t_H	1.699	1.960	2.214	1.978	ns
	GCLK PLL	t_{SU}	1.277	1.352	1.347	1.381	ns
		t_H	–0.572	–0.549	–0.463	–0.575	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.284	–1.455	–1.614	–1.478	ns
		t_H	1.529	1.739	1.931	1.762	ns
	GCLK PLL	t_{SU}	1.447	1.573	1.630	1.597	ns
		t_H	–0.742	–0.770	–0.746	–0.791	ns

Table 1–82. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
SSTL-18 Class II	GCLK	t_{SU}	–1.284	–1.455	–1.614	–1.478	ns
		t_H	1.529	1.739	1.931	1.762	ns
	GCLK PLL	t_{SU}	1.447	1.573	1.630	1.597	ns
		t_H	–0.742	–0.770	–0.746	–0.791	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.284	–1.455	–1.614	–1.478	ns
		t_H	1.529	1.739	1.931	1.762	ns
	GCLK PLL	t_{SU}	1.447	1.573	1.630	1.597	ns
		t_H	–0.742	–0.770	–0.746	–0.791	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.284	–1.455	–1.614	–1.478	ns
		t_H	1.529	1.739	1.931	1.762	ns
	GCLK PLL	t_{SU}	1.447	1.573	1.630	1.597	ns
		t_H	–0.742	–0.770	–0.746	–0.791	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.375	–1.563	–1.742	–1.586	ns
		t_H	1.620	1.847	2.059	1.870	ns
	GCLK PLL	t_{SU}	1.356	1.465	1.502	1.489	ns
		t_H	–0.651	–0.662	–0.618	–0.683	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.375	–1.563	–1.742	–1.586	ns
		t_H	1.620	1.847	2.059	1.870	ns
	GCLK PLL	t_{SU}	1.356	1.465	1.502	1.489	ns
		t_H	–0.651	–0.662	–0.618	–0.683	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.187	–1.318	–1.460	–1.351	ns
		t_H	1.432	1.602	1.777	1.635	ns
	GCLK PLL	t_{SU}	1.544	1.710	1.784	1.724	ns
		t_H	–0.839	–0.907	–0.900	–0.918	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–1.187	–1.318	–1.460	–1.351	ns
		t_H	1.432	1.602	1.777	1.635	ns
	GCLK PLL	t_{SU}	1.544	1.710	1.784	1.724	ns
		t_H	–0.839	–0.907	–0.900	–0.918	ns
3.0-V PCI	GCLK	t_{SU}	–1.559	–1.741	–1.913	–1.763	ns
		t_H	1.805	2.025	2.229	2.046	ns
	GCLK PLL	t_{SU}	1.147	1.261	1.328	1.290	ns
		t_H	–0.443	–0.459	–0.445	–0.484	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.559	–1.741	–1.913	–1.763	ns
		t_H	1.805	2.025	2.229	2.046	ns
	GCLK PLL	t_{SU}	1.147	1.261	1.328	1.290	ns
		t_H	–0.443	–0.459	–0.445	–0.484	ns

Table 1–83. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.523	–1.677	–1.823	–1.698	ns
		t_{H}	1.767	1.959	2.138	1.980	ns
	GCLK PLL	t_{SU}	1.195	1.314	1.391	1.339	ns
		t_{H}	–0.492	–0.512	–0.509	–0.534	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.523	–1.677	–1.823	–1.698	ns
		t_{H}	1.767	1.959	2.138	1.980	ns
	GCLK PLL	t_{SU}	1.195	1.314	1.391	1.339	ns
		t_{H}	–0.492	–0.512	–0.509	–0.534	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.518	–1.673	–1.825	–1.695	ns
		t_{H}	1.762	1.955	2.140	1.977	ns
	GCLK PLL	t_{SU}	1.200	1.318	1.389	1.342	ns
		t_{H}	–0.497	–0.516	–0.507	–0.537	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.518	–1.673	–1.825	–1.695	ns
		t_{H}	1.762	1.955	2.140	1.977	ns
	GCLK PLL	t_{SU}	1.200	1.318	1.389	1.342	ns
		t_{H}	–0.497	–0.516	–0.507	–0.537	ns
2.5 V	GCLK	t_{SU}	–1.485	–1.646	–1.805	–1.668	ns
		t_{H}	1.729	1.928	2.120	1.950	ns
	GCLK PLL	t_{SU}	1.233	1.345	1.409	1.369	ns
		t_{H}	–0.530	–0.543	–0.527	–0.564	ns
1.8 V	GCLK	t_{SU}	–1.383	–1.579	–1.768	–1.599	ns
		t_{H}	1.627	1.861	2.083	1.881	ns
	GCLK PLL	t_{SU}	1.335	1.412	1.446	1.438	ns
		t_{H}	–0.632	–0.610	–0.564	–0.633	ns
1.5 V	GCLK	t_{SU}	–1.318	–1.492	–1.657	–1.515	ns
		t_{H}	1.562	1.774	1.972	1.797	ns
	GCLK PLL	t_{SU}	1.400	1.499	1.557	1.522	ns
		t_{H}	–0.697	–0.697	–0.675	–0.717	ns
1.2 V	GCLK	t_{SU}	–1.181	–1.313	–1.452	–1.341	ns
		t_{H}	1.425	1.595	1.767	1.623	ns
	GCLK PLL	t_{SU}	1.537	1.678	1.762	1.696	ns
		t_{H}	–0.834	–0.876	–0.880	–0.891	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.405	–1.638	–1.814	–1.656	ns
		t_{H}	1.649	1.921	2.129	1.938	ns
	GCLK PLL	t_{SU}	1.307	1.383	1.419	1.415	ns
		t_{H}	–0.604	–0.582	–0.538	–0.610	ns

Table 1–83. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
SSTL-2 Class II	GCLK	t_{SU}	–1.405	–1.638	–1.814	–1.656	ns
		t_H	1.649	1.921	2.129	1.938	ns
	GCLK PLL	t_{SU}	1.307	1.383	1.419	1.415	ns
		t_H	–0.604	–0.582	–0.538	–0.610	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.228	–1.417	–1.532	–1.442	ns
		t_H	1.472	1.700	1.847	1.724	ns
	GCLK PLL	t_{SU}	1.484	1.604	1.701	1.629	ns
		t_H	–0.781	–0.803	–0.820	–0.824	ns
SSTL-18 Class II	GCLK	t_{SU}	–1.228	–1.417	–1.532	–1.442	ns
		t_H	1.472	1.700	1.847	1.724	ns
	GCLK PLL	t_{SU}	1.484	1.604	1.701	1.629	ns
		t_H	–0.781	–0.803	–0.820	–0.824	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.228	–1.417	–1.532	–1.442	ns
		t_H	1.472	1.700	1.847	1.724	ns
	GCLK PLL	t_{SU}	1.484	1.604	1.701	1.629	ns
		t_H	–0.781	–0.803	–0.820	–0.824	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.228	–1.417	–1.532	–1.442	ns
		t_H	1.472	1.700	1.847	1.724	ns
	GCLK PLL	t_{SU}	1.484	1.604	1.701	1.629	ns
		t_H	–0.781	–0.803	–0.820	–0.824	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.326	–1.523	–1.651	–1.549	ns
		t_H	1.570	1.806	1.966	1.831	ns
	GCLK PLL	t_{SU}	1.386	1.498	1.582	1.522	ns
		t_H	–0.683	–0.697	–0.701	–0.717	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.326	–1.523	–1.651	–1.549	ns
		t_H	1.570	1.806	1.966	1.831	ns
	GCLK PLL	t_{SU}	1.386	1.498	1.582	1.522	ns
		t_H	–0.683	–0.697	–0.701	–0.717	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.127	–1.279	–1.380	–1.314	ns
		t_H	1.371	1.562	1.695	1.596	ns
	GCLK PLL	t_{SU}	1.585	1.742	1.853	1.757	ns
		t_H	–0.882	–0.941	–0.972	–0.952	ns
3.0-V PCI	GCLK	t_{SU}	–1.518	–1.673	–1.825	–1.695	ns
		t_H	1.762	1.955	2.140	1.977	ns
	GCLK PLL	t_{SU}	1.200	1.318	1.389	1.342	ns
		t_H	–0.497	–0.516	–0.507	–0.537	ns

Table 1–83. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C6	C7	C8	I7	Unit
3.0-V PCI-X	GCLK	t_{SU}	–1.518	–1.673	–1.825	–1.695	ns
		t_{H}	1.762	1.955	2.140	1.977	ns
	GCLK PLL	t_{SU}	1.200	1.318	1.389	1.342	ns
		t_{H}	–0.497	–0.516	–0.507	–0.537	ns

Table 1–84. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.360	5.942	11.069	6.023	ns
		GCLK PLL	t_{CO}	3.120	7.773	3.885	7.913	ns
	8 mA	GCLK	t_{CO}	5.044	5.609	8.336	5.679	ns
		GCLK PLL	t_{CO}	2.804	5.180	3.537	5.250	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.109	5.682	9.113	5.758	ns
		GCLK PLL	t_{CO}	2.869	5.978	3.612	6.086	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.171	5.747	9.597	5.826	ns
		GCLK PLL	t_{CO}	2.931	6.435	3.686	6.561	ns
	8 mA	GCLK	t_{CO}	4.980	5.548	7.945	5.620	ns
		GCLK PLL	t_{CO}	2.740	4.809	3.477	4.892	ns
	12 mA	GCLK	t_{CO}	4.923	5.480	7.243	5.546	ns
		GCLK PLL	t_{CO}	2.683	4.156	3.398	4.210	ns
	16 mA	GCLK	t_{CO}	4.894	5.447	6.821	5.513	ns
		GCLK PLL	t_{CO}	2.654	3.752	3.360	3.795	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.987	5.555	7.942	5.627	ns
		GCLK PLL	t_{CO}	2.747	4.806	3.484	4.888	ns
	8 mA	GCLK	t_{CO}	4.893	5.448	6.867	5.514	ns
		GCLK PLL	t_{CO}	2.653	3.788	3.364	3.836	ns
	12 mA	GCLK	t_{CO}	4.861	5.416	6.505	5.482	ns
		GCLK PLL	t_{CO}	2.621	3.456	3.331	3.487	ns
	16 mA	GCLK	t_{CO}	4.847	5.403	6.329	5.469	ns
		GCLK PLL	t_{CO}	2.607	3.277	3.319	3.309	ns
2.5 V	4 mA	GCLK	t_{CO}	5.274	5.853	9.916	5.942	ns
		GCLK PLL	t_{CO}	3.034	6.672	3.804	6.837	ns
	8 mA	GCLK	t_{CO}	5.093	5.673	8.137	5.750	ns
		GCLK PLL	t_{CO}	2.853	4.977	3.619	5.062	ns
	12 mA	GCLK	t_{CO}	5.021	5.590	7.414	5.662	ns
		GCLK PLL	t_{CO}	2.781	4.300	3.524	4.356	ns
	16 mA	GCLK	t_{CO}	4.991	5.561	7.080	5.631	ns
		GCLK PLL	t_{CO}	2.751	3.973	3.495	4.026	ns

Table 1–84. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
1.8 V	2 mA	GCLK	t_{CO}	6.228	6.938	15.206	7.035	ns
		GCLK PLL	t_{CO}	3.988	11.419	5.025	11.704	ns
	4 mA	GCLK	t_{CO}	5.857	6.545	11.257	6.636	ns
		GCLK PLL	t_{CO}	3.617	7.748	4.612	7.879	ns
	6 mA	GCLK	t_{CO}	5.664	6.329	9.662	6.412	ns
		GCLK PLL	t_{CO}	3.424	6.297	4.372	6.402	ns
	8 mA	GCLK	t_{CO}	5.603	6.258	8.876	6.338	ns
		GCLK PLL	t_{CO}	3.363	5.579	4.286	5.659	ns
	10 mA	GCLK	t_{CO}	5.544	6.196	8.488	6.276	ns
		GCLK PLL	t_{CO}	3.304	5.206	4.226	5.274	ns
	12 mA	GCLK	t_{CO}	5.497	6.146	8.113	6.222	ns
		GCLK PLL	t_{CO}	3.257	4.875	4.162	4.937	ns
	16 mA	GCLK	t_{CO}	5.455	6.104	7.742	6.181	ns
		GCLK PLL	t_{CO}	3.215	4.528	4.124	4.584	ns
1.5 V	2 mA	GCLK	t_{CO}	6.715	7.553	14.997	7.647	ns
		GCLK PLL	t_{CO}	4.475	10.963	5.810	11.118	ns
	4 mA	GCLK	t_{CO}	6.309	7.081	11.156	7.172	ns
		GCLK PLL	t_{CO}	4.069	7.538	5.262	7.631	ns
	6 mA	GCLK	t_{CO}	6.168	6.938	9.915	7.024	ns
		GCLK PLL	t_{CO}	3.928	6.410	5.105	6.488	ns
	8 mA	GCLK	t_{CO}	6.082	6.824	9.236	6.912	ns
		GCLK PLL	t_{CO}	3.842	5.813	4.971	5.880	ns
	10 mA	GCLK	t_{CO}	6.044	6.786	8.856	6.864	ns
		GCLK PLL	t_{CO}	3.804	5.470	4.922	5.530	ns
	12 mA	GCLK	t_{CO}	6.011	6.751	8.601	6.830	ns
		GCLK PLL	t_{CO}	3.771	5.244	4.880	5.300	ns
	16 mA	GCLK	t_{CO}	5.903	6.633	8.156	6.710	ns
		GCLK PLL	t_{CO}	3.663	4.857	4.747	4.908	ns

Table 1–84. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
1.2 V	2 mA	GCLK	t_{CO}	7.846	8.971	16.069	9.025	ns
		GCLK PLL	t_{CO}	5.606	11.532	7.585	11.577	ns
	4 mA	GCLK	t_{CO}	7.488	8.557	12.549	8.608	ns
		GCLK PLL	t_{CO}	5.248	8.503	7.103	8.527	ns
	6 mA	GCLK	t_{CO}	7.352	8.394	11.441	8.446	ns
		GCLK PLL	t_{CO}	5.112	7.554	6.906	7.574	ns
	8 mA	GCLK	t_{CO}	7.292	8.326	10.898	8.377	ns
		GCLK PLL	t_{CO}	5.052	7.085	6.830	7.100	ns
	10 mA	GCLK	t_{CO}	7.161	8.157	10.404	8.205	ns
		GCLK PLL	t_{CO}	4.921	6.679	6.607	6.690	ns
	12 mA	GCLK	t_{CO}	7.144	8.140	10.203	8.187	ns
		GCLK PLL	t_{CO}	4.904	6.503	6.592	6.513	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.036	5.611	6.159	5.678	ns
		GCLK PLL	t_{CO}	2.786	3.132	3.507	3.154	ns
	12 mA	GCLK	t_{CO}	5.016	5.589	6.136	5.656	ns
		GCLK PLL	t_{CO}	2.766	3.110	3.484	3.132	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.981	5.550	6.093	5.616	ns
		GCLK PLL	t_{CO}	2.731	3.071	3.441	3.092	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.453	6.095	6.720	6.168	ns
		GCLK PLL	t_{CO}	3.203	3.616	4.068	3.644	ns
	10 mA	GCLK	t_{CO}	5.429	6.064	6.681	6.138	ns
		GCLK PLL	t_{CO}	3.179	3.585	4.029	3.614	ns
	12 mA	GCLK	t_{CO}	5.426	6.063	6.677	6.136	ns
		GCLK PLL	t_{CO}	3.176	3.584	4.025	3.612	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.411	6.045	6.662	6.118	ns
		GCLK PLL	t_{CO}	3.161	3.566	4.010	3.594	ns
	16 mA	GCLK	t_{CO}	5.398	6.033	6.648	6.105	ns
		GCLK PLL	t_{CO}	3.148	3.554	3.996	3.581	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.437	6.071	6.687	6.144	ns
		GCLK PLL	t_{CO}	3.187	3.592	4.035	3.620	ns
	10 mA	GCLK	t_{CO}	5.430	6.067	6.685	6.139	ns
		GCLK PLL	t_{CO}	3.180	3.588	4.033	3.615	ns
	12 mA	GCLK	t_{CO}	5.416	6.048	6.662	6.121	ns
		GCLK PLL	t_{CO}	3.166	3.569	4.010	3.597	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.397	6.026	6.636	6.098	ns
		GCLK PLL	t_{CO}	3.147	3.547	3.984	3.574	ns

Table 1–84. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.935	6.658	7.384	6.734	ns
		GCLK PLL	t_{CO}	3.685	4.179	4.732	4.210	ns
	10 mA	GCLK	t_{CO}	5.931	6.648	7.369	6.726	ns
		GCLK PLL	t_{CO}	3.681	4.169	4.717	4.202	ns
	12 mA	GCLK	t_{CO}	5.924	6.645	7.367	6.722	ns
		GCLK PLL	t_{CO}	3.674	4.166	4.715	4.198	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.889	6.599	7.311	6.676	ns
		GCLK PLL	t_{CO}	3.639	4.120	4.659	4.152	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.114	8.111	9.179	8.157	ns
		GCLK PLL	t_{CO}	4.864	5.632	6.527	5.633	ns
	10 mA	GCLK	t_{CO}	7.037	8.001	9.020	8.046	ns
		GCLK PLL	t_{CO}	4.787	5.522	6.368	5.522	ns
	12 mA	GCLK	t_{CO}	7.039	8.003	9.024	8.049	ns
		GCLK PLL	t_{CO}	4.789	5.524	6.372	5.525	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.977	7.930	8.952	7.978	ns
		GCLK PLL	t_{CO}	4.727	5.451	6.300	5.454	ns
3.0-V PCI	—	GCLK	t_{CO}	5.156	5.718	6.780	5.788	ns
		GCLK PLL	t_{CO}	2.916	3.688	3.641	3.728	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.156	5.718	6.780	5.788	ns
		GCLK PLL	t_{CO}	2.916	3.688	3.641	3.728	ns

Table 1–85. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.576	6.166	6.735	6.255	ns
		GCLK PLL	t_{CO}	7.121	7.708	8.338	7.852	ns
	8 mA	GCLK	t_{CO}	5.129	5.703	6.254	5.781	ns
		GCLK PLL	t_{CO}	4.711	5.125	5.611	5.191	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.223	5.790	6.345	5.872	ns
		GCLK PLL	t_{CO}	5.494	5.942	6.397	6.044	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.328	5.889	6.435	5.970	ns
		GCLK PLL	t_{CO}	5.925	6.387	6.885	6.523	ns
	8 mA	GCLK	t_{CO}	5.072	5.634	6.175	5.708	ns
		GCLK PLL	t_{CO}	4.369	4.774	5.239	4.854	ns
	12 mA	GCLK	t_{CO}	4.956	5.508	6.048	5.577	ns
		GCLK PLL	t_{CO}	3.721	4.123	4.543	4.179	ns
	16 mA	GCLK	t_{CO}	4.907	5.453	5.981	5.521	ns
		GCLK PLL	t_{CO}	3.367	3.723	4.121	3.767	ns

Table 1–85. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.070	5.633	6.173	5.706	ns
		GCLK PLL	t_{CO}	4.368	4.772	5.237	4.851	ns
	8 mA	GCLK	t_{CO}	4.908	5.456	5.985	5.523	ns
		GCLK PLL	t_{CO}	3.396	3.757	4.165	3.805	ns
	12 mA	GCLK	t_{CO}	4.868	5.416	5.945	5.483	ns
		GCLK PLL	t_{CO}	3.087	3.435	3.816	3.468	ns
	16 mA	GCLK	t_{CO}	4.847	5.396	5.926	5.463	ns
		GCLK PLL	t_{CO}	2.911	3.255	3.636	3.287	ns
2.5 V	4 mA	GCLK	t_{CO}	5.454	6.029	6.593	6.118	ns
		GCLK PLL	t_{CO}	6.104	6.632	7.209	6.794	ns
	8 mA	GCLK	t_{CO}	5.185	5.759	6.316	5.836	ns
		GCLK PLL	t_{CO}	4.498	4.943	5.437	5.029	ns
	12 mA	GCLK	t_{CO}	5.070	5.639	6.193	5.713	ns
		GCLK PLL	t_{CO}	3.849	4.268	4.715	4.328	ns
	16 mA	GCLK	t_{CO}	5.017	5.583	6.134	5.656	ns
		GCLK PLL	t_{CO}	3.543	3.941	4.381	3.996	ns
1.8 V	2 mA	GCLK	t_{CO}	6.595	7.306	8.030	7.429	ns
		GCLK PLL	t_{CO}	10.349	11.353	12.468	11.636	ns
	4 mA	GCLK	t_{CO}	6.039	6.736	7.438	6.834	ns
		GCLK PLL	t_{CO}	6.958	7.705	8.542	7.834	ns
	6 mA	GCLK	t_{CO}	5.777	6.442	7.106	6.533	ns
		GCLK PLL	t_{CO}	5.636	6.261	6.958	6.367	ns
	8 mA	GCLK	t_{CO}	5.661	6.313	6.961	6.399	ns
		GCLK PLL	t_{CO}	4.976	5.542	6.170	5.625	ns
	10 mA	GCLK	t_{CO}	5.600	6.259	6.914	6.344	ns
		GCLK PLL	t_{CO}	4.627	5.173	5.785	5.242	ns
	12 mA	GCLK	t_{CO}	5.539	6.183	6.825	6.266	ns
		GCLK PLL	t_{CO}	4.324	4.845	5.414	4.908	ns
	16 mA	GCLK	t_{CO}	5.495	6.134	6.769	6.215	ns
		GCLK PLL	t_{CO}	4.018	4.509	5.058	4.568	ns

Table 1–85. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
1.5 V	2 mA	GCLK	t_{CO}	7.008	7.877	8.783	7.978	ns
		GCLK PLL	t_{CO}	9.715	10.905	12.264	11.057	ns
	4 mA	GCLK	t_{CO}	6.448	7.234	8.039	7.324	ns
		GCLK PLL	t_{CO}	6.656	7.498	8.441	7.590	ns
	6 mA	GCLK	t_{CO}	6.258	7.029	7.823	7.115	ns
		GCLK PLL	t_{CO}	5.641	6.376	7.207	6.452	ns
	8 mA	GCLK	t_{CO}	6.160	6.919	7.685	7.003	ns
		GCLK PLL	t_{CO}	5.133	5.805	6.558	5.868	ns
	10 mA	GCLK	t_{CO}	6.093	6.847	7.615	6.930	ns
		GCLK PLL	t_{CO}	4.815	5.460	6.175	5.517	ns
	12 mA	GCLK	t_{CO}	6.054	6.796	7.551	6.878	ns
		GCLK PLL	t_{CO}	4.612	5.231	5.917	5.284	ns
	16 mA	GCLK	t_{CO}	5.981	6.713	7.460	6.794	ns
		GCLK PLL	t_{CO}	4.270	4.843	5.469	4.891	ns
1.2 V	2 mA	GCLK	t_{CO}	8.097	9.256	10.532	9.313	ns
		GCLK PLL	t_{CO}	9.924	11.483	13.348	11.530	ns
	4 mA	GCLK	t_{CO}	7.605	8.688	9.871	8.741	ns
		GCLK PLL	t_{CO}	7.307	8.467	9.842	8.492	ns
	6 mA	GCLK	t_{CO}	7.451	8.505	9.656	8.558	ns
		GCLK PLL	t_{CO}	6.513	7.548	8.772	7.568	ns
	8 mA	GCLK	t_{CO}	7.363	8.407	9.543	8.459	ns
		GCLK PLL	t_{CO}	6.100	7.074	8.223	7.091	ns
	10 mA	GCLK	t_{CO}	7.240	8.258	9.357	8.311	ns
		GCLK PLL	t_{CO}	5.759	6.663	7.721	6.676	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.084	5.646	6.192	5.716	ns
		GCLK PLL	t_{CO}	2.799	3.139	3.519	3.166	ns
	12 mA	GCLK	t_{CO}	5.051	5.612	6.156	5.682	ns
		GCLK PLL	t_{CO}	2.766	3.105	3.483	3.132	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.001	5.558	6.099	5.627	ns
		GCLK PLL	t_{CO}	2.716	3.051	3.426	3.077	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.481	6.110	6.735	6.187	ns
		GCLK PLL	t_{CO}	3.206	3.613	4.072	3.647	ns
	10 mA	GCLK	t_{CO}	5.462	6.087	6.705	6.164	ns
		GCLK PLL	t_{CO}	3.187	3.590	4.042	3.624	ns
	12 mA	GCLK	t_{CO}	5.439	6.062	6.678	6.139	ns
		GCLK PLL	t_{CO}	3.164	3.565	4.015	3.599	ns

Table 1–85. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.432	6.055	6.671	6.130	ns
		GCLK PLL	t_{CO}	3.157	3.558	4.008	3.590	ns
	16 mA	GCLK	t_{CO}	5.416	6.040	6.657	6.116	ns
		GCLK PLL	t_{CO}	3.141	3.543	3.994	3.576	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.461	6.082	6.696	6.158	ns
		GCLK PLL	t_{CO}	3.186	3.585	4.033	3.618	ns
	10 mA	GCLK	t_{CO}	5.454	6.078	6.695	6.153	ns
		GCLK PLL	t_{CO}	3.179	3.581	4.032	3.613	ns
	12 mA	GCLK	t_{CO}	5.443	6.064	6.677	6.140	ns
		GCLK PLL	t_{CO}	3.168	3.567	4.014	3.600	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.410	6.026	6.635	6.101	ns
		GCLK PLL	t_{CO}	3.135	3.529	3.972	3.561	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.966	6.681	7.404	6.757	ns
		GCLK PLL	t_{CO}	3.691	4.184	4.741	4.217	ns
	10 mA	GCLK	t_{CO}	5.964	6.677	7.396	6.754	ns
		GCLK PLL	t_{CO}	3.689	4.180	4.733	4.214	ns
	12 mA	GCLK	t_{CO}	5.954	6.670	7.392	6.746	ns
		GCLK PLL	t_{CO}	3.679	4.173	4.729	4.206	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.916	6.624	7.338	6.699	ns
		GCLK PLL	t_{CO}	3.641	4.127	4.675	4.159	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.159	8.149	9.219	8.197	ns
		GCLK PLL	t_{CO}	4.884	5.652	6.556	5.657	ns
	10 mA	GCLK	t_{CO}	7.074	8.033	9.058	8.081	ns
		GCLK PLL	t_{CO}	4.799	5.536	6.395	5.541	ns
3.0-V PCI	—	GCLK	t_{CO}	5.165	5.720	6.257	5.791	ns
		GCLK PLL	t_{CO}	3.273	3.646	4.066	3.687	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.165	5.720	6.257	5.791	ns
		GCLK PLL	t_{CO}	3.273	3.646	4.066	3.687	ns

Table 1–86. EP3C80 Column Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
LVDS	—	GCLK	t_{SU}	–1.531	–1.713	–1.889	–1.748	ns
	—		t_{H}	1.801	2.026	2.238	2.060	ns
	—	GCLK PLL	t_{SU}	1.200	1.299	1.349	1.312	ns
	—		t_{H}	–0.470	–0.467	–0.433	–0.477	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.007	5.575	6.127	5.645	ns
	—	GCLK PLL	t_{CO}	2.720	3.066	3.443	3.092	ns

Table 1–86. EP3C80 Column Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
BLVDS	—	GCLK	t_{SU}	–1.483	–1.660	–1.828	–1.694	ns
	—		t_{H}	1.752	1.971	2.175	2.005	ns
	—	GCLK PLL	t_{SU}	1.230	1.336	1.389	1.351	ns
	—		t_{H}	–0.625	–0.643	–0.626	–0.658	ns
	8 mA	GCLK	t_{CO}	5.310	5.880	6.432	5.952	ns
		GCLK PLL	t_{CO}	2.912	3.246	3.608	3.272	ns
	12 mA	GCLK	t_{CO}	5.310	5.880	6.432	5.952	ns
		GCLK PLL	t_{CO}	2.912	3.246	3.608	3.272	ns
	16 mA	GCLK	t_{CO}	5.310	5.880	6.432	5.952	ns
		GCLK PLL	t_{CO}	2.912	3.246	3.608	3.272	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.007	5.575	6.127	5.645	ns
	—	GCLK PLL	t_{CO}	2.720	3.066	3.443	3.092	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.007	5.575	6.127	5.645	ns
	—	GCLK PLL	t_{CO}	2.720	3.066	3.443	3.092	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.932	5.476	6.001	5.541	ns
	—	GCLK PLL	t_{CO}	2.645	2.967	3.317	2.988	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.007	5.575	6.127	5.645	ns
	—	GCLK PLL	t_{CO}	2.720	3.066	3.443	3.092	ns

Table 1–87. EP3C80 Row Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
LVDS	—	GCLK	t_{SU}	–1.492	–1.670	–1.838	–1.704	ns
	—		t_{H}	1.761	1.981	2.185	2.014	ns
	—		t_{CO}	4.247	4.753	5.200	4.718	ns
	—	GCLK PLL	t_{SU}	1.237	1.341	1.395	1.354	ns
	—		t_{H}	–0.509	–0.510	–0.481	–0.521	ns
	—		t_{CO}	1.978	2.262	2.536	2.182	ns
BLVDS	—	GCLK	t_{SU}	–1.496	–1.672	–1.842	–1.705	ns
	—		t_{H}	1.765	1.983	2.188	2.015	ns
	—	GCLK PLL	t_{SU}	1.243	1.348	1.403	1.362	ns
	—		t_{H}	–0.638	–0.655	–0.639	–0.668	ns
	8 mA	GCLK	t_{CO}	5.302	5.872	6.422	5.945	ns
		GCLK PLL	t_{CO}	2.920	3.254	3.618	3.279	ns
	12 mA	GCLK	t_{CO}	5.302	5.872	6.422	5.945	ns
		GCLK PLL	t_{CO}	2.920	3.254	3.618	3.279	ns
	16 mA	GCLK	t_{CO}	5.302	5.872	6.422	5.945	ns
		GCLK PLL	t_{CO}	2.920	3.254	3.618	3.279	ns

Table 1–87. EP3C80 Row Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Drive Strength	Clock	Parameter	C6	C7	C8	I7	Unit
mini-LVDS	—	GCLK	t_{CO}	4.247	4.753	5.200	4.718	ns
	—	GCLK PLL	t_{CO}	1.978	2.262	2.536	2.182	ns
PPDS	—	GCLK	t_{CO}	4.247	4.753	5.200	4.718	ns
	—	GCLK PLL	t_{CO}	1.978	2.262	2.536	2.182	ns
RSDS	—	GCLK	t_{CO}	4.247	4.753	5.200	4.718	ns
	—	GCLK PLL	t_{CO}	1.978	2.262	2.536	2.182	ns

EP3C120 I/O Timing Parameters

Table 1–88 through Table 1–93 show the maximum I/O timing parameters for EP3C120 devices. EP3C120 devices are offered in C7, C8, and I7 speed grades only.

Table 1–88. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C7	C8	I7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.858	–2.031	–1.886	ns
		t_{H}	2.146	2.353	2.175	ns
	GCLK PLL	t_{SU}	1.370	1.446	1.399	ns
		t_{H}	–0.563	–0.554	–0.587	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.858	–2.031	–1.886	ns
		t_{H}	2.146	2.353	2.175	ns
	GCLK PLL	t_{SU}	1.370	1.446	1.399	ns
		t_{H}	–0.563	–0.554	–0.587	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.855	–2.034	–1.884	ns
		t_{H}	2.143	2.356	2.173	ns
	GCLK PLL	t_{SU}	1.373	1.443	1.401	ns
		t_{H}	–0.566	–0.551	–0.589	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.855	–2.034	–1.884	ns
		t_{H}	2.143	2.356	2.173	ns
	GCLK PLL	t_{SU}	1.373	1.443	1.401	ns
		t_{H}	–0.566	–0.551	–0.589	ns
2.5 V	GCLK	t_{SU}	–1.828	–2.009	–1.858	ns
		t_{H}	2.116	2.331	2.147	ns
	GCLK PLL	t_{SU}	1.400	1.468	1.427	ns
		t_{H}	–0.593	–0.576	–0.615	ns
1.8 V	GCLK	t_{SU}	–1.761	–1.972	–1.788	ns
		t_{H}	2.049	2.294	2.077	ns
	GCLK PLL	t_{SU}	1.467	1.505	1.497	ns
		t_{H}	–0.660	–0.613	–0.685	ns

Table 1–88. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C7	C8	I7	Unit
1.5 V	GCLK	t_{SU}	–1.674	–1.860	–1.704	ns
		t_H	1.962	2.182	1.993	ns
	GCLK PLL	t_{SU}	1.554	1.617	1.581	ns
		t_H	–0.747	–0.725	–0.769	ns
1.2 V	GCLK	t_{SU}	–1.496	–1.656	–1.531	ns
		t_H	1.784	1.978	1.820	ns
	GCLK PLL	t_{SU}	1.732	1.821	1.754	ns
		t_H	–0.925	–0.929	–0.942	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.779	–2.015	–1.802	ns
		t_H	2.066	2.337	2.091	ns
	GCLK PLL	t_{SU}	1.433	1.454	1.462	ns
		t_H	–0.627	–0.563	–0.649	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.779	–2.015	–1.802	ns
		t_H	2.066	2.337	2.091	ns
	GCLK PLL	t_{SU}	1.433	1.454	1.462	ns
		t_H	–0.627	–0.563	–0.649	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.558	–1.732	–1.586	ns
		t_H	1.845	2.054	1.875	ns
	GCLK PLL	t_{SU}	1.654	1.737	1.678	ns
		t_H	–0.848	–0.846	–0.865	ns
SSTL-18 Class II	GCLK	t_{SU}	–1.558	–1.732	–1.586	ns
		t_H	1.845	2.054	1.875	ns
	GCLK PLL	t_{SU}	1.654	1.737	1.678	ns
		t_H	–0.848	–0.846	–0.865	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.558	–1.732	–1.586	ns
		t_H	1.845	2.054	1.875	ns
	GCLK PLL	t_{SU}	1.654	1.737	1.678	ns
		t_H	–0.848	–0.846	–0.865	ns
1.8-V HSTL Class II	GCLK	t_{SU}	–1.558	–1.732	–1.586	ns
		t_H	1.845	2.054	1.875	ns
	GCLK PLL	t_{SU}	1.654	1.737	1.678	ns
		t_H	–0.848	–0.846	–0.865	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.666	–1.860	–1.694	ns
		t_H	1.953	2.182	1.983	ns
	GCLK PLL	t_{SU}	1.546	1.609	1.570	ns
		t_H	–0.740	–0.718	–0.757	ns

Table 1–88. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C7	C8	I7	Unit
1.5-V HSTL Class II	GCLK	t_{SU}	–1.666	–1.860	–1.694	ns
		t_H	1.953	2.182	1.983	ns
	GCLK PLL	t_{SU}	1.546	1.609	1.570	ns
		t_H	–0.740	–0.718	–0.757	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.421	–1.578	–1.459	ns
		t_H	1.708	1.900	1.748	ns
	GCLK PLL	t_{SU}	1.791	1.891	1.805	ns
		t_H	–0.985	–1.000	–0.992	ns
1.2-V HSTL Class II	GCLK	t_{SU}	–1.421	–1.578	–1.459	ns
		t_H	1.708	1.900	1.748	ns
	GCLK PLL	t_{SU}	1.791	1.891	1.805	ns
		t_H	–0.985	–1.000	–0.992	ns
3.0-V PCI	GCLK	t_{SU}	–1.855	–2.034	–1.884	ns
		t_H	2.143	2.356	2.173	ns
	GCLK PLL	t_{SU}	1.373	1.443	1.401	ns
		t_H	–0.566	–0.551	–0.589	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.855	–2.034	–1.884	ns
		t_H	2.143	2.356	2.173	ns
	GCLK PLL	t_{SU}	1.373	1.443	1.401	ns
		t_H	–0.566	–0.551	–0.589	ns

Table 1–89. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Clock	Parameter	C7	C8	I7	Unit
3.3-V LVTTL	GCLK	t_{SU}	–1.795	–1.949	–1.819	ns
		t_H	2.081	2.270	2.106	ns
	GCLK PLL	t_{SU}	1.413	1.488	1.440	ns
		t_H	–0.607	–0.598	–0.629	ns
3.3-V LVCMOS	GCLK	t_{SU}	–1.795	–1.949	–1.819	ns
		t_H	2.081	2.270	2.106	ns
	GCLK PLL	t_{SU}	1.413	1.488	1.440	ns
		t_H	–0.607	–0.598	–0.629	ns
3.0-V LVTTL	GCLK	t_{SU}	–1.791	–1.951	–1.816	ns
		t_H	2.077	2.272	2.103	ns
	GCLK PLL	t_{SU}	1.417	1.486	1.443	ns
		t_H	–0.611	–0.596	–0.632	ns
3.0-V LVCMOS	GCLK	t_{SU}	–1.791	–1.951	–1.816	ns
		t_H	2.077	2.272	2.103	ns
	GCLK PLL	t_{SU}	1.417	1.486	1.443	ns
		t_H	–0.611	–0.596	–0.632	ns

Table 1–89. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Clock	Parameter	C7	C8	I7	Unit
2.5 V	GCLK	t_{SU}	–1.764	–1.931	–1.789	ns
		t_{H}	2.050	2.252	2.076	ns
	GCLK PLL	t_{SU}	1.444	1.506	1.470	ns
		t_{H}	–0.638	–0.616	–0.659	ns
1.8 V	GCLK	t_{SU}	–1.697	–1.894	–1.720	ns
		t_{H}	1.983	2.215	2.007	ns
	GCLK PLL	t_{SU}	1.511	1.543	1.539	ns
		t_{H}	–0.705	–0.653	–0.728	ns
1.5 V	GCLK	t_{SU}	–1.610	–1.783	–1.636	ns
		t_{H}	1.896	2.104	1.923	ns
	GCLK PLL	t_{SU}	1.598	1.654	1.623	ns
		t_{H}	–0.792	–0.764	–0.812	ns
1.2 V	GCLK	t_{SU}	–1.431	–1.578	–1.462	ns
		t_{H}	1.717	1.899	1.749	ns
	GCLK PLL	t_{SU}	1.777	1.859	1.797	ns
		t_{H}	–0.971	–0.969	–0.986	ns
SSTL-2 Class I	GCLK	t_{SU}	–1.740	–1.951	–1.758	ns
		t_{H}	2.027	2.271	2.046	ns
	GCLK PLL	t_{SU}	1.486	1.517	1.518	ns
		t_{H}	–0.682	–0.628	–0.707	ns
SSTL-2 Class II	GCLK	t_{SU}	–1.740	–1.951	–1.758	ns
		t_{H}	2.027	2.271	2.046	ns
	GCLK PLL	t_{SU}	1.486	1.517	1.518	ns
		t_{H}	–0.682	–0.628	–0.707	ns
SSTL-18 Class I	GCLK	t_{SU}	–1.519	–1.669	–1.544	ns
		t_{H}	1.806	1.989	1.832	ns
	GCLK PLL	t_{SU}	1.707	1.799	1.732	ns
		t_{H}	–0.903	–0.910	–0.921	ns
SSTL-18 Class II	GCLK	t_{SU}	–1.519	–1.669	–1.544	ns
		t_{H}	1.806	1.989	1.832	ns
	GCLK PLL	t_{SU}	1.707	1.799	1.732	ns
		t_{H}	–0.903	–0.910	–0.921	ns
1.8-V HSTL Class I	GCLK	t_{SU}	–1.519	–1.669	–1.544	ns
		t_{H}	1.806	1.989	1.832	ns
	GCLK PLL	t_{SU}	1.707	1.799	1.732	ns
		t_{H}	–0.903	–0.910	–0.921	ns

Table 1–89. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Clock	Parameter	C7	C8	I7	Unit
1.8-V HSTL Class II	GCLK	t_{SU}	–1.519	–1.669	–1.544	ns
		t_{H}	1.806	1.989	1.832	ns
	GCLK PLL	t_{SU}	1.707	1.799	1.732	ns
		t_{H}	–0.903	–0.910	–0.921	ns
1.5-V HSTL Class I	GCLK	t_{SU}	–1.625	–1.788	–1.651	ns
		t_{H}	1.912	2.108	1.939	ns
	GCLK PLL	t_{SU}	1.601	1.680	1.625	ns
		t_{H}	–0.797	–0.791	–0.814	ns
1.5-V HSTL Class II	GCLK	t_{SU}	–1.625	–1.788	–1.651	ns
		t_{H}	1.912	2.108	1.939	ns
	GCLK PLL	t_{SU}	1.601	1.680	1.625	ns
		t_{H}	–0.797	–0.791	–0.814	ns
1.2-V HSTL Class I	GCLK	t_{SU}	–1.381	–1.517	–1.416	ns
		t_{H}	1.668	1.837	1.704	ns
	GCLK PLL	t_{SU}	1.845	1.951	1.860	ns
		t_{H}	–1.041	–1.062	–1.049	ns
3.0-V PCI	GCLK	t_{SU}	–1.791	–1.951	–1.816	ns
		t_{H}	2.077	2.272	2.103	ns
	GCLK PLL	t_{SU}	1.417	1.486	1.443	ns
		t_{H}	–0.611	–0.596	–0.632	ns
3.0-V PCI-X	GCLK	t_{SU}	–1.791	–1.951	–1.816	ns
		t_{H}	2.077	2.272	2.103	ns
	GCLK PLL	t_{SU}	1.417	1.486	1.443	ns
		t_{H}	–0.611	–0.596	–0.632	ns

Table 1–90. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	6.038	6.618	6.126	ns
		GCLK PLL	t_{CO}	3.335	3.723	3.360	ns
	8 mA	GCLK	t_{CO}	5.705	6.270	5.782	ns
		GCLK PLL	t_{CO}	3.002	3.375	3.016	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.778	6.345	5.861	ns
		GCLK PLL	t_{CO}	3.075	3.450	3.095	ns

Table 1–90. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.843	6.419	5.929	ns
		GCLK PLL	t_{CO}	3.140	3.524	3.163	ns
	8 mA	GCLK	t_{CO}	5.644	6.210	5.723	ns
		GCLK PLL	t_{CO}	2.941	3.315	2.957	ns
	12 mA	GCLK	t_{CO}	5.576	6.131	5.649	ns
		GCLK PLL	t_{CO}	2.873	3.236	2.883	ns
	16 mA	GCLK	t_{CO}	5.543	6.093	5.616	ns
		GCLK PLL	t_{CO}	2.840	3.198	2.850	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.651	6.217	5.730	ns
		GCLK PLL	t_{CO}	2.948	3.322	2.964	ns
	8 mA	GCLK	t_{CO}	5.544	6.097	5.617	ns
		GCLK PLL	t_{CO}	2.841	3.202	2.851	ns
	12 mA	GCLK	t_{CO}	5.512	6.064	5.585	ns
		GCLK PLL	t_{CO}	2.809	3.169	2.819	ns
	16 mA	GCLK	t_{CO}	5.499	6.052	5.572	ns
		GCLK PLL	t_{CO}	2.796	3.157	2.806	ns
2.5 V	4 mA	GCLK	t_{CO}	5.949	6.537	6.045	ns
		GCLK PLL	t_{CO}	3.246	3.642	3.279	ns
	8 mA	GCLK	t_{CO}	5.769	6.352	5.853	ns
		GCLK PLL	t_{CO}	3.066	3.457	3.087	ns
	12 mA	GCLK	t_{CO}	5.686	6.257	5.765	ns
		GCLK PLL	t_{CO}	2.983	3.362	2.999	ns
	16 mA	GCLK	t_{CO}	5.657	6.228	5.734	ns
		GCLK PLL	t_{CO}	2.954	3.333	2.968	ns
1.8 V	2 mA	GCLK	t_{CO}	7.034	7.758	7.138	ns
		GCLK PLL	t_{CO}	4.331	4.863	4.372	ns
	4 mA	GCLK	t_{CO}	6.641	7.345	6.739	ns
		GCLK PLL	t_{CO}	3.938	4.450	3.973	ns
	6 mA	GCLK	t_{CO}	6.425	7.105	6.515	ns
		GCLK PLL	t_{CO}	3.722	4.210	3.749	ns
	8 mA	GCLK	t_{CO}	6.354	7.019	6.441	ns
		GCLK PLL	t_{CO}	3.651	4.124	3.675	ns
	10 mA	GCLK	t_{CO}	6.292	6.959	6.379	ns
		GCLK PLL	t_{CO}	3.589	4.064	3.613	ns
	12 mA	GCLK	t_{CO}	6.242	6.895	6.325	ns
		GCLK PLL	t_{CO}	3.539	4.000	3.559	ns
	16 mA	GCLK	t_{CO}	6.200	6.857	6.284	ns
		GCLK PLL	t_{CO}	3.497	3.962	3.518	ns

Table 1–90. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
1.5 V	2 mA	GCLK	t_{CO}	7.649	8.543	7.750	ns
		GCLK PLL	t_{CO}	4.946	5.648	4.984	ns
	4 mA	GCLK	t_{CO}	7.177	7.995	7.275	ns
		GCLK PLL	t_{CO}	4.474	5.100	4.509	ns
	6 mA	GCLK	t_{CO}	7.034	7.838	7.127	ns
		GCLK PLL	t_{CO}	4.331	4.943	4.361	ns
	8 mA	GCLK	t_{CO}	6.920	7.704	7.015	ns
		GCLK PLL	t_{CO}	4.217	4.809	4.249	ns
	10 mA	GCLK	t_{CO}	6.882	7.655	6.967	ns
		GCLK PLL	t_{CO}	4.179	4.760	4.201	ns
	12 mA	GCLK	t_{CO}	6.847	7.613	6.933	ns
		GCLK PLL	t_{CO}	4.144	4.718	4.167	ns
	16 mA	GCLK	t_{CO}	6.729	7.480	6.813	ns
		GCLK PLL	t_{CO}	4.026	4.585	4.047	ns
1.2 V	2 mA	GCLK	t_{CO}	9.067	10.318	9.128	ns
		GCLK PLL	t_{CO}	6.364	7.423	6.362	ns
	4 mA	GCLK	t_{CO}	8.653	9.836	8.711	ns
		GCLK PLL	t_{CO}	5.950	6.941	5.945	ns
	6 mA	GCLK	t_{CO}	8.490	9.639	8.549	ns
		GCLK PLL	t_{CO}	5.787	6.744	5.783	ns
	8 mA	GCLK	t_{CO}	8.422	9.563	8.480	ns
		GCLK PLL	t_{CO}	5.719	6.668	5.714	ns
	10 mA	GCLK	t_{CO}	8.253	9.340	8.308	ns
		GCLK PLL	t_{CO}	5.550	6.445	5.542	ns
	12 mA	GCLK	t_{CO}	8.236	9.325	8.290	ns
		GCLK PLL	t_{CO}	5.533	6.430	5.524	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.697	6.268	5.771	ns
		GCLK PLL	t_{CO}	2.997	3.375	3.024	ns
	12 mA	GCLK	t_{CO}	5.675	6.245	5.749	ns
		GCLK PLL	t_{CO}	2.975	3.352	3.002	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.636	6.202	5.709	ns
		GCLK PLL	t_{CO}	2.936	3.309	2.962	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.181	6.829	6.261	ns
		GCLK PLL	t_{CO}	3.481	3.936	3.514	ns
	10 mA	GCLK	t_{CO}	6.150	6.790	6.231	ns
		GCLK PLL	t_{CO}	3.450	3.897	3.484	ns
	12 mA	GCLK	t_{CO}	6.149	6.786	6.229	ns
		GCLK PLL	t_{CO}	3.449	3.893	3.482	ns

Table 1–90. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.131	6.771	6.211	ns
		GCLK PLL	t_{CO}	3.431	3.878	3.464	ns
	16 mA	GCLK	t_{CO}	6.119	6.757	6.198	ns
		GCLK PLL	t_{CO}	3.419	3.864	3.451	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.157	6.796	6.237	ns
		GCLK PLL	t_{CO}	3.457	3.903	3.490	ns
	10 mA	GCLK	t_{CO}	6.153	6.794	6.232	ns
		GCLK PLL	t_{CO}	3.453	3.901	3.485	ns
	12 mA	GCLK	t_{CO}	6.134	6.771	6.214	ns
		GCLK PLL	t_{CO}	3.434	3.878	3.467	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.112	6.745	6.191	ns
		GCLK PLL	t_{CO}	3.412	3.852	3.444	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.744	7.493	6.827	ns
		GCLK PLL	t_{CO}	4.044	4.600	4.080	ns
	10 mA	GCLK	t_{CO}	6.734	7.478	6.819	ns
		GCLK PLL	t_{CO}	4.034	4.585	4.072	ns
	12 mA	GCLK	t_{CO}	6.731	7.476	6.815	ns
		GCLK PLL	t_{CO}	4.031	4.583	4.068	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.685	7.420	6.769	ns
		GCLK PLL	t_{CO}	3.985	4.527	4.022	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.197	9.288	8.250	ns
		GCLK PLL	t_{CO}	5.497	6.395	5.503	ns
	10 mA	GCLK	t_{CO}	8.087	9.129	8.139	ns
		GCLK PLL	t_{CO}	5.387	6.236	5.392	ns
	12 mA	GCLK	t_{CO}	8.089	9.133	8.142	ns
		GCLK PLL	t_{CO}	5.389	6.240	5.395	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	8.016	9.061	8.071	ns
		GCLK PLL	t_{CO}	5.316	6.168	5.324	ns
3.0-V PCI	—	GCLK	t_{CO}	5.814	6.374	5.891	ns
		GCLK PLL	t_{CO}	3.111	3.479	3.125	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.814	6.374	5.891	ns
		GCLK PLL	t_{CO}	3.111	3.479	3.125	ns

Table 1–91. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
3.3-V LVTTL	4 mA	GCLK	t_{CO}	6.238	6.820	6.331	ns
		GCLK PLL	t_{CO}	3.523	3.913	3.557	ns
	8 mA	GCLK	t_{CO}	5.775	6.339	5.857	ns
		GCLK PLL	t_{CO}	3.060	3.432	3.083	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.862	6.430	5.948	ns
		GCLK PLL	t_{CO}	3.147	3.523	3.174	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.961	6.520	6.046	ns
		GCLK PLL	t_{CO}	3.246	3.613	3.272	ns
	8 mA	GCLK	t_{CO}	5.706	6.260	5.784	ns
		GCLK PLL	t_{CO}	2.991	3.353	3.010	ns
	12 mA	GCLK	t_{CO}	5.580	6.133	5.653	ns
		GCLK PLL	t_{CO}	2.865	3.226	2.879	ns
	16 mA	GCLK	t_{CO}	5.525	6.066	5.597	ns
		GCLK PLL	t_{CO}	2.810	3.159	2.823	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.705	6.258	5.782	ns
		GCLK PLL	t_{CO}	2.990	3.351	3.008	ns
	8 mA	GCLK	t_{CO}	5.528	6.070	5.599	ns
		GCLK PLL	t_{CO}	2.813	3.163	2.825	ns
	12 mA	GCLK	t_{CO}	5.488	6.030	5.559	ns
		GCLK PLL	t_{CO}	2.773	3.123	2.785	ns
	16 mA	GCLK	t_{CO}	5.468	6.011	5.539	ns
		GCLK PLL	t_{CO}	2.753	3.104	2.765	ns
2.5 V	4 mA	GCLK	t_{CO}	6.101	6.678	6.194	ns
		GCLK PLL	t_{CO}	3.386	3.771	3.420	ns
	8 mA	GCLK	t_{CO}	5.831	6.401	5.912	ns
		GCLK PLL	t_{CO}	3.116	3.494	3.138	ns
	12 mA	GCLK	t_{CO}	5.711	6.278	5.789	ns
		GCLK PLL	t_{CO}	2.996	3.371	3.015	ns
	16 mA	GCLK	t_{CO}	5.655	6.219	5.732	ns
		GCLK PLL	t_{CO}	2.940	3.312	2.958	ns

Table 1–91. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
1.8 V	2 mA	GCLK	t_{CO}	7.388	8.125	7.515	ns
		GCLK PLL	t_{CO}	4.673	5.218	4.741	ns
	4 mA	GCLK	t_{CO}	6.818	7.533	6.920	ns
		GCLK PLL	t_{CO}	4.103	4.626	4.146	ns
	6 mA	GCLK	t_{CO}	6.524	7.201	6.619	ns
		GCLK PLL	t_{CO}	3.809	4.294	3.845	ns
	8 mA	GCLK	t_{CO}	6.395	7.056	6.485	ns
		GCLK PLL	t_{CO}	3.680	4.149	3.711	ns
	10 mA	GCLK	t_{CO}	6.341	7.009	6.430	ns
		GCLK PLL	t_{CO}	3.626	4.102	3.656	ns
	12 mA	GCLK	t_{CO}	6.265	6.920	6.352	ns
		GCLK PLL	t_{CO}	3.550	4.013	3.578	ns
	16 mA	GCLK	t_{CO}	6.216	6.864	6.301	ns
		GCLK PLL	t_{CO}	3.501	3.957	3.527	ns
1.5 V	2 mA	GCLK	t_{CO}	7.959	8.878	8.064	ns
		GCLK PLL	t_{CO}	5.244	5.971	5.290	ns
	4 mA	GCLK	t_{CO}	7.316	8.134	7.410	ns
		GCLK PLL	t_{CO}	4.601	5.227	4.636	ns
	6 mA	GCLK	t_{CO}	7.111	7.918	7.201	ns
		GCLK PLL	t_{CO}	4.396	5.011	4.427	ns
	8 mA	GCLK	t_{CO}	7.001	7.780	7.089	ns
		GCLK PLL	t_{CO}	4.286	4.873	4.315	ns
	10 mA	GCLK	t_{CO}	6.929	7.710	7.016	ns
		GCLK PLL	t_{CO}	4.214	4.803	4.242	ns
	12 mA	GCLK	t_{CO}	6.878	7.646	6.964	ns
		GCLK PLL	t_{CO}	4.163	4.739	4.190	ns
	16 mA	GCLK	t_{CO}	6.795	7.555	6.880	ns
		GCLK PLL	t_{CO}	4.080	4.648	4.106	ns
1.2 V	2 mA	GCLK	t_{CO}	9.338	10.627	9.399	ns
		GCLK PLL	t_{CO}	6.623	7.720	6.625	ns
	4 mA	GCLK	t_{CO}	8.770	9.966	8.827	ns
		GCLK PLL	t_{CO}	6.055	7.059	6.053	ns
	6 mA	GCLK	t_{CO}	8.587	9.751	8.644	ns
		GCLK PLL	t_{CO}	5.872	6.844	5.870	ns
	8 mA	GCLK	t_{CO}	8.489	9.638	8.545	ns
		GCLK PLL	t_{CO}	5.774	6.731	5.771	ns
	10 mA	GCLK	t_{CO}	8.340	9.452	8.397	ns
		GCLK PLL	t_{CO}	5.625	6.545	5.623	ns

Table 1–91. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.717	6.277	5.792	ns
		GCLK PLL	t_{CO}	3.016	3.384	3.043	ns
	12 mA	GCLK	t_{CO}	5.683	6.241	5.758	ns
		GCLK PLL	t_{CO}	2.982	3.348	3.009	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.629	6.184	5.703	ns
		GCLK PLL	t_{CO}	2.928	3.291	2.954	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.191	6.830	6.273	ns
		GCLK PLL	t_{CO}	3.490	3.937	3.524	ns
	10 mA	GCLK	t_{CO}	6.168	6.800	6.250	ns
		GCLK PLL	t_{CO}	3.467	3.907	3.501	ns
	12 mA	GCLK	t_{CO}	6.143	6.773	6.225	ns
		GCLK PLL	t_{CO}	3.442	3.880	3.476	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.136	6.766	6.216	ns
		GCLK PLL	t_{CO}	3.435	3.873	3.467	ns
	16 mA	GCLK	t_{CO}	6.121	6.752	6.202	ns
		GCLK PLL	t_{CO}	3.420	3.859	3.453	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.163	6.791	6.244	ns
		GCLK PLL	t_{CO}	3.462	3.898	3.495	ns
	10 mA	GCLK	t_{CO}	6.159	6.790	6.239	ns
		GCLK PLL	t_{CO}	3.458	3.897	3.490	ns
	12 mA	GCLK	t_{CO}	6.145	6.772	6.226	ns
		GCLK PLL	t_{CO}	3.444	3.879	3.477	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.107	6.730	6.187	ns
		GCLK PLL	t_{CO}	3.406	3.837	3.438	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.762	7.499	6.843	ns
		GCLK PLL	t_{CO}	4.061	4.606	4.094	ns
	10 mA	GCLK	t_{CO}	6.758	7.491	6.840	ns
		GCLK PLL	t_{CO}	4.057	4.598	4.091	ns
	12 mA	GCLK	t_{CO}	6.751	7.487	6.832	ns
		GCLK PLL	t_{CO}	4.050	4.594	4.083	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.705	7.433	6.785	ns
		GCLK PLL	t_{CO}	4.004	4.540	4.036	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.230	9.314	8.283	ns
		GCLK PLL	t_{CO}	5.529	6.421	5.534	ns
	10 mA	GCLK	t_{CO}	8.114	9.153	8.167	ns
		GCLK PLL	t_{CO}	5.413	6.260	5.418	ns
3.0-V PCI	—	GCLK	t_{CO}	5.792	6.342	5.867	ns
		GCLK PLL	t_{CO}	3.077	3.435	3.093	ns

Table 1–91. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
3.0-V PCI-X	—	GCLK	t_{CO}	5.792	6.342	5.867	ns
		GCLK PLL	t_{CO}	3.077	3.435	3.093	ns

Table 1–92. EP3C120 Column Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
LVDS	—	GCLK	t_{SU}	–1.829	–2.019	–1.868	ns
	—		t_{H}	2.146	2.373	2.185	ns
	—	GCLK PLL	t_{SU}	1.407	1.463	1.419	ns
	—		t_{H}	–0.572	–0.540	–0.578	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.643	6.209	5.720	ns
	—	GCLK PLL	t_{CO}	2.940	3.316	2.969	ns
BLVDS	—	GCLK	t_{SU}	–1.801	–1.982	–1.836	ns
	—		t_{H}	2.117	2.335	2.152	ns
	—	GCLK PLL	t_{SU}	1.438	1.500	1.455	ns
	—		t_{H}	–0.746	–0.734	–0.761	ns
	8 mA	GCLK	t_{CO}	5.951	6.514	6.029	ns
		GCLK PLL	t_{CO}	3.110	3.468	3.138	ns
	12 mA	GCLK	t_{CO}	5.951	6.514	6.029	ns
		GCLK PLL	t_{CO}	3.110	3.468	3.138	ns
	16 mA	GCLK	t_{CO}	5.951	6.514	6.029	ns
		GCLK PLL	t_{CO}	3.110	3.468	3.138	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.643	6.209	5.720	ns
	—	GCLK PLL	t_{CO}	2.940	3.316	2.969	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.643	6.209	5.720	ns
	—	GCLK PLL	t_{CO}	2.940	3.316	2.969	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.544	6.083	5.616	ns
	—	GCLK PLL	t_{CO}	2.841	3.190	2.865	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.643	6.209	5.720	ns
	—	GCLK PLL	t_{CO}	2.940	3.316	2.969	ns

Table 1–93. EP3C120 Row Pin Differential I/O Timing Parameters

IO Standard	Drive Strength	Clock	Parameter	C7	C8	I7	Unit
LVDS	—	GCLK	t_{SU}	–1.780	–1.962	–1.816	ns
	—		t_{H}	2.096	2.315	2.131	ns
	—		t_{CO}	4.824	5.285	4.794	ns
	—	GCLK PLL	t_{SU}	1.439	1.500	1.455	ns
	—		t_{H}	–0.604	–0.578	–0.616	ns
	—		t_{CO}	2.132	2.399	2.055	ns
BLVDS	—	GCLK	t_{SU}	–1.781	–1.962	–1.816	ns
	—		t_{H}	2.097	2.315	2.132	ns
	—	GCLK PLL	t_{SU}	1.418	1.480	1.435	ns
	—		t_{H}	–0.726	–0.714	–0.741	ns
	8 mA	GCLK	t_{CO}	5.953	6.517	6.031	ns
		GCLK PLL	t_{CO}	3.108	3.465	3.136	ns
	12 mA	GCLK	t_{CO}	5.953	6.517	6.031	ns
		GCLK PLL	t_{CO}	3.108	3.465	3.136	ns
	16 mA	GCLK	t_{CO}	5.953	6.517	6.031	ns
		GCLK PLL	t_{CO}	3.108	3.465	3.136	ns
mini-LVDS	—	GCLK	t_{CO}	4.824	5.285	4.794	ns
	—	GCLK PLL	t_{CO}	2.132	2.399	2.055	ns
PPDS	—	GCLK	t_{CO}	4.824	5.285	4.794	ns
	—	GCLK PLL	t_{CO}	2.132	2.399	2.055	ns
RSDS	—	GCLK	t_{CO}	4.824	5.285	4.794	ns
	—	GCLK PLL	t_{CO}	2.132	2.399	2.055	ns

Dedicated Clock Pin Timing Parameters

Table 1–94 through Table 1–109 show clock pin timing for Cyclone III devices.

EP3C5 Clock Timing Parameters

Table 1–94 and Table 1–95 show the maximum clock timing parameters for EP3C5 devices.

Table 1–94. EP3C5 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.537	1.598	2.287	2.517	2.723	2.540	2.585	ns
tcout	1.565	1.626	2.327	2.561	2.773	2.586	2.632	ns
tpllcin	0.962	0.986	1.222	1.313	1.417	1.328	1.300	ns
tpllcout	0.990	1.014	1.262	1.357	1.467	1.374	1.347	ns

Table 1–95. EP3C5 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.522	1.581	2.257	2.480	2.680	2.502	2.543	ns
tcout	1.550	1.609	2.297	2.524	2.730	2.548	2.590	ns
tpllcin	0.947	0.969	1.192	1.276	1.374	1.290	1.258	ns
tpllcout	0.975	0.997	1.232	1.320	1.424	1.336	1.305	ns

EP3C10 Clock Timing Parameters

Table 1–96 and Table 1–97 show the maximum clock timing parameters for EP3C10 devices.

Table 1–96. EP3C10 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.538	1.600	2.289	2.518	2.728	2.540	2.585	ns
tcout	1.566	1.628	2.329	2.562	2.778	2.586	2.632	ns
tpllcin	0.963	0.988	1.224	1.314	1.422	1.328	1.300	ns
tpllcout	0.991	1.016	1.264	1.358	1.472	1.374	1.347	ns

Table 1–97. Table 1-96. EP3C10 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.525	1.582	2.258	2.482	2.686	2.504	2.544	ns
tcout	1.553	1.610	2.298	2.526	2.736	2.550	2.591	ns
tpllcin	0.950	0.970	1.193	1.278	1.380	1.292	1.259	ns
tpllcout	0.978	0.998	1.233	1.322	1.430	1.338	1.306	ns

EP3C16 Clock Timing Parameters

Table 1–98 and Table 1–99 show the maximum clock timing parameters for EP3C16 devices.

Table 1–98. EP3C16 Column Pin Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.695	1.769	2.538	2.789	3.024	2.818	2.868	ns
tcout	1.723	1.797	2.578	2.833	3.074	2.864	2.915	ns

Table 1–98. EP3C16 Column Pin Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tpllcin	1.204	1.247	1.595	1.720	1.863	1.743	1.727	ns
tpllcout	1.232	1.275	1.635	1.764	1.913	1.789	1.774	ns

Table 1–99. EP3C16 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.673	1.746	2.499	2.743	2.975	2.771	2.820	ns
tcout	1.701	1.774	2.539	2.787	3.025	2.817	2.867	ns
tpllcin	1.182	1.224	1.556	1.674	1.814	1.696	1.679	ns
tpllcout	1.210	1.252	1.596	1.718	1.864	1.742	1.726	ns

EP3C25 Clock Timing Parameters

Table 1–100 and Table 1–101 show the maximum clock timing parameters for EP3C25 devices.

Table 1–100. EP3C25 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.686	1.756	2.523	2.772	2.994	2.798	2.852	ns
tcout	1.714	1.784	2.563	2.816	3.044	2.844	2.899	ns
tpllcin	1.182	1.220	1.637	1.765	1.903	1.784	1.775	ns
tpllcout	1.210	1.248	1.677	1.809	1.953	1.830	1.822	ns

Table 1–101. EP3C25 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.660	1.731	2.484	2.723	2.942	2.748	2.801	ns
tcout	1.688	1.759	2.524	2.767	2.992	2.794	2.848	ns
tpllcin	1.156	1.195	1.598	1.716	1.851	1.734	1.724	ns
tpllcout	1.184	1.223	1.638	1.760	1.901	1.780	1.771	ns

EP3C40 Clock Timing Parameters

Table 1–102 and Table 1–103 show the maximum clock timing parameters for EP3C40 device.

Table 1–102. EP3C40 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.777	1.857	2.671	2.932	3.177	2.962	3.020	ns
tcout	1.805	1.885	2.711	2.976	3.227	3.008	3.067	ns
tpllcin	1.269	1.313	1.771	1.910	2.071	1.935	1.929	ns
tpllcout	1.297	1.341	1.811	1.954	2.121	1.981	1.976	ns

Table 1–103. EP3C40 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	A7	Unit
	Automotive and Industrial	Commercial						
tcin	1.750	1.834	2.633	2.886	3.119	2.907	2.974	ns
tcout	1.778	1.862	2.673	2.930	3.169	2.953	3.021	ns
tpllcin	1.242	1.290	1.733	1.864	2.013	1.880	1.883	ns
tpllcout	1.270	1.318	1.773	1.908	2.063	1.926	1.930	ns

EP3C55 Clock Timing Parameters

Table 1–104 and Table 1–105 show the maximum clock timing parameters for EP3C55 devices.

Table 1–104. EP3C55 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	Unit
	Automotive and Industrial	Commercial					
tcin	1.819	1.906	2.729	2.993	3.230	3.022	ns
tcout	1.847	1.934	2.769	3.037	3.280	3.068	ns
tpllcin	1.318	1.371	1.836	1.978	2.125	1.999	ns
tpllcout	1.346	1.399	1.876	2.022	2.175	2.045	ns

Table 1–105. EP3C55 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	Unit
	Automotive and Industrial	Commercial					
tcin	1.787	1.866	2.669	2.931	3.162	2.959	ns
tcout	1.815	1.894	2.709	2.975	3.212	3.005	ns
tpllcin	1.286	1.331	1.776	1.916	2.057	1.936	ns
tpllcout	1.314	1.359	1.816	1.960	2.107	1.982	ns

EP3C80 Clock Timing Parameters

Table 1–106 and Table 1–107 show the maximum clock timing parameters for EP3C80 devices.

Table 1–106. EP3C80 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	Unit
	Automotive and Industrial	Commercial					
tcin	1.905	1.988	2.846	3.119	3.362	3.153	ns
tcout	1.933	2.016	2.886	3.163	3.412	3.199	ns
tpllcin	1.401	1.445	1.942	2.087	2.239	2.115	ns
tpllcout	1.429	1.473	1.982	2.131	2.289	2.161	ns

Table 1–107. EP3C80 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		C6	C7	C8	I7	Unit
	Automotive and Industrial	Commercial					
tcin	1.874	1.967	2.805	3.068	3.308	3.096	ns
tcout	1.902	1.995	2.845	3.112	3.358	3.142	ns
tpllcin	1.370	1.424	1.901	2.036	2.185	2.058	ns
tpllcout	1.398	1.452	1.941	2.080	2.235	2.104	ns

EP3C120 Clock Timing Parameters

Table 1–108 and Table 1–109 show the maximum clock timing parameters for EP3C120 devices. EP3C120 devices are offered in C7, C8, and I7 speed grades only.

Table 1–108. EP3C120 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		C7	C8	I7	Unit
	Automotive and Industrial	Commercial				
tcin	1.955	2.050	3.225	3.481	3.261	ns
tcout	1.983	2.078	3.269	3.531	3.307	ns
tpllcin	1.389	1.445	2.064	2.219	2.092	ns
tpllcout	1.417	1.473	2.108	2.269	2.138	ns

Table 1–109. EP3C120 Row Pin Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Model		C7	C8	I7	Unit
	Automotive and Industrial	Commercial				
tcin	1.932	2.032	3.181	3.423	3.209	ns
tcout	1.960	2.060	3.225	3.473	3.255	ns

Table 1–109. EP3C120 Row Pin Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Model		C7	C8	I7	Unit
	Automotive and Industrial	Commercial				
tpllcin	1.366	1.427	2.020	2.161	2.040	ns
tpllcout	1.394	1.455	2.064	2.211	2.086	ns

Glossary

Table 1–110 shows the glossary for this chapter.

Table 1–110. Glossary (Part 1 of 5)

Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	HIGH-SPEED I/O Block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through PLL.
H	HSIODR	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard	

Table 1–110. Glossary (Part 2 of 5)

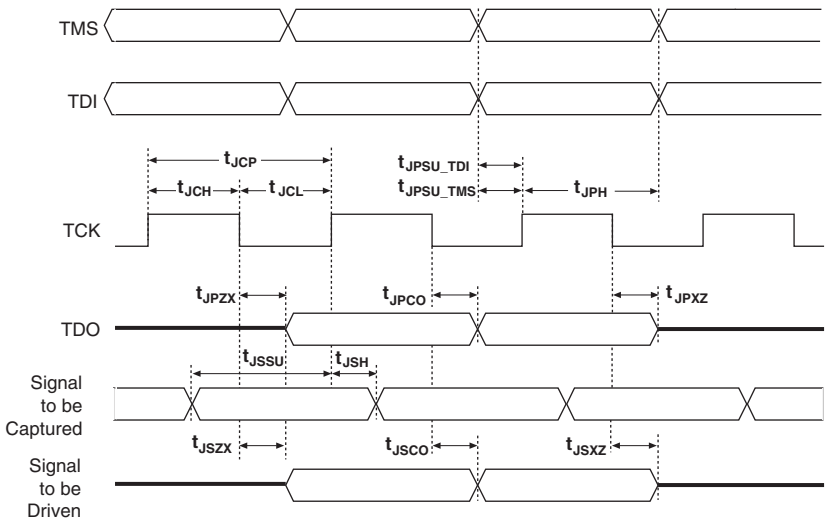
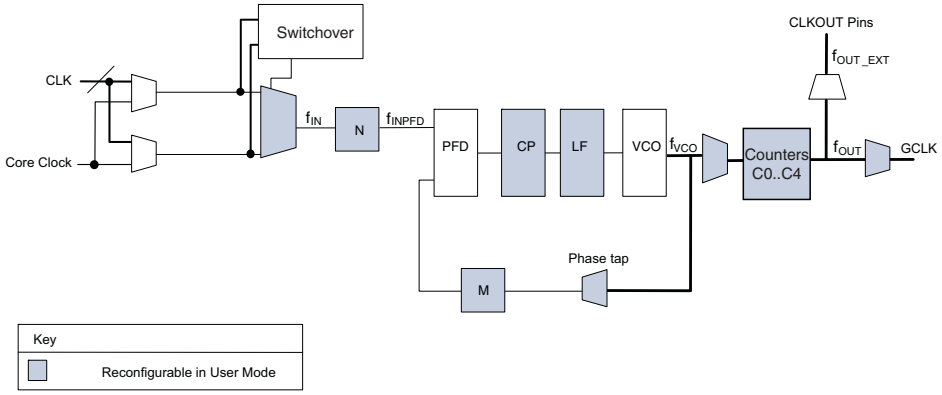
Letter	Term	Definitions
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following block diagram highlights the PLL Specification parameters. 
Q	—	—

Table 1–110. Glossary (Part 3 of 5)

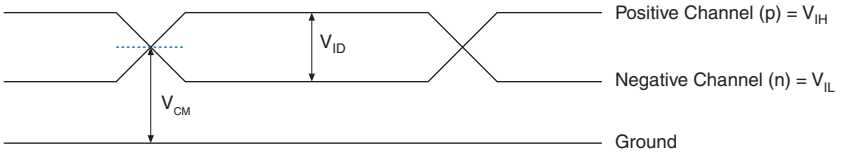
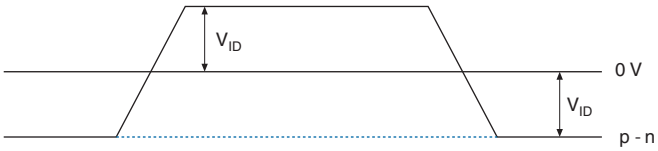
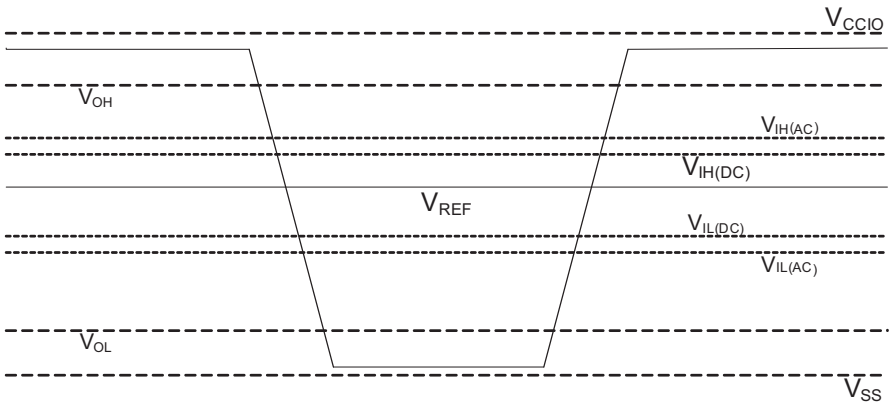
Letter	Term	Definitions
R	R_L	Receiver differential input discrete resistor (external to Cyclone III device).
	Receiver Input Waveform	Receiver Input Waveform for LVDS and LVPECL Differential Standards. **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	RSKM (Receiver input skew margin)	HIGH-SPEED I/O Block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
S	Single-ended Voltage referenced I/O Standard	 The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*.
	SW (Sampling Window)	HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.

Table 1–110. Glossary (Part 4 of 5)

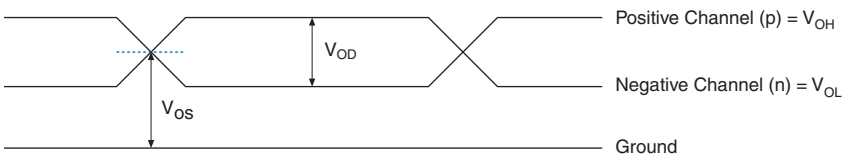
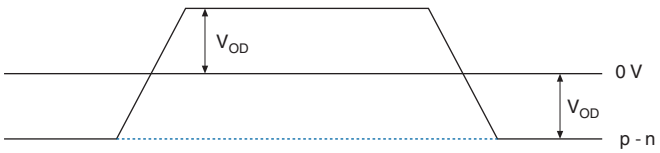
Letter	Term	Definitions
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (Channel-to-channel-skew)	HIGH-SPEED I/O Block: The timing difference between the fastest and slowest output edges, including t_{C0} variation and clock skew. The clock is included in the TCCS measurement.
	tcin	Delay from clock pad to I/O input register.
	t_{CO}	Delay from clock pad to I/O output.
	tcout	Delay from clock pad to I/O output register.
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal High-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
	$t_{INJITTER}$	Period jitter on PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on general purpose I/O driven by a PLL.
	tpllcin	Delay from PLL inclk pad to I/O input register.
	tpllcout	Delay from PLL inclk pad to I/O output register.
	Transmitter Output Waveform	Transmitter Output Waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	t_{RISE}	Signal Low-to-high transition time (20–80%).
	t_{SU}	Input register setup time.
U	—	—

Table 1–110. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	$V_{DIF(AC)}$	AC differential Input Voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
	V_{OH}	Voltage Output High: The maximum positive voltage from an output which the device considers will be accepted as the minimum positive high level.
	V_{OL}	Voltage Output Low: The maximum positive voltage from an output which the device considers will be accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for SSTL, HSTL I/O Standards.
	$V_{REF\ (AC)}$	AC input reference voltage for SSTL, HSTL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
	$V_{REF\ (DC)}$	DC input reference voltage for SSTL, HSTL I/O Standards.
	$V_{SWING\ (AC)}$	AC differential Input Voltage: AC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.
	$V_{SWING\ (DC)}$	DC differential Input Voltage: DC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.
	V_{TT}	Termination voltage for SSTL, HSTL I/O Standards.
	$V_{X\ (AC)}$	AC differential Input cross point Voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Referenced Documents

This chapter references the following documents:

- *AN 366: Understanding I/O Output Timing for Altera Devices*
- *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *PowerPlay Early Power Estimator User Guide for Cyclone III FPGAs*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*

Document Revision History

Table 1–111 shows the revision history for this chapter.

Table 1–111. Document Revision History (Part 1 of 3)

Date and Document Version	Changes Made	Summary of Changes
October 2008 v2.2	■ Updated chapter to new template ■ Updated Table 1–1, Table 1–3, and Table 1–18 ■ Added *(Note 7)* to Table 1–3 ■ Added the "OCT Calibration Timing Specification" section ■ Updated "Glossary" section	—
July 2008 v2.1	■ Updated Table 1–38 ■ Added BLVDS information (I/O standard) into Table 1–39, Table 1–40, Table 1–41, Table 1–42 ■ Updated Table 1–43, Table 1–46, Table 1–47, Table 1–48, Table 1–49, Table 1–50, Table 1–51, Table 1–52, Table 1–53, Table 1–54, Table 1–55, Table 1–56, Table 1–57, Table 1–58, Table 1–59, Table 1–60, Table 1–61, Table 1–62, Table 1–63, Table 1–68, Table 1–69, Table 1–74, Table 1–75, Table 1–80, Table 1–81, Table 1–86, Table 1–87, Table 1–92, Table 1–93, Table 1–94, Table 1–95, Table 1–96, Table 1–97, Table 1–98, Table 1–99	—

Table 1–111. Document Revision History (Part 2 of 3)

Date and Document Version	Changes Made	Summary of Changes
May 2008 v2.0	■ Updated "Operating Conditions" section and included information on automotive device ■ Updated Table 1–3, Table 1–6, and Table 1–7, and added automotive information ■ Under "Pin Capacitance" section, updated Table 1–9 and Table 1–10 ■ Added new "Schmitt Trigger Input" section with Table 1–12 ■ Under "I/O Standard Specifications" section, updated Table 1–13, 1–12 and 1–12 ■ Under "Switching Characteristics" section, updated Table 1–19, 1–15, 1–16, 1–16, 1–18, 1–19, 1–19, 1–20, 1–21, 1–22, 1–23, 1–23, 1–23, 1–24, and 1–25 ■ Updated Figure 1–5 and 1–29 ■ Deleted previous Table 1-35 "DDIO Outputs Half-Period Jitter" ■ Under "I/O Timing" section, updated Table 1–38, 1–29, 1–32, 1–33, 1–39, and 1–40 ■ Under "Typical Design Performance" section updated Table 1–46 through 1–145	Updated the non-I/O Timing and I/O Timing sections and added automotive information.
December 2007 v1.5	■ Under "Core Performance Specifications", updated Tables 1-18 and 1-19 ■ Under "Preliminary, Correlated, and Final Timing", updated Table 1-37 ■ Under "Typical Design Performance", updated Tables 1-45, 1-46, 1-51, 1-52, 1-57, 1-58, Tables 1-63 through 1-68. 1-69, 1-70, 1-75, 1-76, 1-81, 1-82, Tables 1-87 through 1-92, Tables 1-99, 1-100, 1-107, and 1-108	Updated I/O timing numbers for EP3C25 and EP3C120 devices in conjunction with the Quartus II v7.2 SP1 release.
October 2007 v1.4	■ Updated the C_{VREFTB} value in Table 1-9 ■ Updated Table 1-21 ■ Under "High-Speed I/O Specification" section, updated Tables 1-25 through 1-30 ■ Updated Tables 1-31 through 1-38 ■ Added new Table 1-32 ■ Under "Maximum Input and Output Clock Toggle Rate" section, updated Tables 1-40 through 1-42 ■ Under "IOE Programmable Delay" section, updated Tables 1-43 through 1-44 ■ Under "User I/O Pin Timing Parameters" section, updated Tables 1-45 through 1-92 ■ Under "Dedicated Clock Pin Timing Parameters" section, updated Tables 1-93 through 1-108	Updated I/O Timing section and other parts of the document as well.

Table 1–111. Document Revision History (Part 3 of 3)

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.3	■ Updated Table 1-1 with V_{ESDHBM} and V_{ESDCDM} information ■ Updated R_{CONF_PD} information in Tables 1-10 ■ Added *Note (3)* to Table 1-12 ■ Updated t_{DLOCK} information in Table 1-19 ■ Updated Table 1-43 and Table 1-44 ■ Added "Referenced Documents" section	—
June 2007 v1.2	Updated Cyclone III graphic in cover page.	Revised Cover
May 2007 v1.1	■ Corrected current unit in Tables 1-1, 1-12, and 1-14 ■ Added *Note (3)* to Table 1-3 ■ Updated Table 1-4 with I_{CCINT0}, I_{CCA0}, I_{CCD_PLL0}, and I_{CCIO0} information ■ Updated Table 1-9 and added *Note (2)* ■ Updated Table 1-19 ■ Updated Table 1-22 and added *Note (1)* ■ Changed I/O standard from 1.5-V LVTTL/LVCMOS and 1.2-V LVTTL/LVCMOS to 1.5-V LVCMOS and 1.2-V LVCMOS in Tables 1-41, 1-42, 1-43, 1-44, and 1-45 ■ Updated Table 1-43 with changes to LVPEC and LVDS and added *Note (5)* ■ Updated Tables 1-46, 1-47, Tables 1-54 through 1-95, and Tables 1-98 through 1-111 ■ Removed speed grade –6 from Tables 1-90 through 1-95, and from Tables 1-110 through 1-111 ■ Added a waveform (Receiver Input Waveform) in glossary under letter "R" (Table 1-112)	Updated I/O Timing section and other parts of the document as well.
March 2007 v1.0	Initial release.	—

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support
www.altera.com/support

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