

This chapter describes the electrical and switching characteristics for Cyclone® IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

This chapter includes the following sections:


- “Operating Conditions” on page 1–1
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- “Switching Characteristics” on page 1–16
- “I/O Timing” on page 1–38
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Operating Conditions

When Cyclone IV devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone IV devices, you must consider the operating requirements described in this chapter.

Cyclone IV devices are offered in commercial, industrial, extended industrial and, automotive grades. Cyclone IV E devices offer –6 (fastest), –7, –8, –8L, and –9L speed grades for commercial devices, –8L speed grades for industrial devices, and –7 speed grade for extended industrial and automotive devices. Cyclone IV GX devices offer –6 (fastest), –7, and –8 speed grades for commercial devices and –7 speed grade for industrial devices.

 For more information about the supported speed grades for respective Cyclone IV devices, refer to the *Cyclone IV FPGA Device Family Overview* chapter.

 Cyclone IV E devices are offered in core voltages of 1.0 and 1.2 V. Cyclone IV E devices with a core voltage of 1.0 V have an ‘L’ prefix attached to the speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a “C” prefix, industrial with an “I” prefix, and automotive with an “A” prefix. Therefore, commercial devices are indicated as C6, C7, C8, C8L, or C9L per respective speed grade. Industrial devices are indicated as I7, I8, or I8L. Automotive devices are indicated as A7.

 Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1-1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1-1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Table 1-1. Absolute Maximum Ratings for Cyclone IV Devices ⁽¹⁾—Preliminary

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---|------|-------|------|
| V_{CCINT} | Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply | -0.5 | 1.8 | V |
| V_{CCA} | Phase-locked loop (PLL) analog power supply | -0.5 | 3.75 | V |
| V_{CCD_PLL} | PLL digital power supply | -0.5 | 1.8 | V |
| V_{CCIO} | I/O banks power supply | -0.5 | 3.9 | V |
| V_{CC_CLKIN} | Differential clock input pins power supply | -0.5 | 3.9 | V |
| V_{CCH_GXB} | Transceiver output buffer power supply | -0.5 | 2.625 | V |
| V_{CCA_GXB} | Transceiver physical medium attachment (PMA) and auxiliary power supply | -0.5 | 2.625 | V |
| V_{CCL_GXB} | Transceiver PMA and auxiliary power supply | -0.5 | 1.8 | V |
| V_I | DC input voltage | -0.5 | 3.95 | V |
| I_{OUT} | DC output current, per pin | -25 | 40 | mA |
| T_{STG} | Storage temperature | -65 | 150 | °C |
| T_J | Operating junction temperature | -40 | 125 | °C |

Note to Table 1-1:

- (1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1-2 and undershoot to -2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1-2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.


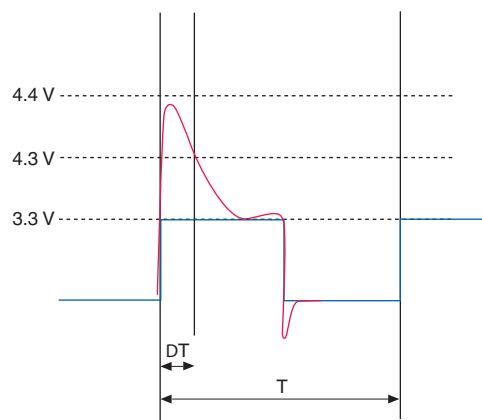
 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1-2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

| Symbol | Parameter | Condition (V) | Overshoot Duration as % of High Time | Unit |
|--------|------------------|---------------|--------------------------------------|------|
| V_i | AC Input Voltage | $V_i = 4.20$ | 100 | % |
| | | $V_i = 4.25$ | 98 | % |
| | | $V_i = 4.30$ | 65 | % |
| | | $V_i = 4.35$ | 43 | % |
| | | $V_i = 4.40$ | 29 | % |
| | | $V_i = 4.45$ | 20 | % |
| | | $V_i = 4.50$ | 13 | % |
| | | $V_i = 4.55$ | 9 | % |
| | | $V_i = 4.60$ | 6 | % |

Figure 1-1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1-2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1-1. Cyclone IV Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1-3 and Table 1-4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1-3. Recommended Operating Conditions for Cyclone IV E Devices ^{(1), (2)} (Part 1 of 2)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|--|------------|-----|------------|------|
| V_{CCINT} ⁽³⁾ | Supply voltage for internal logic, 1.2-V operation | — | 1.15 | 1.2 | 1.25 | V |
| | Supply voltage for internal logic, 1.0-V operation | — | 0.97 | 1.0 | 1.03 | V |
| V_{CCIO} ^{(3), (4)} | Supply voltage for output buffers, 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | Supply voltage for output buffers, 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | Supply voltage for output buffers, 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | Supply voltage for output buffers, 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| V_{CCA} ⁽³⁾ | Supply (analog) voltage for PLL regulator | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCD_PLL} ⁽³⁾ | Supply (digital) voltage for PLL, 1.2-V operation | — | 1.15 | 1.2 | 1.25 | V |
| | Supply (digital) voltage for PLL, 1.0-V operation | — | 0.97 | 1.0 | 1.03 | V |
| V_I | Input voltage | — | -0.5 | — | 3.6 | V |
| V_O | Output voltage | — | 0 | — | V_{CCIO} | V |
| T_J | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | -40 | — | 100 | °C |
| | | For extended temperature ⁽⁵⁾ | -40 | — | 125 | °C |
| | | For automotive use | -40 | — | 125 | °C |
| t_{RAMP} | Power supply ramp time | Standard power-on reset (POR) ⁽⁶⁾ | 50 μ s | — | 50 ms | — |
| | | Fast POR ⁽⁷⁾ | 50 μ s | — | 3 ms | — |

Table 1-3. Recommended Operating Conditions for Cyclone IV E Devices ^{(1), (2)} (Part 2 of 2)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|------------|-----|-----|-----|------|
| I_{Diode} | Magnitude of DC current across PCI-clamp diode when enable | — | — | — | 10 | mA |

Notes to Table 1-3:

- (1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.
- (2) V_{CCIO} for all I/O banks must be powered up during device operation. All v_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (3) V_{CC} must rise monotonically.
- (4) V_{CCIO} powers all input buffers.
- (5) The I7 devices support extended operating junction temperature up to 125°C (usual range is -40°C to 100°C). When using I7 devices at the extended junction temperature ranging from -40°C to 125°C, select C8 as the target device when designing in the Quartus® II software. The I7 devices meet all C8 timing specifications when I7 devices operate beyond 100°C and up to 125°C.
- (6) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.
- (7) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)—Preliminary

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|------------|-------|-----|-------|------|
| V_{CCINT} ⁽³⁾ | Core voltage, PCIe hard IP block, and transceiver PCS power supply | — | 1.16 | 1.2 | 1.24 | V |
| V_{CCA} ^{(1), (3)} | PLL analog power supply | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCD_PLL} ⁽²⁾ | PLL digital power supply | — | 1.16 | 1.2 | 1.24 | V |
| V_{CCIO} ^{(3), (4)} | I/O banks power supply for 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | I/O banks power supply for 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | I/O banks power supply for 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | I/O banks power supply for 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | I/O banks power supply for 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | I/O banks power supply for 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| V_{CC_CLKIN} ^{(3), (5), (6)} | Differential clock input pins power supply for 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | Differential clock input pins power supply for 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | Differential clock input pins power supply for 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | Differential clock input pins power supply for 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | Differential clock input pins power supply for 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | Differential clock input pins power supply for 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)—Preliminary

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|--|------------|-----|------------|------|
| V_{CCH_GXB} | Transceiver output buffer power supply | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCA_GXB} | Transceiver PMA and auxiliary power supply | — | 2.375 | 2.5 | 2.625 | V |
| V_{CCL_GXB} | Transceiver PMA and auxiliary power supply | — | 1.16 | 1.2 | 1.24 | V |
| V_I | DC input voltage | — | -0.5 | — | 3.6 | V |
| V_O | DC output voltage | — | 0 | — | V_{CCIO} | V |
| T_J | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | -40 | — | 100 | °C |
| t_{RAMP} | Power supply ramp time | Standard power-on reset (POR) ⁽⁷⁾ | 50 μ s | — | 50 ms | — |
| | | Fast POR ⁽⁸⁾ | 50 μ s | — | 3 ms | — |
| I_{Diode} | Magnitude of DC current across PCI-clamp diode when enabled | — | — | — | 10 | mA |

Notes to Table 1-4:

- All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- Power supplies must rise monotonically.
- V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- You must set V_{CC_CLKIN} to 2.5 V if you use $CLKIN$ as a high-speed serial interface (HSSI) $refclk$ or as a $DIFFCLK$ input.
- The $CLKIN$ pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

| Symbol | Parameter | Passing Voltage | Unit |
|--------------|--|-----------------|------|
| V_{ESDHBM} | ESD voltage using the HBM (GPIOs) ⁽¹⁾ | ± 2000 | V |
| | ESD using the HBM (HSSI I/Os) ⁽²⁾ | ± 1000 | V |
| V_{ESDCDM} | ESD using the CDM (GPIOs) | ± 500 | V |
| | ESD using the CDM (HSSI I/Os) ⁽²⁾ | ± 250 | V |

Notes to Table 1-5:

- The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is $\pm 1000V$.
- This value is applicable only to Cyclone IV GX devices.

DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1-6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1-6. I/O Pin Leakage Current for Cyclone IV Devices (1), (2)

| Symbol | Parameter | Conditions | Device | Min | Typ | Max | Unit |
|----------|-----------------------------------|--|--------|-----|-----|-----|---------------|
| I_I | Input pin leakage current | $V_I = 0\text{ V to }V_{CCIO\text{MAX}}$ | — | -10 | — | 10 | μA |
| I_{OZ} | Tristated I/O pin leakage current | $V_O = 0\text{ V to }V_{CCIO\text{MAX}}$ | — | -10 | — | 10 | μA |

Notes to Table 1-6:

- (1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) The 10 μA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-7 lists bus hold specifications for Cyclone IV devices.

Table 1-7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2) (1)—Preliminary

| Parameter | Condition | V_{CCIO} (V) | | | | | | | | | | | | Unit |
|-----------------------------------|----------------------------------|----------------|------|-----|------|-----|------|-----|------|-----|------|-----|------|---------------|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | μA |
| Bus hold high, sustaining current | $V_{IN} < V_{IL}$ (minimum) | -8 | — | -12 | — | -30 | — | -50 | — | -70 | — | -70 | — | μA |
| Bus hold low, overdrive current | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | μA |
| Bus hold high, overdrive current | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | -125 | — | -175 | — | -200 | — | -300 | — | -500 | — | -500 | μA |

Table 1-7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2) ⁽¹⁾—Preliminary

| Parameter | Condition | V_{CCIO} (V) | | | | | | | | | | | | Unit |
|---------------------|-----------|----------------|-----|-------|-------|------|------|-----|-----|-----|-----|-----|-----|------|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold trip point | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

Note to Table 1-7:

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

OCT Specifications

Table 1-8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

Table 1-8. Series OCT Without Calibration Specifications for Cyclone IV Devices—Preliminary

| Description | V_{CCIO} (V) | Resistance Tolerance | | Unit |
|--------------------------------|----------------|----------------------|---|------|
| | | Commercial Maximum | Industrial, Extended industrial, and Automotive Maximum | |
| Series OCT without calibration | 3.0 | ±30 | ±40 | % |
| | 2.5 | ±30 | ±40 | % |
| | 1.8 | ±40 | ±50 | % |
| | 1.5 | ±50 | ±50 | % |
| | 1.2 | ±50 | ±50 | % |

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1-9 lists the OCT calibration accuracy at device power-up.

Table 1-9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices—Preliminary

| Description | V_{CCIO} (V) | Calibration Accuracy | | Unit |
|--|----------------|----------------------|---|------|
| | | Commercial Maximum | Industrial, Extended industrial, and Automotive Maximum | |
| Series OCT with calibration at device power-up | 3.0 | ±10 | ±10 | % |
| | 2.5 | ±10 | ±10 | % |
| | 1.8 | ±10 | ±10 | % |
| | 1.5 | ±10 | ±10 | % |
| | 1.2 | ±10 | ±10 | % |

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use [Table 1-10](#) and [Equation 1-1](#) to determine the final OCT resistance considering the variations after calibration at device power-up. [Table 1-10](#) lists the change percentage of the OCT resistance with voltage and temperature.

Table 1-10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices—Preliminary

| Nominal Voltage | dR/dT (%/°C) | dR/dV (%/mV) |
|-----------------|--------------|--------------|
| 3.0 | 0.262 | -0.026 |
| 2.5 | 0.234 | -0.039 |
| 1.8 | 0.219 | -0.086 |
| 1.5 | 0.199 | -0.136 |
| 1.2 | 0.161 | -0.288 |

Equation 1-1. Final OCT Resistance (1), (2), (3), (4), (5), (6)

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV \text{ — (7)}$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \text{ — (8)}$$

$$\text{For } \Delta R_x < 0; MF_x = 1 / (|\Delta R_x|/100 + 1) \text{ — (9)}$$

$$\text{For } \Delta R_x > 0; MF_x = \Delta R_x/100 + 1 \text{ — (10)}$$

$$MF = MF_V \times MF_T \text{ — (11)}$$

$$R_{\text{final}} = R_{\text{initial}} \times MF \text{ — (12)}$$

Notes to Equation 1-1:

- (1) T_2 is the final temperature.
- (2) T_1 is the initial temperature.
- (3) MF is multiplication factor.
- (4) R_{final} is final resistance.
- (5) R_{initial} is initial resistance.
- (6) Subscript x refers to both v and T .
- (7) ΔR_V is a variation of resistance with voltage.
- (8) ΔR_T is a variation of resistance with temperature.
- (9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- (10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- (11) V_2 is final voltage.
- (12) V_1 is the initial voltage.

Example 1-1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1-1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because ΔR_V is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = 55.71 \Omega$$

Pin Capacitance

Table 1-11 lists the pin capacitance for Cyclone IV devices.

Table 1-11. Pin Capacitance for Cyclone IV Devices —Preliminary

| Symbol | Parameter | Typical – Quad Flat Pack (QFP) | Typical – Quad Flat No Leads (QFN) | Typical – Fineline BGA (FBGA) | Unit |
|---------------------|---|---|---|--|------|
| C_{IOTB} | Input capacitance on top and bottom I/O pins | 7 | 7 | 6 | pF |
| C_{IOLR} | Input capacitance on right I/O pins | 7 | 7 | 5 | pF |
| $C_{LVDSLRL}$ | Input capacitance on right I/O pins with dedicated LVDS output | 8 | 8 | 7 | pF |
| C_{VREFLR} (1) | Input capacitance on right dual-purpose V_{REF} pin when used as V_{REF} or user I/O pin | 21 | 21 | 21 | pF |
| C_{VREFTB} (1) | Input capacitance on top and bottom dual-purpose V_{REF} pin when used as V_{REF} or user I/O pin | 23 (2) | 23 | 23 | pF |
| C_{CLKTB} | Input capacitance on top and bottom dedicated clock input pins | 7 | 7 | 6 | pF |
| C_{CLKLR} | Input capacitance on right dedicated clock input pins | 6 | 6 | 5 | pF |

Notes to Table 1-11:

- (1) When you use the V_{REF} pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.
- (2) C_{VREFTB} for the EP4CE22 device is 30 pF.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1-12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1-12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices ⁽¹⁾—Preliminary

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--|--|-----|-----|-----|------|
| R _{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option | V _{CCIO} = 3.3 V ± 5% ^{(2), (3)} | 7 | 25 | 41 | kΩ |
| | | V _{CCIO} = 3.0 V ± 5% ^{(2), (3)} | 7 | 28 | 47 | kΩ |
| | | V _{CCIO} = 2.5 V ± 5% ^{(2), (3)} | 8 | 35 | 61 | kΩ |
| | | V _{CCIO} = 1.8 V ± 5% ^{(2), (3)} | 10 | 57 | 108 | kΩ |
| | | V _{CCIO} = 1.5 V ± 5% ^{(2), (3)} | 13 | 82 | 163 | kΩ |
| | | V _{CCIO} = 1.2 V ± 5% ^{(2), (3)} | 19 | 143 | 351 | kΩ |
| R _{PD} | Value of the I/O pin pull-down resistor before and during configuration | V _{CCIO} = 3.3 V ± 5% ⁽⁴⁾ | 6 | 19 | 30 | kΩ |
| | | V _{CCIO} = 3.0 V ± 5% ⁽⁴⁾ | 6 | 22 | 36 | kΩ |
| | | V _{CCIO} = 2.5 V ± 5% ⁽⁴⁾ | 6 | 25 | 43 | kΩ |
| | | V _{CCIO} = 1.8 V ± 5% ⁽⁴⁾ | 7 | 35 | 71 | kΩ |
| | | V _{CCIO} = 1.5 V ± 5% ⁽⁴⁾ | 8 | 50 | 112 | kΩ |

Notes to Table 1-12:

- All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- R_{PU} = (V_{CCIO} - V_I)/I_{R_PU}
 Minimum condition: -40°C; V_{CCIO} = V_{CC} + 5%, V_I = V_{CC} + 5% - 50 mV;
 Typical condition: 25°C; V_{CCIO} = V_{CC}, V_I = 0 V;
 Maximum condition: 100°C; V_{CCIO} = V_{CC} - 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.
- R_{PD} = V_I/I_{R_PD}
 Minimum condition: -40°C; V_{CCIO} = V_{CC} + 5%, V_I = 50 mV;
 Typical condition: 25°C; V_{CCIO} = V_{CC}, V_I = V_{CC} - 5%;
 Maximum condition: 100°C; V_{CCIO} = V_{CC} - 5%, V_I = V_{CC} - 5%; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 1-13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1-13. Hot-Socketing Specifications for Cyclone IV Devices —Preliminary

| Symbol | Parameter | Maximum |
|-------------------------|-----------------------------------|---------------------|
| I _{IOPIN(DC)} | DC current per I/O pin | 300 μA |
| I _{IOPIN(AC)} | AC current per I/O pin | 8 mA ⁽¹⁾ |
| I _{XCVRTX(DC)} | DC current per transceiver TX pin | 100 mA |
| I _{XCVRRX(DC)} | DC current per transceiver RX pin | 50 mA |

Note to Table 1-13:

- The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.



During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Cyclone IV devices.

Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices—Preliminary

| Symbol | Parameter | Conditions (V) | Minimum | Unit |
|---------------|--------------------------------------|------------------|---------|------|
| $V_{SCHMITT}$ | Hysteresis for Schmitt trigger input | $V_{CCIO} = 3.3$ | 200 | mV |
| | | $V_{CCIO} = 2.5$ | 200 | mV |
| | | $V_{CCIO} = 1.8$ | 140 | mV |
| | | $V_{CCIO} = 1.5$ | 110 | mV |

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices (1), (2) —Preliminary

| I/O Standard | V_{CCIO} (V) | | | V_{IL} (V) | | V_{IH} (V) | | V_{OL} (V) | V_{OH} (V) | I_{OL} (mA) | I_{OH} (mA) |
|------------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|---------------|---------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTTL (3) | 3.135 | 3.3 | 3.465 | — | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3-V LVCMOS (3) | 3.135 | 3.3 | 3.465 | — | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 2 | –2 |
| 3.0-V LVTTTL (3) | 2.85 | 3.0 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO} + 0.3$ | 0.45 | 2.4 | 4 | –4 |
| 3.0-V LVCMOS (3) | 2.85 | 3.0 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO} + 0.3$ | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | –0.1 |
| 2.5 V (3) | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | $V_{CCIO} + 0.3$ | 0.4 | 2.0 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | 2.25 | 0.45 | $V_{CCIO} - 0.45$ | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | –2 |
| 3.0-V PCI | 2.85 | 3.0 | 3.15 | — | $0.3 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3.0 | 3.15 | — | $0.35 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | 1.5 | –0.5 |

Notes to Table 1–15:

- (1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to “Glossary” on page 1–38.
- (2) AC load $CL = 10$ pF
- (3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O standards, refer to AN 447: *Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems*.

Table 1-16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices⁽¹⁾
—Preliminary

| I/O Standard | V _{CCIO} (V) | | | V _{REF} (V) | | | V _{TT} (V) ⁽²⁾ | | |
|---------------------|-----------------------|-----|-------|---|--|---|------------------------------------|-------------------------|-------------------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 1.19 | 1.25 | 1.31 | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 x V _{CCIO} ⁽³⁾ | 0.5 x V _{CCIO} ⁽³⁾ | 0.52 x V _{CCIO} ⁽³⁾ | — | 0.5 x V _{CCIO} | — |
| | | | | 0.47 x V _{CCIO} ⁽⁴⁾ | 0.5 x V _{CCIO} ⁽⁴⁾ | 0.53 x V _{CCIO} ⁽⁴⁾ | | | |

Notes to Table 1-16:

- (1) For an explanation of terms used in Table 1-16, refer to "Glossary" on page 1-38.
- (2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
- (3) Value shown refers to DC input reference voltage, V_{REF(DC)}.
- (4) Value shown refers to AC input reference voltage, V_{REF(AC)}.

Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices—Preliminary

| I/O Standard | V _{IL(DC)} (V) | | V _{IH(DC)} (V) | | V _{IL(AC)} (V) | | V _{IH(AC)} (V) | | V _{OL} (V) | V _{OH} (V) | I _{OL} (mA) | I _{OH} (mA) |
|------------------|-------------------------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------------|-------------------------|--------------------------|--------------------------|--------------------------|----------------------|----------------------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Max | Min | | |
| SSTL-2 Class I | — | V _{REF} - 0.18 | V _{REF} + 0.18 | — | — | V _{REF} - 0.35 | V _{REF} + 0.35 | — | V _{TT} - 0.57 | V _{TT} + 0.57 | 8.1 | -8.1 |
| SSTL-2 Class II | — | V _{REF} - 0.18 | V _{REF} + 0.18 | — | — | V _{REF} - 0.35 | V _{REF} + 0.35 | — | V _{TT} - 0.76 | V _{TT} + 0.76 | 16.4 | -16.4 |
| SSTL-18 Class I | — | V _{REF} - 0.125 | V _{REF} + 0.125 | — | — | V _{REF} - 0.25 | V _{REF} + 0.25 | — | V _{TT} - 0.475 | V _{TT} + 0.475 | 6.7 | -6.7 |
| SSTL-18 Class II | — | V _{REF} - 0.125 | V _{REF} + 0.125 | — | — | V _{REF} - 0.25 | V _{REF} + 0.25 | — | 0.28 | V _{CCIO} - 0.28 | 13.4 | -13.4 |
| HSTL-18 Class I | — | V _{REF} - 0.1 | V _{REF} + 0.1 | — | — | V _{REF} - 0.2 | V _{REF} + 0.2 | — | 0.4 | V _{CCIO} - 0.4 | 8 | -8 |
| HSTL-18 Class II | — | V _{REF} - 0.1 | V _{REF} + 0.1 | — | — | V _{REF} - 0.2 | V _{REF} + 0.2 | — | 0.4 | V _{CCIO} - 0.4 | 16 | -16 |
| HSTL-15 Class I | — | V _{REF} - 0.1 | V _{REF} + 0.1 | — | — | V _{REF} - 0.2 | V _{REF} + 0.2 | — | 0.4 | V _{CCIO} - 0.4 | 8 | -8 |
| HSTL-15 Class II | — | V _{REF} - 0.1 | V _{REF} + 0.1 | — | — | V _{REF} - 0.2 | V _{REF} + 0.2 | — | 0.4 | V _{CCIO} - 0.4 | 16 | -16 |
| HSTL-12 Class I | -0.15 | V _{REF} - 0.08 | V _{REF} + 0.08 | V _{CCIO} + 0.15 | -0.24 | V _{REF} - 0.15 | V _{REF} + 0.15 | V _{CCIO} + 0.24 | 0.25 x V _{CCIO} | 0.75 x V _{CCIO} | 8 | -8 |
| HSTL-12 Class II | -0.15 | V _{REF} - 0.08 | V _{REF} + 0.08 | V _{CCIO} + 0.15 | -0.24 | V _{REF} - 0.15 | V _{REF} + 0.15 | V _{CCIO} + 0.24 | 0.25 x V _{CCIO} | 0.75 x V _{CCIO} | 14 | -14 |


 For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1-18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾—Preliminary

| I/O Standard | V _{CCIO} (V) | | | V _{Swing(DC)} (V) | | V _{X(AC)} (V) | | | V _{Swing(AC)} (V) | | V _{Ox(AC)} (V) | | |
|------------------------|-----------------------|-----|-------|----------------------------|-------------------|------------------------------|-----|------------------------------|----------------------------|-------------------|------------------------------|-----|------------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.36 | V _{CCIO} | V _{CCIO} /2 - 0.2 | — | V _{CCIO} /2 + 0.2 | 0.7 | V _{CCIO} | V _{CCIO} /2 - 0.125 | — | V _{CCIO} /2 + 0.125 |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.90 | 0.25 | V _{CCIO} | V _{CCIO} /2 - 0.175 | — | V _{CCIO} /2 + 0.175 | 0.5 | V _{CCIO} | V _{CCIO} /2 - 0.125 | — | V _{CCIO} /2 + 0.125 |

Note to Table 1-18:

(1) Differential SSTL requires a V_{REF} input.

Table 1-19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾—Preliminary

| I/O Standard | V _{CCIO} (V) | | | V _{DIF(DC)} (V) | | V _{X(AC)} (V) | | | V _{CM(DC)} (V) | | | V _{DIF(AC)} (V) | |
|------------------------|-----------------------|-----|-------|--------------------------|-------------------|--------------------------|-----|--------------------------|--------------------------|-----|--------------------------|--------------------------|--------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.85 | — | 0.95 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | V _{CCIO} | 0.48 x V _{CCIO} | — | 0.52 x V _{CCIO} | 0.48 x V _{CCIO} | — | 0.52 x V _{CCIO} | 0.3 | 0.48 x V _{CCIO} |

Note to Table 1-19:

(1) Differential HSTL requires a V_{REF} input.

Table 1-20. Differential I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾ (Part 1 of 2)—Preliminary

| I/O Standard | V _{CCIO} (V) | | | V _{ID} (mV) | | V _{ICM} (V) ⁽²⁾ | | | V _{OD} (mV) ⁽³⁾ | | | V _{OS} (V) ⁽³⁾ | | |
|--|-----------------------|-----|-------|----------------------|-----|-------------------------------------|--|------|-------------------------------------|-----|-----|------------------------------------|------|-------|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVPECL (Row I/Os) ⁽⁶⁾ | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | D _{MAX} ≤ 500 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps ≤ D _{MAX} ≤ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | D _{MAX} > 700 Mbps | 1.55 | | | | | | |
| LVPECL (Column I/Os) ⁽⁶⁾ | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | D _{MAX} ≤ 500 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps ≤ D _{MAX} ≤ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | D _{MAX} > 700 Mbps | 1.55 | | | | | | |
| LVDS (Row I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | D _{MAX} ≤ 500 Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps ≤ D _{MAX} ≤ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | D _{MAX} > 700 Mbps | 1.55 | | | | | | |

Table 1-20. Differential I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾ (Part 2 of 2)—Preliminary

| I/O Standard | V _{CCIO} (V) | | | V _{ID} (mV) | | V _{ICM} (V) ⁽²⁾ | | | V _{OD} (mV) ⁽³⁾ | | | V _{OS} (V) ⁽³⁾ | | | |
|---|-----------------------|-----|-------|----------------------|-----|-------------------------------------|---|------|-------------------------------------|-----|-----|------------------------------------|------|-------|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max | |
| LVDS (Column I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq 500$ Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 | |
| | | | | | | 0.55 | $500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps | 1.80 | | | | | | | |
| | | | | | | 1.05 | $D_{MAX} > 700$ Mbps | 1.55 | | | | | | | |
| BLVDS (Row I/Os) ⁽⁴⁾ | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| BLVDS (Column I/Os) ⁽⁴⁾ | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| mini-LVDS (Row I/Os) ⁽⁵⁾ | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 | |
| mini-LVDS (Column I/Os) ⁽⁵⁾ | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 | |
| RSDS [®] (Row I/Os) ⁽⁵⁾ | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 | |
| RSDS (Column I/Os) ⁽⁵⁾ | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 | |
| PPDS (Row I/Os) ⁽⁵⁾ | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 | |
| PPDS (Column I/Os) ⁽⁵⁾ | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 | |

Notes to Table 1-20:


- (1) For an explanation of terms used in Table 1-20, refer to “Glossary” on page 1-38.
- (2) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
- (3) R_L range: 90 ≤ R_L ≤ 110 Ω.
- (4) There are no fixed V_{IN}, V_{OD}, and V_{OS} specifications for BLVDS. They depend on the system topology.
- (5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.
- (6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

Power Consumption

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Quartus[®] II PowerPlay power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

 For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Cyclone IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The upper-right hand corner of these tables show the designation as “Preliminary”.
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

Table 1-21 lists the Cyclone IV GX transceiver specifications.

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)—Preliminary

| Symbol/ Description | Conditions | C6 | | | C7, 17 | | | C8 | | | Unit |
|--|---|--------------------------------|------------|--------|--------------------------------|------------|--------|--------------------------------|------------|--------|--------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | | | | |
| Supported I/O Standards | 1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL | | | | | | | | | | |
| Input frequency from REFCLK input pins | — | 50 | — | 156.25 | 50 | — | 156.25 | 50 | — | 156.25 | MHz |
| Spread-spectrum modulating clock frequency | Physical interface for PCI Express (PIPE) mode | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PIPE mode | — | 0 to -0.5% | — | — | 0 to -0.5% | — | — | 0 to -0.5% | — | — |
| V _{ICM} (AC coupled) | | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | mV |
| V _{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise ⁽¹⁾ | Frequency offset = 1 MHz – 8 MHz | — | — | -123 | — | — | -123 | — | — | -123 | dBc/Hz |
| Transmitter REFCLK Total Jitter ⁽¹⁾ | | — | — | 42.3 | — | — | 42.3 | — | — | 42.3 | ps |
| R _{ref} | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |
| Transceiver Clock | | | | | | | | | | | |
| cal_blk_clk clock frequency | — | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | MHz |
| fixedclk clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | — | 125 | — | MHz |
| reconfig_clk clock frequency | Dynamic reconfiguration clock frequency | 2.5/ 37.5 ⁽²⁾ | — | 50 | 2.5/ 37.5 ⁽²⁾ | — | 50 | 2.5/ 37.5 ⁽²⁾ | — | 50 | MHz |
| Delta time between reconfig_clk | — | — | — | 2 | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down pulse width | — | — | 1 | — | — | 1 | — | — | 1 | — | μs |
| Receiver | | | | | | | | | | | |
| Supported I/O Standards | 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS | | | | | | | | | | |

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)—Preliminary

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|--|--|-------------------------------------|----------------|---|--------|----------------|---|------|----------------|---|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Data rate (F324 and smaller package) | — | 600 | — | 2500 | 600 | — | 2500 | 600 | — | 2500 | Mbps |
| Data rate (F484 and larger package) | — | 600 | — | 3125 | 600 | — | 3125 | 600 | — | 2500 | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽³⁾ | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Operational V_{MAX} for a receiver pin | — | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | V |
| Absolute V_{MIN} for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage V_{ID} (diff p-p) | $V_{ICM} = 0.82$ V setting, Data Rate = 600 Mbps to 3.125 Gbps | 0.1 | — | 2.7 | 0.1 | — | 2.7 | 0.1 | — | 2.7 | V |
| V_{ICM} | $V_{ICM} = 0.82$ V setting | — | $820 \pm 10\%$ | — | — | $820 \pm 10\%$ | — | — | $820 \pm 10\%$ | — | mV |
| Differential on-chip termination resistors | 100- Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| | 150- Ω setting | — | 150 | — | — | 150 | — | — | 150 | — | Ω |
| Differential and common mode return loss | PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI | Compliant | | | | | | | | | — |
| Programmable ppm detector ⁽⁴⁾ | — | $\pm 62.5, 100, 125, 200, 250, 300$ | | | | | | | | | ppm |
| Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled) | — | — | — | ± 300 ⁽⁵⁾ , ± 350 ^{(6), (7)} | — | — | ± 300 ⁽⁵⁾ , ± 350 ^{(6), (7)} | — | — | ± 300 ⁽⁵⁾ , ± 350 ^{(6), (7)} | ppm |
| CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) ⁽⁸⁾ | — | — | — | 350 to -5350 ^{(7), (9)} | — | — | 350 to -5350 ^{(7), (9)} | — | — | 350 to -5350 ^{(7), (9)} | ppm |
| Run length | — | — | 80 | — | — | 80 | — | — | 80 | — | UI |
| Programmable equalization | No Equalization | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | dB |
| | Medium Low | — | — | 4.5 | — | — | 4.5 | — | — | 4.5 | dB |
| | Medium High | — | — | 5.5 | — | — | 5.5 | — | — | 5.5 | dB |
| | High | — | — | 7 | — | — | 7 | — | — | 7 | dB |
| Signal detect/loss threshold | PIPE mode | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | mV |
| t_{LTR} ⁽¹⁰⁾ | — | — | — | 75 | — | — | 75 | — | — | 75 | μ s |
| $t_{LTR-LTD_Manual}$ ⁽¹¹⁾ | — | 15 | — | — | 15 | — | — | 15 | — | — | μ s |
| t_{LTD} ⁽¹²⁾ | — | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | ns |

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)—Preliminary

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|--|---|-----------|-----|-------|--------|-----|-------|-----|-----|-------|---------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t_{LTD_Manual} ⁽¹³⁾ | — | — | — | 4000 | — | — | 4000 | — | — | 4000 | ns |
| t_{LTD_Auto} ⁽¹⁴⁾ | — | — | — | 4000 | — | — | 4000 | — | — | 4000 | ns |
| Receiver buffer and CDR offset cancellation time (per channel) | — | — | — | 17000 | — | — | 17000 | — | — | 17000 | reconfig_clk cycles |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| Transmitter | | | | | | | | | | | |
| Supported I/O Standards | 1.5 V PCML | | | | | | | | | | |
| Data rate (F324 and smaller package) | — | 600 | — | 2500 | 600 | — | 2500 | 600 | — | 2500 | Mbps |
| Data rate (F484 and larger package) | — | 600 | — | 3125 | 600 | — | 3125 | 600 | — | 2500 | Mbps |
| V_{OCM} | 0.65 V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Differential on-chip termination resistors | 100- Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| | 150- Ω setting | — | 150 | — | — | 150 | — | — | 150 | — | Ω |
| Differential and common mode return loss | PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA | Compliant | | | | | | | | | — |
| Rise time | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |
| Fall time | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |
| Intra-differential pair skew | — | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block skew | — | — | — | 120 | — | — | 120 | — | — | 120 | ps |

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)—Preliminary

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|--|------------|------------------------------------|-----|--------|--------|-----|--------|-----|-----|--------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| PLD-Transceiver Interface | | | | | | | | | | | |
| Interface speed (F324 and smaller package) | — | 25 | — | 125 | 25 | — | 125 | 25 | — | 125 | MHz |
| Interface speed (F484 and larger package) | — | 25 | — | 156.25 | 25 | — | 156.25 | 25 | — | 156.25 | MHz |
| Digital reset pulse width | — | Minimum is 2 parallel clock cycles | | | | | | | | | |

Notes to Table 1–21:

- (1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.
- (2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to ± 300 parts per million (ppm).
- (5) Supported for the N148, F169, and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than ± 300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ± 200 ppm.
- (10) Time taken until `p11_locked` goes high after `p11_powerdown` deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).
- (13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.
- (14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.

Figure 1-2 shows the lock time parameters in manual mode.


 LTD = lock-to-data. LTR = lock-to-reference.

Figure 1-2. Lock Time Parameters for Manual Mode

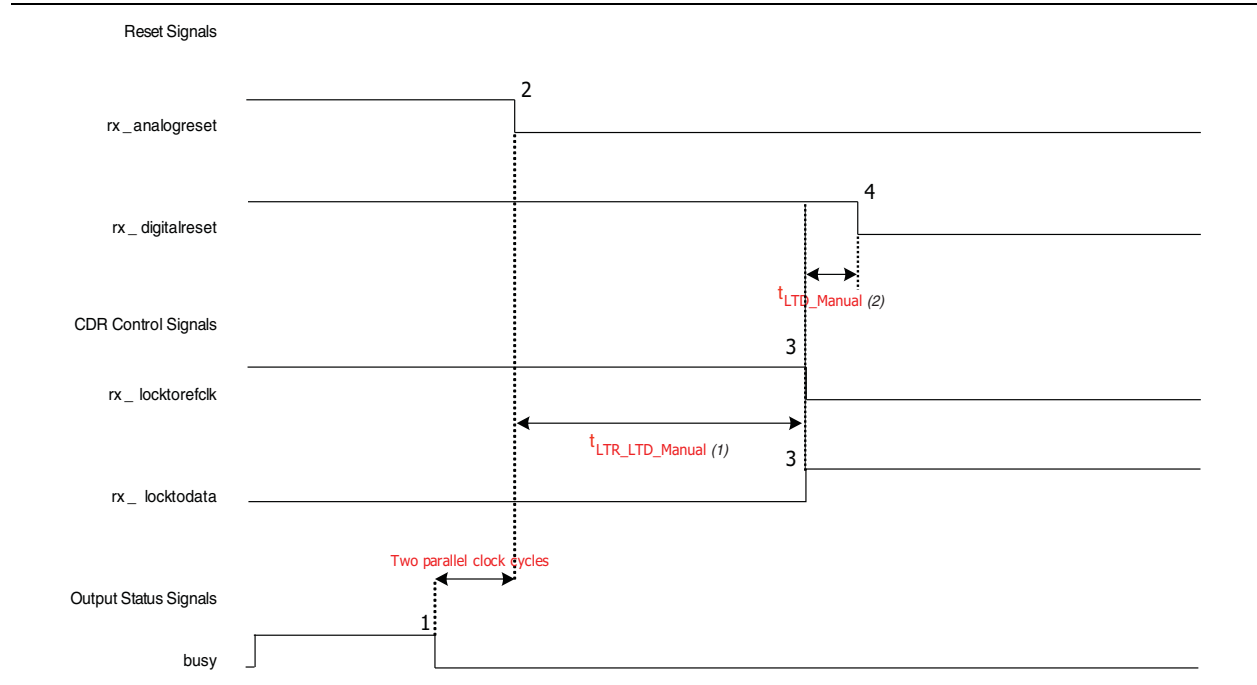


Figure 1-3 shows the lock time parameters in automatic mode.

Figure 1-3. Lock Time Parameters for Automatic Mode

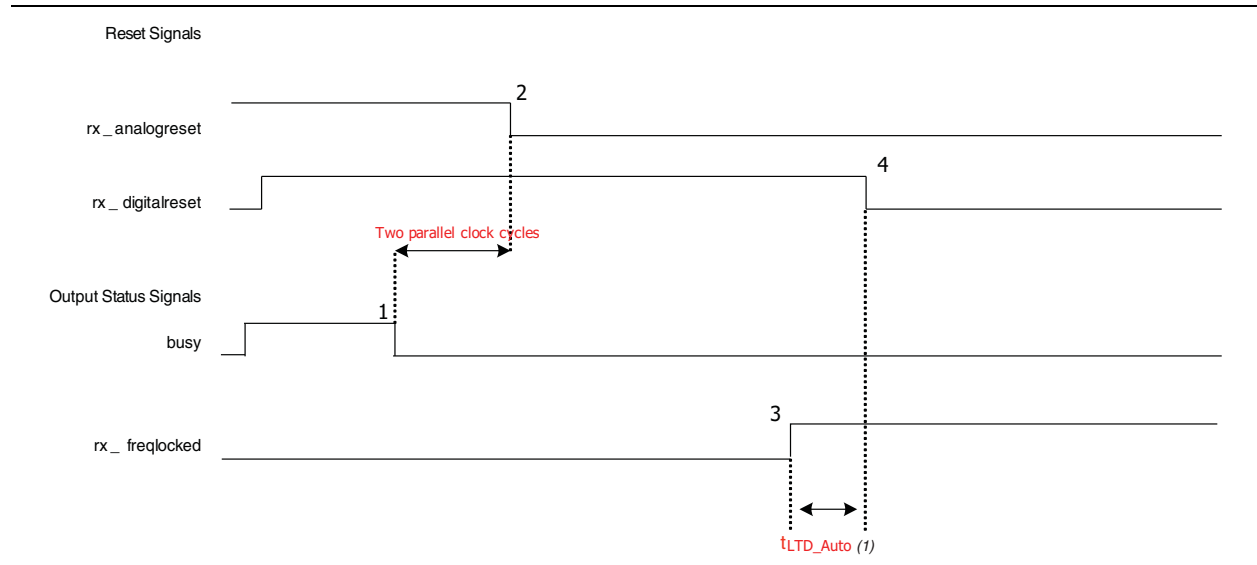


Figure 1-4 shows the differential receiver input waveform.

Figure 1-4. Receiver Input Waveform



Figure 1-5 shows the transmitter output waveform.

Figure 1-5. Transmitter Output Waveform—Preliminary

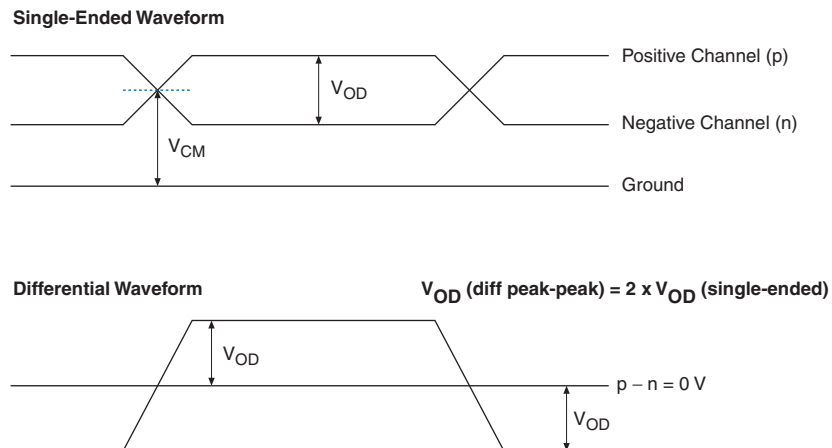


Table 1-22 lists the typical V_{OD} for Tx term that equals 100Ω .

Table 1-22. Typical V_{OD} Setting, Tx Term = 100Ω —Preliminary

| Symbol | V_{OD} Setting (mV) | | | | | |
|-----------------------|-----------------------|-----|-----|-------|------|------|
| | 1 | 2 | 3 | 4 (1) | 5 | 6 |
| V_{OD} Typical (mV) | 400 | 600 | 800 | 900 | 1000 | 1200 |

Note to Table 1-22:

(1) This setting is required for compliance with the PCIe protocol.

Table 1-23 lists the Cyclone IV GX transceiver block AC specifications.

Table 1-23. Transceiver Block AC Specification for Cyclone IV GX Devices ⁽¹⁾, ⁽²⁾—Preliminary

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|--------------------|--------|-----|-------|--------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| PCIe Transmit Jitter Generation ⁽³⁾ | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | — | — | 0.25 | — | — | 0.25 | — | — | 0.25 | UI |
| PCIe Receiver Jitter Tolerance ⁽³⁾ | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | > 0.6 | | | > 0.6 | | | > 0.6 | | | UI |
| GIGE Transmit Jitter Generation ⁽⁴⁾ | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| GIGE Receiver Jitter Tolerance ⁽⁴⁾ | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |

Notes to Table 1-23:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1-24 lists the clock tree specifications for Cyclone IV devices.

Table 1-24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)—Preliminary

| Device | Performance | | | | | | | | Unit |
|---------|-------------|-------|-----|--------------------|--------------------|-------|--------------------|-----|------|
| | C6 | C7 | C8 | C8L ⁽¹⁾ | C9L ⁽¹⁾ | I7 | I8L ⁽¹⁾ | A7 | |
| EP4CE6 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE10 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE15 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE22 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE30 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE40 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |

Table 1-24. Clock Tree Performance for Cyclone IV Devices (Part 2 of 2)—Preliminary

| Device | Performance | | | | | | | | Unit |
|-----------|-------------|-------|-----|--------------------|--------------------|-------|--------------------|----|------|
| | C6 | C7 | C8 | C8L ⁽¹⁾ | C9L ⁽¹⁾ | I7 | I8L ⁽¹⁾ | A7 | |
| EP4CE55 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | — | MHz |
| EP4CE75 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | — | MHz |
| EP4CE115 | — | 437.5 | 402 | 362 | 265 | 437.5 | 362 | — | MHz |
| EP4CGX15 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |
| EP4CGX22 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |
| EP4CGX30 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |
| EP4CGX50 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |
| EP4CGX75 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |
| EP4CGX110 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |
| EP4CGX150 | 500 | 437.5 | 402 | — | — | 437.5 | — | — | MHz |

Note to Table 1-24:

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

PLL Specifications

Table 1-25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C). For more information about the PLL block, refer to “Glossary” on page 1-38.

Table 1-25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 1 of 2)—Preliminary

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|-----|-----|-------|------|
| f_{IN} ⁽³⁾ | Input clock frequency (–6, –7, –8 speed grades) | 5 | — | 472.5 | MHz |
| | Input clock frequency (–8L speed grade) | 5 | — | 362 | MHz |
| | Input clock frequency (–9L speed grade) | 5 | — | 265 | MHz |
| f_{INPFD} | PFD input frequency | 5 | — | 325 | MHz |
| f_{VCO} ⁽⁴⁾ | PLL internal VCO operating range | 600 | — | 1300 | MHz |
| f_{INDUTY} | Input clock duty cycle | 40 | — | 60 | % |
| $t_{INJITTER_CCJ}$ ⁽⁵⁾ | Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz | — | — | 0.15 | UI |
| | $F_{REF} < 100$ MHz | — | — | ±750 | ps |
| f_{OUT_EXT} (external clock output) ⁽³⁾ | PLL output frequency | — | — | 472.5 | MHz |
| f_{OUT} (to global clock) | PLL output frequency (–6 speed grade) | — | — | 472.5 | MHz |
| | PLL output frequency (–7 speed grade) | — | — | 450 | MHz |
| | PLL output frequency (–8 speed grade) | — | — | 402.5 | MHz |
| | PLL output frequency (–8L speed grade) | — | — | 362 | MHz |
| | PLL output frequency (–9L speed grade) | — | — | 265 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{LOCK} | Time required to lock from end of device configuration | — | — | 1 | ms |

Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 2 of 2)—Preliminary

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|-----|--------------------|----------|----------------|
| t_{DLOCK} | Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or <code>areset</code> is deasserted) | — | — | 1 | ms |
| $t_{OUTJITTER_PERIOD_DEDCLK}$ ⁽⁶⁾ | $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER_CCJ_DEDCLK}$ ⁽⁶⁾ | Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER_PERIOD_IO}$ ⁽⁶⁾ | Regular I/O period jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{OUTJITTER_CCJ_IO}$ ⁽⁶⁾ | Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ± 50 | ps |
| t_{ARESET} | Minimum pulse width on <code>areset</code> signal. | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | 3.5 ⁽⁷⁾ | — | SCANCLK cycles |
| $f_{SCANCLK}$ | <code>scanclk</code> frequency | — | — | 100 | MHz |
| $t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ ^{(8), (9)} | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz) | — | — | 425 | ps |
| | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz) | — | — | 42.5 | mUI |

Notes to Table 1–25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz `scanclk` frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
 - Upstream PLL— 0.59 MHz \leq Upstream PLL bandwidth < 1 MHz
 - Downstream PLL—Downstream PLL bandwidth > 2 MHz
- (9) PLL cascading is not supported for transceiver applications.

Embedded Multiplier Specifications

Table 1-26 lists the embedded multiplier specifications for Cyclone IV devices.

Table 1-26. Embedded Multiplier Specifications for Cyclone IV Devices —Preliminary

| Mode | Resources Used | Performance | | | | | Unit |
|------------------------|-----------------------|-------------|------------|-----|----------|-----|------|
| | Number of Multipliers | C6 | C7, I7, A7 | C8 | C8L, I8L | C9L | |
| 9 × 9-bit multiplier | 1 | 340 | 300 | 260 | 240 | 175 | MHz |
| 18 × 18-bit multiplier | 1 | 287 | 250 | 200 | 185 | 135 | MHz |

Memory Block Specifications

Table 1-27 lists the M9K memory block specifications for Cyclone IV devices.

Table 1-27. Memory Block Performance Specifications for Cyclone IV Devices —Preliminary

| Memory | Mode | Resources Used | | Performance | | | | | Unit |
|-----------|------------------------------------|----------------|------------|-------------|------------|-----|----------|-----|------|
| | | LEs | M9K Memory | C6 | C7, I7, A7 | C8 | C8L, I8L | C9L | |
| M9K Block | FIFO 256 × 36 | 47 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |
| | Single-port 256 × 36 | 0 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |
| | Simple dual-port 256 × 36 CLK | 0 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |
| | True dual port 512 × 18 single CLK | 0 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |

Configuration and JTAG Specifications

Table 1-28 lists the configuration mode specifications for Cyclone IV devices.

Table 1-28. Passive Configuration Mode Specifications for Cyclone IV Devices ⁽¹⁾

| Programming Mode | V _{CCINT} Voltage Level (V) | DCLK f _{MAX} | Unit |
|--|--------------------------------------|-----------------------|------|
| Passive Serial (PS) | 1.0 ⁽³⁾ | 66 | MHz |
| | 1.2 | 133 | MHz |
| Fast Passive Parallel (FPP) ⁽²⁾ | 1.0 ⁽³⁾ | 66 | MHz |
| | 1.2 ⁽⁴⁾ | 100 | MHz |

Notes to Table 1-28:

- (1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.
- (2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.
- (3) V_{CCINT} = 1.0 V is only supported for Cyclone IV E 1.0 V core voltage devices.
- (4) Cyclone IV E devices support 1.2 V V_{CCINT}. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK f_{MAX} for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1-29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1-29. Active Configuration Mode Specifications for Cyclone IV Devices—Preliminary

| Programming Mode | DCLK Range | Unit |
|-------------------------------------|------------|------|
| Active Parallel (AP) ⁽¹⁾ | 20 to 40 | MHz |
| Active Serial (AS) | 20 to 40 | MHz |

Note to Table 1-29:

- (1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1-30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1-30. JTAG Timing Parameters for Cyclone IV Devices ⁽¹⁾—Preliminary

| Symbol | Parameter | Min | Max | Unit |
|-----------------------|--|-----|-----|------|
| t _{JCP} | TCK clock period | 40 | — | ns |
| t _{JCH} | TCK clock high time | 19 | — | ns |
| t _{JCL} | TCK clock low time | 19 | — | ns |
| t _{JPSU_TDI} | JTAG port setup time for TDI | 1 | — | ns |
| t _{JPSU_TMS} | JTAG port setup time for TMS | 3 | — | ns |
| t _{JPH} | JTAG port hold time | 10 | — | ns |
| t _{JPCO} | JTAG port clock to output ^{(2), (3)} | — | 15 | ns |
| t _{JPZX} | JTAG port high impedance to valid output ^{(2), (3)} | — | 15 | ns |
| t _{JPXZ} | JTAG port valid output to high impedance ^{(2), (3)} | — | 15 | ns |
| t _{JSSU} | Capture register setup time | 5 | — | ns |
| t _{JSH} | Capture register hold time | 10 | — | ns |
| t _{JSCO} | Update register clock to output | — | 25 | ns |
| t _{JSZX} | Update register high impedance to valid output | — | 25 | ns |
| t _{JSXZ} | Update register valid output to high impedance | — | 25 | ns |


Notes to Table 1-30:


- (1) For more information about JTAG waveforms, refer to “JTAG Waveform” in “Glossary” on page 1-38.
 (2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.
 (3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

 For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

 Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1-31 through Table 1-36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to “Glossary” on page 1-38.

Table 1-31. RSDS Transmitter Timing Specifications for Cyclone IV Devices ⁽¹⁾, ⁽²⁾, ⁽⁴⁾ (Part 1 of 2)—Preliminary

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|-----|-----|-----|--------|-----|-------|--------|-----|-------|----------|-----|-------|-----|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{HSCLK} (input clock frequency) | ×10 | 10 | — | 180 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×8 | 10 | — | 180 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×7 | 10 | — | 180 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×4 | 10 | — | 180 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×2 | 10 | — | 180 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×1 | 10 | — | 360 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 360 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | 100 | — | 265 | Mbps |
| | ×8 | 80 | — | 360 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | 80 | — | 265 | Mbps |
| | ×7 | 70 | — | 360 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | 70 | — | 265 | Mbps |
| | ×4 | 40 | — | 360 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | 40 | — | 265 | Mbps |
| | ×2 | 20 | — | 360 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | 20 | — | 265 | Mbps |
| | ×1 | 10 | — | 360 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | Mbps |
| t_{DUTY} | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Transmitter channel-to-channel skew (TCCS) | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| t_{RISE} | 20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$ | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| t_{FALL} | 20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$ | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

Table 1-31. RSDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)} (Part 2 of 2)—Preliminary

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|----------------------------------|-------|-----|-----|-----|--------|-----|-----|--------|-----|-----|----------|-----|-----|-----|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t _{LOCK} ⁽³⁾ | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

Notes to Table 1-31:

- (1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.
- (2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1-32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)—Preliminary

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|--|-----|-----|-----|--------|-----|-----|--------|-----|-----|----------|-----|-----|-----|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f _{HCLK} (input clock frequency) | ×10 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 72.5 | MHz |
| | ×8 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 72.5 | MHz |
| | ×7 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 72.5 | MHz |
| | ×4 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 72.5 | MHz |
| | ×2 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 85 | 10 | — | 72.5 | MHz |
| | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 145 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | 100 | — | 145 | Mbps |
| | ×8 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | 80 | — | 145 | Mbps |
| | ×7 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | 70 | — | 145 | Mbps |
| | ×4 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | 40 | — | 145 | Mbps |
| | ×2 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | 20 | — | 145 | Mbps |
| | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 145 | Mbps |
| t _{DUTY} | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| t _{RISE} | 20 – 80%, C _{LOAD} = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| t _{FALL} | 20 – 80%, C _{LOAD} = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)
—Preliminary

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|----------------------------------|-------|-----|-----|-----|--------|-----|-----|--------|-----|-----|----------|-----|-----|-----|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t_{LOCK} ⁽²⁾ | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

Notes to Table 1–32:

- (1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)} (Part 1 of 2)—Preliminary

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|--|---|-----|-----|-----|--------|-----|-------|--------|-----|-------|----------|-----|-------|-----|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{HSCLK} (input clock frequency) | ×10 | 10 | — | 200 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×8 | 10 | — | 200 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×7 | 10 | — | 200 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×4 | 10 | — | 200 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×2 | 10 | — | 200 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 155.5 | 10 | — | 132.5 | MHz |
| | ×1 | 10 | — | 400 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 400 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | 100 | — | 265 | Mbps |
| | ×8 | 80 | — | 400 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | 80 | — | 265 | Mbps |
| | ×7 | 70 | — | 400 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | 70 | — | 265 | Mbps |
| | ×4 | 40 | — | 400 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | 40 | — | 265 | Mbps |
| | ×2 | 20 | — | 400 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | 20 | — | 265 | Mbps |
| | ×1 | 10 | — | 400 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | Mbps |
| t_{DUTY} | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| t_{RISE} | 20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$ | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| t_{FALL} | 20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$ | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

Table 1-33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)} (Part 2 of 2)—Preliminary

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|----------------------------------|-------|-----|-----|-----|--------|-----|-----|--------|-----|-----|----------|-----|-----|-----|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t _{LOCK} ⁽³⁾ | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

Notes to Table 1-33:

- (1) Applicable for true and emulated mini-LVDS transmitter.
- (2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1-34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} —Preliminary

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|-------|-----|-----|--------|-------|--------|-------|----------|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| f _{HCLK} (input clock frequency) | ×10 | 10 | 420 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×8 | 10 | 420 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×7 | 10 | 420 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×4 | 10 | 420 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×2 | 10 | 420 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×1 | 10 | 420 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | MHz |
| HSIODR | ×10 | 100 | 840 | 100 | 740 | 100 | 640 | 100 | 640 | 100 | 500 | Mbps |
| | ×8 | 80 | 840 | 80 | 740 | 80 | 640 | 80 | 640 | 80 | 500 | Mbps |
| | ×7 | 70 | 840 | 70 | 740 | 70 | 640 | 70 | 640 | 70 | 500 | Mbps |
| | ×4 | 40 | 840 | 40 | 740 | 40 | 640 | 40 | 640 | 40 | 500 | Mbps |
| | ×2 | 20 | 840 | 20 | 740 | 20 | 640 | 20 | 640 | 20 | 500 | Mbps |
| | ×1 | 10 | 420 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |
| t _{DUTY} | — | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | — | 200 | — | 200 | ps |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| t _{LOCK} ⁽²⁾ | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

Notes to Table 1-34:

- (1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.
Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)}—Preliminary

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|--|-------|-----|-------|--------|-------|--------|-------|----------|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| f _{HSCLK} (input clock frequency) | ×10 | 10 | 320 | 10 | 320 | 10 | 275 | 10 | 275 | 10 | 250 | MHz |
| | ×8 | 10 | 320 | 10 | 320 | 10 | 275 | 10 | 275 | 10 | 250 | MHz |
| | ×7 | 10 | 320 | 10 | 320 | 10 | 275 | 10 | 275 | 10 | 250 | MHz |
| | ×4 | 10 | 320 | 10 | 320 | 10 | 275 | 10 | 275 | 10 | 250 | MHz |
| | ×2 | 10 | 320 | 10 | 320 | 10 | 275 | 10 | 275 | 10 | 250 | MHz |
| | ×1 | 10 | 402.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | MHz |
| HSIODR | ×10 | 100 | 640 | 100 | 640 | 100 | 550 | 100 | 550 | 100 | 500 | Mbps |
| | ×8 | 80 | 640 | 80 | 640 | 80 | 550 | 80 | 550 | 80 | 500 | Mbps |
| | ×7 | 70 | 640 | 70 | 640 | 70 | 550 | 70 | 550 | 70 | 500 | Mbps |
| | ×4 | 40 | 640 | 40 | 640 | 40 | 550 | 40 | 550 | 40 | 500 | Mbps |
| | ×2 | 20 | 640 | 20 | 640 | 20 | 550 | 20 | 550 | 20 | 500 | Mbps |
| | ×1 | 10 | 402.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |
| t _{DUTY} | — | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | — | 200 | — | 200 | ps |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| t _{LOCK} ⁽²⁾ | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

Notes to Table 1–35:

- (1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)—Preliminary

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|--|-------|-----|-------|--------|-------|--------|-------|----------|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| f _{HSCLK} (input clock frequency) | ×10 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×8 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×7 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×4 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×2 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | MHz |
| HSIODR | ×10 | 100 | 875 | 100 | 740 | 100 | 640 | 100 | 640 | 100 | 500 | Mbps |
| | ×8 | 80 | 875 | 80 | 740 | 80 | 640 | 80 | 640 | 80 | 500 | Mbps |
| | ×7 | 70 | 875 | 70 | 740 | 70 | 640 | 70 | 640 | 70 | 500 | Mbps |
| | ×4 | 40 | 875 | 40 | 740 | 40 | 640 | 40 | 640 | 40 | 500 | Mbps |
| | ×2 | 20 | 875 | 20 | 740 | 20 | 640 | 20 | 640 | 20 | 500 | Mbps |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |

Table 1-36. LVDS Receiver Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)—Preliminary

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|----------------------------------|-------|-----|-----|--------|-----|--------|-----|----------|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| SW | — | — | 400 | — | 400 | — | 400 | — | 550 | — | 640 | ps |
| Input jitter tolerance | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| t _{LOCK} ⁽²⁾ | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

Notes to Table 1-36:

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.



For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to [Section III: System Performance Specifications](#) of the *External Memory Interface Handbook*.

Table 1-37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1-37. Memory Output Clock Jitter Specifications for Cyclone IV Devices ^{(1), (2)} — Preliminary

| Parameter | Symbol | Min | Max | Unit |
|------------------------------|------------------------|------|-----|------|
| Clock period jitter | t _{JIT(per)} | -125 | 125 | ps |
| Cycle-to-cycle period jitter | t _{JIT(cc)} | -200 | 200 | ps |
| Duty cycle jitter | t _{JIT(duty)} | -150 | 150 | ps |

Notes to Table 1-37:

- (1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1-38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1-38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins ⁽¹⁾, ⁽²⁾, ⁽³⁾—Preliminary

| Symbol | C6 | | C7, I7 | | C8, I8L, A7 | | C9L | | Unit |
|-------------------|-----|-----|--------|-----|-------------|-----|-----|-----|------|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

Notes to Table 1-38:

- (1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.
- (2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1-39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1-39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices ⁽¹⁾—Preliminary

| Symbol | Description | Maximum | Units |
|---------------------|--|---------|---------------|
| t_{OCTCAL} | Duration of series OCT with calibration at device power-up | 20 | μs |

Note to Table 1-39:

- (1) OCT calibration takes place after device configuration and before entering user mode.

IOE Programmable Delay

Table 1-40 and Table 1-41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1-40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 2)—Preliminary

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|--|----------------------------|-------------------|------------|-------------|-------|-------------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.054 | 1.924 | 3.387 | 4.017 | 3.411 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.010 | 1.875 | 3.341 | 4.252 | 3.367 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.641 | 0.631 | 1.111 | 1.377 | 1.124 | ns |

Table 1-40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices ^{(1), (2)} (Part 2 of 2)—Preliminary

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|-----------------------------|-------------------|------------|-------------|-------|-------------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.971 | 0.931 | 1.684 | 2.298 | 1.684 | ns |

Notes to Table 1-40:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1-41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices ^{(1), (2)}—Preliminary

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|-----------------------------|-------------------|------------|-------------|-------|-------------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.057 | 1.921 | 3.389 | 4.146 | 3.412 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.059 | 1.919 | 3.420 | 4.374 | 3.441 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.670 | 0.623 | 1.160 | 1.420 | 1.168 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.960 | 0.919 | 1.656 | 2.258 | 1.656 | ns |

Notes to Table 1-41:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1-42 and Table 1-43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1-42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices ^{(1), (2)} (Part 1 of 2)—Preliminary

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | Unit | |
|--|----------------------------|-------------------|------------|-------------|-------|-------|-------------|-------|-------|-------|-------|----|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | | A7 |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.211 | 1.211 | 2.177 | 2.340 | 2.433 | 2.388 | 2.508 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.307 | 1.203 | 1.203 | 2.19 | 2.387 | 2.540 | 2.430 | 2.545 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.437 | 0.402 | 0.402 | 0.747 | 0.820 | 0.880 | 0.834 | 0.873 | ns |

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices ^{(1), (2)} (Part 2 of 2)—Preliminary

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | Unit | |
|---|-----------------------------|-------------------|------------|-------------|-------|-------|-------------|-------|-------|-------|-------|----|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | | A7 |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.693 | 0.665 | 0.665 | 1.200 | 1.379 | 1.532 | 1.393 | 1.441 | ns |

Notes to Table 1–42:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices ^{(1), (2)}—Preliminary

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | Unit | |
|---|-----------------------------|-------------------|------------|-------------|-------|-------|-------------|-------|-------|-------|-------|----|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | | A7 |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.209 | 1.209 | 2.201 | 2.386 | 2.510 | 2.429 | 2.548 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.207 | 1.207 | 2.202 | 2.402 | 2.558 | 2.447 | 2.557 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.458 | 0.419 | 0.419 | 0.783 | 0.861 | 0.924 | 0.875 | 0.915 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.686 | 0.657 | 0.657 | 1.185 | 1.360 | 1.506 | 1.376 | 1.422 | ns |

Notes to Table 1–43:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices ^{(1), (2)} (Part 1 of 2)—Preliminary

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|--|----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.313 | 1.209 | 2.184 | 2.336 | 2.451 | 2.387 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.208 | 2.200 | 2.399 | 2.554 | 2.446 | ns |

Table 1-44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices ^{(1), (2)} (Part 2 of 2)—Preliminary

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|-----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.438 | 0.404 | 0.751 | 0.825 | 0.886 | 0.839 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.713 | 0.682 | 1.228 | 1.41 | 1.566 | 1.424 | ns |

Notes to Table 1-44:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1-45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices ^{(1), (2)} —Preliminary

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|-----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.210 | 2.209 | 2.398 | 2.526 | 2.443 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.313 | 1.208 | 2.205 | 2.406 | 2.563 | 2.450 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.461 | 0.421 | 0.789 | 0.869 | 0.933 | 0.884 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.712 | 0.682 | 1.225 | 1.407 | 1.562 | 1.421 | ns |

Notes to Table 1-45:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Excel-based I/O Timing spreadsheet is downloadable from [Cyclone IV Devices Literature](#) website.

Glossary

Table 1-46 lists the glossary for this chapter.

Table 1-46. Glossary (Part 1 of 5)

| Letter | Term | Definitions |
|--------|--|---|
| A | — | — |
| B | — | — |
| C | — | — |
| D | — | — |
| E | — | — |
| F | f_{HSCLK} | High-speed I/O block: High-speed receiver/transmitter input and output clock frequency. |
| G | GCLK | Input pin directly to Global Clock network. |
| | GCLK PLL | Input pin to Global Clock network through the PLL. |
| H | HSIODR | High-speed I/O block: Maximum/minimum LVDS data transfer rate ($\text{HSIODR} = 1/\text{TUI}$). |
| I | Input Waveforms for the SSTL Differential I/O Standard | |

Table 1-46. Glossary (Part 2 of 5)

| Letter | Term | Definitions |
|--------|---------------|---|
| J | JTAG Waveform | |
| K | — | — |
| L | — | — |
| M | — | — |
| N | — | — |
| O | — | — |
| P | PLL Block | <p>The following highlights the PLL specification parameters:</p> <p>Key</p> <p>Reconfigurable in User Mode</p> |
| Q | — | — |

Table 1-46. Glossary (Part 3 of 5)

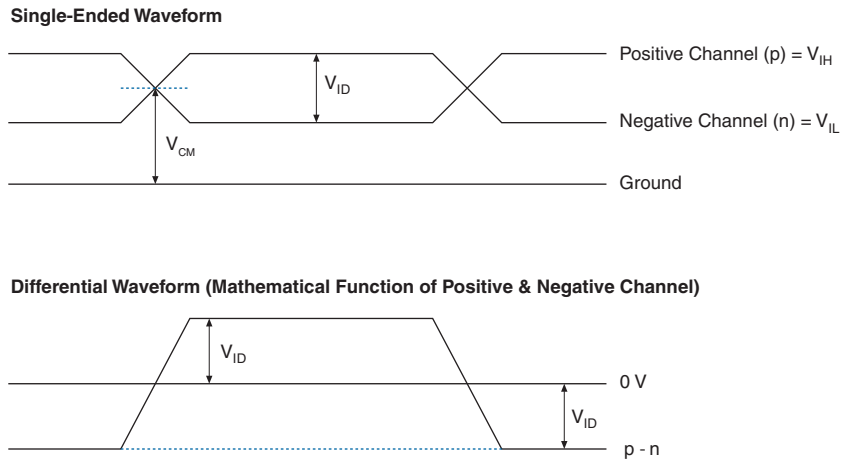
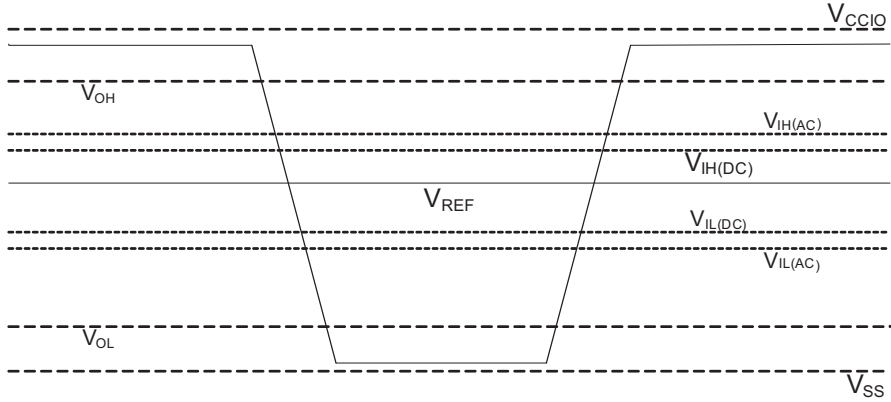
| Letter | Term | Definitions |
|--------|--|---|
| R | R_L | Receiver differential input discrete resistor (external to Cyclone IV devices). |
| | Receiver Input Waveform | <p>Receiver input waveform for LVDS and LVPECL differential standards:</p>  <p>Single-Ended Waveform</p> <p>Positive Channel (p) = V_{IH}</p> <p>Negative Channel (n) = V_{IL}</p> <p>Ground</p> <p>V_{ID}</p> <p>V_{CM}</p> <p>Differential Waveform (Mathematical Function of Positive & Negative Channel)</p> <p>V_{ID}</p> <p>0 V</p> <p>V_{ID}</p> <p>p - n</p> |
| | Receiver input skew margin (RSKM) | High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$. |
| S | Single-ended voltage-referenced I/O Standard |  <p>V_{CCIO}</p> <p>V_{OH}</p> <p>$V_{IH(AC)}$</p> <p>$V_{IH(DC)}$</p> <p>V_{REF}</p> <p>$V_{IL(DC)}$</p> <p>$V_{IL(AC)}$</p> <p>V_{OL}</p> <p>V_{SS}</p> <p>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform <i>ringing</i>.</p> |
| | SW (Sampling Window) | High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. |

Table 1-46. Glossary (Part 4 of 5)

| Letter | Term | Definitions |
|------------|--|---|
| T | t_C | High-speed receiver and transmitter input and output clock period. |
| | Channel-to-channel-skew (TCCS) | High-speed I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement. |
| | t_{cin} | Delay from the clock pad to the I/O input register. |
| | t_{CO} | Delay from the clock pad to the I/O output. |
| | t_{cout} | Delay from the clock pad to the I/O output register. |
| | t_{DUTY} | High-speed I/O block: Duty cycle on high-speed transmitter output clock. |
| | t_{FALL} | Signal high-to-low transition time (80–20%). |
| | t_H | Input register hold time. |
| | Timing Unit Interval (TUI) | High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_C/w$). |
| | $t_{INJITTER}$ | Period jitter on the PLL clock input. |
| | $t_{OUTJITTER_DEDCLK}$ | Period jitter on the dedicated clock output driven by a PLL. |
| | $t_{OUTJITTER_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| | t_{pllcin} | Delay from the PLL inclk pad to the I/O input register. |
| | $t_{pllcout}$ | Delay from the PLL inclk pad to the I/O output register. |
| | Transmitter Output Waveform | <p>Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards:</p> <p>Single-Ended Waveform</p> <p>Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground</p> <p>V_{OS} V_{OD}</p> <p>Differential Waveform (Mathematical Function of Positive & Negative Channel)</p> <p>V_{OD} 0 V V_{OD} p - n</p> |
| t_{RISE} | Signal low-to-high transition time (20–80%). | |
| t_{SU} | Input register setup time. | |
| U | — | — |

Table 1-46. Glossary (Part 5 of 5)

| Letter | Term | Definitions |
|-----------------|--|--|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{DIF(AC)}$ | AC differential input voltage: The minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage: The minimum DC input differential voltage required for switching. |
| | V_{ICM} | Input common mode voltage: The common mode of the differential signal at the receiver. |
| | V_{ID} | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | V_{IH} | Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage. |
| | $V_{IH(DC)}$ | High-level DC input voltage. |
| | V_{IL} | Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage. |
| | $V_{IL(DC)}$ | Low-level DC input voltage. |
| | V_{IN} | DC input voltage. |
| | V_{OCM} | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| | V_{OD} | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$. |
| | V_{OH} | Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level. |
| | V_{OL} | Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level. |
| | V_{OS} | Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$. |
| | $V_{OX(AC)}$ | AC differential output cross point voltage: the voltage at which the differential output signals must cross. |
| | V_{REF} | Reference voltage for the SSTL and HSTL I/O standards. |
| | $V_{REF(AC)}$ | AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$. |
| $V_{REF(DC)}$ | DC input reference voltage for the SSTL and HSTL I/O standards. | |
| $V_{SWING(AC)}$ | AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms. | |
| $V_{SWING(DC)}$ | DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms. | |
| V_{TT} | Termination voltage for the SSTL and HSTL I/O standards. | |
| $V_X(AC)$ | AC differential input cross point voltage: The voltage at which the differential input signals must cross. | |
| W | — | — |
| X | — | — |
| Y | — | — |
| Z | — | — |

Document Revision History

Table 1-47 lists the revision history for this chapter.

Table 1-47. Document Revision History

| Date | Version | Changes |
|---------------|---------|--|
| November 2011 | 1.5 | <ul style="list-style-type: none"> ■ Updated “Maximum Allowed Overshoot or Undershoot Voltage”, “Operating Conditions”, and “PLL Specifications” sections. ■ Updated Table 1-2, Table 1-3, Table 1-4, Table 1-5, Table 1-8, Table 1-9, Table 1-15, Table 1-18, Table 1-19, and Table 1-21. ■ Updated Figure 1-1. |
| December 2010 | 1.4 | <ul style="list-style-type: none"> ■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1-21 and Table 1-25. ■ Minor text edits. |
| July 2010 | 1.3 | <p>Updated for the Quartus II software version 10.0 release:</p> <ul style="list-style-type: none"> ■ Updated Table 1-3, Table 1-4, Table 1-21, Table 1-25, Table 1-28, Table 1-30, Table 1-40, Table 1-41, Table 1-42, Table 1-43, Table 1-44, and Table 1-45. ■ Updated Figure 1-2 and Figure 1-3. ■ Removed SW Requirement and TCCS for Cyclone IV Devices tables. ■ Minor text edits. |
| March 2010 | 1.2 | <p>Updated to include automotive devices:</p> <ul style="list-style-type: none"> ■ Updated the “Operating Conditions” and “PLL Specifications” sections. ■ Updated Table 1-1, Table 1-8, Table 1-9, Table 1-21, Table 1-26, Table 1-27, Table 1-31, Table 1-32, Table 1-33, Table 1-34, Table 1-35, Table 1-36, Table 1-37, Table 1-38, Table 1-40, Table 1-42, and Table 1-43. ■ Added Table 1-5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os. ■ Added Table 1-44 and Table 1-45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. ■ Minor text edits. |
| February 2010 | 1.1 | <ul style="list-style-type: none"> ■ Updated Table 1-3 through Table 1-44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release. ■ Minor text edits. |
| November 2009 | 1.0 | Initial release. |

