Section I. Stratix IV Device Datasheet and Addendum

This section includes the following chapters:

- Chapter 1, DC and Switching Characteristics
- Chapter 2, Addendum to the Stratix IV Device Handbook

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

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Electrical Characteristics

This chapter covers the electrical and switching characteristics for Stratix® IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

For information regarding the densities and packages of devices in the Stratix IV family, refer to Table 1-1 and Table 1-2 of the *Stratix IV Device Family Overview* chapter.

Operating Conditions

When you use Stratix IV devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Stratix IV devices, you must consider the operating requirements described in this chapter.

Stratix IV devices are offered in both commercial and industrial grades. Commercial devices are offered in –2 (fastest), –2×, –3, and –4 speed grades. Industrial devices are offered in –1, –2, –3, and –4 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix IV devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

CAUTION

Conditions other than those listed in Table 1–1, Table 1–2, and Table 1–3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Stratix IV Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	-0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V_{CCPGM}	Configuration pins power supply	-0.5	3.75	V
V_{CCAUX}	Auxiliary supply for the programmable power technology	-0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_{CCPD}	I/O pre-driver power supply	-0.5	3.75	V
V_{CCIO}	I/O power supply	-0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply	-0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	-0.5	1.35	V

Table 1–1. Absolute Maximum Ratings for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_PLL}	PLL analog power supply	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
I_{OUT}	DC output current per pin	-25	40	mA
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (No bias)	-65	150	°C

Table 1–2. Transceiver Power Supply Absolute Maximum Ratings for Stratix IV GX Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	-0.5	3.75	V
V_{CCA_R}	Transceiver high voltage power (right side)	-0.5	3.75	V
V_{CCHIP_L}	Transceiver HIP digital power (left side)	-0.5	1.35	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	-0.5	1.35	V
V_{CCR_L}	Receiver power (left side)	-0.5	1.35	V
V_{CCR_R}	Receiver power (right side)	-0.5	1.35	V
V_{CCT_L}	Transmitter power (left side)	-0.5	1.35	V
V_{CCT_R}	Transmitter power (right side)	-0.5	1.35	V
V_{CCL_GXBLn} *(1)*	Transceiver clock power (left side)	-0.5	1.35	V
V_{CCL_GXBRn} *(1)*	Transceiver clock power (right side)	-0.5	1.35	V
V_{CCH_GXBLn} *(1)*	Transmitter output buffer power (left side)	-0.5	1.8	V
V_{CCH_GXBRn} *(1)*	Transmitter output buffer power (right side)	-0.5	1.8	V

Note to Table 1–2:

(1) n = 0, 1, 2, or 3.

Table 1–3. Transceiver Power Supply Absolute Maximum Ratings for Stratix IV GT Devices *(Note 1)* (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	-0.5	3.75	V
V_{CCA_R}	Transceiver high voltage power (right side)	-0.5	3.75	V
V_{CCHIP_L}	Transceiver HIP digital power (left side)	-0.5	1.35	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	-0.5	1.35	V
V_{CCR_L}	Receiver power (left side)	-0.5	1.35	V
V_{CCR_R}	Receiver power (right side)	-0.5	1.35	V
V_{CCT_L}	Transmitter power (left side)	-0.5	1.35	V
V_{CCT_R}	Transmitter power (right side)	-0.5	1.35	V
V_{CCL_GXBLn} *(2)*	Transceiver clock power (left side)	-0.5	1.35	V
V_{CCL_GXBRn} *(2)*	Transceiver clock power (right side)	-0.5	1.35	V
V_{CCH_GXBLn} *(2)*	Transmitter output buffer power (left side)	-0.5	1.8	V

Table 1–3. Transceiver Power Supply Absolute Maximum Ratings for Stratix IV GT Devices *(Note 1)* (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCH_GXBRn} *(2)*	Transmitter output buffer power (right side)	-0.5	1.8	V

Notes to Table 1–3:

(1) For absolute maximum ratings for Stratix IV GT engineering sample (ES1) devices, contact your local Altera sales representative.

(2) n = 0, 1, 2, or 3.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–4 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–4 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half of a year.

Table 1–4. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	4.0 V	100.000	%
		4.05 V	79.330	%
		4.1 V	46.270	%
		4.15 V	27.030	%
		4.2 V	15.800	%
		4.25 V	9.240	%
		4.3 V	5.410	%
		4.35 V	3.160	%
		4.4 V	1.850	%
		4.45 V	1.080	%
		4.5 V	0.630	%
		4.55 V	0.370	%
		4.6 V	0.220	%

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Stratix IV devices. Table 1–5 shows the steady-state voltage and current values expected from Stratix IV devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 1–5. Recommended Operating Conditions for Stratix IV Devices (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC} (Stratix IV GX and Stratix IV E)	Core voltage and periphery circuitry power supply	—	0.87	0.90	0.93	V
V_{CC} (Stratix IV GT)	Core voltage and periphery circuitry power supply	—	0.92	0.95	0.98	V

Table 1–5. Recommended Operating Conditions for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CCAUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} *(2)*	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_PLL} (Stratix IV GX and Stratix IV E)	PLL digital voltage regulator power supply	—	0.87	0.90	0.93	V
V_{CCD_PLL} (Stratix IV GT)	PLL digital voltage regulator power supply	—	0.92	0.95	0.98	V
V_{CC_CLKIN}	Differential clock input power supply	—	2.375	2.5	2.625	V
V_{CCBAT} *(1)*	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.3	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J (Stratix IV GX and Stratix IV E)	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
T_J (Stratix IV GT)	Operating junction temperature	Industrial	0	—	100	°C
t_{RAMP}	Power supply ramp time	Normal POR (PORSEL=0)	0.05	—	100	ms
		Fast POR (PORSEL=1)	0.05	—	4	ms

Notes to Table 1–5:

(1) Altera recommends a 3.0-V nominal battery voltage when connecting V_{CCBAT} to a battery for volatile key backup. If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.

(2) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

Table 1–6 shows the transceiver power supply recommended operating conditions for Stratix IV GX devices.

Table 1–6. Transceiver Power Supply Operating Conditions for Stratix IV GX Devices (Part 1 of 2) *(Note 4)*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	2.85/2.375	3.0/2.5 *(2)*	3.15/2.625	V
V_{CCA_R}	Transceiver high voltage power (right side)				

Table 1–6. Transceiver Power Supply Operating Conditions for Stratix IV GX Devices (Part 2 of 2) *(Note 4)*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.87	0.9	0.93	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	0.87	0.9	0.93	V
V_{CCR_L}	Receiver power (left side)	1.05	1.1	1.15	V
V_{CCR_R}	Receiver power (right side)	1.05	1.1	1.15	V
V_{CCT_L}	Transmitter power (left side)	1.05	1.1	1.15	V
V_{CCT_R}	Transmitter power (right side)	1.05	1.1	1.15	V
V_{CCL_GXBLn} *(1)*	Transceiver clock power (left side)	1.05	1.1	1.15	V
V_{CCL_GXBRn} *(1)*	Transceiver clock power (right side)	1.05	1.1	1.15	V
V_{CCH_GXBLn} *(1)*	Transmitter output buffer power (left side)	1.33/1.425	1.4/1.5 *(3)*	1.47/1.575	V
V_{CCH_GXBRn} *(1)*	Transmitter output buffer power (right side)				

Notes to Table 1–6:

(1) n = 0, 1, 2, or 3.

(2) $V_{CCA\_L/R}$ must be connected to a 3.0-V supply if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(3) $V_{CCH\_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.25 Gbps. For data rates up to 6.25 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

(4) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

Table 1–7 shows the recommended operating conditions for the Stratix IV GT transceiver power supply.

Table 1–7. Transceiver Power Supply Operating Conditions for Stratix IV GT Devices *(Note 1)*, *(3)*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	3.25	3.3	3.35	V
V_{CCA_R}	Transceiver high voltage power (right side)	3.25	3.3	3.35	V
V_{CCHIP_L}	Transceiver HIP digital power (left side)	0.92	0.95	0.98	V
V_{CCHIP_R}	Transceiver HIP digital power (right side)	0.92	0.95	0.98	V
V_{CCR_L}	Receiver power (left side)	1.15	1.2	1.25	V
V_{CCR_R}	Receiver power (right side)	1.15	1.2	1.25	V
V_{CCT_L}	Transmitter power (left side)	1.15	1.2	1.25	V
V_{CCT_R}	Transmitter power (right side)	1.15	1.2	1.25	V
V_{CCL_GXBLn} *(2)*	Transceiver clock power (left side)	1.15	1.2	1.25	V
V_{CCL_GXBRn} *(2)*	Transceiver clock power (right side)	1.15	1.2	1.25	V
V_{CCH_GXBLn} *(2)*	Transmitter output buffer power (left side)	1.33	1.4	1.47	V
V_{CCH_GXBRn} *(2)*	Transmitter output buffer power (right side)	1.33	1.4	1.47	V

Notes to Table 1–7:

(1) For recommended operating conditions for Stratix IV GT engineering sample (ES1) devices, contact your local Altera sales representative.

(2) n = 0, 1, 2, or 3.

(3) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 1–8 defines the Stratix IV I/O pin leakage current specifications.

Table 1–8. I/O Pin Leakage Current for Stratix IV Devices

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0V to $V_{CCIOMAX}$	-20	—	20	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0V to $V_{CCIOMAX}$	-20	—	20	µA

Bus Hold Specifications

Table 1–9 shows the Stratix IV device family bus hold specifications.

Table 1–9. Bus Hold Parameters

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	—	-160	—	-200	—	-300	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 1–10 lists the Stratix IV OCT termination calibration accuracy specifications.

Table 1–10. Stratix IV On-Chip Termination Calibration Accuracy Specifications *(Note 1)*

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
25-Ω R_S *(2)* 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R_T 2.5, 1.8, 1.5, 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%
20-Ω, 40-Ω, and 60-Ω R_S *(3)* 3.0, 2.5, 1.8, 1.5, 1.2	Expanded range for internal series termination with calibration (20-Ω, 40-Ω, and 60-Ω R_S setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%
25-Ω $R_{S\_left\_shift}$ 3.0, 2.5, 1.8, 1.5, 1.2	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%

Notes to Table 1–10:

(1) OCT calibration accuracy is valid at the time of calibration only.
(2) 25-Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.
(3) 20-Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change. Table 1–11 lists the Stratix IV OCT without calibration resistance tolerance to PVT changes.

Table 1–11. Stratix IV On-Chip Termination Without Calibration Resistance Tolerance Specifications (Part 1 of 2)

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3,I3	C4,I4	
25-Ω R_S 3.0 and 2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	± 30	± 40	± 40	%
25-Ω R_S 1.8 and 1.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	± 30	± 40	± 40	%
25-Ω R_S 1.2	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	± 35	± 50	± 50	%
50-Ω R_S 3.0 and 2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	± 30	± 40	± 40	%
50-Ω R_S 1.8 and 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	± 30	± 40	± 40	%

Table 1–11. Stratix IV On-Chip Termination Without Calibration Resistance Tolerance Specifications (Part 2 of 2)

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3,I3	C4,I4	
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	± 35	± 50	± 50	%
100-Ω R_D 2.5	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5 V	± 25	± 25	± 25	%

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 1–12 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–12 to determine the OCT variation after power-up calibration and Equation 1–1 to determine the OCT variation without re-calibration.

Equation 1–1. OCT Variation Without Re-Calibration *(Note 1)*, *(2)*, *(3)*, *(4)*, *(5)*, *(6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1–1:

(1) The R_{OCT} value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1–12 shows the on-chip termination variation after the power-up calibration.

Table 1–12. On-Chip Termination Variation after Power-Up Calibration *(Note 1)*

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 1–12:

(1) Valid for V_{CCIO} range of ±5% and temperature range of 0° to 85°C.

Pin Capacitance

Table 1–13 shows the Stratix IV device family pin capacitance.

Table 1–13. Pin Capacitance for Stratix IV Devices

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	4	pF
C_{IOLR}	Input capacitance on left/right I/O pins	4	pF
C_{CLKTB}	Input capacitance on top/bottom non-dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on left/right non-dedicated clock input pins	4	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Hot Socketing

Table 1–14 shows the hot socketing specifications for Stratix IV devices.

Table 1–14. Hot Socketing Specifications for Stratix IV Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA *(1)*
$I_{XCVR\text{-}TX\ (DC)}$ *(2)*	DC current per transceiver TX pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$ *(2)*	DC current per transceiver RX pin	50 mA

Notes to Table 1–14:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

(2) These specifications are preliminary.

Internal Weak Pull-Up Resistor

Table 1–15 lists the weak pull-up resistor values for Stratix IV devices.

Table 1–15. Stratix IV Internal Weak Pull-Up Resistor *(Note 1)*, *(3)*

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.0 V ±5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 2.5 V ±5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 1.8 V ±5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 1.5 V ±5% *(2)*	—	25	—	kΩ
		V_{CCIO} = 1.2 V ±5% *(2)*	—	25	—	kΩ

Notes to Table 1–15:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

I/O Standard Specifications

Table 1–16 through Table 1–21 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix IV devices. These tables also show the Stratix IV device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of terms used in Table 1–16 through Table 1–21, refer to "Glossary" on page 1–54.

Table 1–16. Single-Ended I/O Standards

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V_{CCIO} - 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} - 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	3.6	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 * V_{CCIO}	0.5 * V_{CCIO}	—	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5

Table 1–17. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	0.47 * V_{CCIO}	V_{REF}	0.53 * V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—

Table 1–18. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$(V)		$V_{IH(DC)}$(V)		$V_{IL(AC)}$(V)	$V_{IH(AC)}$(V)	V_{OL}(V)	V_{OH}(V)	I_{oi} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.57	V_{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.76	V_{TT} + 0.76	16.2	-16.2
SSTL-18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	V_{TT} - 0.475	V_{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	-13.4
SSTL-15 Class I	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	-8
SSTL-15 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	-16
HSTL-18 Class I	—	V_{REF} -0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-18 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-15 Class I	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-15 Class II	—	V_{REF} - 0.1	V_{REF} + 0.1	—	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	-8
HSTL-12 Class II	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	-16

Table 1–19. Differential SSTL I/O Standards

I/O Standard	V_{CCIO}(V)			$V_{SWING(DC)}$(V)		$V_{X(AC)}$(V)			$V_{SWING(AC)}$(V)		$V_{OX(AC)}$(V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	V_{CCIO}/2	—	0.35	—	—	V_{CCIO}/2	—

Table 1–20. Differential HSTL I/O Standards (Part 1 of 2)

I/O Standard	V_{CCIO}(V)			$V_{DIF(DC)}$(V)		$V_{X(AC)}$(V)			$V_{CM(DC)}$(V)			$V_{DIF(AC)}$(V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—

Table 1–20. Differential HSTL I/O Standards (Part 2 of 2)

I/O Standard	V_{CCIO}(V)			$V_{DIF(DC)}$(V)		$V_{X(AC)}$(V)			$V_{CM(DC)}$(V)			$V_{DIF(AC)}$(V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	V_{CCIO} + 0.48

Table 1–21. Differential I/O Standard Specifications *(Note 1)*, *(2)*

I/O Standard	V_{CCIO}(V)			V_{ID}(mV)			$V_{ICM(DC)}$(V)			V_{OD}(V) *(3)*			V_{OCM}(V) *(3)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 1–22 on page 1–14 and Table 1–23 on page 1–21.														
2.5 V LVDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D_{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
2.5 V LVDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1	1.25	1.5
						—	1.05	D_{MAX} > 700 Mbps	1.55	0.247	—	0.6	1	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.5
LVPECL	2.375	2.5	2.625	300	—	—	0.6	D_{MAX} ≤ 700 Mbps	1.8 *(4)*	—	—	—	—	—	—
	2.375	2.5	2.625	300	—	—	1	D_{MAX} > 700 Mbps	1.6 *(4)*	—	—	—	—	—	—

Notes to Table 1–21:

(1) Vertical (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.

(2) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–14.

(3) RL range: 90 ≤ RL ≤ 110 Ω.

(4) For D_{MAX} > 700 Mbps, the minimum input voltage is 0.85 V; the maximum input voltage is 1.75 V. For F_{MAX} ≤ 700 Mbps, the minimum input voltage is 0.45 V; the maximum input voltage is 1.95 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design: the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide for Stratix III and Stratix IV FPGAs* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Stratix IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary".
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 1–22 lists the Stratix IV GX transceiver specifications.

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 1 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	697	50	—	697	50	—	637.5	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	425	50	—	325	50	—	325	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a REFCLK pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Rise/fall time *(19)*	—	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCI Express	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCI Express	—	0 to -0.5%	—	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	1100 ± 10%			1100 ± 10%			1100 ± 10%			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCI Express reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
R_{REF}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 2 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
`fixedclk` clock frequency	PCI Express Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
`reconfig_clk` clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	—
Delta time between `reconfig_clks` *(17)*	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down (`gxb_powerdown`) pulse width	—	1	—	—	1	—	—	1	—	—	µs
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (Single width, non-PMA Direct)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	8500	1000	—	6500	1000	—	6375 *(20)*	Mbps
Data rate (Single width, PMA Direct)	—	600	—	3250	600	—	3250	600	—	3250	Mbps
Data rate (Double width, PMA Direct)	—	1000	—	6500	1000	—	6500	1000	—	6375	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	V
	V_{ICM} =1.1 V setting *(4)*	—	—	1.6	—	—	1.6	—	—	1.6	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p) *(18)*	Data Rate = 600 Mbps to 5 Gbps	100	—	—	100	—	—	165	—	—	mV
	Data Rate > 5 Gbps	165	—	—	165	—	—	165	—	—	mV

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 3 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ICM}	V_{ICM} = 0.82 V setting	820 ± 10%			820 ± 10%			820 ± 10%			mV
	V_{ICM} = 1.1 V setting *(4)*	1100 ± 10%			1100 ± 10%			1100 ± 10%			mV
Receiver DC Coupling Support	—	For more information about receiver DC coupling support, refer to the "DC-Coupled Links" section in the *Stratix IV Transceiver Architecture* chapter.									
Differential on-chip termination resistors	85-Ω setting	85 ± 20%			85 ± 20%			85 ± 20%			Ω
	100-Ω setting	100 ± 20%			100 ± 20%			100 ± 20%			Ω
	120-Ω setting	120 ± 20%			120 ± 20%			120 ± 20%			Ω
	150-Ω setting	150 ± 20%			150 ± 20%			150 ± 20%			Ω
Differential and common mode return loss	PCI Express (PIPE) (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, Serial RapidIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant									—
Programmable PPM detector *(5)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000									ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization *(16)*	—	—	—	16	—	—	16	—	—	16	dB
t_{LTR} *(6)*	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR\_LTD\_Manual}$ *(7)*	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD_Manual} *(8)*	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} *(9)*	—	—	—	4000	—	—	4000	—	—	4000	ns
Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode	PCI Express (PIPE) Gen1	20 - 35									MHz
	PCI Express (PIPE) Gen2	40 - 65									MHz
	(OIF) CEI PHY at 6.375 Gbps	20 - 35									MHz
	XAUI	10 - 18									MHz
	Serial RapidIO 1.25 Gbps	10 - 18									MHz
	Serial RapidIO 2.5 Gbps	10 - 18									MHz
	Serial RapidIO 3.125 Gbps	6 - 10									MHz
	GIGE	6 - 10									MHz
	SONET OC12	3 - 6									MHz
	SONET OC48	14 - 19									MHz

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 4 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	—	—	17000	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 3	—	9	—	—	9	—	—	9	—	dB
	DC Gain Setting = 4	—	12	—	—	12	—	—	12	—	dB
EyeQ Max Data Rate	—	600	—	3250	600	—	3250	600	—	3250	Mbps
Transmitter											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML										
Data rate (Single width, non-PMA Direct)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	8500	1000	—	6500	1000	—	6375 *(20)*	Mbps
Data rate (Single width, PMA Direct)	—	600	—	3250	600	—	3250	600	—	3250	Mbps
Data rate (Double width, PMA Direct) *(10)*	—	1000	—	6500	1000	—	6500	1000	—	6375	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	85 ± 15%			85 ± 15%			85 ± 15%			Ω
	100-Ω setting	100 ± 15%			100 ± 15%			100 ± 15%			Ω
	120-Ω setting	120 ± 15%			120 ± 15%			120 ± 15%			Ω
	150-Ω setting	150 ± 15%			150 ± 15%			150 ± 15%			Ω
Differential and common mode return loss	PCI Express (PIPE) Gen1 and Gen2 (TX V_{OD}=4), XAUI (TX V_{OD}=6), HiGig+ (TX V_{OD}=6), CEI SR/LR (TX V_{OD}=8), Serial RapidIO SR (V_{OD}=6), Serial RapidIO LR (V_{OD}=8), CPRI LV (V_{OD}=6), CPRI HV (V_{OD}=2), OBSAI (V_{OD}=6), SATA (V_{OD}=4),	Compliant									—
Rise time *(11)*	—	50	—	200	50	—	200	50	—	200	ps
Fall time *(11)*	—	50	—	200	50	—	200	50	—	200	ps

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 5 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCI EXpress (PIPE), ×4, Basic ×4	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCI Express (PIPE) ×8, Basic ×8	—	—	500	—	—	500	—	—	500	ps
Inter-transceiver block skew in Basic (PMA Direct) ×N mode *(12)*	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	—	—	400	—	—	400	ps
	N ≥ 18 channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks	—	—	650	—	—	650	—	—	650	ps
CMU PLL0 and CMU PLL1											
Supported Data Range	—	600	—	8500	600	—	6500	600	—	6375	Mbps
`pll_powerdown` minimum pulse width (`tpll_powerdown`)	—	1									µs
CMU PLL lock time from `pll_powerdown` de-assertion	—	—	—	100	—	—	100	—	—	100	µs

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 6 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
-3 dB Bandwidth	PCI Express (PIPE) Gen1	2.5 - 3.5									MHz
	PCI Express (PIPE) Gen2	6 - 8									MHz
	(OIF) CEI PHY at 4.976 Gbps	7 - 11									MHz
	(OIF) CEI PHY at 6.375 Gbps	5 - 10									MHz
	XAUI	2 - 4									MHz
	Serial RapidIO 1.25 Gbps	3 - 5.5									MHz
	Serial RapidIO 2.5 Gbps	3 - 5.5									MHz
	Serial RapidIO 3.125 Gbps	2 - 4									MHz
	GIGE	2.5 - 4.5									MHz
	SONET OC12	1.5 - 2.5									MHz
	SONET OC48	3.5 - 6									MHz
ATX PLL (6G)											
Supported Data Range *(14)*	/L = 1	4800-5400 and 6000-6500			4800-5400 and 6000-6500			—			Mbps
	/L = 2	2400-2700 and 3000-3250			2400-2700 and 3000-3250			—			Mbps
	/L = 4	1200-1350 and 1500-1625			1200-1350 and 1500-1625			—			Mbps
-3 dB Bandwidth	PCI Express (PIPE) Gen 2	—	1.5	—	—	1.5	—	allows LC			MHz
	(OIF) CEI PHY at 6.375 Gbps	3 - 4.5			3 - 4.5			allows LC			MHz
Transceiver-FPGA Fabric Interface											
Interface speed (non-PMA Direct)	—	25	—	265.625	25	—	250	25	—	250	MHz
Interface speed (PMA Direct)	—	50	—	325	50	—	325	50	—	325	MHz

Table 1–22. Transceiver Specifications for Stratix IV GX Devices (Part 7 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/Industrial and –2× Commercial Speed Grade *(1)*			–4 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is two parallel clock cycles									—

Notes to Table 1–22:

(1) The –2× speed grade is the fastest speed grade offered in the following Stratix IV GX devices: EP4SGX70DF29, EP4SGX110DF29, EP4SGX110FF35, EP4SGX230DF29, EP4SGX110FF35, EP4SGX230DF29, EP4SGX230FF35, EP4SGX290FF35, EP4SGX290FH29, EP4SGX360FF35, and EPSGX360FH29.

(2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in transmitter only mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in receiver only or receiver and transmitter mode. For more information, refer to the *Stratix IV Dynamic Reconfiguration* chapter in volume 2 of the *Stratix IV Device Handbook*.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS.

(5) The rate matcher supports only up to ±300 ppm.

(6) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–2 on page 1–28.

(7) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–2 on page 1–28.

(8) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–2 on page 1–28.

(9) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–3 on page 1–28.

(10) A GPLL may be required to meet PMA-FPGA fabric interface timing above certain data rates. Refer to the "Left/Right PLL Requirements in Basic (PMA Direct) Mode" section in the *Stratix IV GX Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

(11) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(12) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of the device by configuring them in Basic (PMA Direct) xN mode. For more information about clocking requirements in this mode, refer to the "Basic (PMA Direct) Mode Clocking" section in the *Stratix IV GX Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

(13) Pending Characterization.

(14) The Quartus II software automatically selects the appropriate /L divider depending upon the configured data.

(15) The maximum Transceiver-FPGA Fabric interface speed of 265.625 MHz is allowed only in Basic Low-Latency PCS mode with a 32-bit interface width. For more information, refer to the "Basic Double-Width Mode Configurations" section in the *Stratix IV Transceiver Architecture* chapter in volume 2 of the *Stratix IV Device Handbook*.

(16) Figure 1–1 shows the AC gain curves for each of the 16 available equalization settings.

(17) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(18) The outer envelope of the eye diagram measured at the receiver input pins must meet the minimum V_{ID} specifications if **RX equalization** is enabled. The inner envelope of the eye diagram measured at the receiver input pins must meet the minimum V_{ID} specifications if **RX equalization** is not enabled.

(19) The rise and fall time transition is specified from 20% to 80%.

(20) Stratix IV GX devices in -4 speed grade support Basic mode and Deterministic Latency mode transceiver configurations up to 6375 Mbps. These configurations are shown in the figures 1-90, 1-92, 1-94, 1-96, and 1-101 in the *Stratix IV Transceiver Architecture* chapter.

Figure 1–1 shows the top-to-bottom AC gain curve for equalization settings 0 to 15.

Figure 1–1. AC Gain Curves for Equalization Settings 0 to 15 (Bottom to Top)

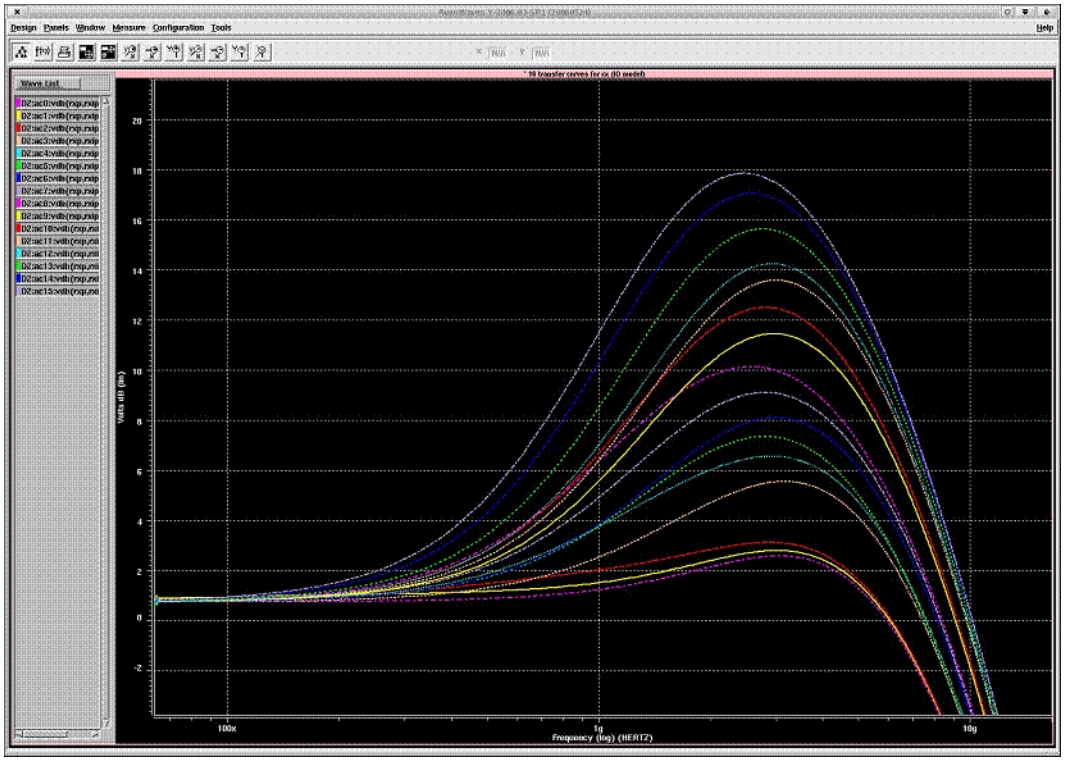


Table 1–23 lists the Stratix IV GT transceiver specifications.

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 1 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL, LVDS										
Input frequency from REFCLK input pins	—	50	—	706.25	50	—	706.25	50	—	706.25	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	425	50	—	425	50	—	425	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a REFCLK pin	—	-0.3	—	—	-0.3	—	—	-0.3	—	—	V
Rise/fall time	—	—	0.2	—	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 2 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak-to-peak differential input voltage after device configuration	—	200	—	1600	200	—	1600	200	—	1600	mV
Max peak-to-peak differential input voltage before device configuration	—	—	—	900	—	—	900	—	—	900	mV
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM}	—	1200 ± 10%			1200 ± 10%			1200 ± 10%			mV
R_{REF}	—	—	—	2000 ± 1%	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
`reconfig_clk` clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 *(1)*	—	—	2.5/ 37.5 *(1)*	—	50	2.5/ 37.5 *(1)*	—	50	MHz
`fixedclk` clock frequency	PCI Express Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Delta time between `reconfig_clks` *(13)*	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum (`gxb_powerdown`) power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (Single width, non-PMA Direct)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	11300	1000	-	10312.5	1000	—	8500	Mbps
Data rate (Single width, PMA Direct)	—	600	-	3250	600	-	3250	600	—	3250	Mbps
Data rate (Double width, PMA Direct)	—	1000	-	6500	1000	-	6500	1000	—	6500	Mbps
Absolute V_{MAX} for a receiver pin *(2)*	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	—	-0.4	—	-0.4	—	—	-0.4	—	—	V

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 3 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	V
	V_{ICM} = 1.2 V setting *(3)*	—	—	1.2	—	—	1.2	—	—	1.2	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	Data Rate = 2488 Mbps to 5 Gbps	100	—	—	100	—	—	100	—	—	mV
	Data Rate > 5 Gbps	165	—	—	165	—	—	165	—	—	mV
V_{ICM}	V_{ICM} = 0.82 V setting	820 ± 10%			820 ± 10%			820 ± 10%			mV
	V_{ICM} = 1.2 V setting *(3)*	1200 ± 10%			1200 ± 10%			1200 ± 10%			mV
Differential on-chip termination resistors	85-Ω setting	85 ± 20%			85 ± 20%			85 ± 20%			Ω
	100-Ω setting	100 ± 20%			100 ± 20%			100 ± 20%			Ω
	120-Ω setting	120 ± 20%			120 ± 20%			120 ± 20%			Ω
	150-Ω setting	150 ± 20%			150 ± 20%			150 ± 20%			Ω
Differential and common mode return loss	PCI Express (PIPE) (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, Serial RapidIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant									—
Programmable PPM detector *(4)*	—	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000								ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	16	—	—	16	—	—	16	dB
t_{LTR} *(5)*	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR\_LTD\_Manual}$ *(6)*	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD_Manual} *(7)*	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} *(8)*	—	—	—	4000	—	—	4000	—	—	4000	ns

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 4 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	—	—	17000	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 3	—	9	—	—	9	—	—	9	—	dB
	DC Gain Setting = 4	—	12	—	—	12	—	—	12	—	dB
EyeQ Max Data Rate	—	—	—	4.0	—	—	4.0	—	—	4.0	Gbps
Transmitter											
Supported I/O Standards	1.4 V PCML										
Data rate (Single width, non-PMA Direct)	—	600	—	3750	600	—	3750	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	11300	1000	—	10312.5	1000	—	8500	Mbps
Data rate (Single width, PMA Direct)	—	600	—	3250	600	—	3250	600	—	3250	Mbps
Data rate (Double width, PMA Direct) *(9)*	—	1000	—	6500	1000	—	6500	1000	—	6500	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	85 ± 15%			85 ± 15%			85 ± 15%			Ω
	100-Ω setting	100 ± 15%			100 ± 15%			100 ± 15%			Ω
	120-Ω setting	120 ± 15%			120 ± 15%			120 ± 15%			Ω
	150-Ω setting	150 ± 15%			150 ± 15%			150 ± 15%			Ω

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 5 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential and common mode return loss	PCI Express (PIPE) Gen1 and Gen2 (TX V_{OD}=4), XAUI (TX V_{OD}=6), HiGig+ (TX V_{OD}=6), CEI SR/LR (TX V_{OD}=8), Serial RapidIO SR (V_{OD}=6), Serial RapidIO LR (V_{OD}=8), CPRI LV (V_{OD}=6), CPRI HV (V_{OD}=2), OBSAI (V_{OD}=6), SATA (V_{OD}=4),	Compliant									—
Rise time *(10)*	—	50	—	200	50	—	200	50	—	200	ps
Fall time *(10)*	—	50	—	200	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCI EXpress (PIPE), ×4, Basic ×4	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCI Express (PIPE) ×8, Basic ×8	—	—	500	—	—	500	—	—	500	ps

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 6 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block skew in Basic (PMA Direct) ×N mode *(11)*	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	—	—	400	—	—	400	ps
	N ≥ 18 channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks	—	—	650	—	—	650	—	—	650	ps
CMU PLL0 and CMU PLL1											
Supported data range	—	600			600			600			Mbps
CMU PLL lock time from `pll_powerdown` de-assertion	—	—	—	100	—	—	100	—	—	100	µs
ATX PLL (6G)											
Supported Data Range	/L = 1	4800-5400 and 6000-6500			4800-5400 and 6000-6500			—			Mbps
	/L = 2	2400-2700 and 3000-3250			2400-2700 and 3000-3250			—			Mbps
	/L = 4	1200-1350 and 1500-1625			1200-1350 and 1500-1625			—			Mbps
ATX PLL (10G)											
Supported Data Range	—	9900	—	11300	9900	—	10312.5	—			Mbps
Transceiver-FPGA Fabric Interface											
Interface speed (non-PMA Direct)	—	62.2	—	—	62.2	—	265.625	62.2	—	265.625	MHz
Interface speed (PMA Direct)	—	124.4	—	—	124.4	—	325	124.4	—	325	MHz

Table 1–23. Transceiver Specifications for Stratix IV GT Devices (Part 7 of 7)

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	—	—	—	Minimum is two parallel clock cycles						—

Notes to Table 1–23:

(1) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in transmitter only mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in receiver only or receiver and transmitter mode. For more information, refer to the *Stratix IV Dynamic Reconfiguration* chapter in volume 1 of the *Stratix IV Device Handbook*.

(2) The device cannot tolerate prolonged operation at this absolute maximum.

(3) You must use the 1.2-V RXV_{ICM} setting if the input serial data standard is LVDS.

(4) The rate matcher supports only up to ±300 ppm.

(5) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–2 on page 1–28.

(6) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–2 on page 1–28.

(7) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–2 on page 1–28.

(8) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–3 on page 1–28.

(9) A GPLL may be required to meet PMA-FPGA fabric interface timing above certain data rates. Refer to the "Left/Right PLL Requirements in Basic (PMA Direct) Mode" section in the *Stratix IV GX Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

(10) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(11) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of the device by configuring them in Basic (PMA Direct) xN mode. For more information about clocking requirements in this mode, refer to the "Basic (PMA Direct) Mode Clocking" section in the *Stratix IV GX Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

(12) Pending Characterization.

(13) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = Lock-To-Data; LTR = Lock-To-Reference

Figure 1–2. Lock Time Parameters for Manual Mode

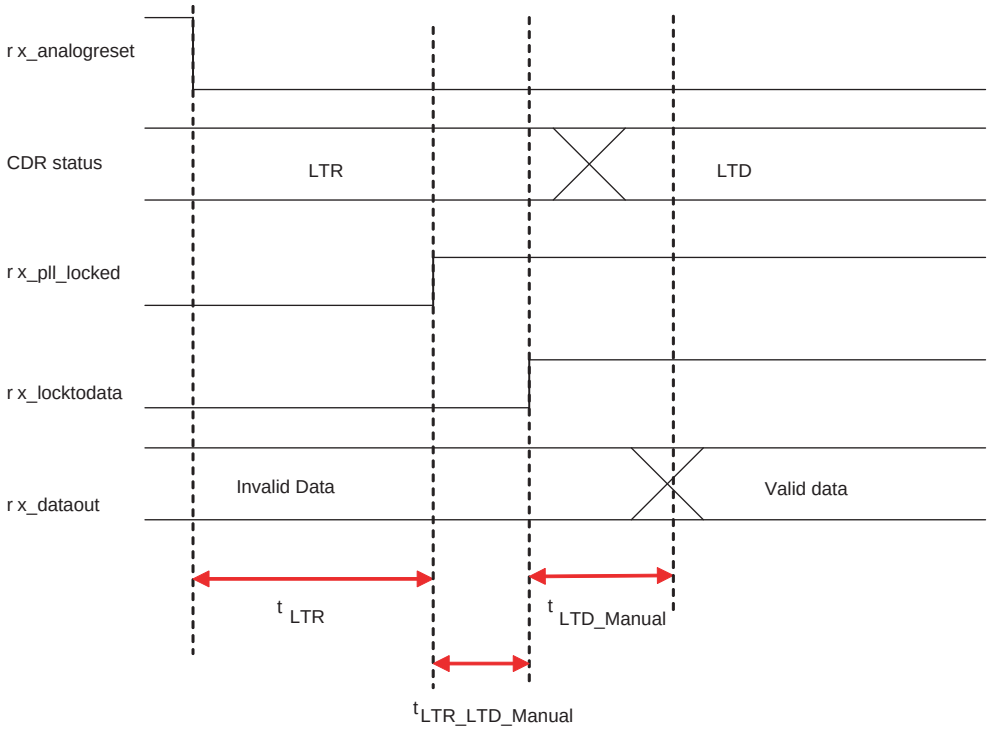


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode

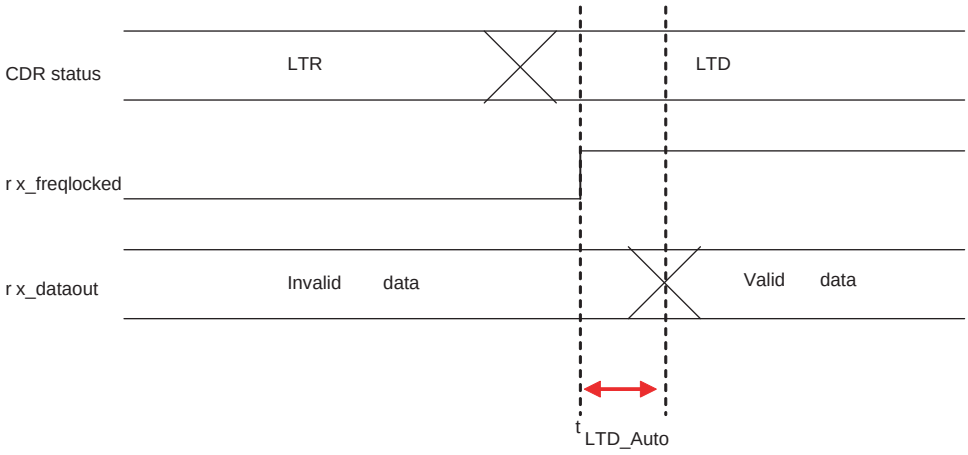


Table 1–24 through Table 1–27 show the typical differential V_{OD} termination settings for Stratix IV GX and GT devices.

Table 1–24. Typical V_{OD} Setting, TX Term = 85 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-peak Typical (mV)	170 ± 20%	340 ± 20%	510 ± 20%	595 ± 20%	680 ± 20%	765 ± 20%	850 ± 20%	1020 ± 20%

Table 1–25. Typical V_{OD} Setting, TX Term = 100 Ω

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-peak Typical (mV)	200 ± 20%	400 ± 20%	600 ± 20%	700 ± 20%	800 ± 20%	900 ± 20%	1000 ± 20%	1200 ± 20%

Table 1–26. Typical V_{OD} Setting, TX Term = 120 Ω

Symbol	V_{OD} Setting (mV)						
	0	1	2	3	4	5	6
V_{OD} differential peak-peak Typical (mV)	240 ± 20%	480 ± 20%	720 ± 20%	840 ± 20%	960 ± 20%	1080 ± 20%	1200 ± 20%

Table 1–27. Typical V_{OD} Setting, TX Term = 150 Ω

Symbol	V_{OD} Setting (mV)					
	0	1	2	3	4	5
V_{OD} differential peak-peak Typical (mV)	300 ± 20%	600 ± 20%	900 ± 20%	1050 ± 20%	1200 ± 20%	1350 ± 20%

Table 1–28 shows typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels shown in Table 1–28 are a representation of possible pre-emphasis levels under the specified conditions only and it should be noted that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Stratix IV HSSI HSPICE models.

Table 1–28. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 1 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0
4	N/A	2	0.7	0.3	0	0	0	0

Table 1–28. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–29 lists the Stratix IV GX transceiver jitter specifications for all supported protocols. For protocols supported by Stratix IV GT industrial speed grade devices, refer to the Stratix IV GX –2 commercial speed grade column in Table 1–29.

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 1 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(3)*											
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance *(3)*											
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			UI
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS15	> 15			> 15			> 15			UI
	Jitter frequency = 100 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 1 MHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			UI
	Jitter frequency = 10 MHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			UI
Fibre Channel Transmit Jitter Generation *(4)*, *(12)*											
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	—	—	0.23	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	—	—	0.11	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	—	—	0.33	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	—	—	0.2	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	—	—	0.52	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	—	—	0.33	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance *(4)*, *(13)*											
Deterministic jitter FC-1	Pattern = CJTPAT	> 0.37			> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT	> 0.31			> 0.31			> 0.31			UI
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 2 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Deterministic jitter FC-2	Pattern = CJTPAT		> 0.33			> 0.33			> 0.33		UI
Random jitter FC-2	Pattern = CJTPAT		> 0.29			> 0.29			> 0.29		UI
Sinusoidal jitter FC-2	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI
Deterministic jitter FC-4	Pattern = CJTPAT		> 0.33			> 0.33			> 0.33		UI
Random jitter FC-4	Pattern = CJTPAT		> 0.29			> 0.29			> 0.29		UI
Sinusoidal jitter FC-4	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI
XAUI Transmit Jitter Generation *(5)*											
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance *(5)*											
Total jitter	—		> 0.65			> 0.65			> 0.65		UI
Deterministic jitter	—		> 0.37			> 0.37			> 0.37		UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(6)*											
Total jitter at 2.5 Gbps (Gen1)—×1, ×4, and ×8	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)—×1, ×4, and ×8 *(14)*	Compliance pattern	—	—	0.25	—	—	0.25	—	—	—	UI
PCI Express Receiver Jitter Tolerance *(6)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6			> 0.6			—		UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern		Compliant			Compliant			Compliant		UI
PCI Express (Gen 1) Electrical Idle Detect Threshold											
$V_{RX-IDLE-DETDIFFp-p}$ *(15)*	Compliance pattern	65	—	175	65	—	175	65	—	175	UI
Serial RapidIO Transmit Jitter Generation *(7)*											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 3 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Serial RapidIO Receiver Jitter Tolerance *(7)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation *(8)*											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance *(8)*											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(9)*											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance *(9)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	—	—	—	UI

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 4 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	—	—	—	UI
	Jitter Frequency = 1.875MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
(OIF) CEI Transmitter Jitter Generation *(10)*											
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	N/A	—	—	N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(10)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.675			N/A	—	—	N/A	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern=PRBS31 BER = 10^{-12}	> 0.988			N/A	—	—	N/A	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 5			N/A	—	—	N/A	—	—	UI
	Jitter Frequency = 3.82 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.05			N/A	—	—	N/A	—	—	UI
	Jitter Frequency = 20 MHz Data Rate= 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.05			N/A	—	—	N/A	—	—	UI

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 5 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Transmitter Jitter Generation *(11)*											
Alignment jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.2	—	—	0.2	—	—	0.2	—	—	UI
	Data Rate = 2.97 Gbps (3G) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.3	—	—	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance *(11)*											
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 2			> 2			> 2			UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3			> 0.3			> 0.3			UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3			> 0.3			> 0.3			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 1			> 1			> 1			UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 0.2			> 0.2			> 0.2			UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 0.2			> 0.2			> 0.2			UI
SAS Transmit Jitter Generation ***(16)***											
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
SAS Receiver Jitter Tolerance ***(16)***											
Total Jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	> 0.65			> 0.65			> 0.65			UI

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 6 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Deterministic Jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT		> 0.35			> 0.35			> 0.35		UI
Sinusoidal Jitter tolerance at 1.5 Gbps (G1)	Jitter Frequency = 900 KHz - 5 MHz Pattern = CJTPAT BER = 1E-12		> 0.1			> 0.1			> 0.1		UI
CPRI Transmit Jitter Generation *(17)*											
Total Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance *(17)*											
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT		> 0.66			> 0.66			> 0.66		UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT		> 0.4			> 0.4			> 0.4		UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT		> 0.65			> 0.65			> 0.65		UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT		> 0.37			> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT		> 0.55			> 0.55			> 0.55		UI
OBSAI Transmit Jitter Generation *(18)*											
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI

Table 1–29. Transceiver Block Jitter Specifications for Stratix IV GX Devices *(Note 1)*, *(2)* (Part 7 of 7)

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–4 Commercial/ Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance *(18)*											
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.37			> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.55			> 0.55			> 0.55		UI
Sinusoidal Jitter tolerance at 768 Mbps	Jitter Frequency = 5.4 KHz Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 460 MHz - 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
Sinusoidal Jitter tolerance at 1536 Mbps	Jitter Frequency = 10.9 KHz Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 921.6 MHz - 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
Sinusoidal Jitter tolerance at 3072 Mbps	Jitter Frequency = 21.8 KHz Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 1843.2 MHz - 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI

Notes to Table 1–29:

(1) Dedicated `refclk` pins were used to drive the input reference clocks.
(2) The Jitter numbers are valid for the stated conditions only.
(3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(4) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(5) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(6) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(7) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(8) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(9) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(11) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(12) The fibre channel transmitter jitter generation numbers are compliant to the specification at δ_T interoperability point.
(13) The fibre channel receiver jitter tolerance numbers are compliant to the specification at δ_R interoperability point.
(14) You must use the ATX PLL adjacent to the transceiver channels to meet the transmitter jitter generation compliance in PCI Express Gen2 ×8 modes.
(15) Stratix IV PCI Express receivers are compliant to this specification provided the $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$ of the upstream transmitter is less than 50mV.
(16) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
(17) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
(18) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Table 1–30 lists transceiver jitter specifications for protocols supported by Stratix IV GT devices.

Table 1–30. Transceiver Jitter Specifications for Protocols by Stratix IV GT Devices

Symbol/ Description	Conditions	-1 Industrial Speed Grad			-2 Industrial Speed Grade			-3 Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
XLAUI/CAUI Transmit Jitter Generation *(1)*											
Total Jitter	Pattern = PRBS-31	—	—	0.32	—	—	0.32	—	—	0.32	UI
Deterministic Jitter	Pattern = PRBS-31	—	—	0.17	—	—	0.17	—	—	0.17	UI
XLAUI/CAUI Receiver Jitter Tolerance *(1)*											
Sinusoidal Jitter tolerance	Jitter Frequency = 40 KHz Pattern = PRBS-31 BER = 1E-12	> 5			> 5			—			UI
	Jitter Frequency = 4 MHz Pattern = PRBS-31 BER = 1E-12	> 0.05			> 0.05			—			UI

Note to Table 1–30:

(1) The jitter numbers for XLAUI/CAUI are compliant to the IEEE P802.3ba specification.

Transceiver Datapath PCS Latency

For more information about:

- Basic mode PCS latency, refer to Figure 1-90 through Figure 1-97 in the *Stratix IV Transceiver Architecture* chapter.
- PCI Express (PIPE) mode PCS latency, refer to Figure 1-102 in the *Stratix IV Transceiver Architecture* chapter.
- XAUI mode PCS latency, refer to Figure 1-119 in the *Stratix IV Transceiver Architecture* chapter.
- GIGE mode PCS latency, refer to Figure 1-128 in the *Stratix IV Transceiver Architecture* chapter.
- SONET/SDH mode PCS latency, refer to Figure 1-136 in the *Stratix IV Transceiver Architecture* chapter.
- SDI mode PCS latency, refer to Figure 1-141 in the *Stratix IV Transceiver Architecture* chapter.
- (OIF) CEI PHY mode PCS latency, refer to Figure 1-143 in the *Stratix IV Transceiver Architecture* chapter.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), TriMatrix, configuration, and JTAG specifications.

Clock Tree Specifications

Table 1–31 lists the clock tree specifications for Stratix IV devices.

Table 1–31. Clock Tree Performance for Stratix IV Devices—Preliminary

Performance				Unit
Symbol	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade	
GCLK and RCLK	800	700	500	MHz
PCLK	550	500	450	MHz

For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

PLL Specifications

Table 1–32 describes the Stratix IV PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

Table 1–32. PLL Specifications for Stratix IV Devices (Part 1 of 3)—Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–2/–2x speed grade)	5	—	800 *(1)*	MHz
	Input clock frequency (–3 speed grade)	5	—	717 *(1)*	MHz
	Input clock frequency (–4 speed grade)	5	—	717 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range (–2 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–3 speed grade)	600	—	1300	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–2/–2x speed grade)	—	—	800 *(2)*	MHz
	Output frequency for internal global or regional clock (–3 speed grade)	—	—	717 *(2)*	MHz
	Output frequency for internal global or regional clock (–4 speed grade)	—	—	717 *(2)*	MHz
f_{OUT_EXT}	Output frequency for external clock output (–2 speed grade)	—	—	800 *(2)*	MHz
	Output frequency for external clock output (–3 speed grade)	—	—	717 *(2)*	MHz
	Output frequency for external clock output (–4 speed grade)	—	—	717 *(2)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain	—	3.5	—	scanclk cycles

Table 1–32. PLL Specifications for Stratix IV Devices (Part 2 of 3)—Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth *(6)*	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} *(3)*	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} *(4)*	Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC} *(4)*	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} *(4)*, *(7)*	Period Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} *(4)*, *(7)*	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ *(4)*, *(5)*	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$MHz)	—	—	25	mUI (p-p)

Table 1–32. PLL Specifications for Stratix IV Devices (Part 2 of 3)—Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth *(6)*	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} *(3)*	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} *(4)*	Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC} *(4)*	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} *(4)*, *(7)*	Period Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} *(4)*, *(7)*	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ *(4)*, *(5)*	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$MHz)	—	—	25	mUI (p-p)

Table 1–32. PLL Specifications for Stratix IV Devices (Part 3 of 3)—Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 us	—	—	±10	%

Notes to Table 1–32:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you need to provide a clean clock source that is less than 120 ps.

(4) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404 % confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in **Table 1–47 on page 1–52.**

(5) The cascaded PLL specification is only applicable with the following condition:

a. Upstream PLL: 0.59Mhz ≤Upstream PLL BW < 1 MHz

b. Downstream PLL: Downstream PLL BW > 2 MHz

(6) High bandwidth PLL settings are not supported in external feedback mode.

(7) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–45 on page 1–52.

DSP Block Specifications

Table 1–33 shows the Stratix IV DSP block performance specifications.

Table 1–33. Block Performance Specifications for Stratix IV DSP Devices *(Note 1)*—Preliminary

Mode	Resources Used	Performance			Unit
	Number of Multipliers	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade	
9×9-bit multiplier	1	520	460	400	MHz
12×12-bit multiplier	1	540	500	440	MHz
18×18-bit multiplier	1	600	550	480	MHz
36×36-bit multiplier	1	480	440	380	MHz
18×18-bit multiply accumulator	4	490	440	380	MHz
18×18-bit multiply adder	4	510	470	410	MHz
18×18-bit multiply adder-signed full precision	2	490	450	390	MHz
18×18-bit multiply adder with loopback *(2)*	2	390	350	310	MHz
36-bit shift (32-bit data)	1	490	440	380	MHz
Double mode	1	480	440	380	MHz

Notes to Table 1–33:

(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.

(2) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

TriMatrix Memory Block Specifications

Table 1–34 lists the Stratix IV TriMatrix memory block specifications.

Table 1–34. TriMatrix Memory Block Performance Specifications for Stratix IV Devices—Preliminary *(Note 1)* (Part 1 of 2)

Memory	Mode	Resources Used		Performance				
		ALUTs	TriMatrix Memory	–2 /–2× Commercial/ Industrial Speed Grade (MHz)	–3 Commercial/ Industrial Speed Grade (MHz)	–4 Commercial/ Industrial Speed Grade (MHz)	–3 Industrial Speed Grade (MHz) *(2)*	–4 Industrial Speed Grade (MHz) *(2)*
MLAB *(3)*	Single port 64×10	0	1	600	500	450	500	450
	Simple dual-port 32×20	0	1	600	500	450	500	450
	Simple dual-port 64×10	0	1	600	500	450	500	450
	ROM 64×10	0	1	600	500	450	500	450
	ROM 32×20	0	1	600	500	450	500	450
M9K Block *(3)*	Single-port 256×36	0	1	600	540	475	540	475
	Simple dual-port 256×36	0	1	550	490	420	490	420
	Simple dual-port 256×36, with the read-during-write option set to **Old Data**	0	1	375	340	300	340	300
	True dual port 512×18	0	1	490	430	370	430	370
	True dual-port 512×18, with the read-during-write option set to **Old Data**	0	1	375	335	290	335	290
	ROM 1 Port	0	1	600	540	475	540	475
	ROM 2 Port	0	1	600	540	475	540	475
	Min Pulse Width (clock high time)	—	—	750	800	850	800	850
	Min Pulse Width (clock low time)	—	—	500	625	690	625	690

Table 1–34. TriMatrix Memory Block Performance Specifications for Stratix IV Devices—Preliminary *(Note 1)* (Part 2 of 2)

Memory	Mode	Resources Used		Performance				
		ALUTs	TriMatrix Memory	–2 /–2× Commercial/ Industrial Speed Grade (MHz)	–3 Commercial/ Industrial Speed Grade (MHz)	–4 Commercial/ Industrial Speed Grade (MHz)	–3 Industrial Speed Grade (MHz) *(2)*	–4 Industrial Speed Grade (MHz) *(2)*
M144K *(3)*	Single-port 2K×72	0	1	475	440	380	400	350
	Simple dual-port 2K×72	0	1	465	435	385	375	325
	Simple dual-port 2K×72, with the read-during-write option set to **Old Data**	0	1	260	240	205	225	200
	Simple dual-port 2K×64 (with ECC)	0	1	335	300	255	295	250
	True dual-port 4K×36	0	1	400	375	330	350	310
	True dual-port 4K×36, with the read-during-write option set to **Old Data**	0	1	245	230	205	225	200
	ROM 1 Port	0	1	540	500	435	450	420
	ROM 2 Port	0	1	500	465	400	425	400
	Min Pulse Width (clock high time)	—	—	700	755	860	860	950
	Min Pulse Width (clock low time)	—	—	500	625	690	690	690

Notes to Table 1–34:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) This is only applicable to the Stratix IV E and GX devices.

(3) When you use the error detection CRC feature, there is no degradation in F_{MAX}.

For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

Configuration and JTAG Specifications

Table 1–35 lists the Stratix IV configuration mode specifications.

Table 1–35. Configuration Mode Specifications for Stratix IV Devices—Preliminary

Programming Mode	DCLK F_{MAX}	Unit
Passive serial	125	MHz
Fast passive parallel	125	MHz
Fast active serial	40	MHz
Remote update only in fast AS mode	10	MHz

Table 1–36 shows the JTAG timing parameters and values for Stratix IV devices.

Table 1–36. JTAG Timing Parameters and Values for Stratix IV Devices —Preliminary

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 *(1)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(1)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(1)*	ns

Note to Table 1–36:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Temperature Sensing Diode Specifications

Table 1–37 lists the specifications for the Stratix IV temperature sensing diode.

Table 1–37. External Temperature Sensing Diode Specifications—Preliminary

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	500	µA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 5	Ω
Diode ideality factor	—	—	1.030	—

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-LVTTL/LVCMOS are capable of typical 167 MHz and 1.2 LVCMOS at 100 MHz interfacing frequency with 10 pF load.

Actual achievable frequency depends on design- and system-specific factors. You need to perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1–38 shows high-speed I/O timing for Stratix IV devices.

Table 1–38. High-Speed I/O Specifications *(Note 1), (2), (10)* (Part 1 of 2)—Preliminary

Symbol	Conditions	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 *(3)*	5	—	800	5	—	717	5	—	717	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards *(9)*	Clock boost factor W = 1 to 40 *(3)*	5	—	800	5	—	717	5	—	717	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards *(9)*	Clock boost factor W = 1 to 40 *(3)*	5	—	520	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	800 *(7)*	5	—	717 *(7)*	5	—	717 *(7)*	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 *(8)*	*(4)*	—	1600	*(4)*	—	1250	*(4)*	—	1250	Mbps
	SERDES factor J = 2, Uses DDR Registers	*(4)*	—	*(4)*	*(4)*	—	*(4)*	*(4)*	—	*(4)*	Mbps
	SERDES factor J = 1, Uses SDR Register	*(4)*	—	*(4)*	*(4)*	—	*(4)*	*(4)*	—	*(4)*	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) *(5)*	SERDES factor J = 4 to 10	*(4)*	—	1250	*(4)*	—	1152	*(4)*	—	800	Mbps
Emulated Differential I/O Standards with One External Output Resistor - f_{HSDR} (data rate)		*(4)*	—	311	*(4)*	—	200	*(4)*	—	200	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps - 1.6 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.25	UI

Table 1–38. High-Speed I/O Specifications *(Note 1), (2), (10)* (Part 2 of 2)—Preliminary

Symbol	Conditions	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.125	—	—	0.15	—	—	0.15	UI
t_{DUTY}	Tx output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor	—	—	460	—	—	500	—	—	500	ps
TCCS	True Differential I/O Standards	—	—	100	—	—	100	—	—	100	ps
	Emulated Differential I/o Standards	—	—	250	—	—	250	—	—	250	ps
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	—	1600	150	—	1250	150	—	1250	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	*(4)*		*(6)*	*(4)*		*(6)*	*(4)*		*(6)*	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	± PPM
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 1–38:

(1) When J = 3 to 10, use the SERDES block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You should consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.

(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(9) This only applies to DPA and soft-CDR modes.

(10) This only applies to LVDS source synchronous mode.

For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

Table 1–39 lists the DPA lock time specifications for Stratix IV ES devices.

Table 1–39. DPA Lock Time Specifications—Stratix IV ES Devices Only *(Note 1)*, *(2)*, *(3)*

Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetitions per 256 data transitions *(4)*	Condition	Maximum
SPI-4	00000000001111111111	2	128	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles *(5)*
Parallel Rapid I/O	00001111	2	128	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles *(5)*
	10010000	4	64	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles *(5)*
Miscellaneous	10101010	8	32	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles *(5)*
	01010101	8	32	without DPA PLL calibration	256 data transitions
				with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles *(5)*

Notes to Table 1–39:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time applies to both commercial and industrial grade.
(4) This is the number of repetition for the stated training pattern to achieve 256 data transitions.
(5) Slow clock = Data rate (Mbps)/Deserialization factor.

Figure 1–4 shows the DPA lock time specifications with DPA PLL calibration enabled.

Figure 1–4. DPA Lock Time Specification with DPA PLL Calibration Enabled

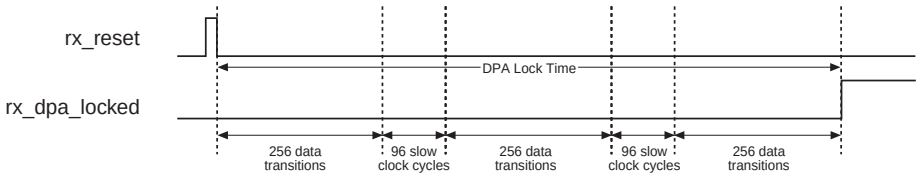


Table 1–40 lists the DPA lock time specifications for Stratix IV GX adn GT devices.

Table 1–40. DPA Lock Time Specifications—Stratix IV GX and GT Devices Only *(Note 1)*, *(2)*, *(3)*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 1–40:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in the table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1–5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to or higher than 1.25 Gbps. Table 1–41 lists this information in table form.

Figure 1–5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to or Higher Than 1.25 Gbps

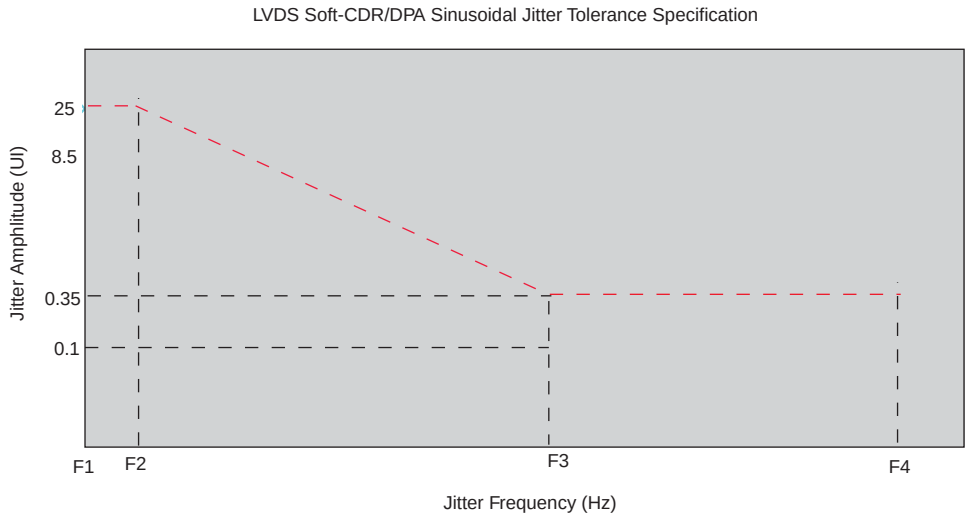


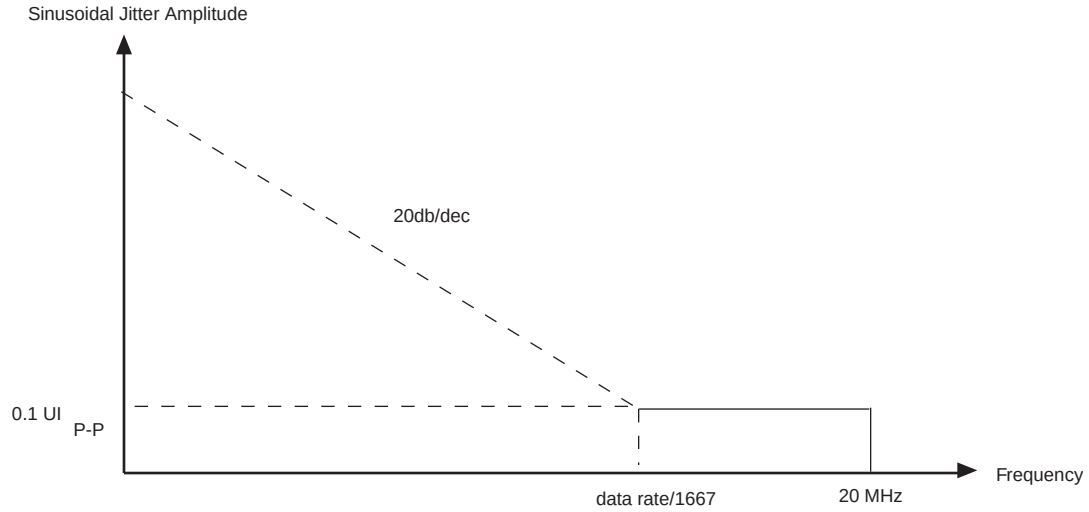
Table 1–41 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to or higher than 1.25 Gbps.

Table 1–41. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to or Higher than 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 1–6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.25 Gbps.

Figure 1–6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL and DQS Logic Block Specifications

Table 1–42 lists the DLL frequency range specifications for Stratix IV devices.

Table 1–42. DLL Frequency Range Specifications for Stratix IV Devices—Preliminary (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)			Available Phase Shift	DQS Delay Buffer Mode *(1)*	Number of Delay Chains
	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade			
0	90-140	90-130	90-120	22.5°, 45°, 67.5°, 90°	Low	16
1	120-180	120-170	120-160	30°, 60°, 90°, 120°	Low	12
2	150-220	150-210	150-200	36°, 72°, 108°, 144°	Low	10
3	180-280	180-260	180-240	45°, 90°,135°, 180°	Low	8
4	240-350	240-320	240-290	30°, 60°, 90°, 120°	High	12
5	290-430	290-380	290-360	36°, 72°, 108°, 144°	High	10
6	360-540	360-450	360-450	45°, 90°, 135°, 180°	High	8

Table 1–42. DLL Frequency Range Specifications for Stratix IV Devices—Preliminary (Part 2 of 2)

Frequency Mode	Frequency Range (MHz)			Available Phase Shift	DQS Delay Buffer Mode *(1)*	Number of Delay Chains
	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade			
7	470-700	470-630	470-590	60°, 120°, 180°, 240°	High	6

Note to Table 1–42:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

☞ For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

Table 1–43 describes the DQS phase offset delay per stage for Stratix IV devices.

Table 1–43. DQS Phase Offset Delay Per Setting for Stratix IV Devices *(Note 1)*, *(2)*, *(3)*

Speed Grade	Min	Max	Unit
–2/–2×	7	13	ps
–3	7	15	ps
–4	7	16	ps

Notes to Table 1–43:

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear, with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10 phase offset settings to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10.5 ps) ± 20 ps] = 730 ps ± 20 ps.

☞ For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

Table 1–44 lists the DQS phase shift error for Stratix IV devices.

Table 1–44. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix IV Devices *(Note 1)*

Number of DQS Delay Buffer	–2/–2X Speed Grade	–3 Speed Grade	–4 Speed Grade	Unit
1	26	28	30	ps
2	52	56	60	ps
3	78	84	90	ps
4	104	112	120	ps

Note to Table 1–44:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2/–2x speed grade is ± 78 ps or ± 39 ps.

☞ For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

Table 1–45 lists the memory output clock jitter specifcations for Stratix IV devices.

Table 1–45. Memory Output Clock Jitter Specification for Stratix IV Devices *(Note 1), (2), (3)*

Parameter	Clock Network	Symbol	–2/–2X Speed Grade		–3 Speed Grade		–4 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	-75	75	-85	85	-100	100	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	-150	150	-170	170	-190	190	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	-80	80	-90	90	-100	100	ps
Clock period jitter	Global	$t_{JIT(per)}$	-113	113	-128	128	-150	150	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-225	225	-255	255	-285	285	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-120	120	-135	135	-150	150	ps

Notes to Table 1–45:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.

(3) The memory output clock jitter stated in Table 1–45 is applicable when an input jitter of 30 ps is applied.

For the Stratix IV GT –1 and –2 speed grade specifications, refer to the –2/–2× speed grade column. For the Stratix IV GT –3 speed grade specifcation, refer to the –3 speed grade column.

OCT Calibration Block Specifications

Table 1–46 lists the OCT calibration block specifications for Stratix IV devices.

Table 1–46. OCT Calibration Block Specifications for Stratix IV Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	28	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T	—	2.5	—	ns

Duty Cycle Distortion (DCD) Specifications

Table 1–47 lists the worst-case DCD for Stratix IV devices.

Table 1–47. Worst-Case DCD on Stratix IV I/O Pins

Symbol	–2/–2× Speed Grade		–3 Speed Grade		–4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

I/O Timing

Altera offers two ways to determine I/O timing: the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

The Excel-based I/O Timing spreadsheet is downloadable from the Stratix IV Devices Literature webpage.

Programmable IOE Delay

Table 1–48 shows Stratix IV IOE programmable delay settings.

Table 1–48. IOE Programmable Delay for Stratix IV Devices

Parameter *(1)*	Available Settings	Min Offset *(2)*	Fast Model		Slow Model					
			Industrial	Commercial *(3)*	C2 *(3)*	C3	C4	I3	I4	Unit
D1	15	0	0.462	0.505	0.732	0.795	0.857	0.801	0.864	ps
D2	7	0	0.234	0.232	0.337	0.372	0.407	0.371	0.405	ps
D3	7	0	1.700	1.769	2.695	2.927	3.157	2.948	3.178	ps
D4	15	0	0.508	0.554	0.813	0.882	0.952	0.889	0.959	ps
D5	15	0	0.473	0.500	0.746	0.812	0.875	0.818	0.882	ps
D6	6	0	0.186	0.195	0.294	0.319	0.345	0.321	0.347	ps

Notes to Table 1–48:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
(2) Minimum offset does not include the intrinsic delay.
(3) For the EP4SGX530 device density, the IOE programmable delays have an additional 5% maximum offset.

Programmable Output Buffer Delay

Table 1–49 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 1–49. Programmable Output Buffer Delay *(Note 1)*

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Note to Table 1–49:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 1–50 shows the glossary for this chapter.

Table 1–50. Glossary Table (Part 1 of 4)

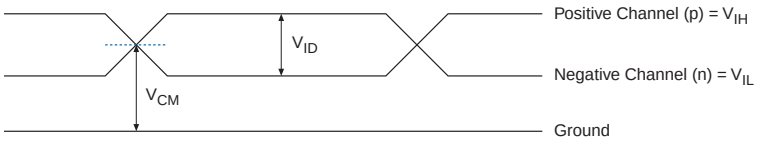
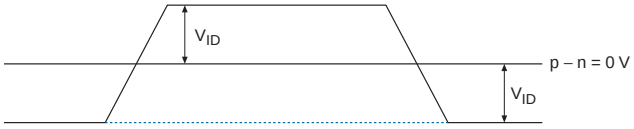
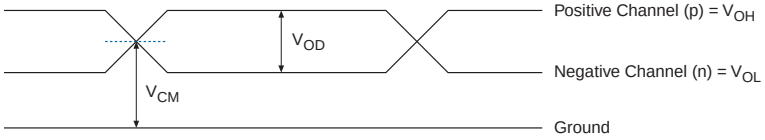
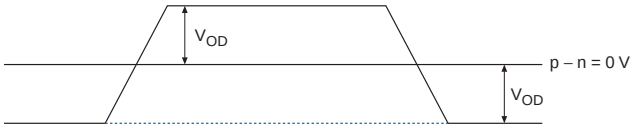
Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G	—	—
H	—	—
I	—	—

Table 1–50. Glossary Table (Part 2 of 4)

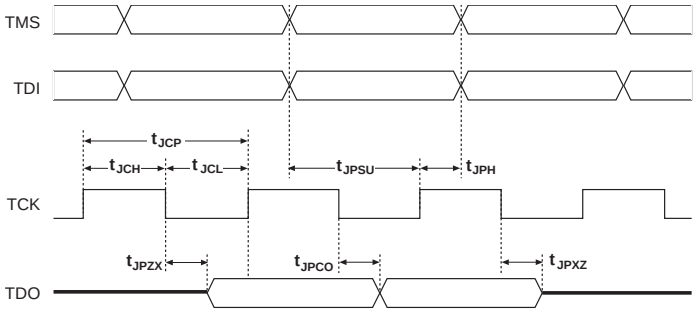
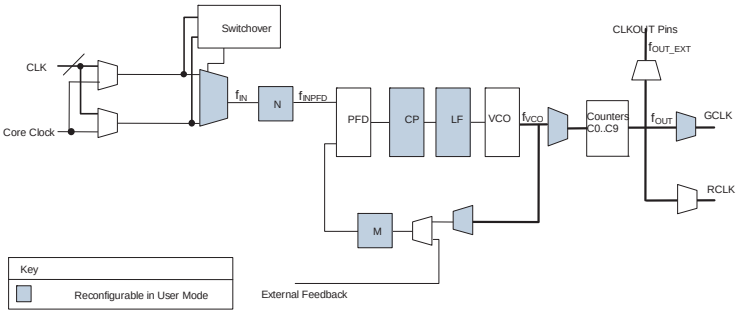
Letter	Subject	Definitions
J	J	High-speed I/O block: Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Stratix IV device).

Table 1–50. Glossary Table (Part 3 of 4)

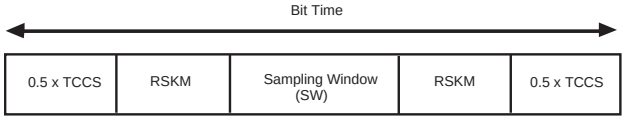
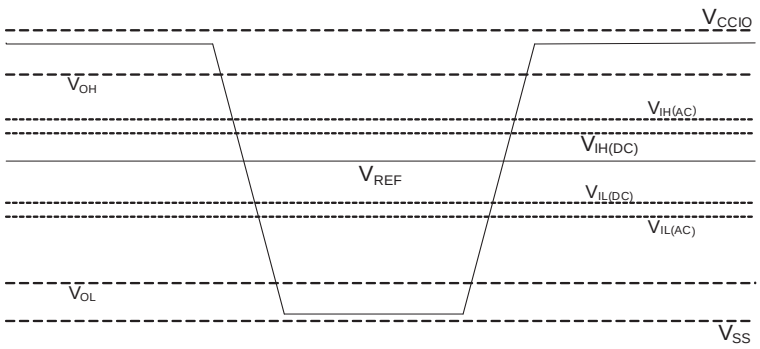
Letter	Subject	Definitions
S	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTI and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—

Table 1–50. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block: Clock Boost Factor
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1–51 shows the revision history for this chapter.

Table 1–51. Document Revision History

Date	Document Version	Changes Made
February 2010	4.1	■ Updated Table 1–11, Table 1–22, Table 1–23, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–29, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–38, Table 1–39, Table 1–42, Table 1–45, and Table 1–48. ■ Added Stratix IV GT speed grade note to Table 1–31, Table 1–34, Table 1–38, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. ■ Added Table 1–28 and Table 1–30. ■ Minor text edits.
November 2009	4.0	■ Added Table 1–9, Table 1–15, Table 1–38, and Table 1–39. ■ Added Figure 1–5 and Figure 1–6. ■ Added the “Transceiver Datapath PCS Latency” section. ■ Updated the “Electrical Characteristics”, “Operating Conditions”, and “I/O Timing” sections. ■ All tables updated except Table 1–16, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–33, Table 1–34, and Table 1–45. ■ Updated Figure 1–2 and Figure 1–3. ■ Updated Equation 1–1. ■ Deleted Table 1-28, Table 1-29, Table 1-30, Table 1-42, Table 1-43, and Table 1-44. ■ Minor text edits.
June 2009	3.1	■ Added “Preliminary Specifications” to the footer of each page. ■ Updated Table 1–1, Table 1–2, Table 1–7, Table 1–10, Table 1–11, Table 1–12, Table 1–21, Table 1–22, Table 1–23, Table 1–25, Table 1–37, Table 1–38, Table 1–39, Table 1–40, and Table 1–44. ■ Minor text edits.
March 2009	3.0	■ Replaced Table 1–31 and Table 1–37. ■ Updated Table 1–1, Table 1–2, Table 1–5, Table 1–19, Table 1–41, Table 1–44, Table 1–45, Table 1–49, and Table 1–51. ■ Added Table 1–21, Table 1–46, and Table 1–47 ■ Added Figure 1–3. ■ Removed “Timing Model”, “Preliminary and Final Timing”, “I/O Timing Measurement Methodology”, “I/O Default Capacitive Loading”, and “Referenced Documents” sections.
December 2009	2.1	Minor changes.
November 2008	2.0	■ Minor text edits. ■ Updated Table 1–19, Table 1–32, Table 1–34 - Table 1–39. ■ Minor text edits.

Table 1–51. Document Revision History

Date	Document Version	Changes Made
August 2008	1.1	■ Updated Table 1–1, Table 1–2, Table 1–4, Table 1–5, and Table 1–26. ■ Removed figures from "Transceiver Performance Specifications" on page 1–10 that are repeated in the glossary. ■ Minor text edits and an additional note to Table 1–26.
May 2008	1.0	Initial release.

2. Addendum to the Stratix IV Device Handbook

SIV54002-1.1

This chapter describes changes to the published version of the *Stratix IV Device Handbook*. It describes the following:

- V_{CCAUX} power supply setting for the power-on reset (POR) circuitry (including a correction to the POR signal pulse width delay times)
- Correct power-up sequence
- On-chip termination (OCT) assignment summary
- JTAG pull-up resistor value specification

Table 2–1 lists the changes and related chapters described in this addendum.

Table 2–1. Changes to the Stratix IV Handbook

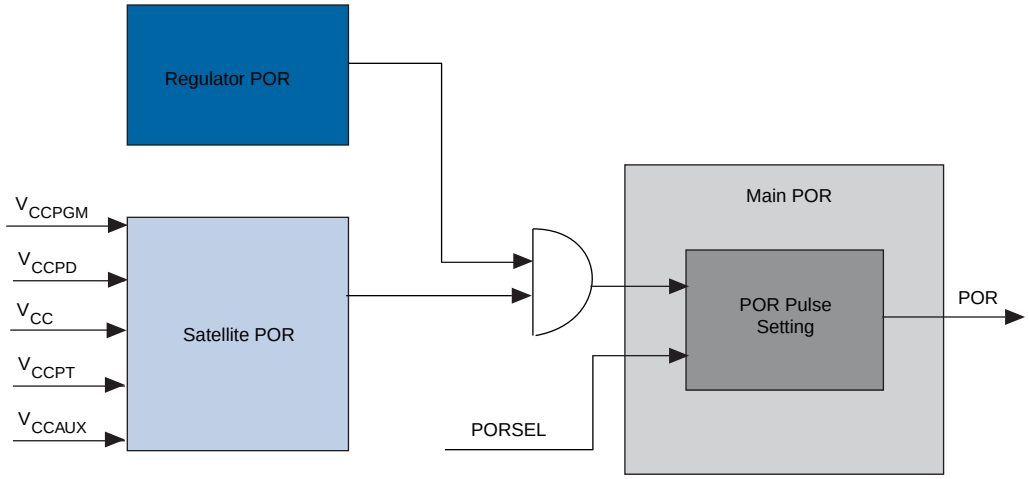
Change	Chapter
Power-On Reset Circuitry	*Hot Socketing and Power-On Reset in Stratix IV Devices*
Power-On Reset Specifications	*Hot Socketing and Power-On Reset in Stratix IV Devices*
Correct Power-Up Sequence for Production Devices	*Hot Socketing and Power-On Reset in Stratix IV Devices*
Power-On Reset Circuit	*Configuration, Design Security, Remote System Upgrades with Stratix IV Devices*
Summary of OCT Assignments	*I/O Features in Stratix IV Devices*
JTAG TMS and TDI Pin Pull-Up Resistor Value Specification	*Configuration, Design Security, Remote System Upgrades with Stratix IV Devices*

Any information not contained in this addendum is considered the same as the information contained in the published version of the *Stratix IV Device Handbook*.

Power-On Reset Circuitry

Figure 2–1 shows the addition of the V_{CCAUX} power supply to "Figure 9-2: Simplified POR Diagram for Stratix IV Devices".

Figure 2–1. Simplified POR Diagram for Stratix IV Devices



Power-On Reset Specifications

Table 2–2 lists the addition of the V_{CCAUX} power supply setting to "Table 9-1: Power Supplies Monitored by the POR Circuitry".

Table 2–2. Power Supplies Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V_{CCAUX}	Auxiliary supply for the programmable power technology	2.5

All power supply specifications not contained in this addendum remain the same as in "Table 9-1: Power Supplies Monitored by the POR Circuitry" of the *Hot Socketing and Power-On Reset in Stratix IV Devices* chapter.

Correction to POR Signal Pulse Width Delay Times

Table 2–3 lists the corrected POR signal pulse delay times (the changes are shown in bold).

Table 2–3. Corrections to Chapter 9: Hot Socketing and Power-On Reset in Stratix IV Devices

Page #	Section Name	Change
Page 5	Power-On Reset Specifications	**Corrected:** When the PORSEL pin is connected to GND, the POR delay time is **100 to 300 ms**. When the PORSEL pin is set to high, the POR delay time is **4 to 12 ms**.

Correct Power-Up Sequence for Production Devices

In order to successfully power-up and to exit POR on production Stratix IV devices, you must fully power up V_{CC} before V_{CCAUX} begins to ramp. Table 2–4 lists the corrections made to the *Hot Socketing and Power-On Reset in Stratix IV Devices* chapter in order to record this new specification (the changes are shown in bold).

Table 2–4. Corrections to Chapter 9: Hot Socketing and Power-On Reset in Stratix IV Devices

Page #	Section Name	Change
Page 1	Second Paragraph	Stratix IV devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of external devices **(provided V_{CC} powers up fully before V_{CCAUX})**.
	Third Paragraph	**Removed:** With the Stratix IV hot-socketing feature, you no longer have to ensure a proper power-up sequence for each device on the board.
	Second bullet	Support for any power-up sequence **(with the exception that V_{CC} must power up fully before V_{CCAUX} for all Stratix IV production devices)**.
	Stratix IV Hot-Socketing Specifications	Stratix IV devices are hot-socketing compliant **(provided V_{CC} powers up fully before V_{CCAUX})** without the need for external components or special design requirements.
Page 2	Stratix IV Devices can be Driven Before Power Up	**Removed:** Stratix IV devices support power-up or power-down of the V_{CCIO}, V_{CC}, V_{CCPGM}, and V_{CCPD} power supplies in any sequence in order to simplify system-level design.
	Insertion or Removal of a Stratix IV Device from a Powered-up System	**Added: To successfully power-up and exit POR on production devices, fully power V_{CC} before V_{CCAUX} begins to ramp.**
		Removed: For more information about the hot-socketing specification, refer to the *DC and Switching Characteristics* and the *Hot Socketing and Power Sequencing Feature and Testing for Altera Devices* white paper.
	Hot-Socketing Feature Implementation in Stratix IV Devices	The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, **V_{CCAUX}**, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. The hot-socketing circuitry generates an internal HOTSCKT signal when the V_{CC}, **V_{CCAUX}**, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies are below the threshold voltage.
Page 3		The POR circuit monitors the voltage level of the power supplies (V_{CC}, **V_{CCAUX}**, V_{CCIO}, V_{CCPGM}, or V_{CCPD}) and keeps the I/O pins tri-stated until the device is in user mode.
		The 3.0-V tolerance control circuit permits the I/O pins to be driven by 3.0 V before the V_{CC}, **V_{CCAUX}**, V_{CCIO}, V_{CCPGM}, or V_{CCPD} supplies are powered.
		Added: **To successfully power-up and exit POR on production devices, fully power V_{CC} before V_{CCAUX} begins to ramp.**
Page 4	Power-On Reset Circuitry	**Added: The satellite POR also monitors the V_{CCAUX} power supply which is the auxiliary supply for the programmable power technology.**

All the power-on reset sequence specifications not contained in this addendum remain the same as in the *Hot Socketing and Power-On Reset in Stratix IV Devices* chapter.

Power-On Reset Circuit

Table 2–5 lists the addition of V_{CCAUX} to the power-on reset information (the change is shown in bold).

Table 2–5. Correction to Chapter 10: Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices

Page #	Section Name	Change
Page 4	Power-On Reset Circuit	After power-up, the device does not release nSTATUS until **V_{CC}, V_{CCAUX}, V_{CCPT}, V_{CCPGM},** and **V_{CCPD}** are above the device's POR trip point. On power down, brown-out occurs if the **V_{CC}, V_{CCAUX}, V_{CCPT}, V_{CCPGM},** or **V_{CCPD} drops below the threshold voltage.**

All the power-on reset circuit information not contained in this addendum remains the same as in the *Configuration, Design Security, Remote System Upgrades with Stratix IV Devices* chapter.

Summary of OCT Assignments

Table 2–6 lists the OCT assignments for the Quartus II software version 9.1 and later.

Table 2–6. Summary of OCT Assignments in the Quartus II Software

Assignment Name	Value	Applies To
Input Termination	Parallel 50 Ω with calibration	Input buffers for single-ended and differential HSTL/SSTL standards
	Differential	Input buffers for LVDS receivers on row I/O banks *(1)*
Output Termination	Series 25 Ω without calibration	Output buffers for single-ended LVTTL/LVCMOS and HSTL/SSTL standards as well as differential HSTL/SSTL standards
	Series 50 Ω without calibration	
	Series 25 Ω with calibration	
	Series 40 Ω with calibration	
	Series 50 Ω with calibration	
	Series 60 Ω with calibration	

Note to Table 2–6:

(1) You can enable differential OCT R_D in row I/O banks when both V_{CCIO} and V_{CCPD} are set to **2.5 V**.

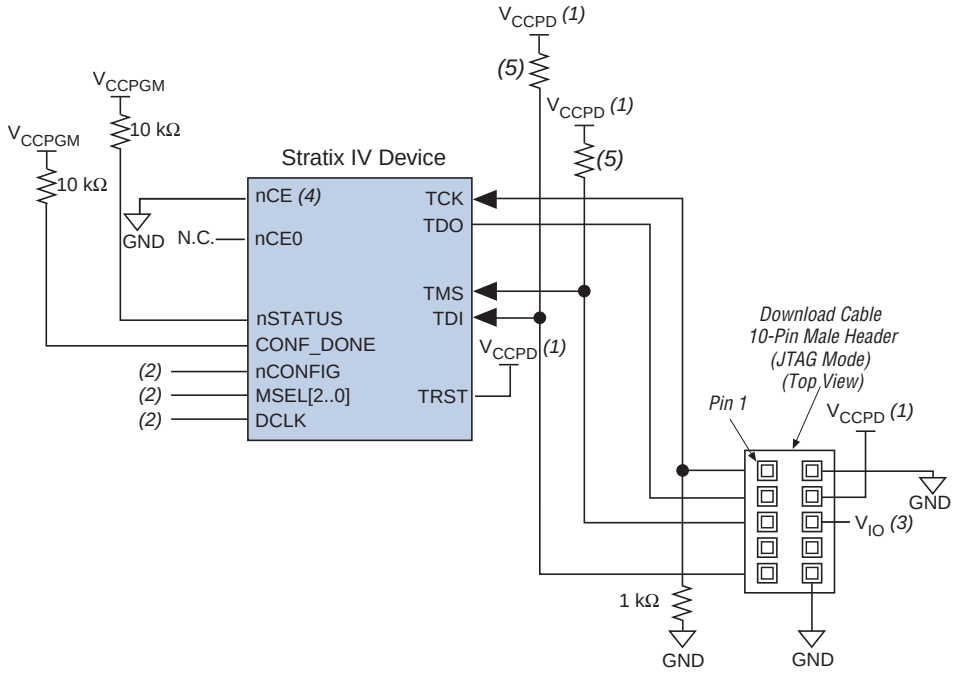
All on-chip termination support and I/O termination schemes not contained in this addendum remain the same as in the *I/O Features in Stratix IV Devices* chapter.

JTAG TMS and TDI Pin Pull-Up Resistor Value Specification

This correction changes the current JTAG TMS and TDI pin pull-up resistor value specification from 10 kΩ to a range of from 1 k to 10 kΩ .

Figure 2–2 shows the addition of Note 5 to "Figure 10-16: JTAG Configuration of a Single Device Using a Download Cable" found in the *JTAG Configuration* section of the *Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices* chapter (the change is shown in bold).

Figure 2–2. JTAG Configuration of a Single Device Using a Download Cable



Notes to Figure 2–2:

(1) Connect the pull-up resistor to the same supply voltage as the USB Blaster, MasterBlaster (VIO pin), ByteBlaster II, ByteBlasterMV, or EthernetBlaster cable. The voltage supply can be connected to the V_{CCPD} of the device.

(2) Connect the nCONFIG and MSEL[2..0] pins to support a non-JTAG configuration scheme. If you only use the JTAG configuration, connect nCONFIG to V_{CCPGM} and MSEL[2..0] to GND. Pull DCLK either high or low, whichever is convenient on your board.

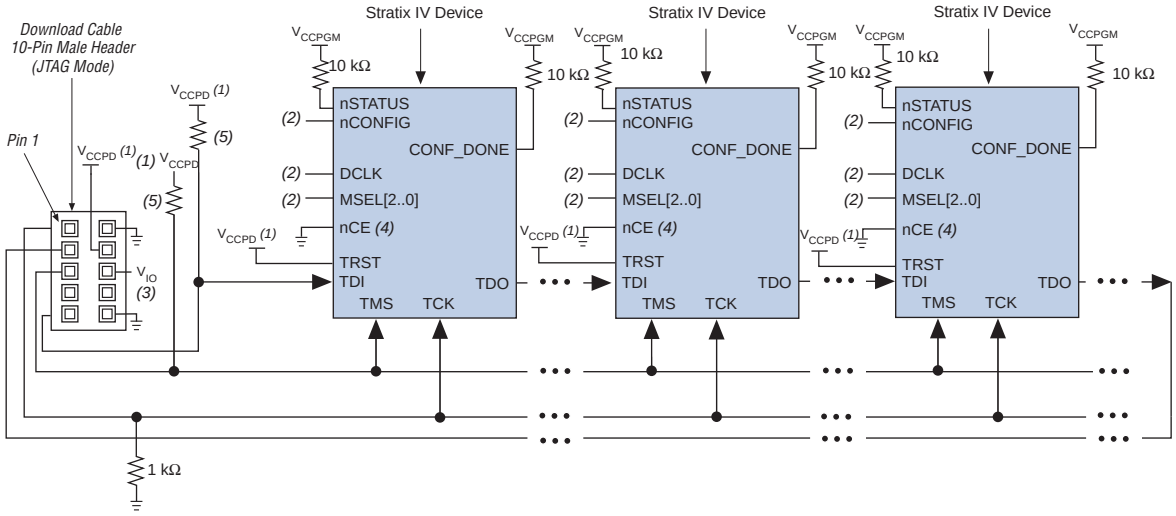
(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the device's V_{CCPD}. For more information about this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the USB-Blaster, ByteBlaster II, and ByteBlasterMV cable, this pin is a no connect.

(4) You must connect nCE to GND or driven low for successful JTAG configuration.

(5) **The pull-up resistor value can vary from 1 k to 10 kΩ.**

Figure 2–3 shows the addition of Note 5 to "Figure 10-17: JTAG Configuration of Multiple Devices Using a Download Cable" found in the *JTAG Configuration* section of the *Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices* chapter (the change is shown in bold).

Figure 2–3. JTAG Configuration of Multiple Devices Using a Download Cable



Notes to Figure 2–3:

(1) Connect the pull-up resistor to the same supply voltage as the USB Blaster, MasterBlaster (V_{IO} pin), ByteBlaster II, ByteBlasterMV, or EthernetBlaster cable. Connect the voltage supply to V_{CCPD} of the device.

(2) Connect the nCONFIG and MSEL[2..0] pins to support a non-JTAG configuration scheme. If you only use JTAG configuration, connect nCONFIG to V_{CCPGM} and MSEL[2..0] to GND. Pull DCLK either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the device's V_{CCPD}. For more information about this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the USB-Blaster, ByteBlaster II, and ByteBlasterMV cables, this pin is a no connect.

(4) You must connect nCE to GND or drive it low for successful JTAG configuration.

(5) **The pull-up resistor value can vary from 1 k to 10 kΩ.**

All other JTAG configuration specifications not contained in this addendum remain the same as in the *Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices* chapter.

Document Revision History

Table 2–7 shows the revision history for this chapter.

Table 2–7. Document Revision History

Date	Document Version	Changes Made
February 2010	1.1	■ Added the "Power-On Reset Circuitry", "Power-On Reset Specifications", "Correction to POR Signal Pulse Width Delay Times", "Correct Power-Up Sequence for Production Devices", "Power-On Reset Circuit", "Summary of OCT Assignments", and "JTAG TMS and TDI Pin Pull-Up Resistor Value Specification" sections. ■ Minor text edits.
November 2009	1.0	■ Stratix IV GX enhanced transceiver data rate specifications in –4 commercial speed grade. ■ Initial release.