MAX II CPLD Applications Brochure

Whether designing for communications, consumer, computing, or industrial applications, MAX® II devices offer the features designers need when developing control path applications that are constrained by cost and power budgets. MAX II devices' lower price, lower power, and higher density make them the ideal solution for complex control applications, including new applications not previously possible in CPLDs.

Using a groundbreaking new CPLD architecture, MAX II devices offer dramatic improvements over previous MAX devices:

- Half the cost
- One-tenth the power consumption
- Four times the density
- Twice the performance

These benefits allow designers to integrate multiple control path applications onto a single device. As shown in Figure 1, key control path functions can be divided into four categories: I/O expansion, interface bridging, power-up sequencing, and system configuration.

At less than half the cost of prior MAX device families, MAX II devices are based on a 0.18-µm flash process and are instant-on and non-volatile. Table 1 shows the features and packages available for the MAX II device family.

Figure 1. MAX II CPLD Application Areas

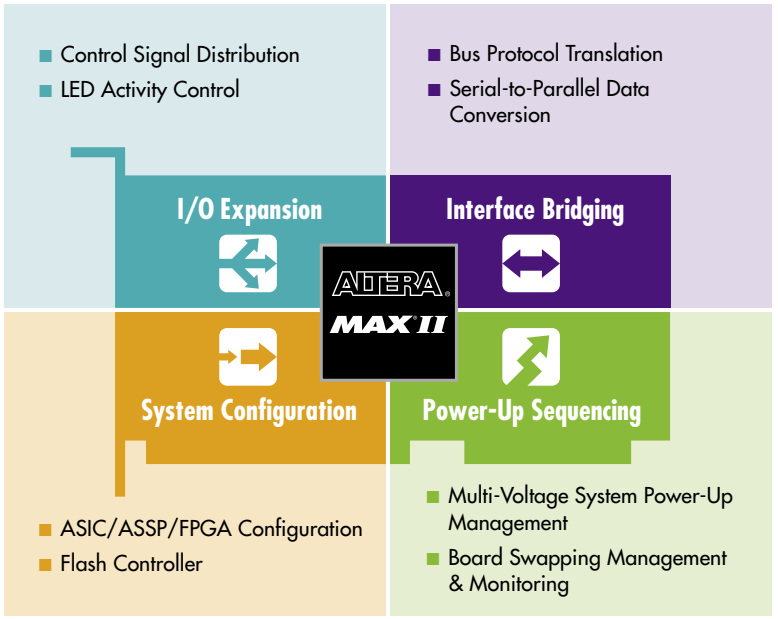


Table 1. MAX II Family Highlights

Feature	EPM240	EPM570	EPM1270	EPM2210
Logic Elements (LEs)	240	570	1,270	2,210
Typical Equivalent Macrocells	192	440	980	1,700
Maximum User I/O Pins	80	160	212	272
User Flash Memory Bits	8,192	8,192	8,192	8,192
Speed Grades	3, 4, 5	3, 4, 5	3, 4, 5	3, 4, 5
Corner-to-Corner Performance (t_{PD1})	4.7 ns	5.5 ns	6.3 ns	7.1 ns
Fastest Performance (t_{PD2})	3.8 ns	3.7 ns	3.7 ns	3.7 ns
Available Packages[1]	100-pin TQFP[2]	100-pin TQFP 144-pin TQFP 256-pin BGA[3]	144-pin TQFP 256-pin BGA[3]	256-pin BGA[3] 324-pin BGA[3]

Notes: [1] All packages support vertical migration across all densities.
[2] TQFP: thin quad flat pack.
[3] FineLine BGA® package (1.0-mm pitch).

Power-Up Sequencing

The high density of MAX II CPLDs gives designers the added logic necessary for controlling complex, system-critical power-up sequences. Power-up sequencing is the process of supplying power to other devices on the board in a sequence, ensuring that all devices operate correctly. Power-up sequencing typically consists of a multi-voltage environment with functions such as system power up, system reset, and chip-select generation. These applications are often combined into a single design that requires a non-volatile, instant-on device such as a MAX II CPLD.

In power-up sequencing, the CPLD ensures that the board powers up according to the requirements of all the devices on the board. This operation is usually comprised of a state machine controlling the timing at either predefined intervals or on receipt of ready signals from other devices on the board. As the CPLD controls all device resets on the board it usually also controls individual chip selects as well.

Multi-voltage system power up requires a device to be instantly on and ready to manage the power-up sequence for other power planes on the printed circuit board (PCB). As board complexity and the number of power planes on a board increase, the complexity of the power-up sequencing logic also increases. Table 2 describes the MAX II CPLD features that apply to power-up sequencing.

Table 2. MAX II Device Advantages: Power-Up Sequencing

Feature	Benefit
Instant-On	Manage the power-up sequences for the other devices on the PCB
MultiVolt™ Core	Operate with a 1.8-, 2.5-, or 3.3-V power supply, minimizing power rails and simplifying board design
Lowest Cost per I/O Pin	Get more I/O capability at a lower cost for controlling I/O-intensive wide buses, resets, and enabling signals
Re-Programmability	Simplify power-up sequencing development with device programmability that provides the greatest flexibility to support last-minute changes
High Density	Manage complex power-up sequencing of highly populated boards

MultiVolt Power-Up Management

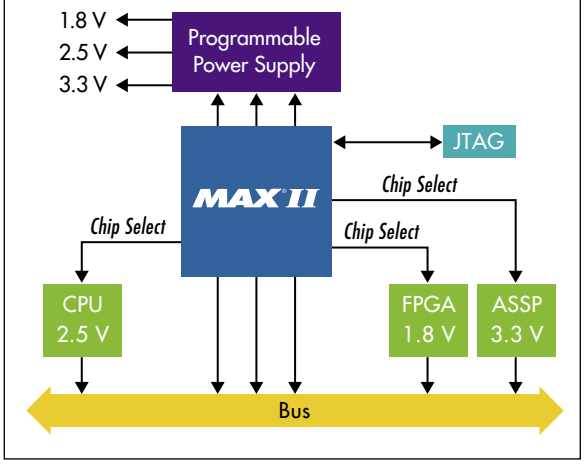
Today's boards require more voltage levels and more complex control logic for managing the power-up sequence—resulting in the need for additional logic. MAX II devices offer the highest density in a CPLD allowing it to implement complex control functions in a single device. The flexible MultiVolt I/O also enables control of critical bus functions during power up. Figure 2 illustrates a typical device power-up sequencing application. Multiple power rails support different devices, and control logic manages the complete power-up sequence of each device.

A JTAG port can also be used to monitor the power-up sequence and identify any errors via the JTAG port to the PC or test equipment. The JTAG port can also be used to set break points in the power-up sequencing, reducing engineering time during the board-level debug and verification process.

Board Swapping Management & Monitoring

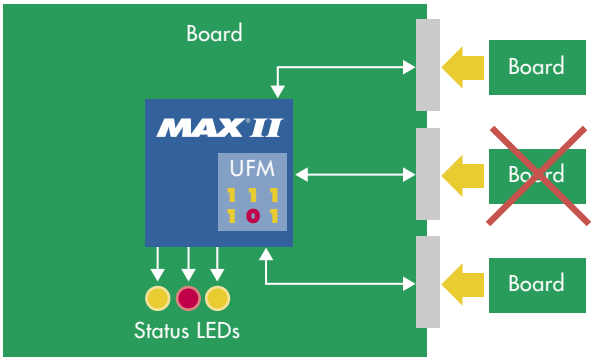
Rack systems often support backplanes with interchangeable plug-in boards. This application requires board management control on the backplane for system monitoring and hot-socketing support on the plug-in boards. In Figure 3, the MAX II device monitors the insertion and removal of boards to and from a backplane. The high current output drive capability of the MAX II device enables signal LEDs to indicate which boards are plugged into the backplane's sockets. Meanwhile, the

Figure 2. Multi-Voltage System Power-Up Management



onboard user flash memory can record a log of when each board is plugged into and out of the backplane. The MAX II device family also supports hot socketing, where devices can be plugged into and out of a live system without damage to the core or requirements for special plug layout.

Figure 3. Board Swapping Management & Monitoring



UFM: User flash memory

System Configuration & Initialization

MAX II CPLDs—with their flexible programmable interfaces, user flash memory, and parallel flash loader features—are the low cost solution for configuring and initializing volatile devices. In combination with a discrete flash memory device, MAX II CPLDs can quickly and easily configure FPGAs, digital signal processors, ASSPs, and ASICs. Unlike vendor-specific configuration devices, MAX II CPLDs can be programmed to interface to any discrete memory device to enable changes in the memory device due to availability or cost.

Table 3. MAX II Device Advantages: System Configuration & Initialization

Feature	Benefit
Non-Volatile and Instant-On Capability	Configure and initialize the power-up sequences to ensure all devices have the required configuration data before they become operational
Real-Time In-System Programmability (ISP)	Reduce programming downtime, allowing MAX II devices to operate while downloading and storing a second programming bit stream
Parallel Flash Loader	Simplify board management by using MAX II devices to configure external non-JTAG-compliant flash devices
User Flash Memory	Minimize device counts and system costs by integrating discrete serial or parallel non-volatile storage onto MAX II devices
Re-Programmability	Improve time-to-market and save future costs by interfacing with newer, cheaper flash standards as they become available

For example, when managing the configuration of an FPGA, a MAX II device can be used to implement a state machine function, which executes the configuration signals. Simultaneously, a memory controller manages the bitstream download to the FPGA. The alternative solution to using a discrete memory device and a CPLD is to use a discrete memory device and a microcontroller. Microcontrollers, though, are often limited by the number of their general purpose I/O pins.

MAX II devices additionally contain 8 Kbits of user flash memory. The user flash memory can be used to store initialization data required by ASSPs and other volatile devices. The user flash memory reduces component count and board costs by replacing small serial or parallel erasable programmable read-only memory (EEPROM) devices on the board.

Table 3 describes some MAX II device features that meet the requirements for system configuration and initialization.

FPGA Configuration Management & Flash Controller

Like other CPLDs, MAX II devices can be used to load a bitstream from a flash device into an FPGA. MAX II devices can also be used to program that bitstream into the flash device during the manufacturing process. As shown in Figure 4, the MAX II device's parallel flash loader can configure the flash device via the MAX II device JTAG pins. This feature allows non-JTAG-enabled devices to benefit from the JTAG capabilities of the MAX II CPLD family by making the JTAG circuitry available to them. This feature reduces manufacturing complexity.

As also shown in Figure 4, MAX II devices can use discrete flash memory devices to configure multiple FPGAs. This method is a cost-effective, fast, and flexible solution utilizing any shared, low-cost flash memory device on a system board. Given the high densities available in the MAX II CPLD family, extremely complex configuration schemes can be employed, including having multiple pages within the flash to reprogram the FPGA as needed.

FIFO Configuration Management

MAX II devices reduce costs and board space by combining a two-chip solution into one. As shown in Figure 5, the FIFO configuration example demonstrates how configuration data for the FIFO buffers is stored in the on-chip user flash memory rather than in an external flash memory. The stored data can include information on the number of FIFO buffers, the number of data streams, and the almost empty/almost full offsets.

Figure 5. FIFO Configuration Management

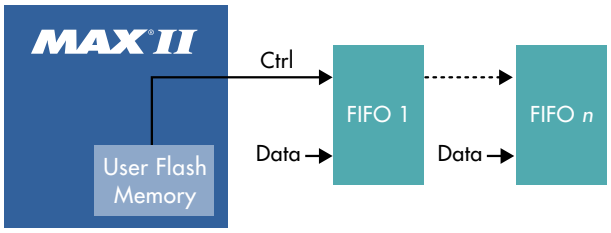
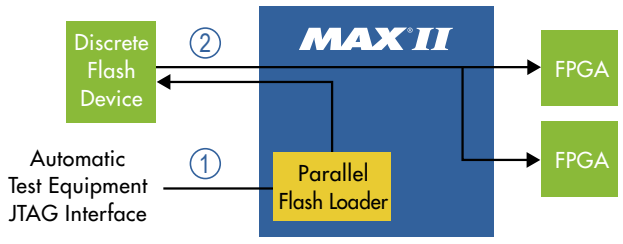


Figure 4. FPGA Configuration Management & Flash Controller



Step 1: Program via Parallel Flash Loader on MAX II Device
Step 2: Configure FPGAs

I/O Expansion

To cost-effectively increase the quantity of I/O pins on ASSPs and microcontollers, a high number of low-cost I/O pins are becoming a key requirement for many digital designs. MAX II devices offer a low-cost and flexible I/O capability for today's I/O-pin-constrained digital logic devices, including ASSPs, digital signal processors, and microcontrollers.

As semiconductor processes shrink, the I/O ring size on a standard device can dictate the unit cost of the product. Naturally, many semiconductor suppliers reduce the amount of general-purpose I/O pins to reduce the die size and cost. Simultaneously many systems are increasingly complex, requiring greater control signal distribution. Because MAX II devices are optimized to achieve the lowest cost per I/O pin, they complement I/O-deficient devices. I/O expansion applications include address-decoding functions to control signal distribution to multiple chips as well as controlling LEDs and switches.

Table 4 describes the MAX II device features that support I/O expansion applications.

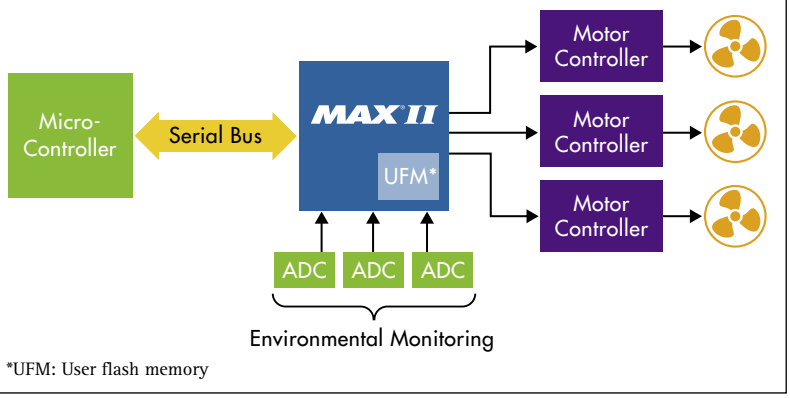
Table 4. MAX II Device Advantages: I/O Expansion

Feature	Benefit
Lowest Cost per I/O Pin	Meet the bus-width requirement I/O counts with the lowest cost per I/O pin solution in the market
Instant-On Capability	Control the power up of system-critical I/O signals to prevent system damage and erroneous signals
Second-Time Fitting	Get better pin-locked fitting by having interconnected high performance and flexible routing, even with locked pin assignments
MultiVolt I/O Interface	Interface seamlessly to other devices using multiple I/O banks supporting multiple I/O voltages, allowing for safe control of components working at different voltage levels
Re-Programmability	Improve I/O distribution—programmability gives designers the flexibility to customize the device to fit the I/O requirement of each application

Control Signal Distribution

Figure 6 shows how a microcontroller with limited I/O capabilities can control many devices in a system by using a two-wire serial bus. This application example depicts a MAX II device accepting serial bus input and distributing instructions to control multiple devices-in this case the fan motor controllers. The application can leverage the on-chip user flash memory to store data, such as the frequency or the duty cycle of the motors. Information can also be converted from parallel to serial, such as taking information from the analog-to-digital converters (ADC) in parallel and communicating it to the microcontroller via the two-wire serial bus.

Figure 6. Control Signal Distribution

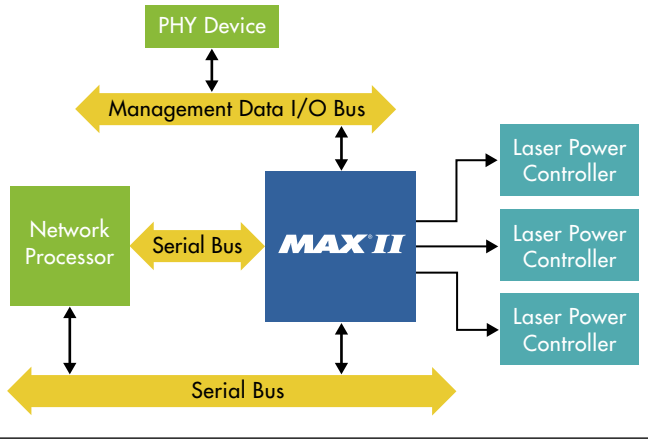


*UFM: User flash memory

Address Decoding

MAX II devices can control a large number of devices on the board with only a minimal number of inputs from the host processor. Address decoding demands high I/O pin requirements and consumes board resources. The efficiency of the MAX II device's LUT-based logic supports address decoding without wasting I/O assets. See Figure 7 for an example of address decoding in MAX II devices.

Figure 7. Address Decoding Using MAX II Devices



Interface Bridging

MAX II devices offer the lowest-cost method for translating one bus protocol into another. These applications include voltage-level shifting (e.g., from 3.3-V in to 1.8-V out), bus translation applications (such as translating a proprietary system to an industry-standard system), multipoint bus bridging, serial-to-parallel/parallel-to-serial bus conversions, and encryption.

MAX II CPLDs' efficient LUT-based architecture can implement address decoding at high frequencies. Optimized for MAX II devices, Altera's PCI Compiler MegaCore® functions enable designers to easily implement 32-bit, 66-MHz PCI master/target or target-only interfaces.

Table 5 describes MAX II device features that support interface bridging applications.

Table 5. MAX II Device Advantages: Interface Bridging

Feature	Benefit
Lowest Cost per I/O Pin	Replace low-density FPGAs for interface bridging applications with MAX II devices—offering the larger pin counts required at a more cost-effective price point
PCI Compliance	Interface to one of the most common bus systems in the industry by using MAX II devices, which support a 32-bit bus running at 66 MHz
MultiVolt I/O Interface	Meet a broad range of I/O requirements—including support for multiple I/O voltages and signal integrity functions such as programmable drive strength and slew rate adjustments
Second-Time Fitting	Get better pin-locked performance with MAX II CPLD's MultiTrack™ interconnect routing
Re-Programmability	Quickly and easily solve key system-specific problems related to bus bridging with MAX II devices

PCI Bus Bridge

MAX II devices allow designers to form a PCI bridge from one board to another. The devices may be physically separated via a cable or as part of a backplane configuration. MAX II devices can also act as repeaters for other bus systems, increasing the drive strength of the bus, and therefore, increasing the number of devices that can be included in the bus system.

As shown in Figure 8, MAX II devices enable the addition of an optional add-on board to the host PCI bus system. The two largest MAX II devices are PCI-compliant and may be added to a PCI bus as a 32-bit, 3.3-V PCI target at 66 MHz. These high-density MAX II

devices enable more complex bus applications to be supported, (e.g., PCI target functions), at a very low price point.

Multipoint Connections

Created for applications that use multipoint connections, MAX II devices can function as a crosspoint switch, as shown in Figure 9. The MAX II CPLD can be divided into three major blocks: 1) the switch matrix, for connecting any input to any output; 2) the configuration register, for configuring the connections during operation; and 3) the address decoder, for decoding the output addresses of the configuration. Because MAX II devices have the lowest cost per I/O pin, they provide the greatest cost optimization for this application.

Figure 8. PCI Bus Bridge

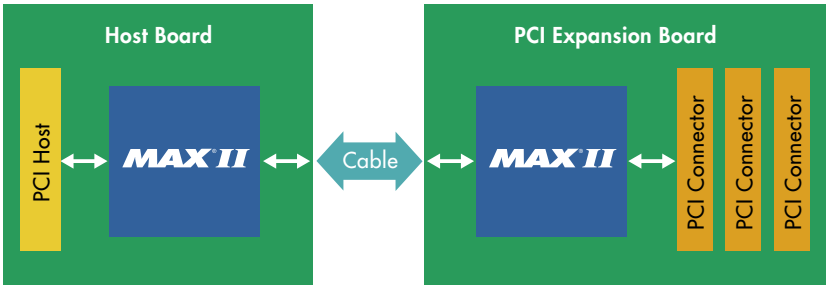
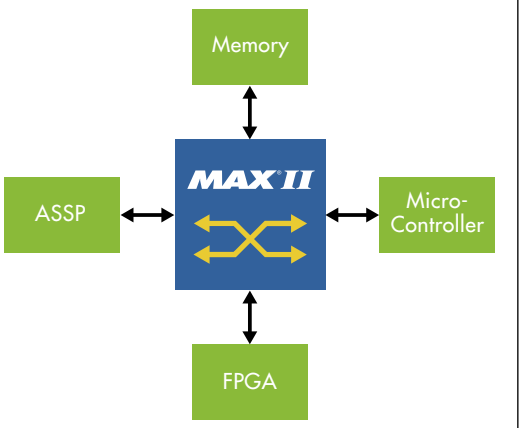


Figure 9. Multipoint Connections

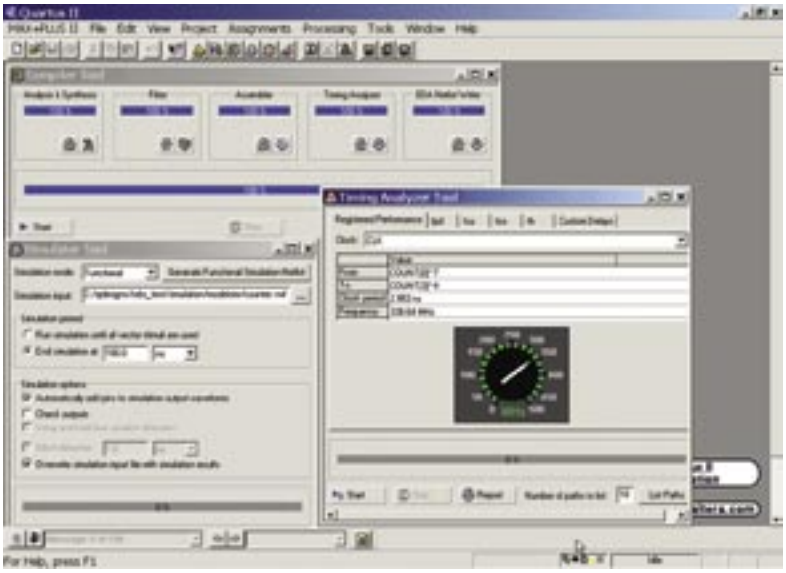


High-Performance Design Software

MAX II devices are supported by Altera's Quartus® II software, the easiest-to-use software for CPLD design. The Quartus II software provides a number of tools to enable the simple and easy design of MAX II devices, including:

- VHDL and Verilog hardware description language (HDL) design entry and synthesis
- Schematic design entry support for less complicated designs
- SOPC Builder design entry and system generation to eliminate mundane and error prone system integration tasks
- PowerPlay power analysis support for design conception through implementation stages
- MAX+PLUS® II software look-and-feel option, so MAX+PLUS II software users can get the full benefits of the advanced features and performance of the Quartus II software without having to learn a new user interface

Figure 10. Quartus II Easy-to-Use Interface



Free Online Quartus II Software Demonstrations

The easiest way to experience the Quartus II software's ease of use is to view the free demonstrations at **www.altera.com/quartusdemos**.

Get Started Today With Free Quartus II Web Edition Software

A free version of the Quartus II Web Edition software, including the SOPC Builder feature, can be downloaded from the Altera website at **www.altera.com** and is available on the free Altera Development Software Suite CD-ROM.

Contact Altera Today

The MAX II CPLD family is the ideal solution for all of your control path requirements including power-up sequencing, system configuration, I/O expansion, and interface bridging. To learn more about MAX II CPLDs, visit the Altera website today at **www.altera.com/max2**.

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