Octal 16-/12-Bit Rail-to-Rail DACs with 10ppm/°C Max Reference

FEATURES

- Precision 10ppm/°C Max Reference
- Maximum INL Error: ±4LSB at 16 Bits
- Guaranteed Monotonic over Temperature
- Selectable Internal or External Reference
- 2.7V to 5.5V Supply Range (LTC2656-L)
- Integrated Reference Buffers
- Ultralow Crosstalk Between DACs(<1nV•s)
- Power-On-Reset to Zero-Scale/Mid-scale
- Asynchronous LDAC Update Pin
- Tiny 20-Lead 4mm × 5mm QFN and 20-Lead Thermally Enhanced TSSOP Packages

APPLICATIONS

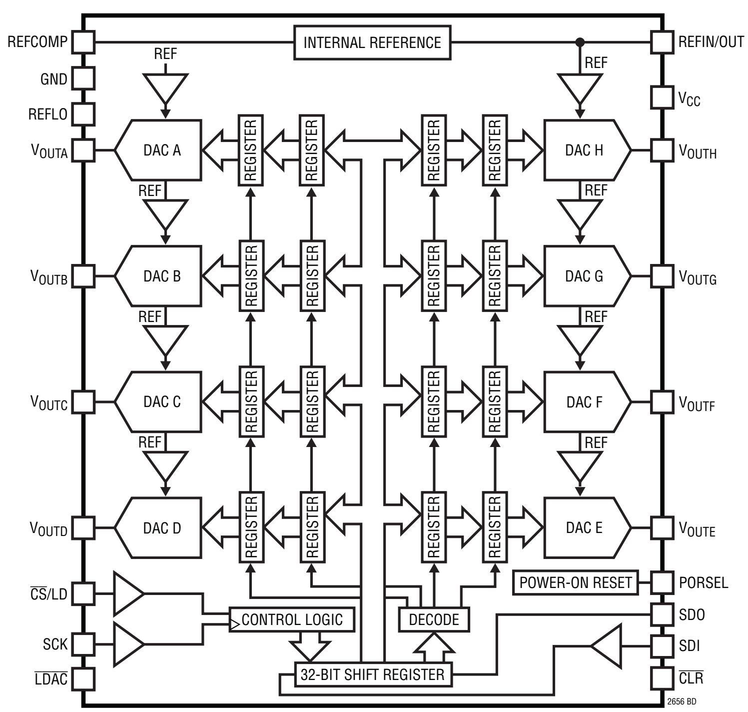
- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment
- Automotive

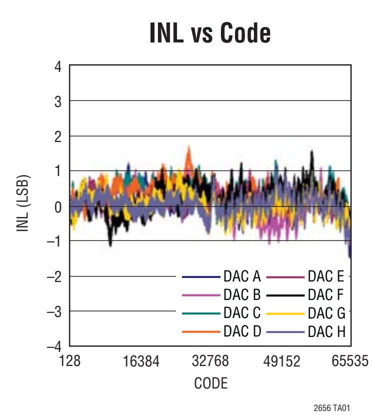
DESCRIPTION

The LTC®2656 is a family of octal 16-/12-bit rail-to-rail DACs with a precision integrated reference. The DACs have built-in high performance, rail-to-rail, output buffers and are guaranteed monotonic. The LTC2656-L has a full-scale output of 2.5V with the integrated 10ppm/°C reference and operates from a single 2.7V to 5.5V supply. The LTC2656-H has a full-scale output of 4.096V with the integrated reference and operates from a 4.5V to 5.5V supply. Each DAC can also operate with an external reference, which sets the DAC full-scale output to two times the external reference voltage.

These DACs communicate via a SPI/MICROWIRE™ compatible 4-wire serial interface which operates at clock rates up to 50MHz. The LTC2656 incorporates a power-on reset circuit that is controlled by the PORSEL pin. If PORSEL is tied to GND the DACs reset to zero-scale. If PORSEL is tied to V_{CC}, the DACs reset to mid-scale.

BLOCK DIAGRAM

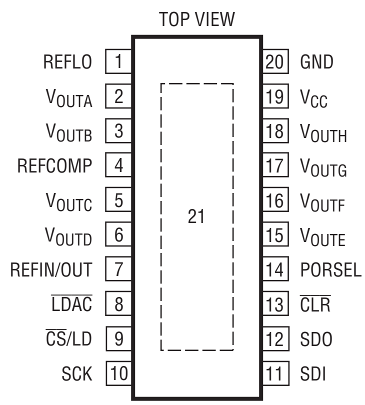




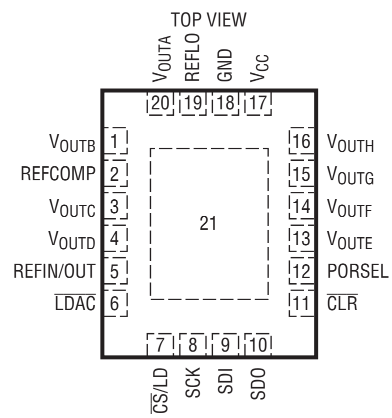
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) .... –0.3V to 6V
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, REFLO .... –0.3V to 6V
V_{OUTA} to V_{OUTH} .... –0.3V to Min(V_{CC} + 0.3V, 6V)
REFIN/OUT, REFCOMP ...... –0.3V to Min(V_{CC} + 0.3V, 6V)
PORSEL, SDO .... –0.3V to Min(V_{CC} + 0.3V, 6V)
Operating Temperature Range
LTC2656C .... 0°C to 70°C
LTC2656I... –40°C to 85°C
Maximum Junction Temperature........................... 150°C
Storage Temperature Range....................... –65 to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package .... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

PRODUCT SELECTOR GUIDE

LTC2656 B C UFD -L 16 #TR PBF

LEAD FREE DESIGNATOR
PBF = Lead Free

TAPE AND REEL
TR = Tape and Reel

RESOLUTION
16 = 16-Bit
12 = 12-Bit

FULL-SCALE VOLTAGE, INTERNAL REFERENCE MODE
L = 2.5V
H = 4.096V

PACKAGE TYPE
UFD = 20-Lead (4mm × 5mm) Plastic QFN
FE = 20-Lead Thermally Enhanced TSSOP

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)

ELECTRICAL GRADE (OPTIONAL)
B = ±4LSB Maximum INL (16-Bit)

PRODUCT PART NUMBER

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE	MAXIMUM INL
LTC2656BCFE-L16#PBF LTC2656BIFE-L16#PBF	LTC2656BCFE-L16#TRPBF LTC2656BIFE-L16#TRPBF	LTC2656FE-L16 LTC2656FE-L16	20-Lead Thermally Enhanced TSSOP 20-Lead Thermally Enhanced TSSOP	0°C to 70°C –40°C to 85°C	±4 ±4
LTC2656BCUFD-L16#PBF LTC2656BIUFD-L16#PBF	LTC2656BCUFD-L16#TRPBF LTC2656BIUFD-L16#TRPBF	56L16 56L16	20-Lead (4mm × 5mm) Plastic QFN 20-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C –40°C to 85°C	±4 ±4
LTC2656BCFE-H16#PBF LTC2656BIFE-H16#PBF	LTC2656BCFE-H16#TRPBF LTC2656BIFE-H16#TRPBF	LTC2656FE-H16 LTC2656FE-H16	20-Lead Thermally Enhanced TSSOP 20-Lead Thermally Enhanced TSSOP	0°C to 70°C –40°C to 85°C	±4 ±4
LTC2656BCUFD-H16#PBF LTC2656BIUFD-H16#PBF	LTC2656BCUFD-H16#TRPBF LTC2656BIUFD-H16#TRPBF	56H16 56H16	20-Lead (4mm × 5mm) Plastic QFN 20-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C –40°C to 85°C	±4 ±4
LTC2656CFE-L12#PBF LTC2656IFE-L12#PBF	LTC2656CFE-L12#TRPBF LTC2656IFE-L12#TRPBF	LTC2656FE-L12 LTC2656FE-L12	20-Lead Thermally Enhanced TSSOP 20-Lead Thermally Enhanced TSSOP	0°C to 70°C –40°C to 85°C	±1 ±1
LTC2656CUFD-L12#PBF LTC2656IUFD-L12#PBF	LTC2656CUFD-L12#TRPBF LTC2656IUFD-L12#TRPBF	56L12 56L12	20-Lead (4mm × 5mm) Plastic QFN 20-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C –40°C to 85°C	±1 ±1
LTC2656CFE-H12#PBF LTC2656IFE-H12#PBF	LTC2656CFE-H12#TRPBF LTC2656IFE-H12#TRPBF	LTC2656FE-H12 LTC2656FE-H12	20-Lead Thermally Enhanced TSSOP 20-Lead Thermally Enhanced TSSOP	0°C to 70°C –40°C to 85°C	±1 ±1
LTC2656CUFD-H12#PBF LTC2656IUFD-H12#PBF	LTC2656CUFD-H12#TRPBF LTC2656IUFD-H12#TRPBF	56H12 56H12	20-Lead (4mm × 5mm) Plastic QFN 20-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C –40°C to 85°C	±1 ±1

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified. LTC2656B-L16/LTC2656-L12 (internal reference = 1.25V)

SYMBOL	PARAMETER	CONDITIONS		LTC2656-12 MIN	TYP	MAX	LTC2656B-16 MIN	TYP	MAX	UNITS
DC Performance										
	Resolution		●	12			16			Bits
	Monotonicity	(Note 3)	●	12			16			Bits
DNL	Differential Nonlinearity	(Note 3)	●		±0.1	±0.5		±0.3	±1	LSB
INL	Integral Nonlinearity (Note 3)	V_{CC} = 5.5V, V_{REF} = 2.5V	●		±0.5	±1		±2	±4	LSB
	Load Regulation	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.125		0.6	2	LSB/mA
		V_{CC} = 3V ±10%, Internal Reference, Mid-Scale, –7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.06	0.25		1	4	LSB/mA
ZSE	Zero-Scale Error		●		1	3		1	3	mV
V_{OS}	Offset Error	V_{REF} = 1.25V (Note 4)	●		±1	±2		±1	±2	mV
	V_{OS} Temperature Coefficient				2			2		μV/°C
GE	Gain Error		●		±0.02	±0.1		±0.02	±0.1	%FSR
	Gain Temperature Coefficient				1			1		ppm/°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	Internal Reference External Reference = V_{EXTREF}			0 to 2.5 0 to 2 • V_{EXTREF}		V V
PSR	Power Supply Rejection	V_{CC} ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.15	Ω
		V_{CC} = 3V ±10%, Internal Reference, Mid-Scale, –7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.04	0.15	Ω
	DC Crosstalk (Note 5)	Due to Full-Scale Output Change Due to Load Current Change Due to Powering Down (per Channel)			±1.5 ±2 ±1		μV μV/mA μV
I_{SC}	Short-Circuit Output Current (Note 6)	V_{CC} = 5.5V, V_{EXTREF} = 2.75V Code: Zero Scale, Forcing Output to V_{CC} Code: Full Scale, Forcing Output to GND	 ● ●	 20 20		 65 65	 mA mA
		V_{CC} = 2.7V, V_{EXTREF} = 1.35V Code: Zero Scale, Forcing Output to V_{CC} Code: Full Scale, Forcing Output to GND	 ● ●	 10 10		 40 40	 mA mA
Reference							
	Reference Output Voltage			1.248	1.25	1.252	V
	Reference Temperature Coefficient	C-Grade (Note 7) I-Grade (Note 7)			±2 ±2	±10	ppm/°C ppm/°C
	Reference Line Regulation	V_{CC} ±10%			–80		dB
	Reference Short-Circuit Current	V_{CC} = 5.5V, Forcing Output to GND	●		3	5	mA
	REFCOMP Pin Short-Circuit Current	V_{CC} = 5.5V, Forcing Output to GND	●		60	200	μA
	Reference Load Regulation	V_{CC} = 3V ±10% or 5V ±10%, I_{OUT} = 100μA Sourcing			40		mV/mA
	Reference Output Voltage Noise Density	$C_{REFCOMP}$ = $C_{REFIN/OUT}$ = 0.1μF at f = 1kHz			30		nV/√Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified. LTC2656B-L16/LTC2656-L12 (internal reference = 1.25V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Reference Input Range	External Reference Mode (Note 13)	●	0.5		$V_{CC}/2$	V
	Reference Input Current		●		0.001	1	µA
	Reference Input Capacitance (Note 9)		●		40		pF
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (Note 8)	V_{CC} = 5V, Internal Reference On V_{CC} = 5V, Internal Reference Off V_{CC} = 3V, Internal Reference On V_{CC} = 3V, Internal Reference Off	● ● ● ●		3.1 2.7 3.0 2.6	4.25 3.7 3.8 3.2	mA mA mA mA
I_{SHDN}	Supply Current in Shutdown Mode (Note 8)	V_{CC} = 5V	●			3	µA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 3.6V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 4.5V	● ●			0.8 0.6	V V
V_{OH}	Digital Output High Voltage	Load Current = –100µA	●	V_{CC}–0.4			V
V_{OL}	Digital Output Low Voltage	Load Current = 100µA	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance (Note 9)		●			8	pF
AC Performance							
t_S	Settling Time (Note 10)	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			4.2 8.9		µs µs
	Settling Time for 1LSB Step	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			2.2 4.9		µs µs
	Voltage Output Slew Rate				1.8		V/µs
	Capacitive Load Driving				1000		pF
	Glitch Impulse (Note 11)	At Mid-Scale Transition, V_{CC} = 3V			3		nV•s
	DAC-to-DAC Crosstalk (Note 12)	Due to Full-Scale Output Change, $C_{REFCOMP}$ = C_{REFOUT} = No Load			2		nV•s
	Multiplying Bandwidth				150		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz			85 80		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, Internal Reference			8 600		μV_{P-P} μV_{P-P}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified. LTC2656B-H16/LTC2656-H12 (internal reference = 2.048V)

SYMBOL	PARAMETER	CONDITIONS		LTC2656-12 MIN	TYP	MAX	LTC2656B-16 MIN	TYP	MAX	UNITS
DC Performance										
	Resolution		●	12			16			Bits
	Monotonicity	(Note 3)	●	12			16			Bits
DNL	Differential Nonlinearity	(Note 3)	●		±0.1	±0.5		±0.3	±1	LSB
INL	Integral Nonlinearity (Note 3)	V_{CC} = 5.5V, V_{REF} = 2.5V	●		±0.5	±1		±2	±4	LSB
	Load Regulation	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.125		0.6	2	LSB/mA
ZSE	Zero-Scale Error		●		1	3		1	3	mV
V_{OS}	Offset Error	V_{REF} = 2.048V (Note 4)	●		±1	±2		±1	±2	mV
	V_{OS} Temperature Coefficient				2			2		µV/°C
GE	Gain Error		●		±0.02	±0.1		±0.02	±0.1	%FSR
	Gain Temperature Coefficient				1			1		ppm/°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	Internal Reference External Reference = V_{EXTREF}			0 to 4.096 0 to 2 • V_{EXTREF}		V V
PSR	Power Supply Rejection	V_{CC} ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{CC} = 5V ±10%, Internal Reference, Midscale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.15	Ω
	DC Crosstalk (Note 5)	Due to Full-Scale Output Change Due to Load Current Change Due to Powering Down (per Channel)			±1.5 ±2 ±1		µV µV/mA µV
I_{SC}	Short-Circuit Output Current (Note 6)	V_{CC} = 5.5V, V_{EXTREF} = 2.75V Code: Zero Scale, Forcing Output to V_{CC} Code: Full Scale, Forcing Output to GND	 ● ●	 20 20		 65 65	 mA mA
Reference							
	Reference Output Voltage			2.044	2.048	2.052	V
	Reference Temperature Coefficient	C-Grade (Note 7) I-Grade (Note 7)			±2 ±2	±10	ppm/°C ppm/°C
	Reference Line Regulation	V_{CC} ±10%			–80		dB
	Reference Short-Circuit Current	V_{CC} = 5.5V, Forcing Output to GND	●		3	5	mA
	REFCOMP Pin Short-Circuit Current	V_{CC} = 5.5V, Forcing Output to GND	●		60	200	µA
	Reference Load Regulation	V_{CC} = 5V ±10%, I_{OUT} = 100µA Sourcing			40		mV/mA
	Reference Output Voltage Noise Density	$C_{REFCOMP}$ = $C_{REFIN/OUT}$ = 0.1µF at f = 1kHz			35		nV/$\sqrt{Hz}$
	Reference Input Range	External Reference Mode (Note 13)	●	0.5		$V_{CC}/2$	V
	Reference Input Current		●		0.001	1	µA
	Reference Input Capacitance (Note 9)		●		40		pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified. LTC2656B-H16/LTC2656-H12 (internal reference = 2.048V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current (Note 8)	V_{CC} = 5V, Internal Reference On V_{CC} = 5V, Internal Reference Off	● ●		3.3 3.0	4.25 3.7	mA mA
I_{SHDN}	Supply Current in Shutdown Mode (Note 8)	V_{CC} = 5V	●			3	µA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 4.5V to 5.5V	●	2.4			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V	●			0.8	V
V_{OH}	Digital Output High Voltage	Load Current = –100µA	●	V_{CC}–0.4			V
V_{OL}	Digital Output Low Voltage	Load Current = 100µA	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance (Note 9)		●			8	pF
AC Performance							
t_S	Settling Time (Note 10)	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			4.6 7.9		µs µs
	Settling Time for 1LSB Step	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			2.0 3.8		µs µs
	Voltage Output Slew Rate				1.8		V/µs
	Capacitive Load Driving				1000		pF
	Glitch Impulse (Note 11)	At Mid-Scale Transition, V_{CC} = 5V			6		nV•s
	DAC-to-DAC Crosstalk (Note 12)	Due to Full-Scale Output Change, $C_{REFCOMP}$ = C_{REFOUT} = No Load			3		nV•s
	Multiplying Bandwidth				150		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz			85 80		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, Internal Reference			12 650		$µV_{P-P}$ $µV_{P-P}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTC2656B-L16/LTC2656-L12/LTC2656B-H16/LTC2656-H12 (see Figure 1).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 2.7V to 5.5V							
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 4.5V	 ● ●			 20 45	 ns ns
t_9	$\overline{CLR}$ Pulse Width		●	20			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
t_{12}	$\overline{LDAC}$ Pulse Width		●	15			ns
t_{13}	$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition		●	200			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND.

Note 3: Linearity and monotonicity are defined from code kL to code $2^N – 1$, where N is the resolution and kL is the lower end code for which no output limiting occurs. For V_{REF} = 2.5V and N = 16, kL = 128 and linearity is defined from code 128 to code 65535. For V_{REF} = 2.5V and N = 12, kL = 8 and linearity is defined from code 8 to code 4,095.

Note 4: Inferred from measurement at code 128 (LTC2656-16) or code 8 (LTC2656-12).

Note 5: DC crosstalk is measured with V_{CC} = 5V and using internal reference with the measured DAC at mid-scale.

Note 6: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 8: Digital inputs at 0V or V_{CC}.

Note 9: Guaranteed by design and not production tested.

Note 10: Internal reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 200pF to GND.

Note 11: V_{CC} = 5V, internal reference mode. DAC is stepped ±1LSB between half scale and half scale – 1LSB. Load is 2k in parallel with 200pF to GND.

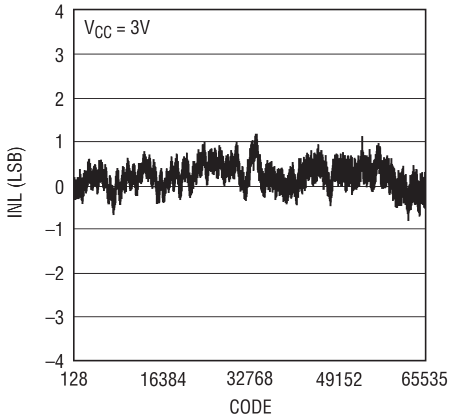
Note 12: DAC-to-DAC crosstalk is the glitch that appears at the output of one DAC due to a full-scale change at the output of another DAC. It is measured with V_{CC} = 5V and using internal reference, with the measured DAC at mid-scale.

Note 13: Gain error specification may be degraded for reference input voltages less than 1V. See Gain Error vs Reference Input Voltage curve in the Typical Performance Characteristics section.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

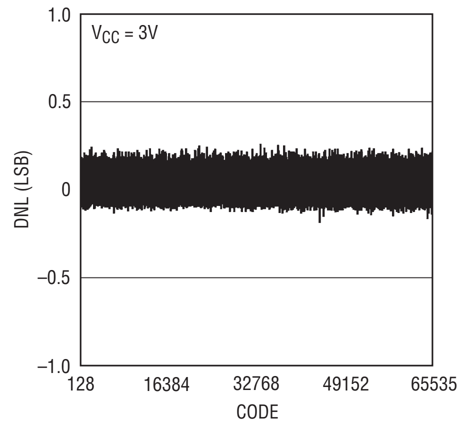
LTC2656-L16

Integral Nonlinearity (INL)



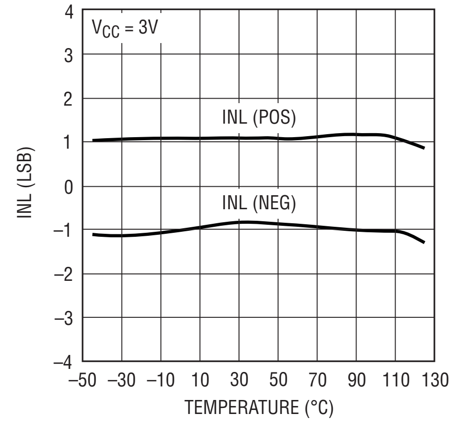
2656 G01

Differential Nonlinearity (DNL)



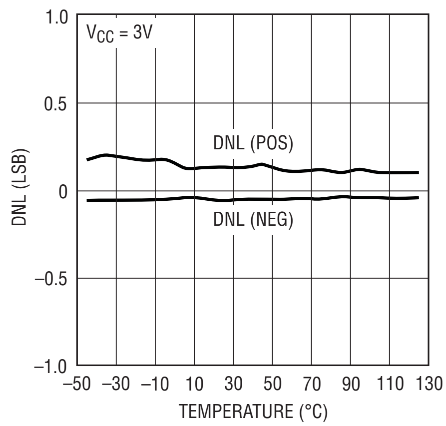
2656 G02

INL vs Temperature



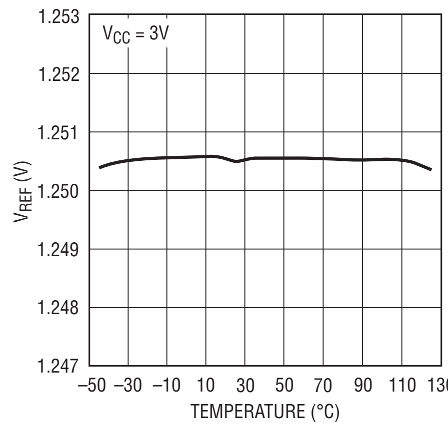
2656 G03

DNL vs Temperature



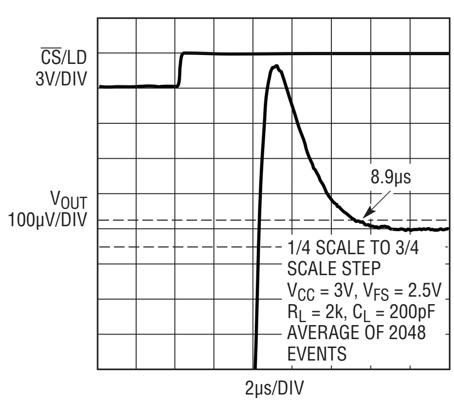
2656 G04

REFOUT Voltage vs Temperature



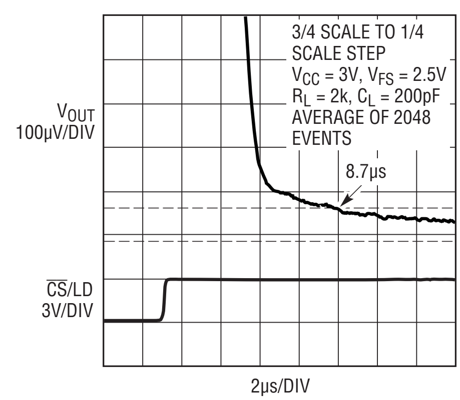
2656 G05

Settling to ±1LSB Rising



2656 G06

Settling to ±1LSB Falling

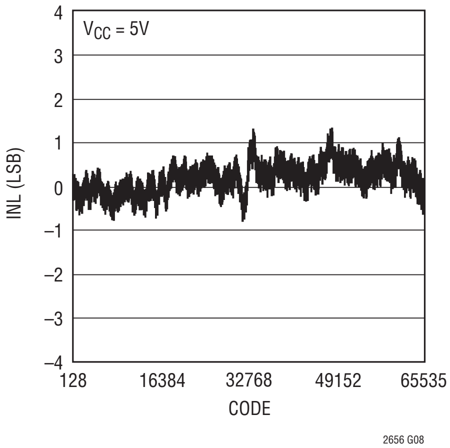


2656 G07

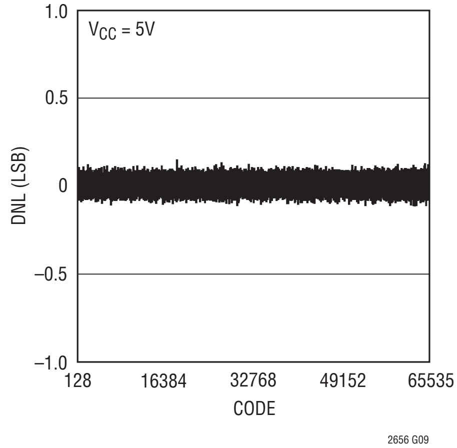
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

LTC2656-H16

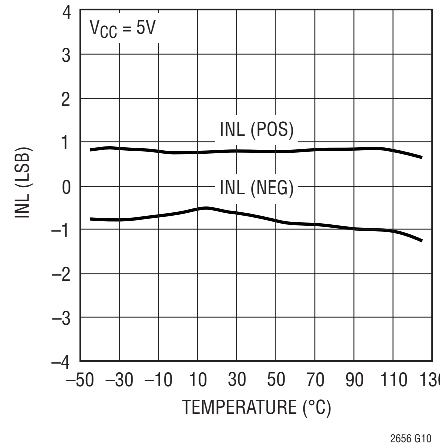
Integral Nonlinearity (INL)



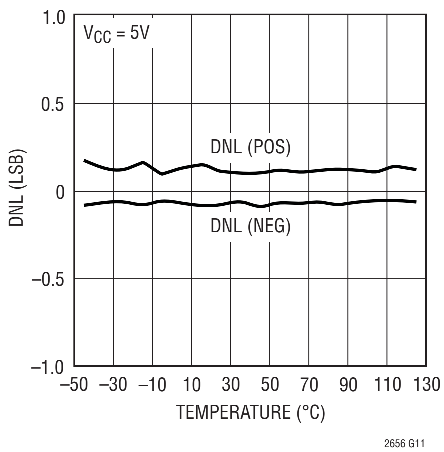
Differential Nonlinearity (DNL)



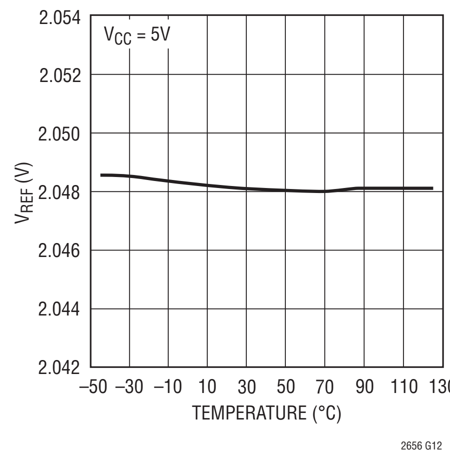
INL vs Temperature



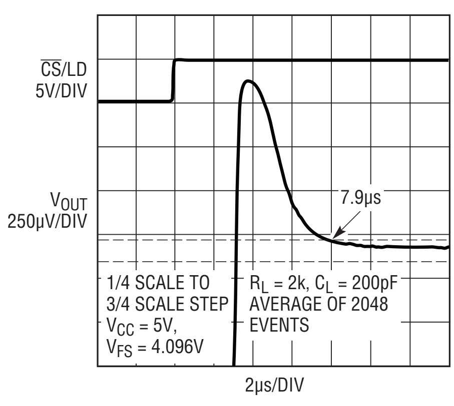
DNL vs Temperature



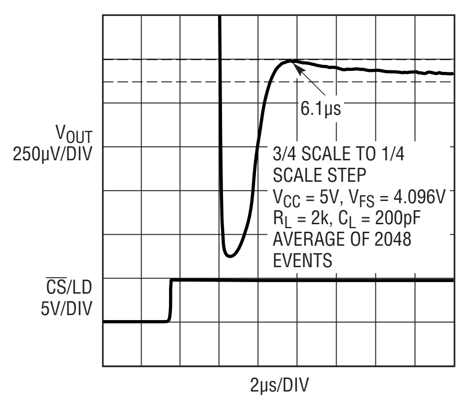
REFOUT Voltage vs Temperature



Settling to ±1LSB Rising



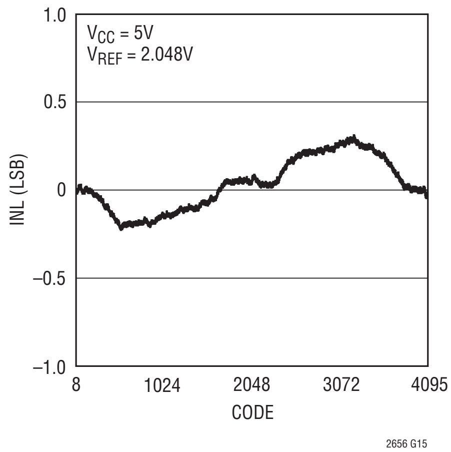
Settling to ±1LSB Falling



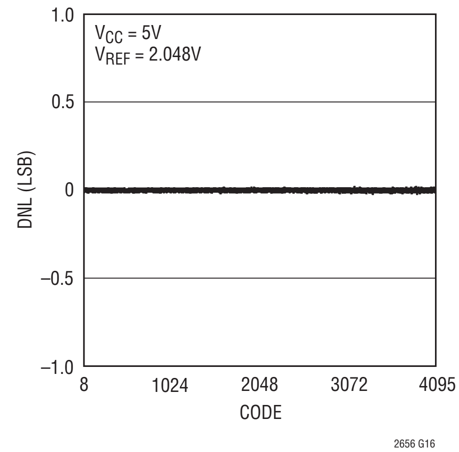
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

LTC2656-12

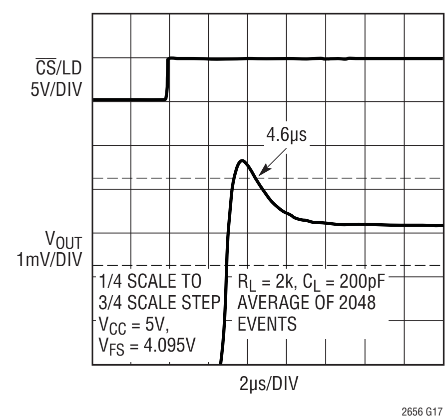
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)

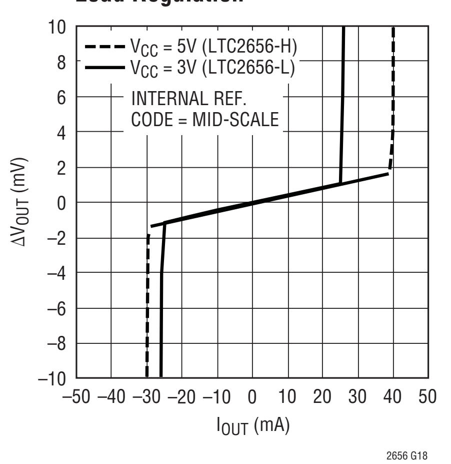


Settling to ±1LSB (12 Bit) Rising

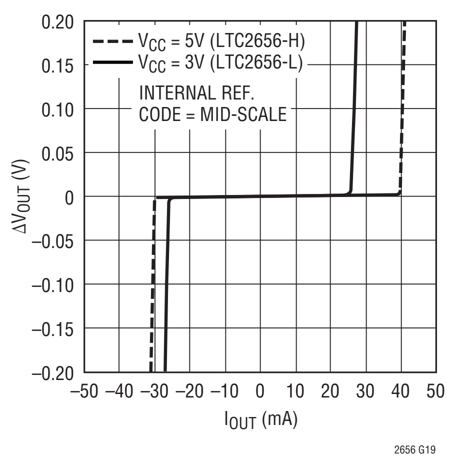


LTC2656-16

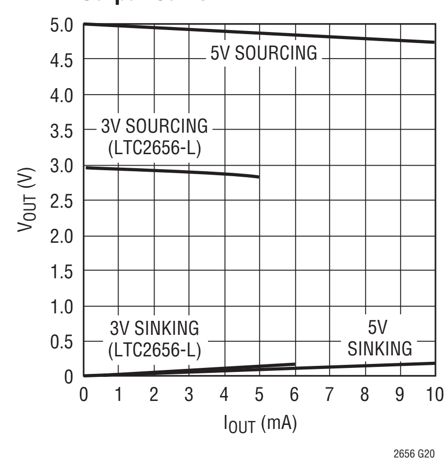
Load Regulation



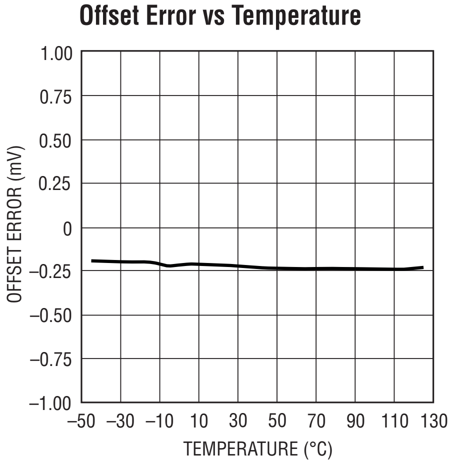
Current Limiting



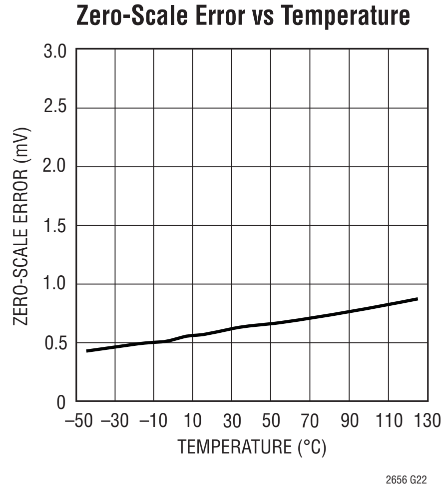
Headroom at Rails vs Output Current



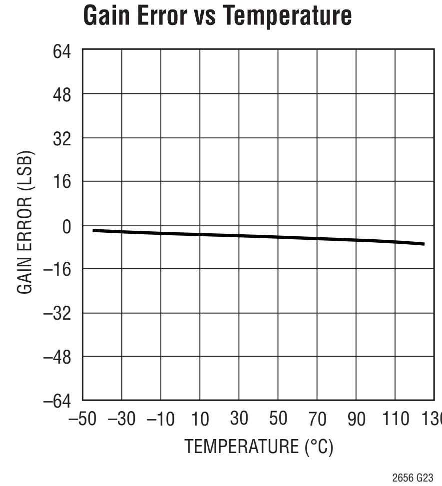
Offset Error vs Temperature



Zero-Scale Error vs Temperature



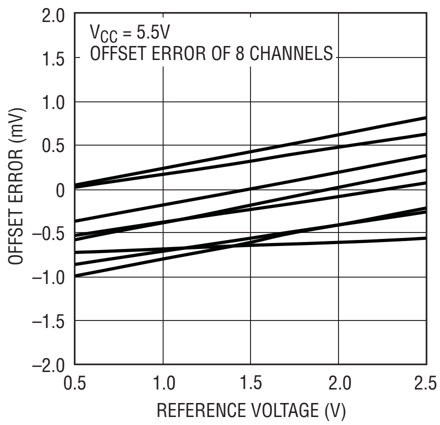
Gain Error vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$ unless otherwise noted.

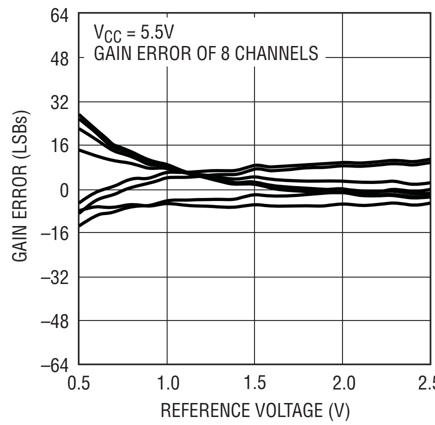
LTC2656-16

Offset Error vs Reference Input



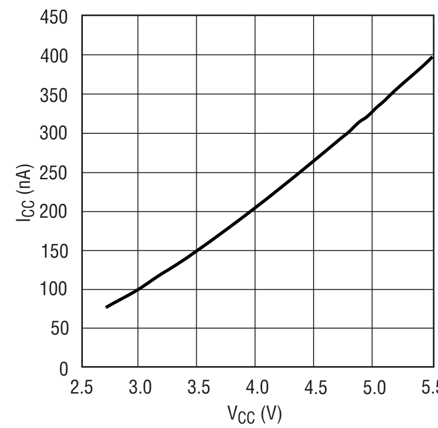
2656 G24

Gain Error vs Reference Input



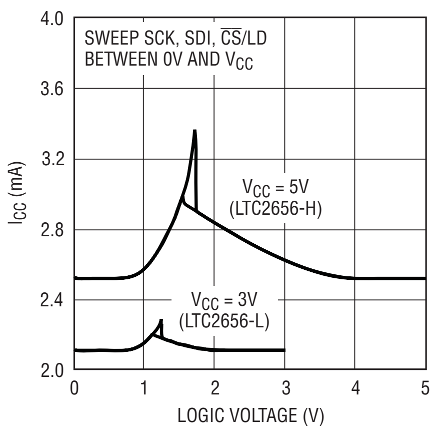
2656 G25

I_{CC} Shutdown vs V_{CC}



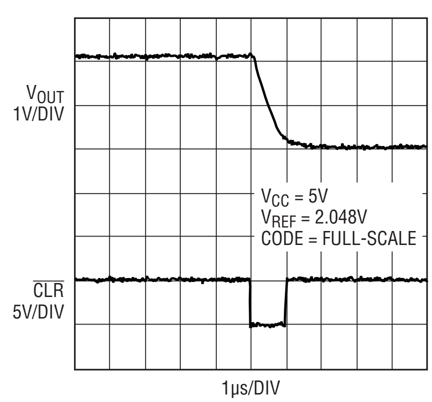
2656 G26

Supply Current vs Logic Voltage



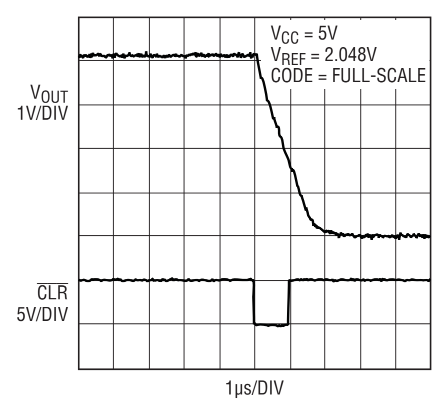
2656 G27

Hardware $\overline{CLR}$ to Mid-Scale



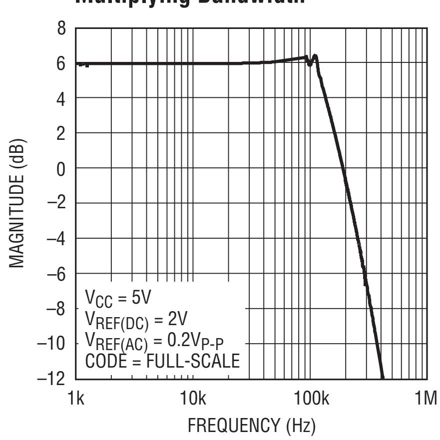
2656 G28

Hardware $\overline{CLR}$ to Zero-Scale



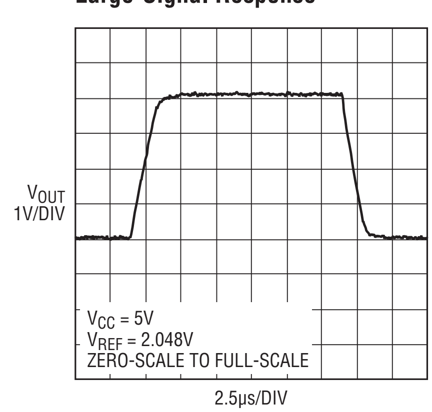
2656 G29

Multiplying Bandwidth



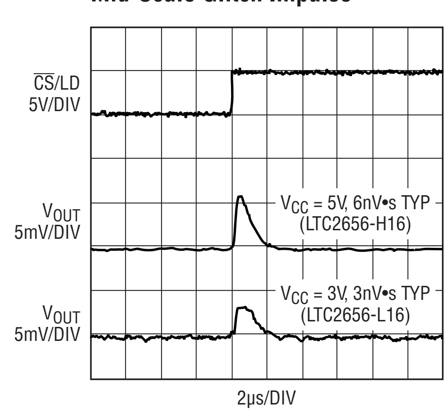
2656 G30

Large-Signal Response



2656 G31

Mid-Scale Glitch Impulse

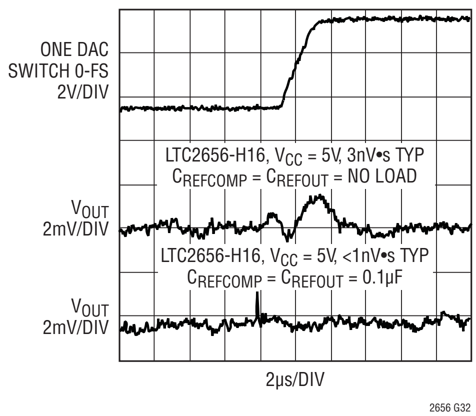


2656 G32

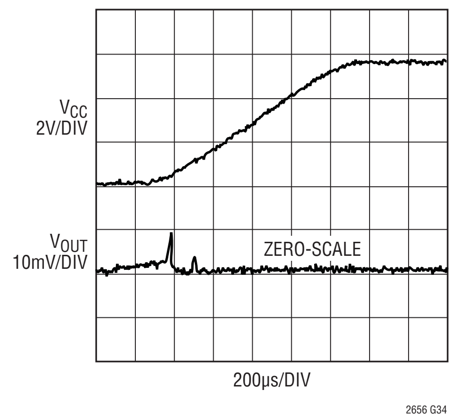
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

LTC2656

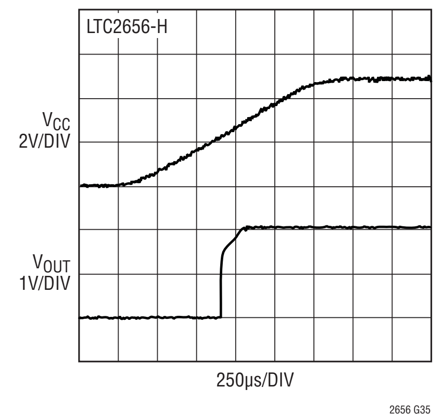
DAC-to-DAC Crosstalk (Dynamic)



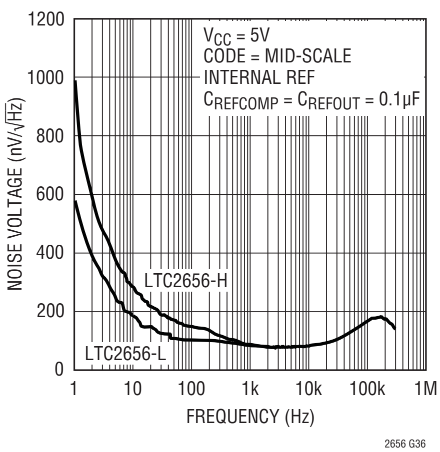
Power-On Reset Glitch



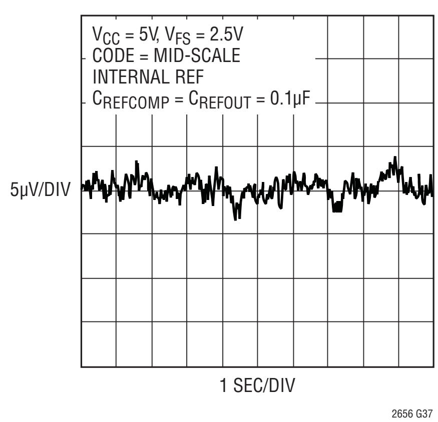
Power-On Reset to Mid-Scale



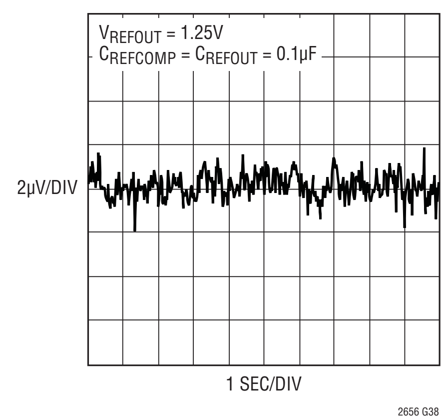
Noise Voltage vs Frequency



0.1Hz to 10Hz Voltage Noise



Reference 0.1Hz to 10Hz Voltage Noise



PIN FUNCTIONS (TSSOP/QFN)

REFLO (Pin 1/Pin 19): Reference Low Pin. The voltage at this pin sets the zero-scale voltage of all DACs. REFLO should be tied to GND.

V_{OUTA} to V_{OUTH} (Pins 2, 3, 5, 6, 15, 16, 17, 18/Pins 20, 1, 3, 4, 13, 14, 15, 16): DAC Analog Voltage Outputs. The output range is 0V to 2 times the voltage at the REFIN/OUT pin.

REFCOMP (Pin 4/Pin 2): Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1µF capacitor to GND. Connect REFCOMP to GND to allow the use of external reference at start-up.

REFIN/OUT (Pin 7/Pin 5): This pin acts as the internal reference output in internal reference mode and acts as the reference input pin in external reference mode. When acting as an output, the nominal voltage at this pin is 1.25V for L options and 2.048V for H options. For low noise and reference stability tie a capacitor from this pin to GND. This capacitor value must be $\le C_{REFCOMP}$, where $C_{REFCOMP}$ is the capacitance tied to the REFCOMP pin. In external reference mode, the allowable reference input voltage range is 0.5V to $V_{CC}/2$.

$\overline{\text{LDAC}}$ (Pin 8/Pin 6): Asynchronous DAC Update Pin. If $\overline{\text{CS}}$/LD is high, a falling edge on $\overline{\text{LDAC}}$ immediately updates the DAC register with the contents of the input register (similar to a software update). If $\overline{\text{CS}}$/LD is low when $\overline{\text{LDAC}}$ goes low, the DAC register is updated after $\overline{\text{CS}}$/LD returns high. A low on the $\overline{\text{LDAC}}$ pin powers up the DAC outputs. All the software power-down commands are ignored if $\overline{\text{LDAC}}$ is low when $\overline{\text{CS}}$/LD goes high.

$\overline{\text{CS}}$/LD (Pin 9/Pin 7): Serial Interface Chip Select/Load Input. When $\overline{\text{CS}}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{\text{CS}}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

SCK (Pin 10/Pin 8): Serial Interface Clock Input. CMOS and TTL compatible.

SDI (Pin 11/Pin 9): Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK (Pin 10). The LTC2656 accepts input word lengths of either 24 or 32 bits.

SDO (Pin 12/Pin 10): Serial Interface Data Output. This pin is used for daisy-chain operation. The serial output of the shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. This pin is continuously driven and does not go high impedance when $\overline{\text{CS}}$/LD is taken active high.

$\overline{\text{CLR}}$ (Pin 13/Pin 11): Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage outputs to drop to 0V if the PORSEL pin is tied to GND. If the PORSEL pin is tied to V_{CC}, a logic low at $\overline{\text{CLR}}$ sets all registers to mid-scale code and causes the DAC voltage outputs to go to mid-scale.

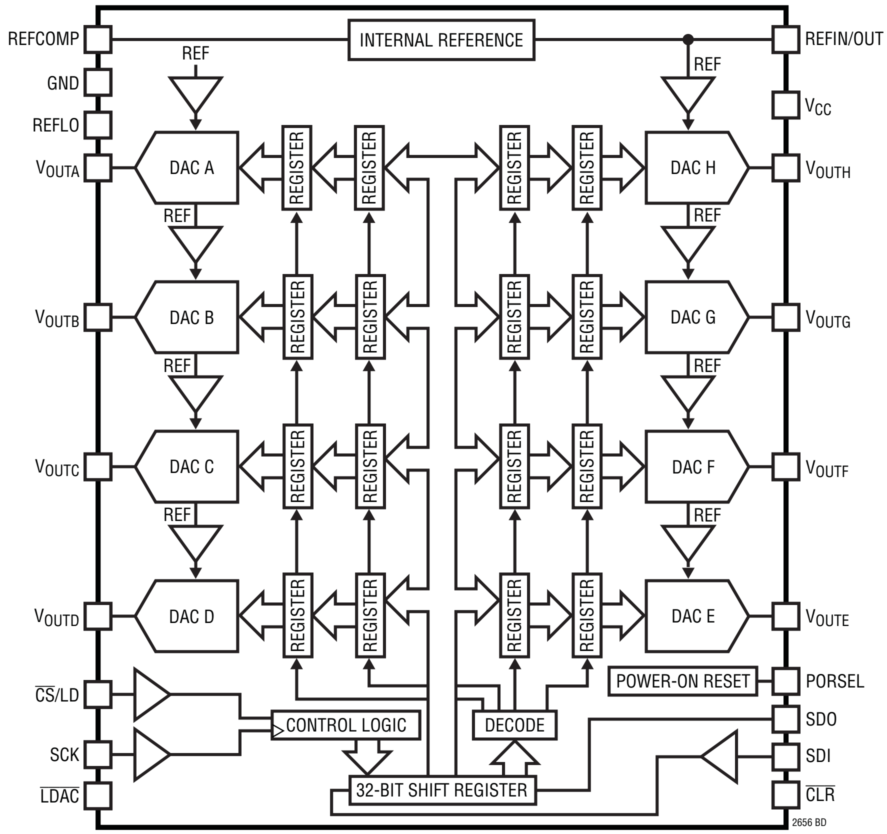
PORSEL (Pin 14/Pin 12): Power-On Reset Select Pin. If tied to GND, the DAC resets to zero-scale at power-up. If tied to V_{CC}, the DAC resets to mid-scale at power-up.

V_{CC} (Pin 19/Pin 17): Supply Voltage Input. For -L options, $2.7V \le V_{CC} \le 5.5V$ and for -H options, $4.5V \le V_{CC} \le 5.5V$.

GND (Pin 20/Pin 18): Ground.

Exposed Pad (Pin 21/Pin 21): Ground. Must be soldered to PCB Ground.

BLOCK DIAGRAM



TIMING DIAGRAMS

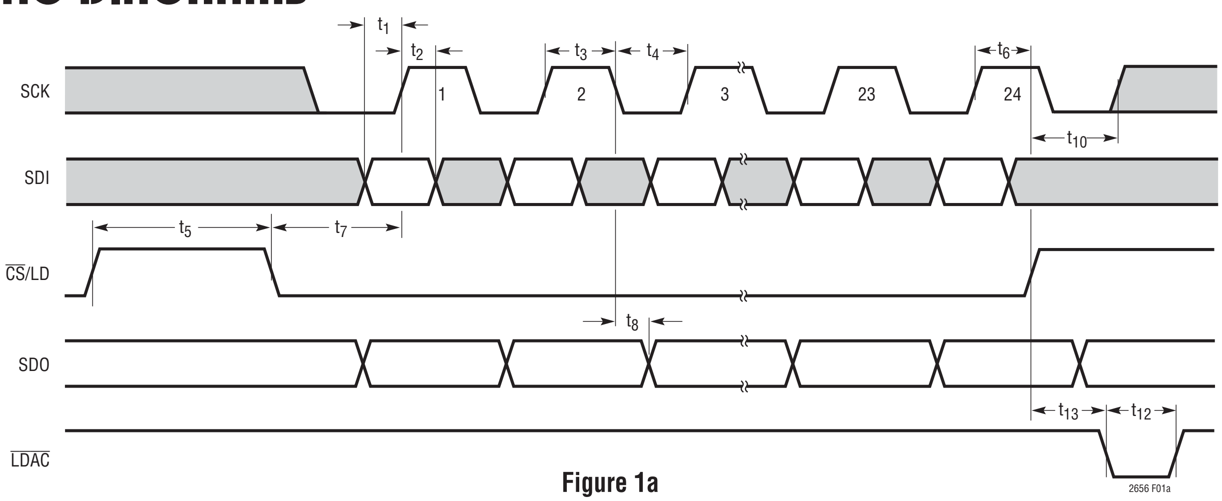


Figure 1a

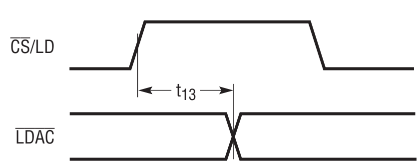


Figure 1b

OPERATION

The LTC2656 is a family of octal voltage output DACs in 20-lead 4mm × 5mm QFN and in 20-lead thermally enhanced TSSOP packages. Each DAC can operate rail-to-rail in external reference mode, or with its full-scale voltage set by an integrated reference. Four combinations of accuracy (16-bit and 12-bit), and full-scale voltage (2.5V or 4.096V) are available. The LTC2656 is controlled using a 4-wire SPI/MICROWIRE compatible interface.

Power-On Reset

The LTC2656-L/ LTC2656-H clear the output to zero scale if the PORSEL pin is tied to GND, when power is first applied, making system initialization consistent and repeatable. For some applications, downstream circuits are active during DAC power-up and may be sensitive to nonzero outputs from the DAC during this time. The LTC2656 contains circuitry to reduce the power-on glitch. The analog outputs typically rise less than 10mV above zero scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See Power-On Reset Glitch in the Typical Performance Characteristics.

Alternatively, if the PORSEL pin is tied to V_{CC}, the LTC2656-L/ LTC2656-H sets the output to mid-scale when power is first applied.

Power Supply Sequencing and Start-Up

For the LTC2656 family of parts, the internal reference is powered up at start-up by default. If an external reference is to be used, the REFCOMP pin must be hardwired to GND. Having REFCOMP hardwired to GND at power up will cause the REFIN/OUT pin to become high impedance and will allow for the use of an external reference at start-up. However in this configuration, the internal reference will still be on even though it is disconnected from the REFIN/OUT pin and will draw supply current. In order to use external reference after power-up, the command Select External Reference (0111b) should be used to turn the internal reference off (see Table 1.)

The voltage at REFIN/OUT should be kept within the range $-0.3V \le$ REFIN/OUT $\le V_{CC} + 0.3V$ if the external reference is to be used (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} is in transition.

Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right) \bullet 2 \bullet \left(V_{REF} - V_{REFLO}\right) + V_{REFLO}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution of the DAC, and V_{REF} is the voltage at the REFIN/OUT pin. The resulting DAC output span is 0V to 2 • V_{REF}, as it is necessary to tie REFLO to GND. V_{REF} is nominally 1.25V for LTC2656-L and 2.048V for LTC2656-H, in internal reference mode.

Table 1. Command and Adress Codes

COMMAND*				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
0	1	0	1	Power Down Chip (All DACs and Reference)
0	1	1	0	Select Internal Reference (Power-Up Reference)
0	1	1	1	Select External Reference (Power-Down Reference)
1	1	1	1	No Operation
ADDRESS (n)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

*Command and address codes not shown are reserved and should not be used.

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, powering on the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges.

OPERATION

The 4-bit command, C3-C0, is loaded first; followed by the 4-bit DAC address, A3-A0; and finally the 16-bit data word. For the LTC2656-16 the data word comprises the 16-bit input code, ordered MSB-to-LSB. For the LTC2656-12 the data word comprizes the 12-bit input code, ordered MSB-to-LSB, followed by four don't care bits. Data can only be transferred to the LTC2656 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 2a.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits must be transferred to the device first, followed by the 24-bit word as just described. Figure 2b shows the 32-bit sequence. The 32-bit word is required for daisy-chain operation, and is also available to accommodate microprocessors that have a minimum word width of 16 bits (2 bytes). The 16-bit data word is ignored for all commands that do not include a write operation.

Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge. The SDO pin is continuously driven and does not go high impedance when $\overline{CS}$/LD is taken active high.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisy-chain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no-operation command (1111) for the other devices in the chain.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than eight DAC outputs are needed. When in power down, the buffer amplifiers, bias circuits and integrated reference circuits are disabled and draw essentially zero current. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 80k resistors. Input- and DAC-register contents are not disturbed during power down.

Any channel or combination of DAC channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, (n). The integrated reference is automatically powered down when external reference is selected using command 0111b. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using power-down chip command 0101b. For all power-down commands the 16-bit data word is ignored.

Normal operation resumes by executing any command which includes a DAC update, in software as shown in Table 1 or by taking the asynchronous $\overline{LDAC}$ pin low. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than eight DACs are in a powered-down state prior to the update command, the power-up delay time is 12μs. If, on the other hand, all eight DACs and the integrated reference

OPERATION

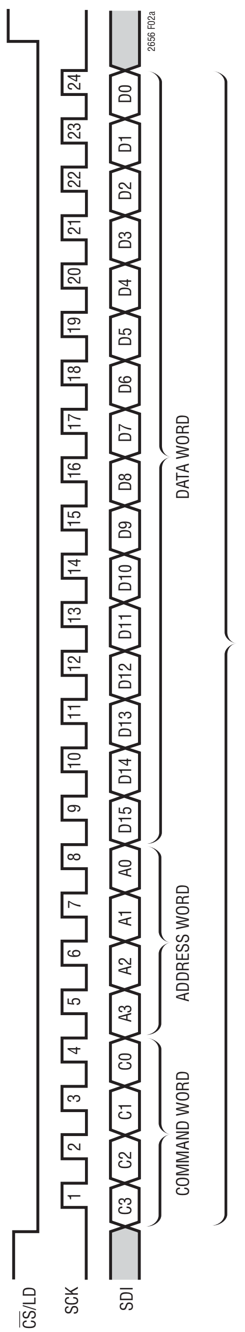


**Figure 2a. LTC2656-16 24-Bit Load Sequence (Minimum Input Word)
LTC2656-12 SDI Data Word: 12-Bit Input Code + 4 Don't-Care Bits**

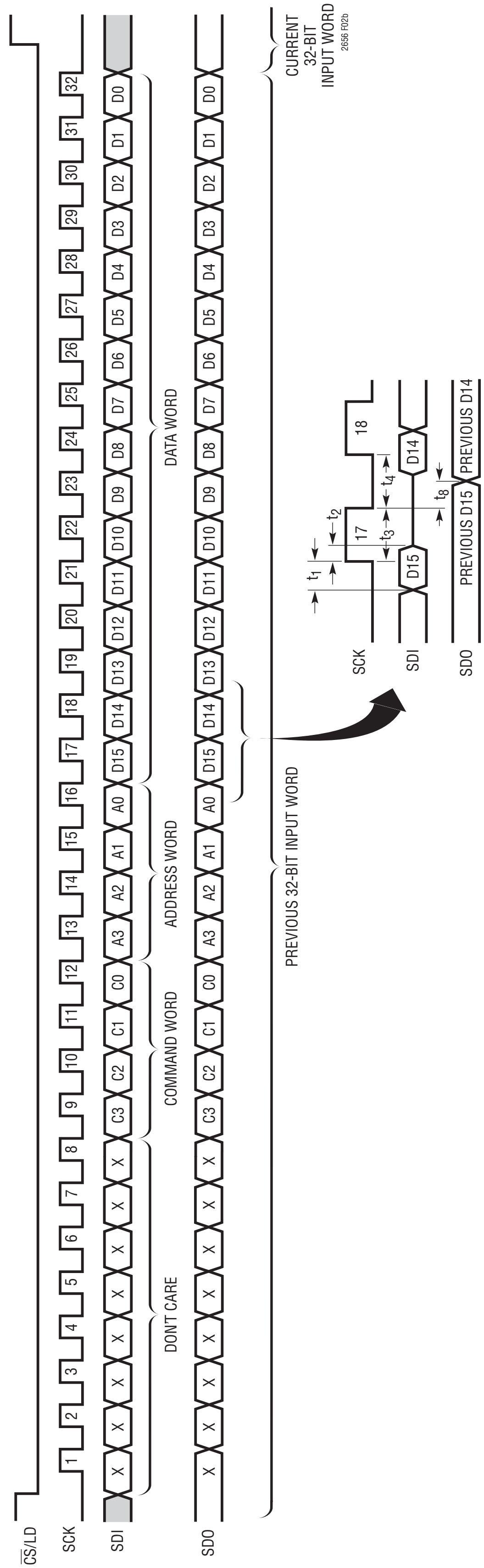


**Figure 2b. LTC2656-16 32-Bit Load Sequence
LTC2656-12 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't-Care Bits**

OPERATION

are powered down, then the main bias generation circuit block has been automatically shut down in addition to the individual DAC amplifiers and integrated reference. In this case, the power-up delay time is 14µs. The power up of the integrated reference depends on the command that powered it down. If the reference is powered down using the select external reference command (0111b), then it can only be powered back up using select internal reference command (0110b). However if the reference was powered down using power-down chip command (0101b), then in addition to select internal reference command (0110b), any command that powers up the DACs will also power up the integrated reference.

Asynchronous DAC Update Using $\overline{\text{LDAC}}$

In addition to the update commands shown in Table 1, the $\overline{\text{LDAC}}$ pin asynchronously updates all the DAC registers with the contents of the input registers.

If $\overline{\text{CS}}$/LD is high, a low on the $\overline{\text{LDAC}}$ pin causes all the DAC registers to be updated with the contents of the input registers.

If $\overline{\text{CS}}$/LD is low, a low going pulse on the $\overline{\text{LDAC}}$ pin before the rising edge of $\overline{\text{CS}}$/LD powers up all the DAC outputs but does not cause the output to be updated. If $\overline{\text{LDAC}}$ remains low after the rising edge of $\overline{\text{CS}}$/LD, then $\overline{\text{LDAC}}$ is recognized, the command specified in the 24-bit word just transferred is executed and the DAC outputs are updated.

The DAC outputs are powered up when $\overline{\text{LDAC}}$ is taken low, independent of the state of $\overline{\text{CS}}$/LD. The integrated reference is also powered up if it was powered down using power-down chip (0101b) command. The integrated reference will not power up when $\overline{\text{LDAC}}$ is taken low, if it was powered down using select external reference (0111b) command.

If $\overline{\text{LDAC}}$ is low at the time $\overline{\text{CS}}$/LD goes high, it inhibits any software power-down command (power down n, power-down chip, select external reference) that was specified in the input word.

Reference Modes

For applications where an accurate external reference is not available, the LTC2656 has a user-selectable, integrated reference. The LTC2656-L has a 1.25V reference that provides a full-scale DAC output of 2.5V. The LTC2656-H has a 2.048V reference that provides a full-scale DAC output of 4.096V. Both references exhibit a typical temperature drift of 2ppm/°C. Internal reference mode can be selected by using command 0110b, and is the power-on default. A buffer is needed if the internal reference is required to drive external circuitry. For reference stability and low noise, it is recommended that a 0.1µF capacitor be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1µF capacitive load without any stability problems. In order to ensure stable operation, the capacitive load on the REFIN/OUT pin should not exceed the capacitive load on the REFCOMP pin.

The DAC can also operate in external reference mode using command 0111b. In this mode, the REFIN/OUT pin acts as an input that sets the DAC's reference voltage. The input is high impedance and does not load the external reference source. The acceptable voltage range at this pin is 0.5V ≤ REFIN/OUT ≤ V_{CC}/2. The resulting full-scale output voltage is 2 • $V_{REFIN/OUT}$. For using external reference at start-up, see the Power Supply Sequencing and Start-Up section.

Integrated Reference Buffers

Each of the eight DACs in LTC2656 has its own integrated high performance reference buffer. The buffers have very high input impedance and do not load the reference voltage source. These buffers shield the reference voltage from glitches caused by DAC switching and thus minimize DAC-to-DAC dynamic crosstalk. Typically DAC-to-DAC crosstalk is less than 3nV•s. By tying 0.1µF capacitors between REFCOMP and GND, and also between REFIN/OUT and GND, this number can be reduced to less than 1nV•s. See the curve DAC-to-DAC Dynamic Crosstalk in the Typical Performance Characteristics section.

Voltage Outputs

Each of the LTC2656's eight rail-to-rail output amplifiers contained in these parts has a guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of

OPERATION

load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.04Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 30Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 30Ω • 1mA = 30mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separate.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin functions as a return path for power supply currents in the device and should be connected to analog ground. The REFLO pin should be connected to the system star ground. Resistance from the REFLO pin to the system star ground should be as low as possible.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit the lowest codes as shown in Figure 3b. Similarly, limiting can occur in external reference mode near full scale when the REFIN/OUT pin is at $V_{CC}/2$. If $V_{REFIN/OUT} = V_{CC}/2$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} are shown in Figure 3c. No full-scale limiting can occur if $V_{REFIN/OUT} \le (V_{CC} - FSE)/2$.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

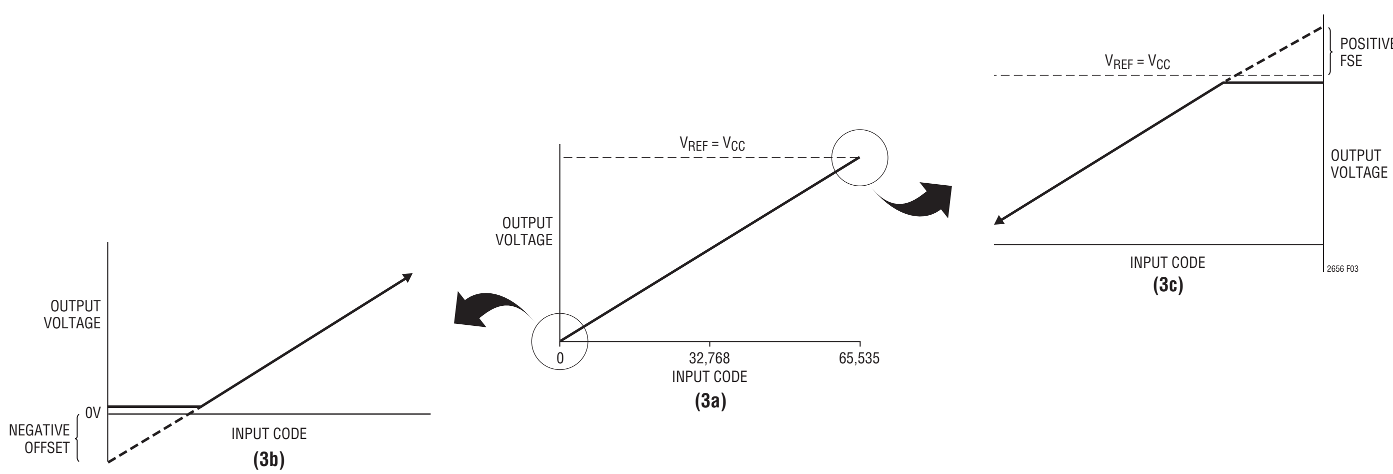
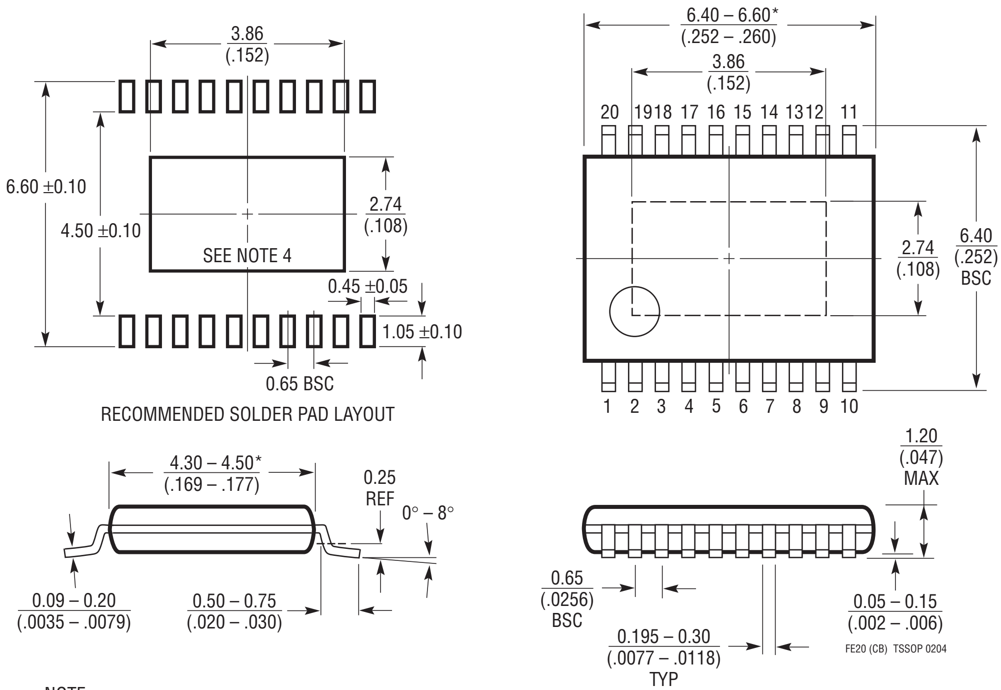


Figure 3. Effects of Rail-to-Rail Operation on a DAC Transfer Curve. (3a) Overall Transfer Function (3b) Effect of Negative Offset for Codes Near Zero-Scale (3c) Effect of Positive Full-Scale Error for Codes Near Full-Scale

PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CB

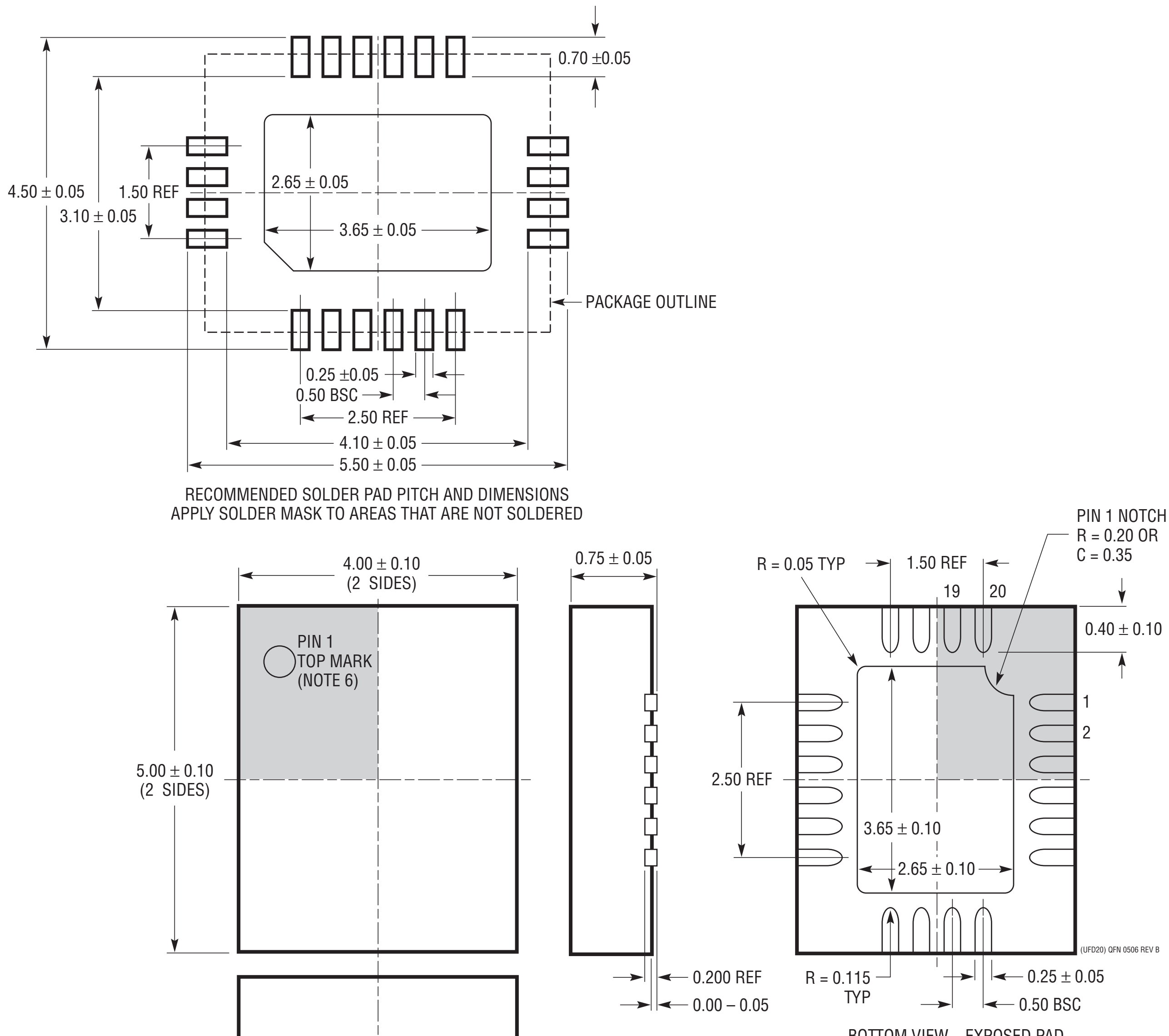


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

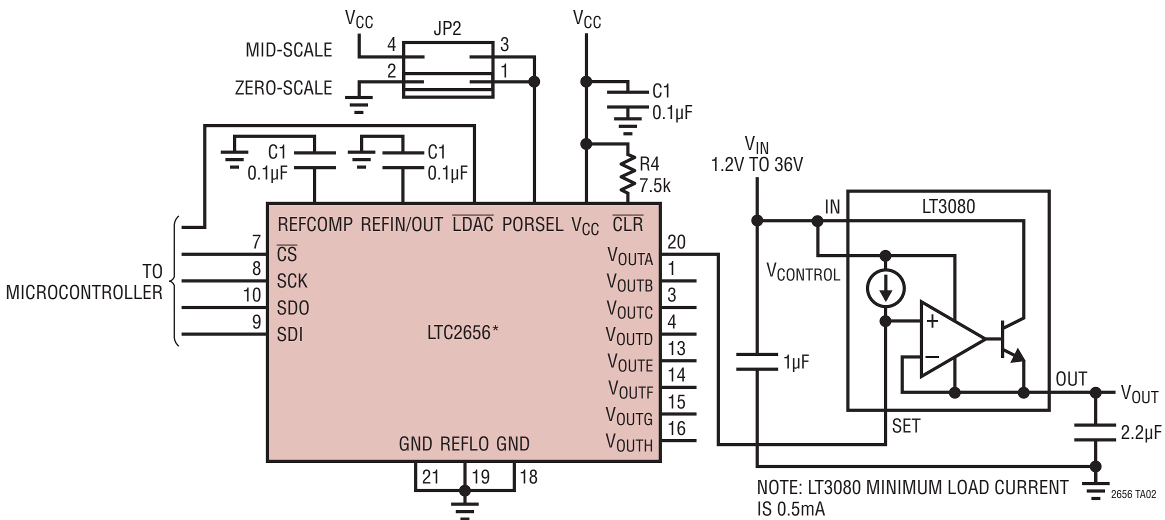
UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Digitally Controlled Output Voltage 1.1A Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1660/LTC1665	Octal 10-/8-Bit V_{OUT} DACs in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1664	Quad 10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1821	Single 16-Bit V_{OUT} DAC with ±1LSB INL, DNL	Parallel Interface, Precision 16-Bit Settling in 2μs for 10V Step
LTC2600/LTC2610/ LTC2620	Octal 16-/14-/12-Bit V_{OUT} DACs in 16-Lead Narrow SSOP	250μA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2601/LTC2611/ LTC2621	Single 16-/14-/12-Bit V_{OUT} DACs in 10-Lead DFN	300μA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP	300μA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2604/LTC2614/ LTC2624	Quad 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250μA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2605/LTC2615/ LTC2625	Octal 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	250μA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output
LTC2606/LTC2616/ LTC2626	Single 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	270μA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output
LTC2609/LTC2619/ LTC2629	Quad 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	250μA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output with Separate V_{REF} Pins for Each DAC
LTC2636	Octal 12-/10-/8-Bit V_{OUT} DACs with 10ppm/°C Reference	125μA per DAC, 2.7V to 5.5V Supply Range, Internal 1.25V or 2.048V Reference, Rail-to-Rail Output, SPI Interface
LTC2641/LTC2642	Single 16-/14-/12-Bit V_{OUT} DACs with ±1LSB INL, DNL	±1LSB (Max) INL, DNL, 3mm x 3mm DFN and MSOP Packages, 120μA Supply Current, SPI Interface
LTC2704	Quad 16-/14-/12-Bit V_{OUT} DACs with ±2LSB INL, ±1LSB DNL	Software Programmable Output Ranges Up to ±10V, SPI Interface
LTC2755	Quad 16-/14-/12-Bit I_{OUT} DACs with ±1LSB INL, ±1LSB DNL	Software Programmable Output Ranges Up to ±10V, Parallel Interface

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