

ACPL-P480 and ACPL-W480

High CMR Intelligent Power Module and Gate Drive Interface Optocoupler



Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

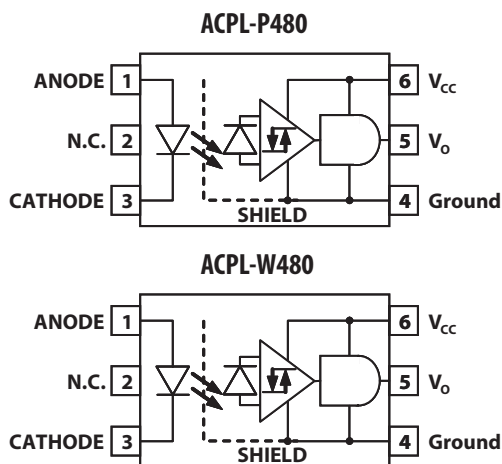
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product



Description

The ACPL-P480 and ACPL-W480 fast speed optocouplers contain a GaAsP LED and photo detector with built-in Schmitt trigger to provide logic-compatible waveforms, eliminating the need for additional wave shaping. The totem pole output eliminates the need for a pull up resistor and allows for direct drive Intelligent Power Module or gate drive. Minimized propagation delay difference between devices make these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time.

Functional Diagrams



Note: A 0.1 μ F bypass capacitor must be connected between pins 4 and 6.

Truth Table (Positive Logic)

LED	V _O
ON	HIGH
OFF	LOW

Features

- Performance Specified for Common IPM Applications Over Industrial Temperature Range.
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- Hysteresis
- Totem Pole Output (No Pull-up Resistor Required)
- Available in Stretched SO-6 package.
- Safety Approval:

UL Recognized with 3750 V_{rms} for 1 minute (5000 V_{rms} for 1 minute for all ACPL-W480 devices and Option 020 device for ACPL-P480) per UL1577.

CSA Approved.

IEC/EN/DIN EN 60747-5-2 Approved:

V_{IORM} = 891 V_{peak} for option 060 of ACPL-P480, and V_{IORM} = 1140 V_{peak} for ACPL-W480.

Specifications

- Wide operating temperature range: -40°C to 100°C.
- Maximum propagation delay $t_{PHL} / t_{PLH} = 350$ ns
- Maximum Pulse Width Distortion (PWD) = 250 ns.
- Propagation Delay Difference: Min. -100 ns, Max. 250 ns
- Wide Operating V_{CC} Range: 4.5 to 20 Volts
- 20 kV/ μ s minimum common mode rejection (CMR) at V_{CM} = 1000 V.

Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters
- General Digital Isolation

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

ACPL-P480 is UL Recognized (ACPL-W480 pending) with 3750 Vrms for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option	Package	Surface Mount	Tape & Reel	UL 1577 5000VRMS / 1 Minute Rating	IEC/EN/DIN EN 60747-5-2	Quantity	
	RoHS Compliant							
ACPL-P480	-000E	7mm Stretched SO-6	X				100 per tube	
	-500E		X	X			1000 per reel	
	-020E		X			X	100 per reel	
	-520E		X	X		X	1000 per reel	
	-060E		X				X	100 per tube
	-560E		X	X			X	1000 per reel
ACPL-W480 [^]	-000E	8mm Stretched SO-6	X		X		100 per tube	
	-500E		X	X	X		1000 per reel	
	-060E		X			X	X	100 per tube
	-560E		X	X	X	X	X	1000 per reel

[^] Advance information, subject to changes.

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P480-560E to order product of Stretched SO-6 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

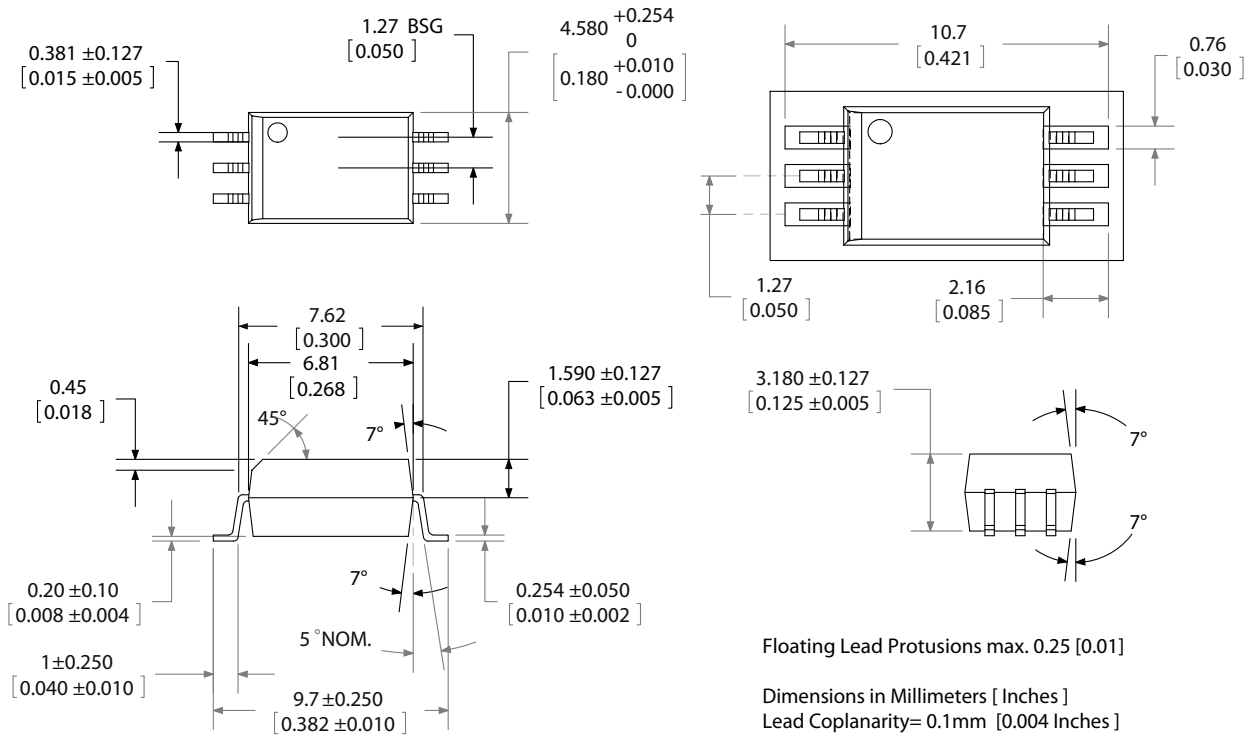
Example 2:

ACPL-P480-000E to order product of Stretched SO-6 package in tube packaging and RoHS compliant.

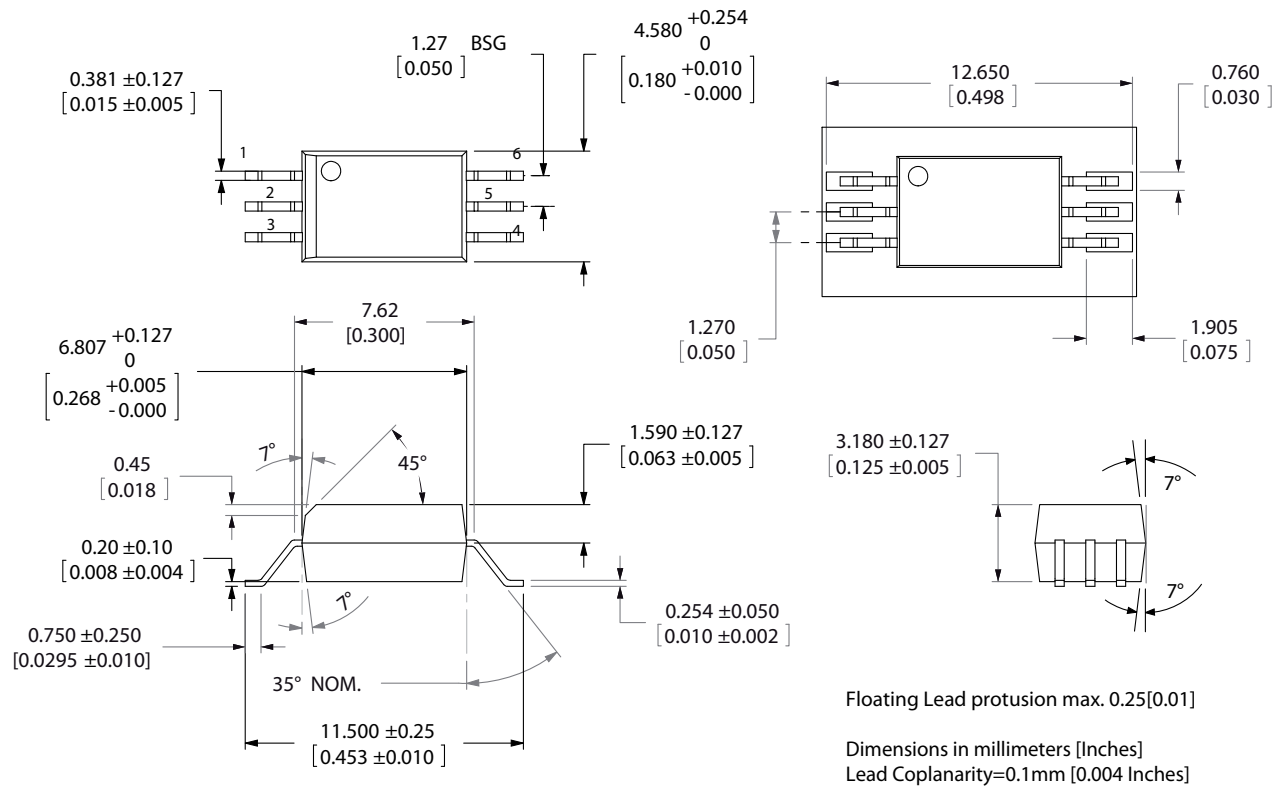
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-P480 Stretched SO-6 Package, 7 mm clearance



ACPL-W480 Stretched SO-6 Package, 8 mm clearance



Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-P480 is approved (ACPL-W480 pending) by the following organizations:

IEC/EN/DIN EN 60747-5-2 (Option 060 only)

Approval under:

IEC 60747-5-2 :1997 + A1:2002

EN 60747-5-2:2001 + A1:2002

DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

CSA

Approval under CSA Component Acceptance Notice #5,
File CA 88324.

UL

ACPL-P480: Approval under UL 1577, component recognition program up to $V_{ISO} = 3750 V_{RMS}$. File E55361.

ACPL-W480: Approval pending under UL 1577, component recognition program up to $V_{ISO} = 5000 V_{RMS}$. File E55361.

Table 1. IEC/EN/DIN EN 60747-5-2 Insulation Characteristics* (ACPL-P480 Option 060)

Description	Symbol	Characteristic		Unit
		ACPL-P480	ACPL-W480	
Installation classification per DIN VDE 0110/1.89, Table 2 for rated mains voltage $\leq 300 V_{rms}$ for rated mains voltage $\leq 450 V_{rms}$ for rated mains voltage $\leq 600 V_{rms}$			I - IV I - III I - III	
Climatic Classification		55/100/21		
Pollution Degree (DIN VDE 0110/1.89)		2		
Maximum Working Insulation Voltage	V_{IORM}	891	1140	Vpeak
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial discharge < 5 pC	V_{PR}	1670	2137	Vpeak
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with $t_m = 10$ sec, Partial discharge < 5 pC	V_{PR}	1426	1824	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 10$ sec)	V_{IOTM}	6000	8000	Vpeak
Safety-limiting values - maximum values allowed in the event of a failure.				
Case Temperature	T_S	175		°C
Input Current	$I_{S,INPUT}$	230		mA
Output Power	$P_{S,OUTPUT}$	600		mW
Insulation Resistance at T_S , $V_{IO} = 500$ V	RS	$>10^9$		Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P480	ACPL-W480	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)			0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)			NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175		V	DIN IEC 112/VDE 0303 Part 1
Isolation Group			IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(avg)}$		10	mA	
Peak Transient Input Current ($<1 \mu s$ pulse width, 300 pps) ($<200 \mu s$ pulse width, $< 1\%$ duty cycle)	$I_{F(tran)}$		1.0 40	A mA	
Reverse Input Voltage	V_R		5	V	
Average Output Current	I_O		25	mA	
Supply Voltage	V_{CC}	0	25		
Output Voltage	V_O	-0.5	25		
Total Package Power Dissipation	P_T		210	mW	1
Solder Reflow Temperature Profile	See Reflow Thermal Profile.				

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply Voltage	V_{CC}	4.5	20	V	
Forward Input Current (ON)	$I_{F(ON)}$	6	10	mA	
Forward Input Voltage (OFF)	$V_{F(OFF)}$	-	0.8	V	
Operating Temperature	T_A	-40	100	°C	

Notes:

- Derate total package power dissipation, P_T , linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.

Table 5. Electrical Specifications

Over recommended operating conditions $T_A = -40\text{ }^\circ\text{C}$ to $100\text{ }^\circ\text{C}$, $V_{CC} = +4.5\text{ V}$ to 20 V , $I_{F(ON)} = 6\text{ mA}$ to 10 mA , $V_{F(OFF)} = 0\text{ V}$ to 0.8 V , unless otherwise specified. All typicals at $T_A = 25\text{ }^\circ\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	$I_{OL} = 6.4\text{ mA}$	1, 3, 9, 10	
Logic High Output Voltage ACPL-P480 ACPL-W480	V_{OH}	2.4 2.7 2.7	$V_{CC} - 1.1$		V	$I_{OH} = -2.6\text{ mA}$ $I_{OH} = -0.4\text{ mA}$ $I_{OH} = -1.6\text{ mA}$	2, 3, 7, 9, 10	
Threshold Input Current Low to High	I_{FLH}		2.2	5.5	mA			
Output Leakage Current ($V_O = V_{CC} + 0.5\text{ V}$)	I_{OHH}			100 500	μA μA	$V_{CC} = 5\text{ V}, I_F = 10\text{ mA}$ $V_{CC} = 20\text{ V}, I_F = 10\text{ mA}$		
Logic Low Supply Current	I_{CCL}		1.9 2.0	3.0 3.0	mA mA	$V_{CC} = 5.5\text{ V}, V_F = 0\text{ V}, I_O = \text{Open}$ $V_{CC} = 20\text{ V}, V_F = 0\text{ V}, I_O = \text{Open}$		
Logic High Supply Current	I_{CCH}		1.5 1.6	2.5 2.5	mA mA	$V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}, I_O = \text{Open}$ $V_{CC} = 20\text{ V}, I_F = 10\text{ mA}, I_O = \text{Open}$		
Logic Low Short Circuit Output Current	I_{OSL}	25 50			mA mA	$V_O = V_{CC} = 5.5\text{ V}, V_F = 0\text{ V}$ $V_O = V_{CC} = 20\text{ V}, V_F = 0\text{ V}$		1
Logic High Short Circuit Output Current	I_{OSH}			-25 -50	mA mA	$V_{CC} = 5.5\text{ V}, I_F = 6\text{ mA}, V_O = \text{GND}$ $V_{CC} = 20\text{ V}, I_F = 6\text{ mA}, V_O = \text{GND}$		1
Input Forward Voltage	V_F		1.5	1.7 1.85	V V	$T_A = 25\text{ }^\circ\text{C}, I_F = 6\text{ mA}$ $I_F = 6\text{ mA}$	4	
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10\text{ }\mu\text{A}$		
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$		1.7		mV/ $^\circ\text{C}$	$I_F = 6\text{ mA}$		
Input Capacitance	C_{IN}		60		pF	$f = 1\text{ MHz}, V_F = 0\text{ V}$		2

Notes:

1. Duration of output short circuit time should not exceed 10 ms.
2. Input capacitance is measured between pin 1 and pin 3.

Table 6. Switching Specifications

Over recommended operating conditions $T_A = -40\text{ }^{\circ}\text{C}$ to $100\text{ }^{\circ}\text{C}$, $V_{CC} = +4.5\text{ V}$ to 20 V , $I_{F(ON)} = 6\text{ mA}$ to 10 mA , $V_{F(OFF)} = 0\text{ V}$ to 0.8 V , unless otherwise specified. All typicals at $T_A = 25\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150	350	ns	With Peaking Capacitor	5, 6	1
Propagation Delay Time to Logic High Output Level	t_{PLH}		110	350	ns	With Peaking Capacitor	5, 6	1
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $ = PWD			250	ns			2
Propagation Delay Difference Between Any 2 Parts	PDD	-100		250	ns			3
Output Rise Time (10-90%)	t_r		16		ns		5, 8	
Output Fall Time (90-10%)	t_f		20		ns		5, 8	
Logic High Common Mode Transient Immunity	$ CM_H $	20			kV/ μs	$ V_{CM} = 1000\text{ V}$, $I_F = 6.0\text{ mA}$, $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$	11	4
Logic Low Common Mode Transient Immunity	$ CM_L $	20			kV/ μs	$ V_{CM} = 1000\text{ V}$, $V_F = 0\text{ V}$, $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$	11	4

Table 7. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750**			V_{rms}	$RH < 50\%$, $t = 1\text{ min.}$ $T_A = 25\text{ }^{\circ}\text{C}$		5, 6
Input-Output Resistance	R_{I-O}		10^{12}			$V_{I-O} = 500\text{ Vdc}$		6
Input-Output Capacitance	C_{I-O}		0.6			$f = 1\text{ MHz}$, $V_{I-O} = 0\text{ Vdc}$		6

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable).

** For all ACPL-P480 devices except Option 020

*** For ACPL-W480 and Option 020 of ACPL-P480)

Notes:

1. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
2. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
3. The difference between t_{PLH} and t_{PHL} between any two devices under the same test condition.
4. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, $V_O > 2.0\text{ V}$. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, $V_O < 0.8\text{ V}$.
5. Device considered a two-terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.
6. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500\text{ V}_{RMS}$ for one second (leakage detection current limit, $I_{I-O} \leq 5\text{ }\mu\text{A}$).; each optocoupler with option 020 is proof tested by applying an insulation test voltage $\geq 6000\text{ V}_{RMS}$ for 1 second (leakage detection current limit, $I_{I-O} \leq 5\text{ }\mu\text{A}$). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.

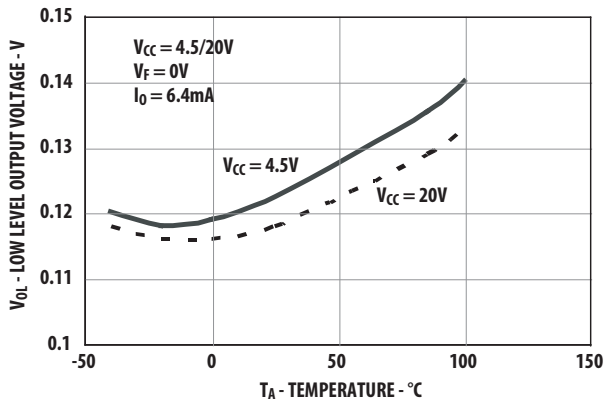


Figure 1. Typical Logic Low Output Voltage vs. Temperature

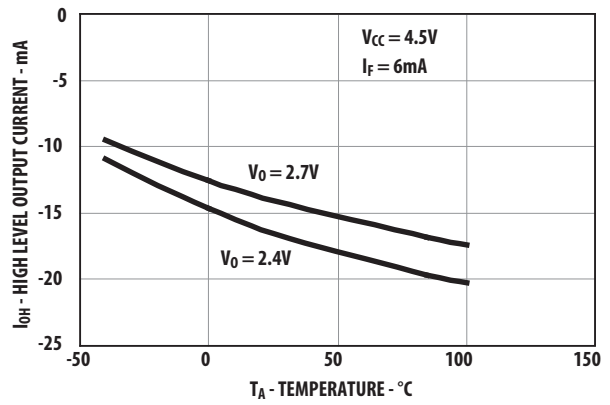


Figure 2. Typical Logic High Output Current vs. Temperature

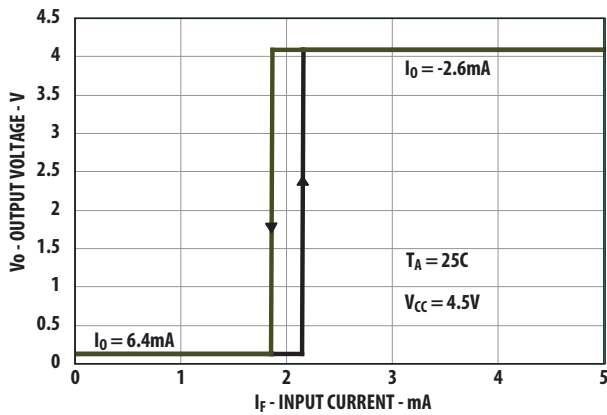


Figure 3. Typical Output Voltage vs. Forward Input Current

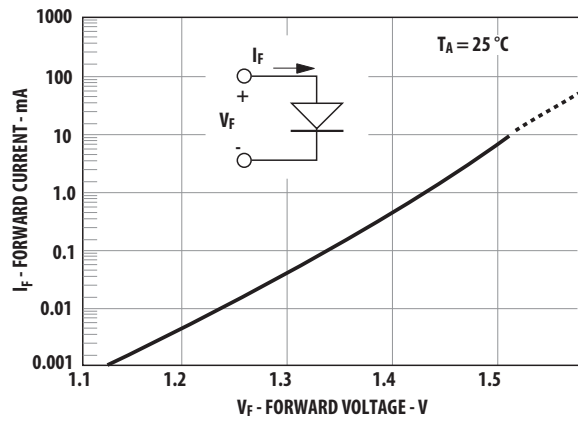


Figure 4. Typical Input Diode Forward Characteristic

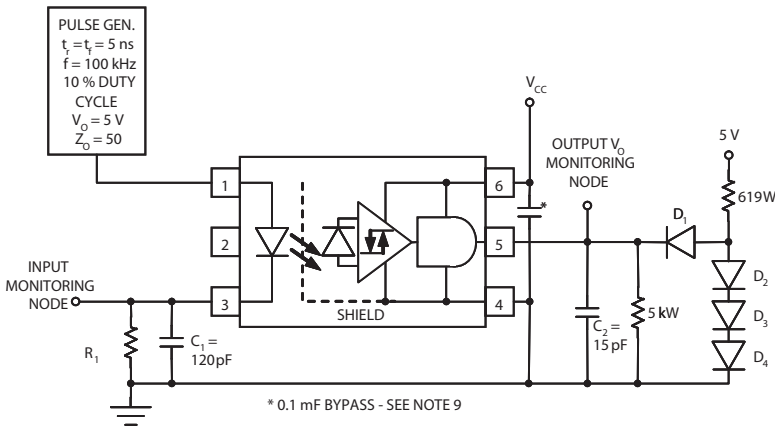
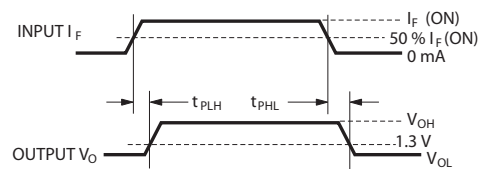


Figure 5. Circuit for t_{PLH} , t_{PHL} , t_r , t_f

THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN C_1 AND C_2 .

R_1	580 W	330 W
$I_{F(ON)}$	6 mA	10 mA

ALL DIODES ARE 1N916 OR 1N3064.



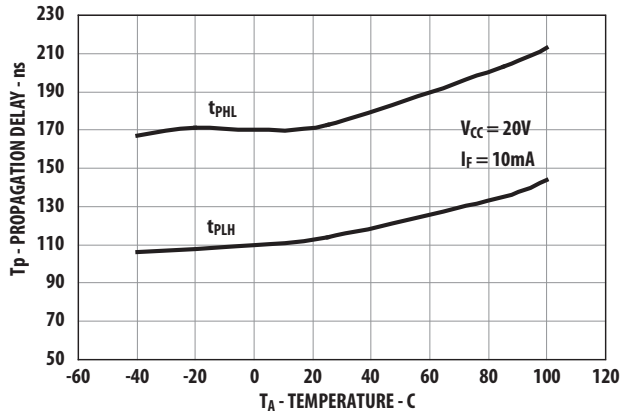


Figure 6. Typical Propagation Delays vs. Temperature.

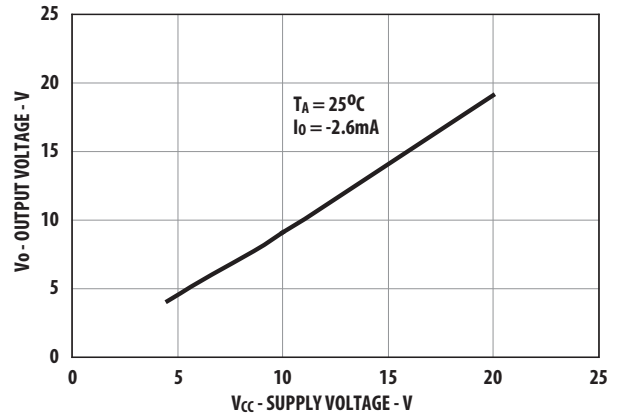


Figure 7. Typical Logic High Output Voltage vs. Supply Voltage

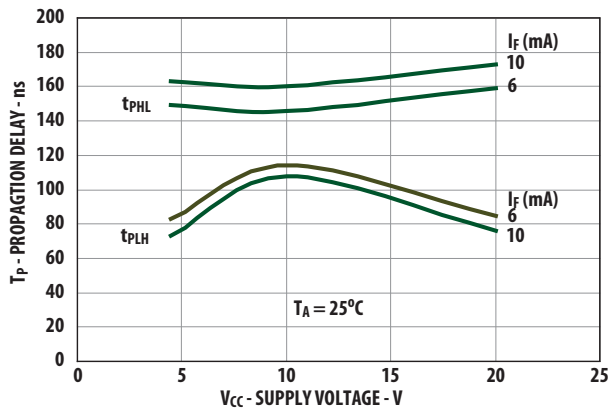


Figure 8. Typical Propagation Delay vs. Supply Voltage

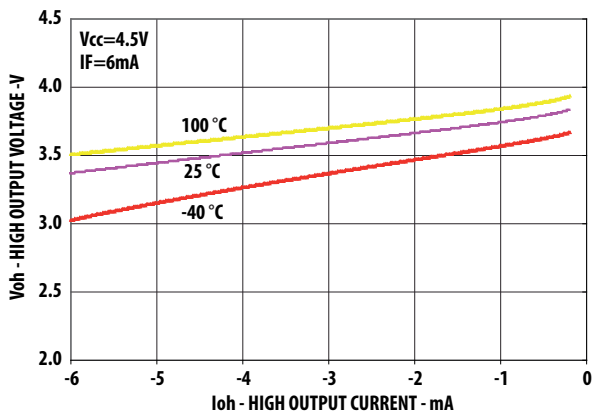


Figure 9. V_{oh} vs I_{oh} Across Temperatures

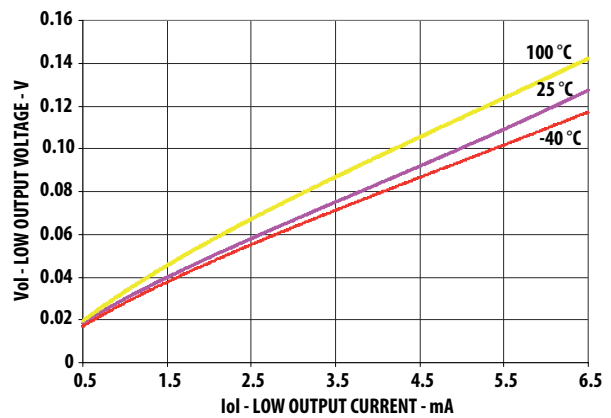


Figure 10. V_{ol} vs I_{ol} Across Temperatures

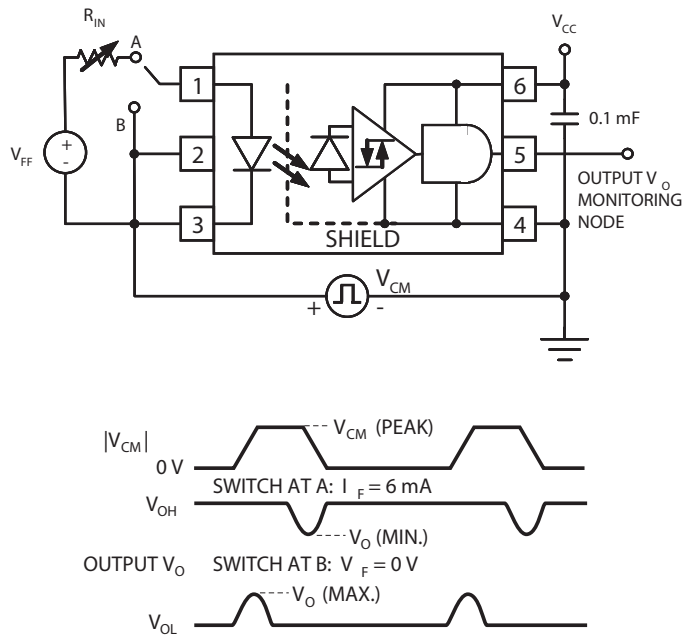


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

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