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ASSP CXPI Transceiver IC for Automotive Network

The S6BT112A01 and S6BT112A02 are integrated transceiver ICs for automotive communication network with Clock Extension Peripheral Interface (CXPI). It has a flexible bit rate ranging from 2.4 kbps to 20 kbps and is JASO CXPI compliant. This CXPI transceiver IC connects the CXPI data link controller and the CXPI Bus line, and enables direct connection to the vehicle battery with a high surge protection. Additionally, these devices have an optional Spread Spectrum Clock Generator (SSCG) function.

During Sleep mode, S6BT112A01 and S6BT112A02 reduce power consumption. The Cypress CXPI transceiver IC supports master node and slave node as selected SELMS pins.

Features

- Compliant with the JASO CXPI (JASO D 015-3: 2015) standard
- Compliant with the SAE CXPI (J3076_201510) standard
- Supports 2.4 kbps to 20 kbps bitrate
- Waveshaping for low Electromagnetic Interference (EMI)
- Operating voltage range: 5.3 V to 18 V
- Direct battery operation with protection against load dump, jump start, and transients
- BUS short to V_{BAT} overcurrent protection
- Loss of ground protection; BUS pin leakage is lower than ±1 mA

- Easy selection of master node or slave node
- Overtemperature protection
- Low-voltage detection
- Supports Sleep and Wakeup modes
- Sleep mode current: 6 µA (typical at Slave)
- Halogen-free 8-pin SOIC package
- ESD protection HBM (1.5 kΩ, 100 pF) ±8 kV (BUS pin, BAT pin)
- Voltage tolerance ±40 V (BUS pin)
- S6BT112A01: With SSCG
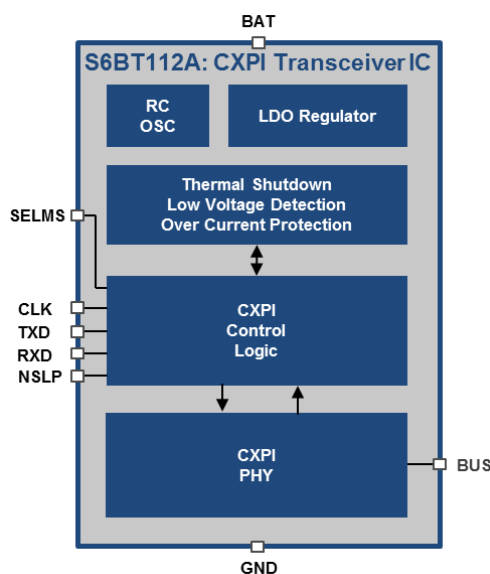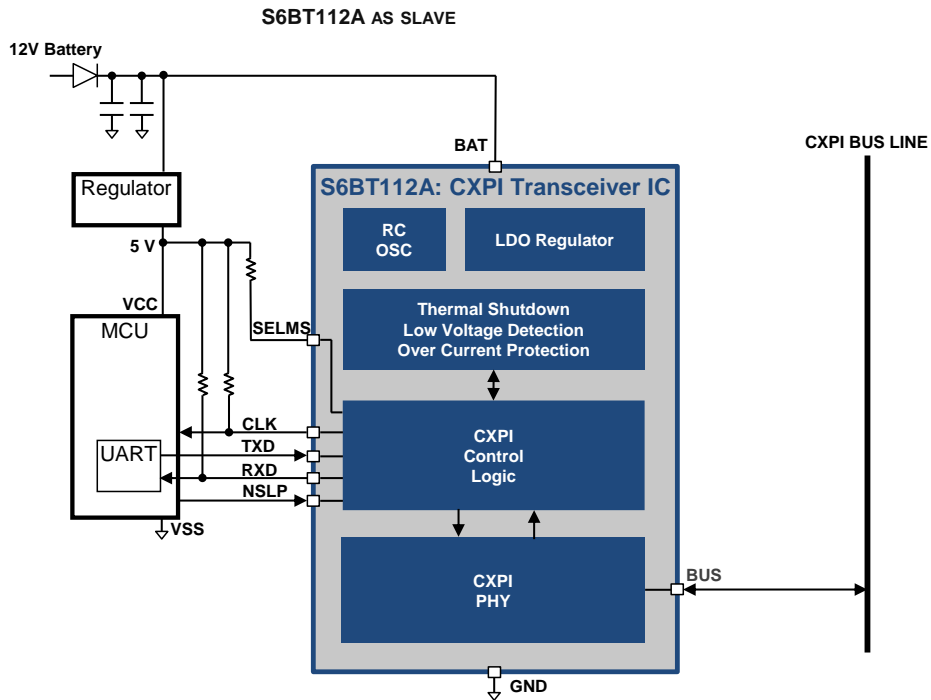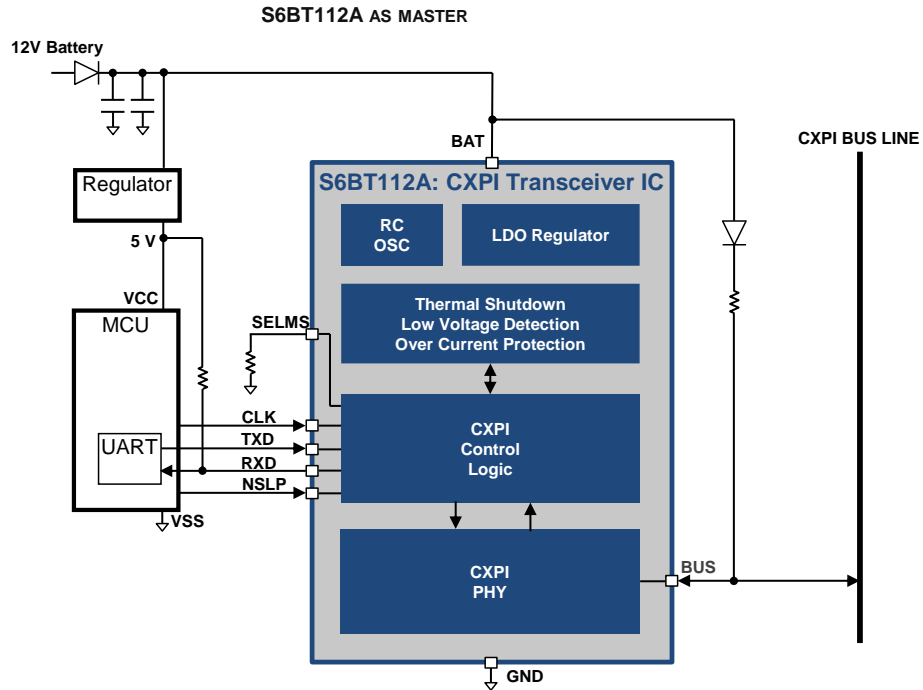 S6BT112A02: Without SSCG

S6BT112A Block Diagram

Table of Contents

1. Applications

The following figures illustrate the typical applications of S6BT112A01 or S6BT112A02.

S6BT112A AS MASTER

S6BT112A AS SLAVE

2. Pin Assignment

Figure 2-1. Pin Assignment
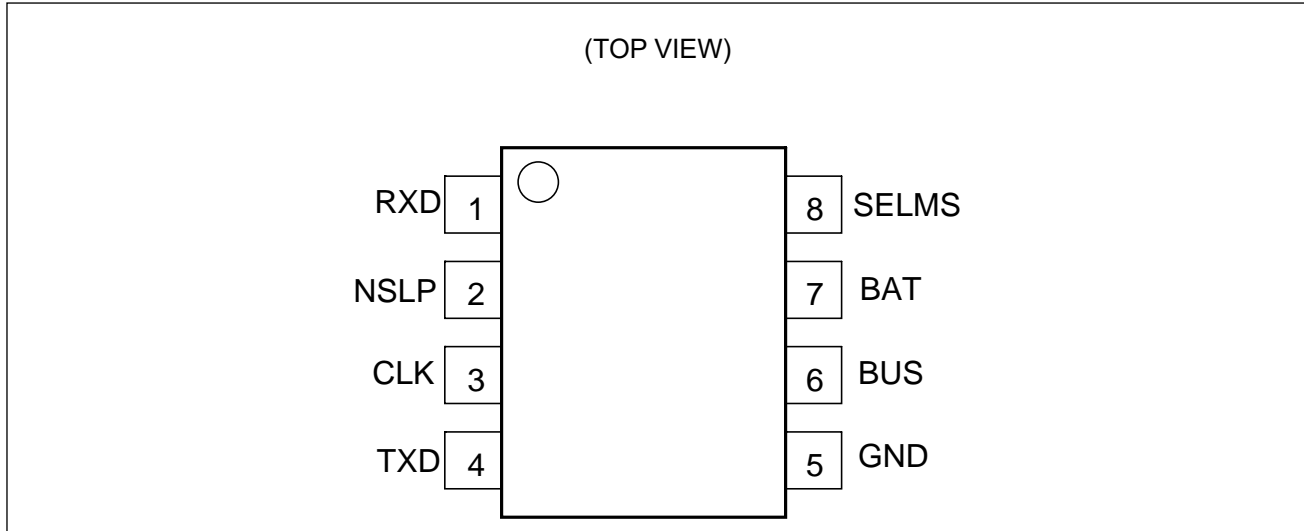
3. Pin Descriptions

Table 3-1. Pin Descriptions

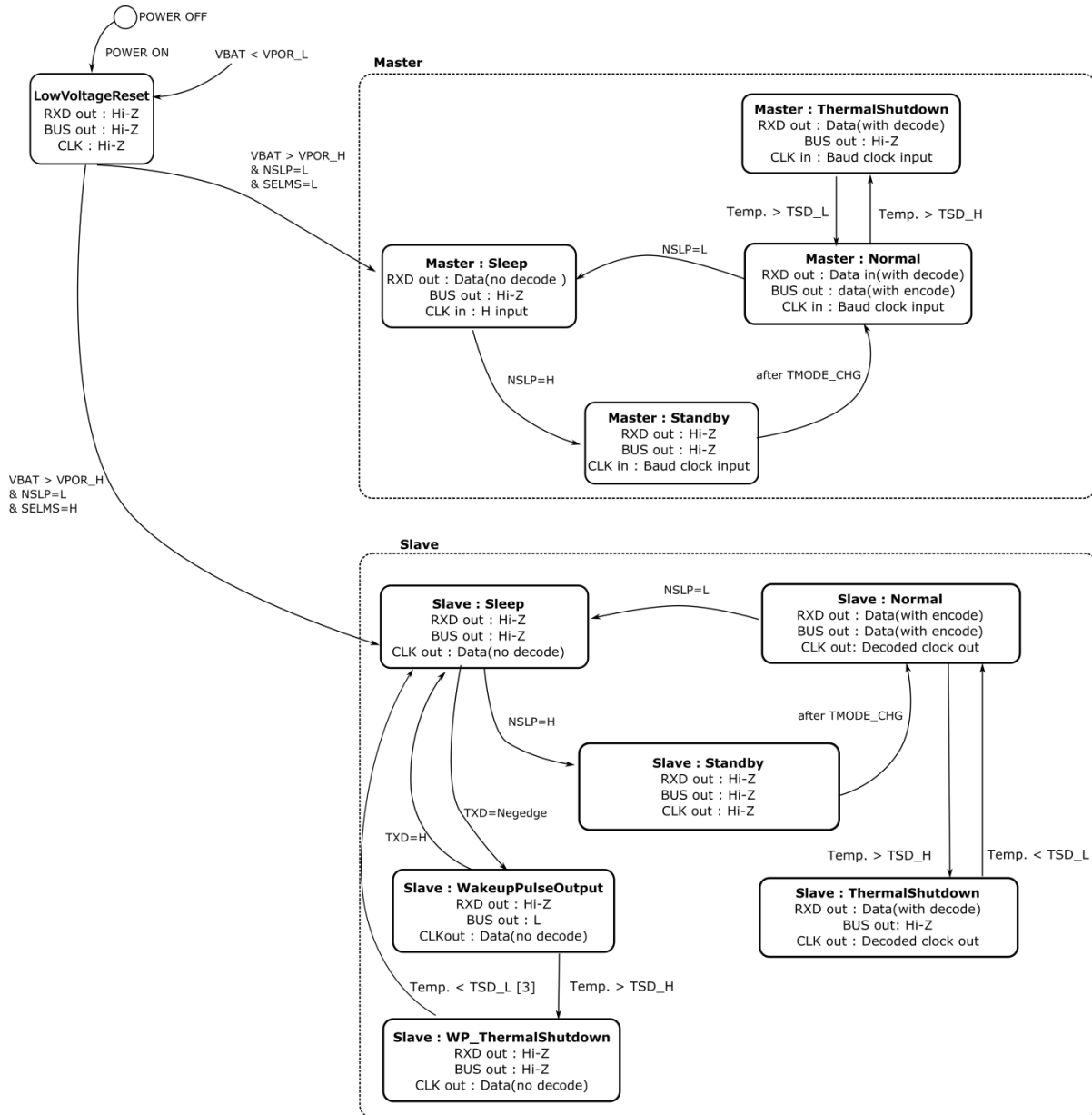| Pin Number	Symbol	Direction	Description
1	RXD	Output	Receive data output (open-drain) Requires external pull-up resistor (refer to Table 7-1)
2	NSLP	Input	Sleep control input Low: Sleep mode or Standby mode High: Normal mode Refer to section 5.2.2 or section 5.3.2
3	CLK	I/O	When the SELMS pin is Low, the CLK pin is the Baud rate clock input Input clock signal with baud rate frequency (When the input clock frequency is 20 kHz, the bit rate is 20 kbps) When the SELMS pin is High, the CLK pin is Baud rate clock output Outputs clock signal with baud rate frequency (When the output clock frequency is 20 kHz , the bit rate is 20 kbps) Open drain output Requires external pull-up resistor (refer to Table 7-1)
4	TXD	Input	Transmit data input
5	GND	-	Ground
6	BUS	I/O	CXPI BUS line Input/Output
7	BAT	-	Battery (voltage source) supply
8	SELMS	Input	Master / slave node select input Low: Master High: Slave

4. Block Diagram

Figure 4-1. Block Diagram
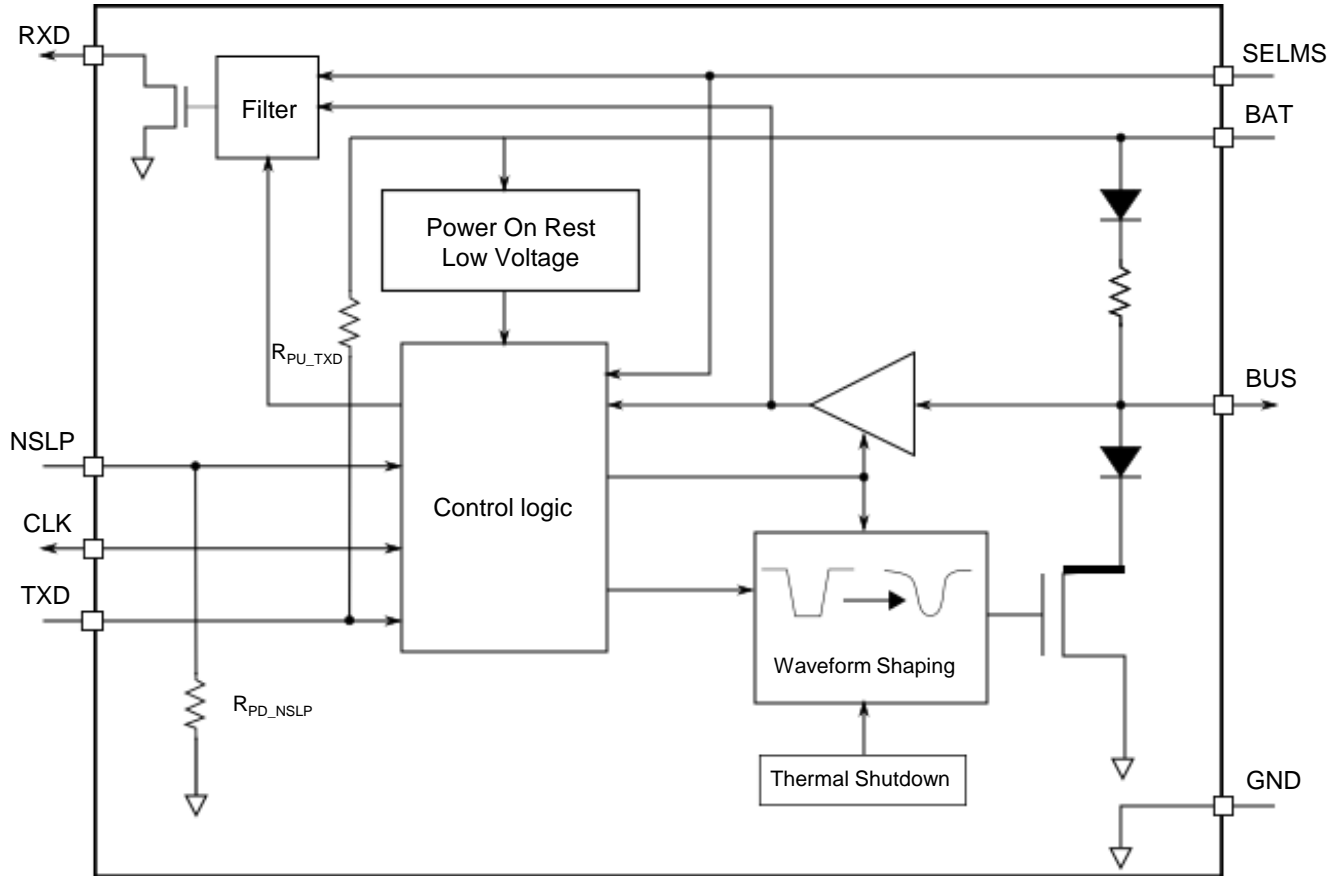
5. Function Description

5.1 Operation Modes

Figure 5-1. State Transition Diagram

POWER OFF

POWER ON
VBAT < VPOR_L

LowVoltageReset
RXD out : Hi-Z
BUS out : Hi-Z
CLK : Hi-Z

VBAT > VPOR_H
& NSLP=L
& SELMS=L

VBAT > VPOR_H
& NSLP=L
& SELMS=H

Master

Master : ThermalShutdown
RXD out : Data(with decode)
BUS out : Hi-Z
CLK in : Baud clock input

Temp. > TSD_L   Temp. > TSD_H

NSLP=L

Master : Sleep
RXD out : Data(no decode)
BUS out : Hi-Z
CLK in : H input

Master : Normal
RXD out : Data in(with decode)
BUS out : data(with encode)
CLK in : Baud clock input

NSLP=H   after TMODE_CHG

Master : Standby
RXD out : Hi-Z
BUS out : Hi-Z
CLK in : Baud clock input

Slave

NSLP=L

Slave : Sleep
RXD out : Hi-Z
BUS out : Hi-Z
CLK out : Data(no decode)

Slave : Normal
RXD out : Data(with encode)
BUS out : Data(with encode)
CLK out: Decoded clock out

NSLP=H   after TMODE_CHG

TXD=Negedge

TXD=H

Slave : Standby
RXD out : Hi-Z
BUS out : Hi-Z
CLK out : Hi-Z

Temp. > TSD_H   Temp. < TSD_L

Slave : WakeupPulseOutput
RXD out : Hi-Z
BUS out : L
CLKout : Data(no decode)

Slave : ThermalShutdown
RXD out : Data(with decode)
BUS out: Hi-Z
CLK out : Decoded clock out

Temp. < TSD_L [3]   Temp. > TSD_H

Slave : WP_ThermalShutdown
RXD out : Hi-Z
BUS out : Hi-Z
CLK out : Data(no decode)

Notes

[1] : "Hi-z" means high-impedance.

[2] : Switching of the master / slave during operation is prohibited. Refer to section 5.4.5.

[3] : The operation mode, after the transceiver powers on, has to start from sleep mode.

[4] : If TXD is Low when releasing the thermal shutdown, TXD has to toggle "High" before valid.
TXD is a Low signal input. For details, refer to section 5.4.7.

5.2   Master Node

■There is only one node in a system, which functions as a schedule manager and a primary clock master.

■The transceiver works in Master mode when low-level is applied on SELMS.

■The baud rate clock is applied on the CLK pin in the Master state.

■The transceiver is usually used as the "Master" or "Slave", except for the "Secondary Clock master function".

■The SELMS input should not be changed in normal mode.

■The SELMS input should not be changed during wakeup pulse transmission in Sleep mode.

■The CLK pin inputs for the baud rate clock in Master state.

Table 5-1. SELMS Pin State for Master

Pin	Input Signal	Master/Slave
SELMS	Low	Master

Figure 5-2. CLK Input -> BUS signal (Master)
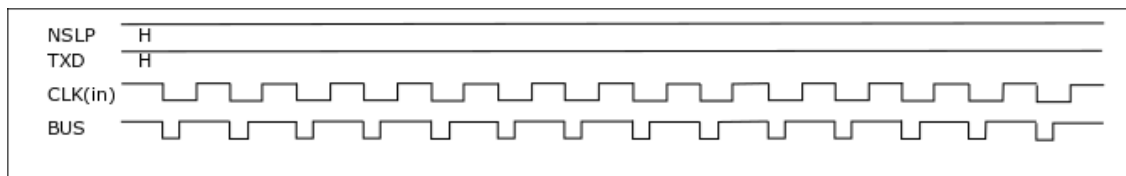
5.2.1   Normal Mode

The Normal mode denotes the state to which communication is possible. The master node transmits the clock to the CXPI BUS, which means that the clock is master. During the Normal mode, the transmitted signal is encoded and the received signal is decoded. When the transmitting node transmits data to the CXPI BUS, it transmits to the TXD pin after converting the data to UART format by 1 byte. The data is transmitted to the CXPI BUS as LSB first.

When the receiving node receives data from the CXPI BUS, it receives from the RXD pin in the UART format by 1 byte. The UART format is listed in Table 5-2. Refer to the JASO CXPI (JASO D 015-3:2015) standard for details of the operation.

Table 5-2. UART Format

Start bit	bit 0 (LSB)	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7(MSB)	Stop bit

5.2.2   *Sleep Mode*

The Sleep mode denotes a power-saving state during which each node stops transmitting and receiving data. All nodes transition to Sleep mode immediately after power-on. The nodes also transition to Sleep mode after the Sleep processing is executed from the Normal mode and transition from Standby mode or Normal mode due to CXPI BUS error.

When each node receives the Wakeup factor during the Sleep mode, it transitions to the Standby mode.The Wakeup factor (for example, detecting that the ignition has been turned on) of each node is different from each application (for example, detecting that the ignition has been turned on) and the external factor that receives the Wakeup pulse from the CXPI BUS. During the Sleep mode, the reception signal is received without decoding. The MCU can detect a wakeup pulse width monitor using the RXD signal.

The sleep mode is initiated by a falling edge on the NSLP pin while TXD is already set High. The CXPI BUS transmit path is immediately disabled when the NSLP pin goes Low. All wake-up events must be maintained for a specific period (refer to the T_{MODE_CHG} parameter in Table 8-7).

Stopping the clock input at high level of CLK is recommended. Then turn the NSLP pin to Low after T_{SLP_WT} as shown in Figure 5-3.

Table 5-3. Transition from Normal to Sleep mode

| Pin	Pin State	Description
TXD	High	No data transmitting
CLK	High	No clock receiving
NSLP	High to Low	-
RXD	High impedance	High level with external pull-up resistor.
BUS	High impedance	High level with external pull-up resistor.
SELMS	Low	-

Note: The "Pin State" indicates before the falling edge in the NSLP pin

Table 5-4. Transition from Sleep to Normal mode

Pin	Pin State	Description
TXD	High	No data transmitting
CLK	High	No clock receiving
NSLP	Low to High	-
RXD	High impedance	High level with external pull-up resistor.
BUS	High impedance	High level with external pull-up resistor.
SELMS	Low	-

Note: The "Pin State" indicates the state before the rising edge in the NSLP pin

Figure 5-3. Transition Sequence Between Sleep and Normal Mode
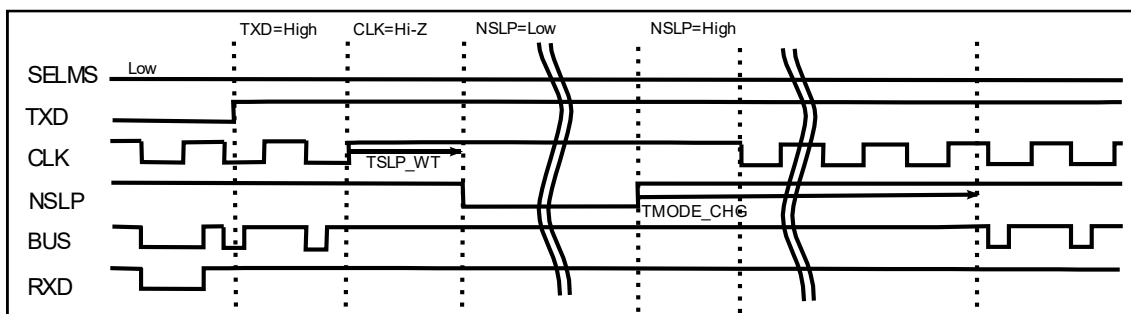
Note:

 [1] "Hi-Z" means high-impedance.

5.2.3 Standby Mode

The Standby mode denotes the prepared state to the Normal mode after releasing the Sleep mode. During the CLK state (in slave node), the RXD pin and the BUS pin are in a high-impedance state. After T_{MODE_CHG}, the state changes to the Normal mode.

5.2.4 Power-on Sequence

The power-on sequence occurs at power-up while setting up Sleep mode. When V_{BAT} is above 5.3 V, the NSLP pin should be in a High state. After transition to the normal mode, activate the BUS pin after a clock input of 33 periods.

Figure 5-4. Power-on Sequence of Master Node
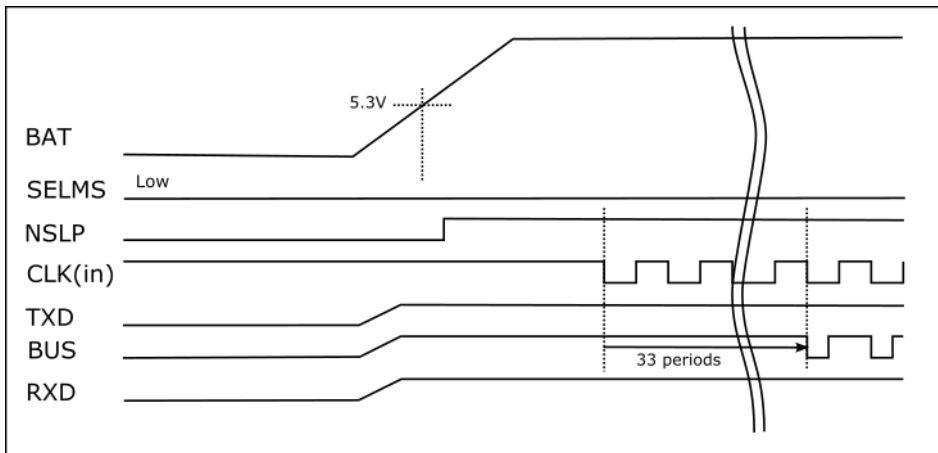
5.3   Slave Node

All the nodes, except the master node, are connected with the system. The transceiver works as Slave when High level is applied on SELMS. The CLK pin outputs the baud rate clock during the Slave state.

The transceiver is usually used as the "Master" or "Slave", except for the "Secondary Clock master function".

Table 5-5. SELMS Pin State for Slave

Pin	Input Signal	Master/Slave
SELMS	High	Slave

The SELMS input should not be changed during the Normal mode or during wakeup pulse transmission in the Sleep mode. The CLK pin outputs the baud rate clock in Slave node.

Figure 5-5. CLK Pin Clock Output (Slave)
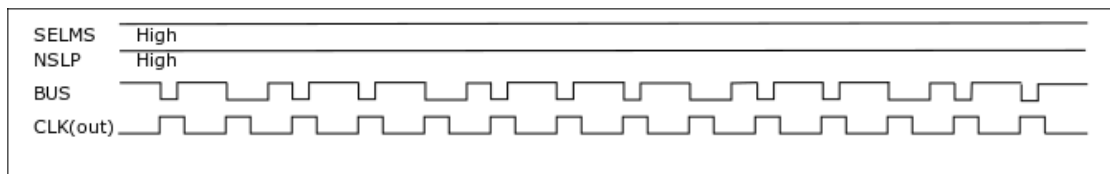
5.3.1   Normal Mode

The Normal mode can perform data transmit and receive. During the Normal mode, the signal that is transmitted is encoded and the signal that is received is decoded. When the transmitting node transmits data to the CXPI BUS, it transmits to the TXD pin after converting the data to UART format by 1 byte. The data is transmitted to the CXPI BUS by LSB first. When the receiving node receives data from the CXPI BUS , it revises from the RXD pin in the UART format by 1 byte. The UART format is shown in Table 5-6. Refer to the JASO CXPI (JASO D 015-3:2015) standard for details of the operation.

Table 5-6. UART Format

Start bit	bit 0 (LSB)	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7(MSB)	Stop bit

5.3.2   Sleep Mode

The Sleep mode denotes a state of power saving during which each node stops transmit and receive of data. All nodes transition to the Sleep mode immediately after power-on. They also transition to the Sleep mode after the sleep processing is executed from the Normal mode and transition from the Standby mode or the Normal mode due to CXPI BUS error.

During the Sleep mode, when each node receives the Wakeup factor, it transitions to the Standby mode. The Wakeup factor is different from each application and is composed of the internal factor (for example, detecting that the ignition has been turned on) and the external factor that receives the Wakeup pulse from the CXPI BUS.

During the Sleep mode, the reception signal is received without decoding. The sleep mode is initiated by a falling edge on the NSLP pin while the TXD pin is already set High. The CXPI BUS transmit path is immediately disabled when the NSLP pin goes Low.

All wake-up events must be maintained for a specific period (refer to T$_{MODE\_CHG}$ in Table 8-7).

Figure 5-6. Transition Sequence Between Sleep and Normal Mode
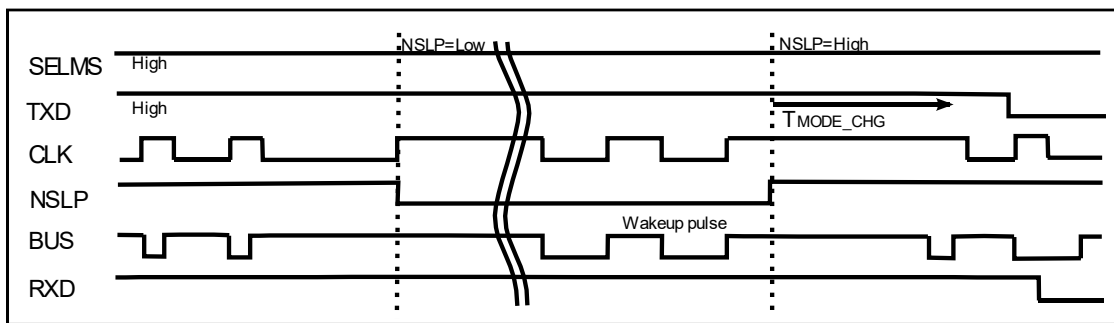
Table 5-7. Transition from Normal to Sleep Mode

Pin	Pin State	Description
TXD	High	No data transmitting
CLK	High impedance	High level with external pull-up resistor.
NSLP	High to Low	-
RXD	High impedance	High level with external pull-up resistor.
BUS	High impedance	High level with external pull-up resistor.
SELMS	High	-

Note: The "Pin State" indicates the state before the falling edge of the NSLP pin.

Table 5-8. Transition from Sleep to Normal Mode

| Pin	Pin State	Description
TXD	High	No data transmitting
CLK	High impedance	High level with external pull-up resistor.
NSLP	Low to High	-
RXD	High impedance	High level with external pull-up resistor.
BUS	High impedance	High level with external pull-up resistor.
SELMS	High	-

Note: The "Pin State" indicates the state before the rising edge of the NSLP pin.

■Receiver Function in Sleep Mode

During the Sleep mode, the received signal will be output from the CLK pin without decoding a received signal. The RXD pin outputs at High level. When the Master node transmits the encoded PWM clock signal to the CXPI BUS during a wake-up sequence, Slave MCUs receive shorter low-level width signals than the UART communication period and possibly get errors. This is because the Slave node is received without decoding. To avoid these errors, S6BT112A01 or S6BT112A02 CXPI transceiver IC outputs receive signals on the CLK pin in the Sleep mode.

MCU can detect a wake-up pulse width to monitor the CLK signal. (Figure 5-7)

Figure 5-7. CLK Output of Receive Signal、RXD Stays High (for Slave Node)
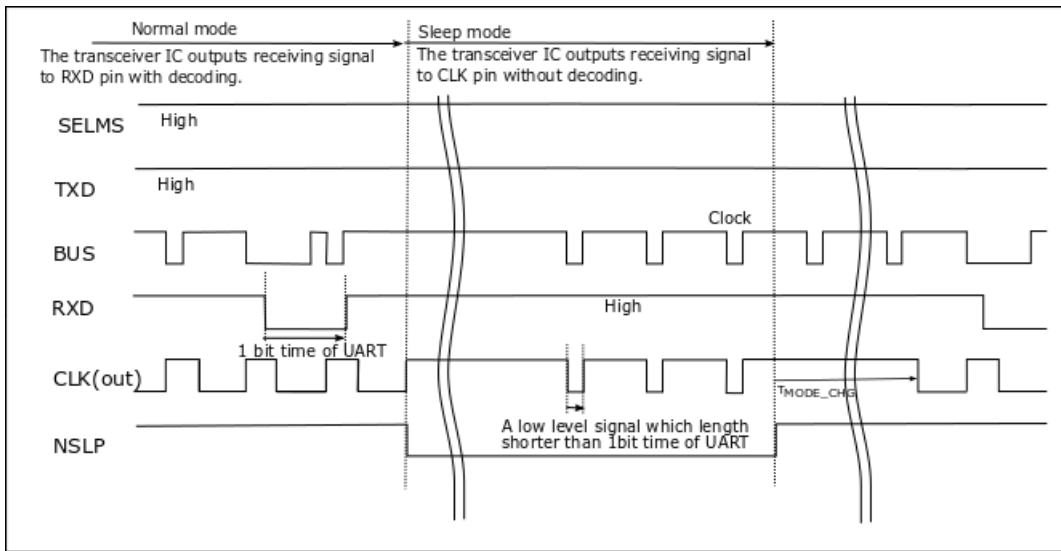
■Wakeup Function

The WakeupPulseOutput state transmits out the wakeup pulse in the Slave node. When the slave device returns from the Sleep mode, it must transmit a wake-up pulse. As the NSLP pin is in a Low state, the TXD pin transmits a Low state. The TXD signal is transmitted to the BUS pin without encode. The TXD pin outputs the signal width, which is a value obtained by subtracting the T_{TXD_BT}:

Signal width = TXD signal ("L") – TTXD_BT("L")

Refer to Table 8-7 for TTXD_BT("L").

Figure 5-8. Wake-Up Pulse Transmission
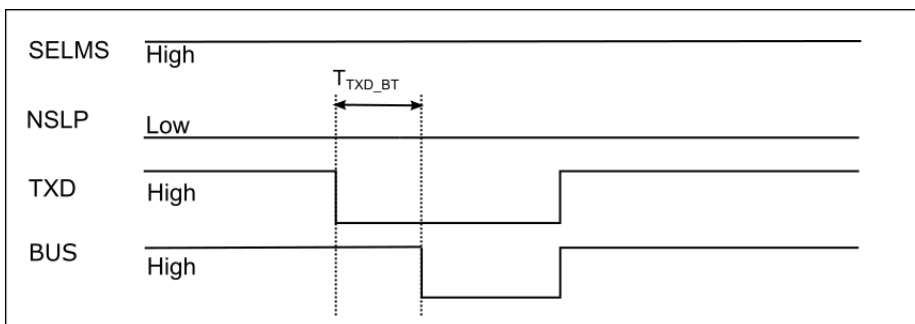
As shown in Table 5-9, in case of 19.2 kbps bitrate, 9 bits (start bit plus 8 bits data) of Low level in TXD signal transmites a 402 µs (min) width wakeup pulse to the BUS. In case of 20 kbps bitrate (50 µs/Bit), to transmite over 400 µs wakeup pulse, over 466 µs TXD Low signal is needed, which can be output by a GPIO port with a timmer.

Table 5-9. Bitrate of 19.2 kbps (52 µs/Bit)

UART Transmission Data	Number of Bits of L Level	TXD signal ("L")	Wakeup Pulse Width (min)
FCH	3-bit	156 µs	90 µs
F8H	4-bit	208 µs	142 µs
F0H	5-bit	260 µs	194 µs
E0H	6-bit	312 µs	246 µs
C0H	7-bit	364 µs	298 µs
80H	8-bit	416 µs	350 µs
00H	9-bit	468 µs	402 µs

5.3.3 Standby Mode

This is the standby state during the Normal mode after releasing the Sleep mode. During this state, CLK (in slave node), the RXD pin, and the BUS pin enter the high-impedance state. After "T_{MODE_CHG}," this state changes to the Normal mode.

5.3.4 Power-on Sequence

This sequence occurs at power-up, while setting up the Sleep mode. When V_{BAT} is above 5.3 V, the NSLP pin should be in a High state.

Figure 5-9. Power-on Sequence of Slave Node
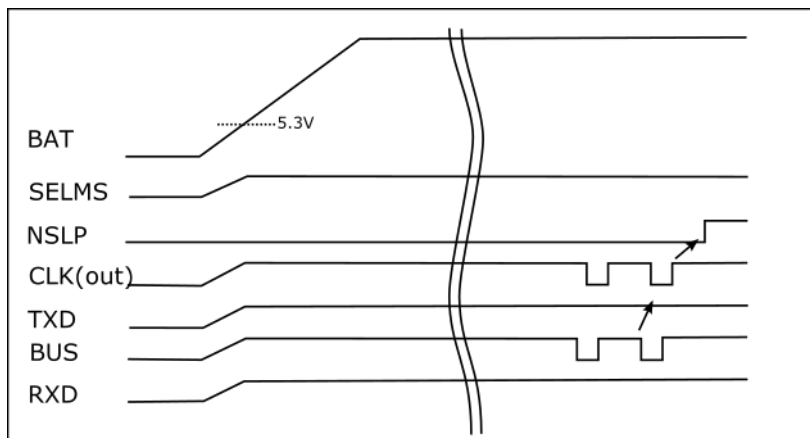
5.4 Common Functions

5.4.1 Overtemperature Protection

The overtemperature protection (OTP) monitors the die temperature. If the junction temperature exceeds the shutdown junction temperature, T_{SD_H}, the thermal protection circuit disables the output driver.

The driver is enabled again when the junction temperature falls below T_{SD_L} and theTXD pin is toggled. (see Table 5-10)

5.4.2 WP_ThermalShutdown

The WP_ThermalShutdown state detects the "shutdown temperature" during the WakeupPulseOutput mode. The overtemperature protection is inactive during the Sleep mode.

Table 5-10. Input Signal Change after Recovery from Thermal Shutdown

Master/Slave	Pin	Toggle of Input Signal
Master	TXD	Required
Slave	TXD	Required

Table 5-11. State Under Thermal Shutdown

Master/Slave	Pin	Description
Master	TXD	Normal function
	NSLP	High: Normal mode / Low: Sleep mode (Thermal protection inactive)
	CLK(input)	Normal function
	RXD	Normal function
	BUS	High impedance
Slave	TXD	Normal function
	NSLP	High: Normal mode / Low: Sleep mode (Thermal protection inactive)
	CLK	Normal function
	RXD	Normal function
	BUS	High impedance

Figure 5-10. Sequence of Thermal Shutdown
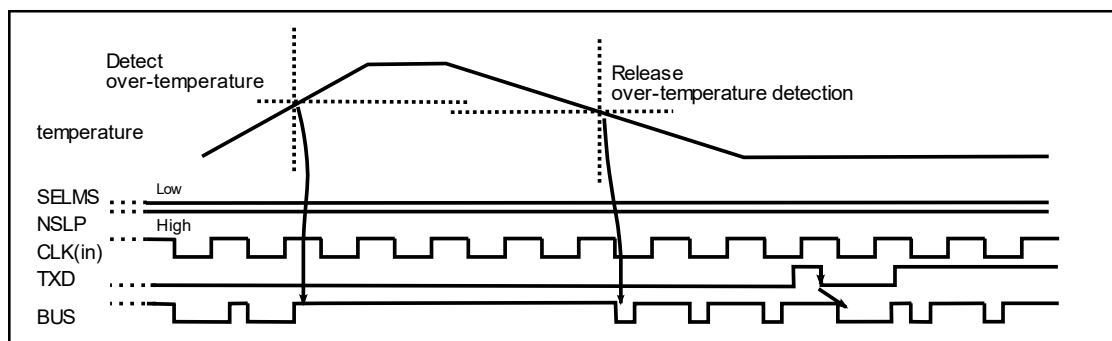
5.4.3   *Low-voltage Reset*

The low-voltage reset state detects the low voltage of the BAT pin. This device has an integrated power-on reset and low-voltage detection at the supply BAT.

If the supply voltage, V_{BAT}, is dropping below the power-on reset level (that is, $V_{BAT}<V_{POR\_L}$), then change the LowPowerReset mode. In the LowPowerReset mode, the output stage is disabled and communication to the CXPI BUS is not possible.

If the power supply reaches a higher level than the low-voltage reset level, $V_{BAT}> V_{POR\_H}$, then change the Standby mode (the NSLP pin is High) or Sleep mode (the NSLP pin is Low).

After releasing LowPowerRest mode, enable the Power-up sequence.

Table 5-12. Input Signal Change after Recovery from Low Voltage Reset

Master/Slave	Pin	Toggle of Input Signal
Master	TXD	Required
Slave	TXD	Required

Table 5-13. State Under Low Voltage Reset

Master/Slave	Pin	Description
Master	SELMS	Reset
	TXD	Reset
	NSLP	Reset
	CLK	Reset(High impedance)
	RXD	High impedance
	BUS	High impedance
Slave	SELMS	Reset
	TXD	Reset
	NSLP	Reset
	CLK	Reset(High impedance)
	RXD	High impedance
	BUS	High impedance

Figure 5-11. Low-Voltage Detection
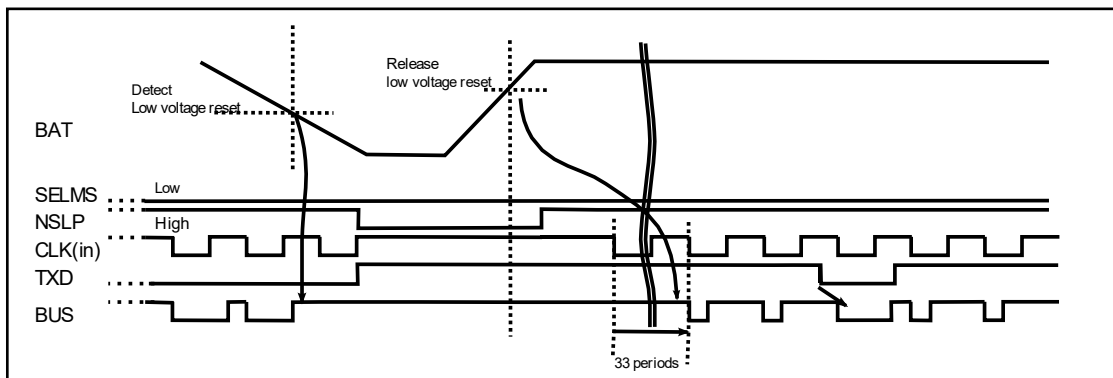
After releasing the low-voltage reset mode, the logical value high is output to the BUS pin after a clock input of 33 periods. The TXD data is valid from the falling edge on the TXD pin.

5.4.4 Overcurrent Protection

The current in the transmitter output stage is limited to protect the transmitter against short-circuit to BAT or GND pins.

Table 5-14. Overcurrent Protection

Master/Slave	Pin	Description
Master	TXD	Normal function
	NSLP	Normal function
	CLK	Normal function
	RXD	Normal function
	BUS	Output current limited by IBUS_LIM
Slave	TXD	Normal function
	NSLP	Normal function
	CLK	Normal function
	RXD	Normal function
	BUS	Output current limited by IBUS_LIM

5.4.5 Secondary Clock Master

The node that detects the wakeup event transmits the wakeup pulse on to the CXPI BUS. If the primary clock master cannot transmit the clock to the CXPI BUS due to failure, the wakeup pulse is retransmitted. If the clock is not transmitted to the CXPI BUS, each node detects the CXPI BUS error.

The secondary clock master may transmit the clock to the CXPI BUS instead of the primary clock master if it detects that the clock does not exist, and confirms that the clock does not exist on the CXPI BUS for the period during which it transitions from the Sleep mode

■Operation sequence from master to slave

The TXD input pin is set High and the CLK pin is high-impedance. A Low setting on the NSLP pin initiates a transition to the Sleep mode. After the RXD pin is confirmed to High state, the SELMS pin goes to High state. Table 5-15 shows the pin states just before the SELMS pin input signal change.

Table 5-15. Pin State Table (from Master to Slave)

Pin	Pin State	Description
TXD	High	No data transmitting
CLK	High impedance	High level with external pull-up resistor.
NSLP	Low	Sleep mode
SELMS	Low to High	-
RXD	High	No data receiving
BUS	High	No wakeup signal receiving preferred

Figure 5-12. Application Example Secondary Clock Master

S6BT112A AS SLAVE (SECONDARY CLOCK MASTER)
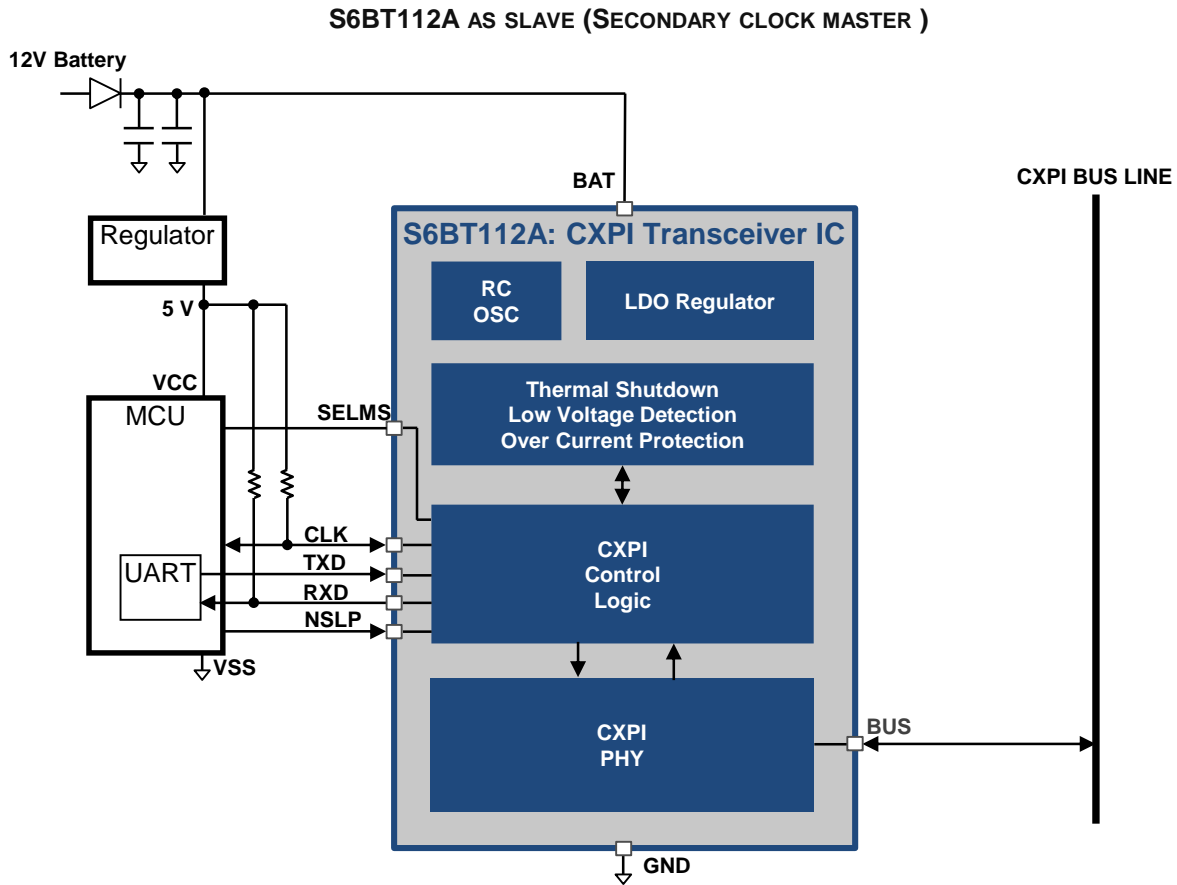
Figure 5-13. Transition Sequence from Master to Slave
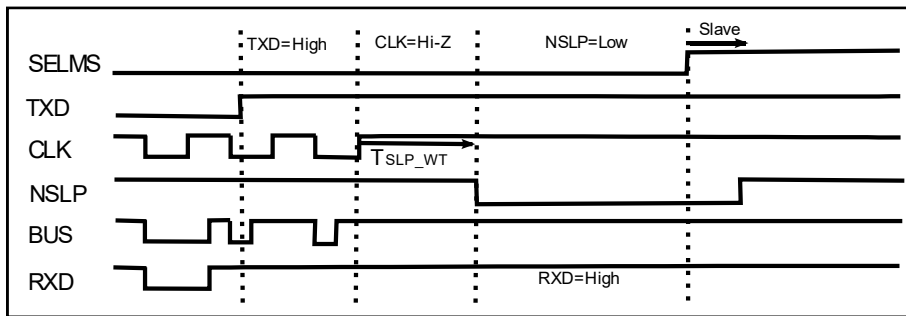
■Operation sequence from slave to master

The TXD pin inputs high and the slave node transitions to the Sleep mode after the CLK pin was confirmed to High, and the SELMS pin goes to Low.

Table 5-16. Pin State Table (from Slave to Master)

Pin	Pin State	Description
TXD	High	No data transmitting
CLK	High impedance	No wakeup signal receiving
NSLP	Low	Sleep mode
SELMS	High to Low	-
RXD	High	-
BUS	High	No wakeup signal receiving preferred

Note: The pin states just before the SELMS input signal change.

Figure 5-14. Transition Sequence from Slave to Master
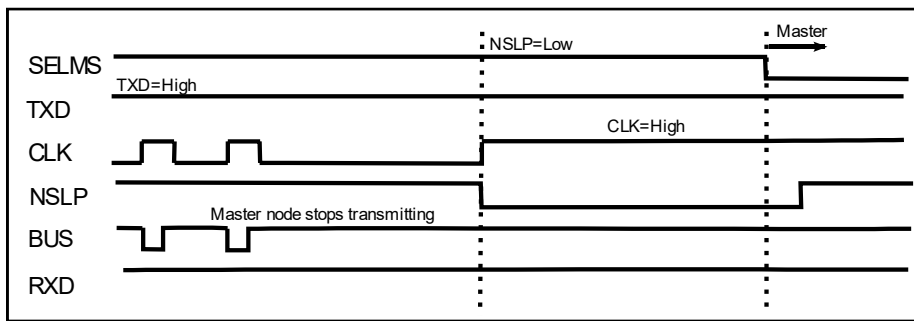
5.4.6 Arbitration

Transceivers arbitrate bit-by-bit. Arbitration in bytes is done in the MCU.

In the Normal mode, each node always compares the received bit from the CXPI BUS with the transmitted bit to the CXPI BUS. When the value of the bit is corresponding, the node may continuously transmit to the CXPI BUS. When the value of the bit is not corresponding, the loss of arbitration is detected, and the transmission of the bit after that shall discontinue. If the transmitting node detects the arbitration loss, it behaves as the receiving node. The data of each bit transmitted on the CXPI BUS performs arbitration from the start by the bit. Moreover, arbitration is targeted at the entire field of the frame. When two or more nodes begin transmitting at the same time, by arbitration only the node that transmits the highest priority frame can complete the transmission.

The MCU compares between the transmitted data (TXD) and received data (RXD). If the data difference is detected, MCU has to stop data transmission until finding IFS.

5.4.7 TXD Toggle

If the TXD pin is short to ground or open, the BUS pin output is not fixed Low (logic value). Therefore, it does not interfere with the communication of the other device.

An initial TXD dominant check prevents the bus line being driven to a permanent dominant state (blocking all network communications) if the TXD pin is forced permanently Low by a hardware and/or software application failure. The TXD input level is checked after a transition to the Normal mode.

If the TXD pin is Low, the transmit path remains disabled and is only enabled when the TXD pin goes High.

A TXD toggle is required in the following cases.

☐ Data transmission after recovery from low-voltage reset.
☐ Data transmission after recovery from thermal shutdown.
☐ First TXD data transmission in the Normal mode.
☐ First wake-up pulse transmission in sleep mode.

■Short-circuit from the TXD pin to ground.(failure detect)

In the event of a short-circuit to ground or an open-wire on the TXD pin, the BUS pin output remains High (logical value '1') by this toggle function. In this case, by comparing the sent data to the TXD pin and received data from the RXD pin of the transceiver IC, the MCU can detect the permanent Low on the TXD pin by the data difference. In this case too, the receiver is active.
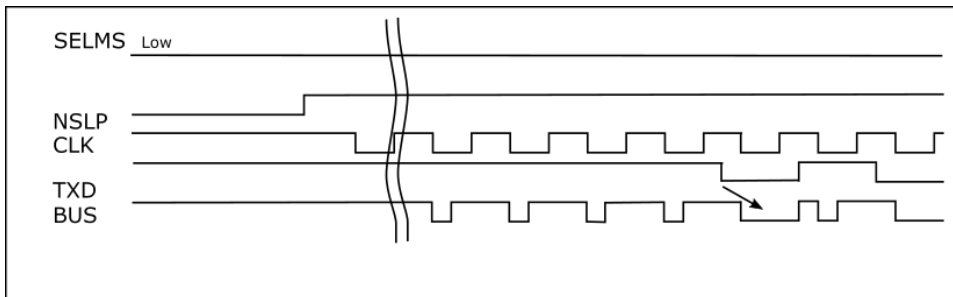
Figure 5-15. Normal Transmission Sequence of Master

Figure 5-16. TXD Toggle of Master after Transition to Normal mode
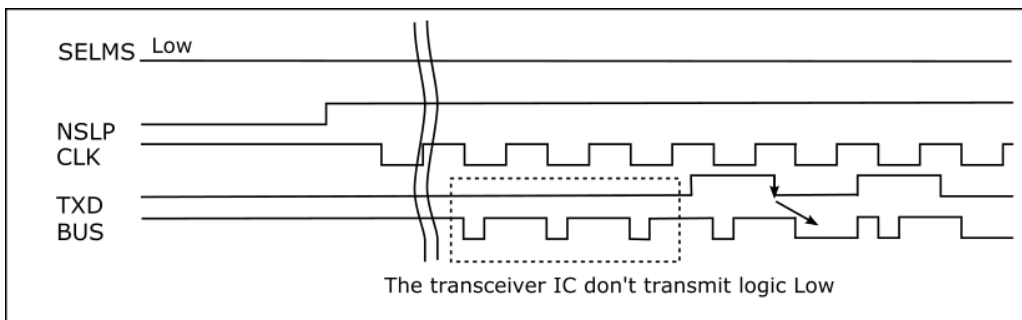
Figure 5-17. Slave TXD Toggle after Recovery from Low voltage State
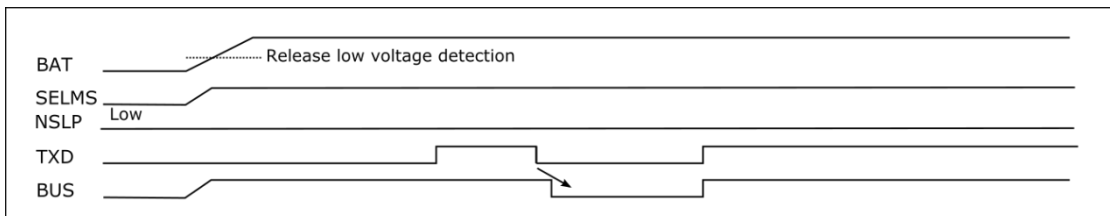
6. Absolute Maximum Ratings

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Parameters	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V_{BAT}	BAT pin	-0.3	40	V
Input voltage	V_{NSLP}	NSLP pin	-0.3	6.9	V
	V_{SELMS}	SELMS pin	-0.3	18	V
	V_{CLK}	CLK pin	-0.3	6.9	V
	V_{TXD}	TXD pin	-0.3	6.9	V
Output voltage	V_{RXD}	RXD pin	-0.3	6.9	V
	V_{CLK}	CLK pin	-0.3	6.9	V
BUS pin voltage	V_{BUS}	BUS pin	-40	40	V
BUS pin ESD (1.5 kΩ, 100 pF)	V_{ESDBUS}	BUS pin	-8	8	kV
BAT pin ESD (1.5 kΩ, 100 pF)	V_{ESDBAT}	BAT pin	-8	8	kV
ESD (1.5 kΩ, 100 pF)	V_{ESD}	NSLP pin SELMS pin CLK pin TXD pin RXD pin	-2	2	kV
Storage temperature	T_{STG}	-	-55	150	°C
Maximum junction temperature	T_{JMAX}	-	-40	150	°C

7. Recommended Operating Conditions

Table 7-1. Recommended Condition

Parameters	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{BAT}	BAT pin [1]	5.3	-	18	V
Operating ambient temperature	T_A	-	−40	+25	+125	°C
BUS pin pull-up resistance	R_{MASTER}	BUS pin (Master node : SELMS=0V)	900	1000	1100	Ω
RXD pin pull-up resistance	R_{RXD}	RXD pin	2.4	10	-	kΩ
CLK pin pull-up resistance	R_{CLK}	CLK pin (SELMS=5V)	2.4	10	-	kΩ

Note:

[1]: (18 V < V_{BAT} ≤ 27 V) less than 2 minutes.

WARNING:

1. *The recommended operating conditions are requiredir to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*

2. *Any use of semiconductor devices will be under their recommended operating condition.*

3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*

4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

8. Electrical Characteristics

Table 8-1. DC Characteristics

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C; All voltages are referenced to Pin 8 (GND); Positive currents flow into the IC; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Power supply current	I_{BAT}	BAT	Normal mode TXD=5 V CLK=20 kHz, Duty 50%	-	1.4	2.9	mA
			Normal mode TXD=0 V CLK=20 kHz, Duty 50%	-	2.0	4.0	mA
			Sleep mode V_{BAT} =12 V TXD=5 V SELMS=5 V BUS= V_{BAT} T_A=25 °C	-	6	10	µA
			Sleep mode V_{BAT} =12 V TXD=5 V SELMS=0 V BUS= V_{BAT} T_A=25 °C	-	16	-	µA
			Sleep mode V_{BAT} =12 V TXD=5 V SELMS=5 V BUS= V_{BAT}	-	-	50	µA
			Sleep mode V_{BAT} =12 V TXD=5 V SELMS=0 V BUS= V_{BAT}	-	-	60	µA
BUS pin pull-up resistance	R_{BUSpu}	BUS	-	20	30	47	kΩ
BUS short circuit current	I_{BUS_LIM}	BUS	V_{BUS}=18 V	40	-	200	mA

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
BUS input leak current (HIGH)	$I_{BUS\_PAS\_rec}$	BUS	BUS=18 V V_{BAT} =5.3 V TXD=5 V T_A=25 °C	-	-	20	μA
BUS input leak current (LOW)	$I_{BUS\_PAS\_dom}$	BUS	BUS=0 V V_{BAT} =12 V TXD=5 V	-1	-	-	mA
loss of ground BUS leak current	$I_{BUS\_NO\_GND}$	BUS	V_{BAT} =GND=18 V BUS=0 V	-1	-	1	mA
loss of battery BUS leak current	$I_{BUS\_NO\_BAT}$	BUS	V_{BAT} =0 V BUS=18 V T_A=25 °C	-	-	30	μA
BUS drop voltage	V_{BUSDR}	BUS	V_{BAT} =13.5 V IBUSsource=-100 μA	2.4	-	5.7	V
BUS low level output voltage	V_{O_dom}	BUS	TXD=0 V V_{BAT} =7 V BUS pull-up resistance= 500 Ω	-	-	1.4	V
	V_{O_dom}	BUS	TXD=0 V V_{BAT} =18 V BUS pull-up resistance= 500 Ω	-	-	2	V
Receiver low level threshold voltage	V_{BUSdom}	BUS	V_{BAT} =12V, T_A=25 °C	-	-	0.423 V_{BAT}	V
Receiver high level threshold voltage	V_{BUSrec}	BUS	V_{BAT} =12V, T_A=25 °C	0.556 V_{BAT}	-	-	V
Receiver hysteresis voltage	V_{HYS}	BUS	V_{BAT} =12V, T_A=25°C	-	-	0.133 V_{BAT}	V
Low level power-on reset threshold voltage	V_{POR_L}	BAT	-	3.1	3.8	4.7	V
High level power-on reset threshold voltage	V_{POR_H}	BAT	-	3.3	4.1	4.9	V
power-on reset hysteresis voltage	V_{POR_HYS}	BAT	-	0.2	0.3	0.5	V
Temperature shutdown threshold	T_{SD_H}	-	[2]	156	165	174	°C
Temperature shutdown release threshold	T_{SD_L}	-	[2]	151	159	168	°C

Notes:

[1]: (18 V < V_{BAT} ≤ 27 V) less than 2 minutes.

[2]: Guaranteed by design

Table 8-2. DC Characteristics CLK Pin

(If SELMS = 5 V, this pin operates as Open Drain Output Pin. If SELMS = 0 V, this pin operates as an input pin)

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C; all voltages are referenced to Pin 8 (GND). Positive current flow into the IC; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH_CLK}	CLK	SELMS = 0 V	2	-	6	V
Low level input voltage	V_{IL_CLK}	CLK	SELMS = 0 V	-0.3	-	0.8	V
Hysteresis range of input voltage	V_{HYS_CLK}	CLK	SELMS = 0 V	0.03	-	0.5	V
Low level output voltage	V_{OL_CLK}	CLK	I_{CLK} = 2.2 mA SELMS = 5 V	-	-	0.6	V
Low level current	I_{OL_CLK}	CLK	SELMS = 5 V	1.3	3	-	mA
High level leak current	I_{ILH_CLK}	CLK	SELMS = 5 V	-3	-	3	µA
Low level leak current	I_{ILL_CLK}	CLK	SELMS = 5 V	-3	-	3	µA

Note:

[1]: (18 V < V_{BAT} ≤ 27 V) less than 2 minutes.

Table 8-3. DC Characteristics NSLP Pin

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C; all voltages are referenced to Pin 8 (GND). Positive current flow into the IC; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH_NSLP}	NSLP	-	2	-	6	V
Low level input voltage	V_{IL_NSLP}	NSLP	-	-0.3	-	0.8	V
Hysteresis range of input voltage	V_{HYS_NSLP}	NSLP	-	0.03	-	0.5	V
Internal pull-down resistance	R_{PD_NSLP}	NSLP	NSLP = 5 V	100	250	650	kΩ
Low level leak current	I_{ILL_NSLP}	NSLP	NSLP = 0 V	-3	-	3	µA

Note:

[1]: (18 V < V_{BAT} ≤ 27 V) less than 2 minutes

Table 8-4. TXD Pin

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C; all voltages are referenced to Pin 8 (GND). Positive current flow into the IC; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH_TXD}	TXD	-	2	-	6	V
Low level input voltage	V_{IL_TXD}	TXD	-	-0.3	-	0.8	V
Hysteresis range of input voltage	V_{HYS_TXD}	TXD	-	0.03	-	0.5	V
Internal pull-up resistance	R_{PU_TXD}	TXD	TXD = 0 V	50	125	325	kΩ
High level leak current	I_{ILH_TXD}	TXD	TXD = 5 V	-3	-	3	µA

Note:

 [1]: (18V < V_{BAT} ≤ 27V) less than 2 minutes

Table 8-5. SELMS Pin

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C; all voltages are referenced to Pin 8 (GND). Positive current flow into the IC; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH_SELMS}	SELMS	-	2	-	6	V
Low level input voltage	V_{IL_SELMS}	SELMS	-	-0.3	-	0.8	V
Hysteresis range of input voltage	V_{HYS_SELMS}	SELMS	-	0.03	-	0.5	V
Internal pull-up resistance	R_{PU_SELMS}	SELMS	SELMS = 0 V	200	500	1300	kΩ
High level leak current	I_{ILH_SELMS}	SELMS	SELMS = 5 V	-3	-	3	µA

Note:

 [1]: (18 V < V_{BAT} ≤ 27 V) less than 2 minutes.

Table 8-6. RXD Pin (Open Drain Output)

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C; all voltages are referenced to Pin 8 (GND). Positive current flow into the IC; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Low level output voltage	V_{OL_RXD}	RXD	I_{RXD} = 2.2 mA	-	-	0.6	V
Low level current	I_{OL_RXD}	RXD	RXD = 0.4 V	1.3	3	-	mA
High level leak current	I_{OLH_RXD}	RXD	RXD = 5 V	-3	-	3	µA
Low level leak current	I_{OLL_RXD}	RXD	RXD = 0 V	-3	-	3	µA

Note:

[1]: (18 V < V_{BAT} ≦ 27 V) less than 2 minutes.

Table 8-7. AC Characteristics

V_{BAT} = 5.3 V~27 V[1], T_A = -40~125 °C BUS Load 1 kΩ /1 nF; unless otherwise specified.

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Bitrate	T_{BUAD}	BUS	V_{TH}(bus) [3] = 0.5V_{BAT}	2.4	-	20	kbps
Mode transition time (Sleep to Normal or Normal to Sleep.)	T_{MODE_CHG}	NSLP	V_{TH}(5v)[4] = 50%	-	-	1	ms
NSLP wait time	T_{SLP_WT}	CLK NSLP	V_{TH}(5 V) [4] = 50%	100	-	-	µs
Minimum sleep time	T_{SLP_MN}	NSLP	-	1	-	-	ms
Driver boot time under sleep mode. [2]	T_{TXD_BT}	TXD	VBAT = 7V~27V NLSP = 0 V SELMS = 5 V V_{TH}(5v)[4]=50% V_{TH}(bus)[3]=0.3V_{BAT}	-	-	66	µs
CLK transmission delay time	T_{CLK_PD}	CLK	NLSP = 5 V SELMS = 0 V CLK=input clock TXD=5 V V_{TH}(5v)[4]=50% V_{TH}(bus)[3]=0.3V_{BAT}	-	-	0.9	Tbit[5]

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Time of Low level of logic value '1'	$T_{tx\_1\_lo\_rec}$	BUS	NLSP = 5 V SELMS = 0 V CLK=input clock TXD=5 V $V_{TH}(bus)$[3] = 0.7V_{BAT}	-	-	0.39Tbit +0.6т	-
Time of Low level of logic value '1'	$T_{tx\_1\_lo\_dom}$	BUS	NLSP = 5 V SELMS = 0 V CLK=input clock TXD=5 V $V_{TH}(bus)$[3] = 0.3 V_{BAT}	0.11	-	-	Tbit
Time of Low level of logic value '0'	$T_{tx\_0\_lo\_rec}$	BUS	NLSP = 5 V TXD = 0 V $V_{TH}(bus)$ [3] = 0.7 V_{BAT}	$T_{tx\_1\_lo\_rec}$ +0.06Tbit	-	-	-
Time of Low level of logic value '0'	$T_{tx\_0\_lo\_dom}$	BUS	NLSP = 5 V TXD=0 V $V_{TH}(bus)$ [3] = 0.3 V_{BAT}	$T_{tx\_1\_lo\_dom}$ +0.06Tbit	-	-	-
High level time at receiving node.	$T_{tx\_0\_hi}$	BUS	NLSP = 5 V TXD = 0 V $V_{TH}(bus)$[3] = 0.556 V_{BAT}	0.06	-	-	Tbit
Receiver delay time	T_{RXD_PD}	RXD	NSLP = 5 V $V_{TH}(bus)$[3] = VBUSdom	-	-	1.0	Tbit
Delay time of transmission if logic value '0'.	T_{TXD_PD}	TXD	NSLP = 5 V $V_{TH}(bus)$ [3]=0.3 V_{BAT}	-	-	2.0	Tbit
Input clock duty	T_{ICLK_DY}	CLK	SELMS = 0 V $V_{TH}(5 V)$[4] = 50%	30	-	70	%
Output clock duty[6]	T_{OCLK_DY}	CLK	SELMS = 5 V $V_{TH}(5 V)$[4] = 50%	14	-	50	%
Wakeup pulse filter constant(Master)	$T_{rx\_wakeup\_master}$	BUS	NSLP = 0 V SELMS = 0 V $V_{TH}(bus)$ [3]=42.3%	30	-	150	µs
Wakeup pulse filter constant(Slave)	$T_{rx\_wakeup\_slave}$	BUS	NSLP = 0 V SELMS = 5 V $V_{TH}(bus)$ [3] = 42.3%	0.5	-	5	µs

Parameters	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Time of bus slope from minimum	$T_{tx\_1\_dom\_m}$	BUS	NSLP = 5 V SELMS = 0 V V_{BAT} = 7V V_{TH}(bus) [3] = 0.3 V_{BAT}	-	-	0.16	Tbit
Recessive level of logical value '0'.	V_rec_0	BUS	NSLP = 5 V	0.93	-	-	V_rec_1

Notes:

[1]: (18 V < V_{BAT} ≤ 27 V) less than 2 minutes
      RXD pin load: 20 pF

[2]: CXPI BUS load (Figure 8-11) : 10 nF/500 Ω

[3]: V_{TH}(bus) : threshold of BUS pin

[4]: V_{TH}(5v) : threshold of NSLP,CLK,TXD,SELMS,RXD pins.

[5]: Tbit stands for 1bit time.(Figure 8-1)

[6]: logic '0/1' threshold clock

Figure 8-1. Definition of Tbit
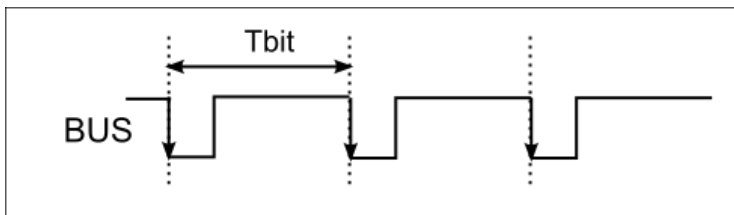
Figure 8-2. Mode Transition Time
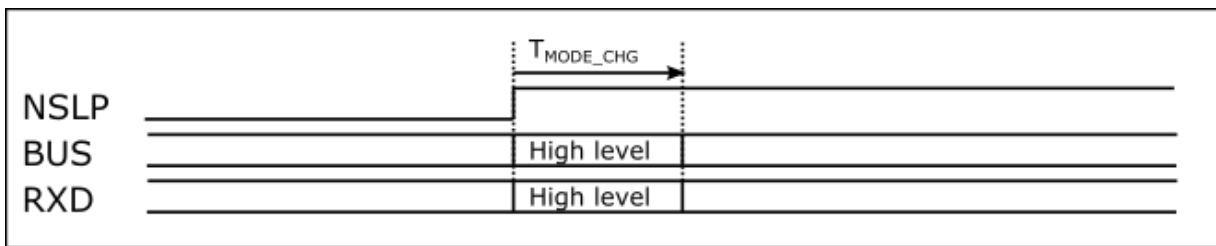
Figure 8-3. NSLP Wait Time
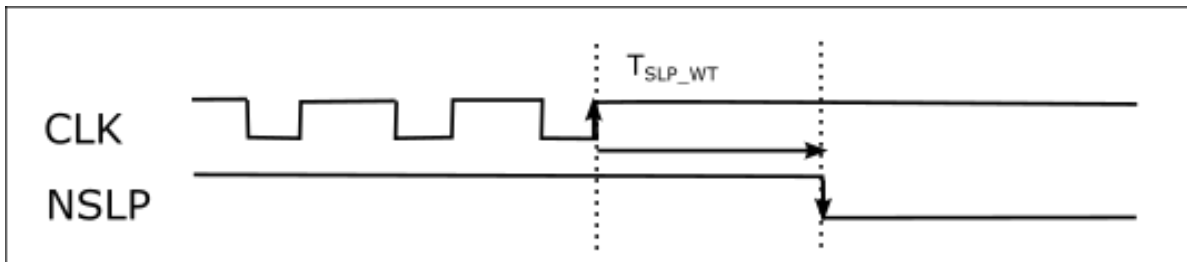
Figure 8-4. Minimum Sleep Time
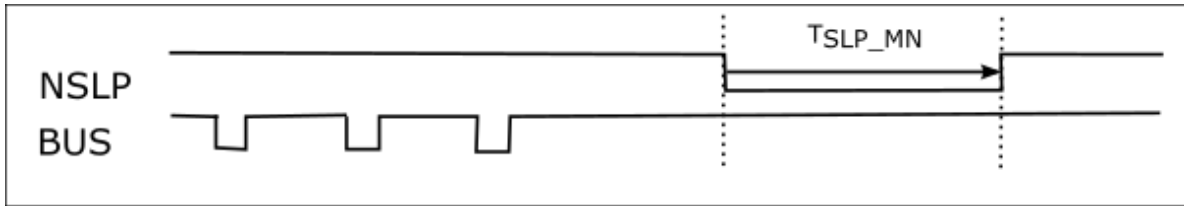
Figure 8-5. Driver Boot Time Under Sleep Mode
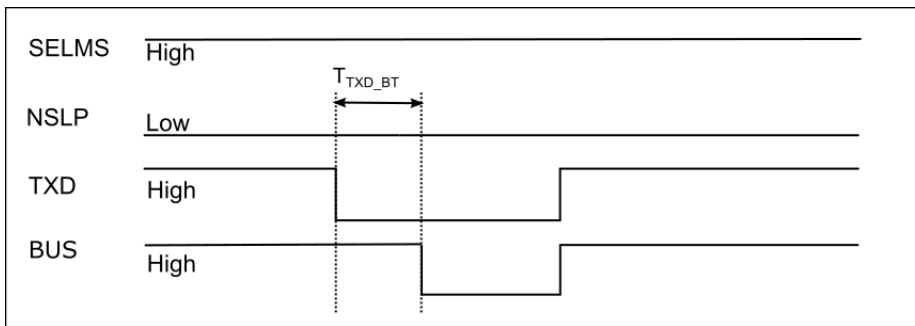
Figure 8-6. CLK Transmission Delay Time
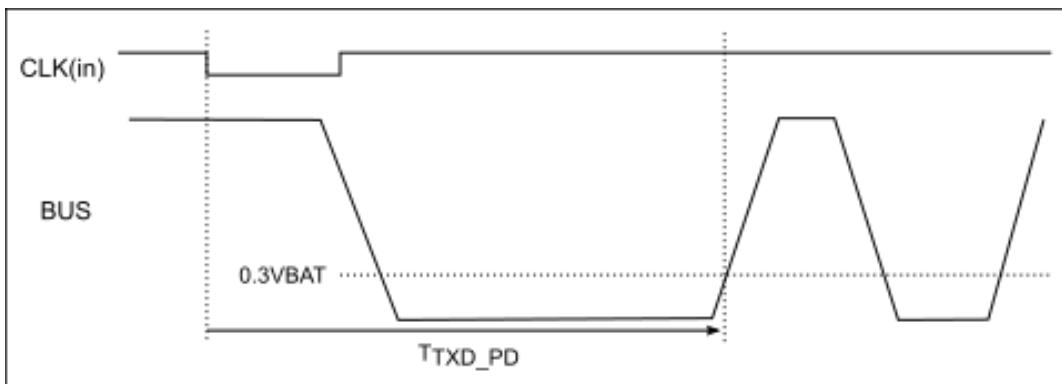
Figure 8-7. Logic Low and High CXPI BUS Waveform
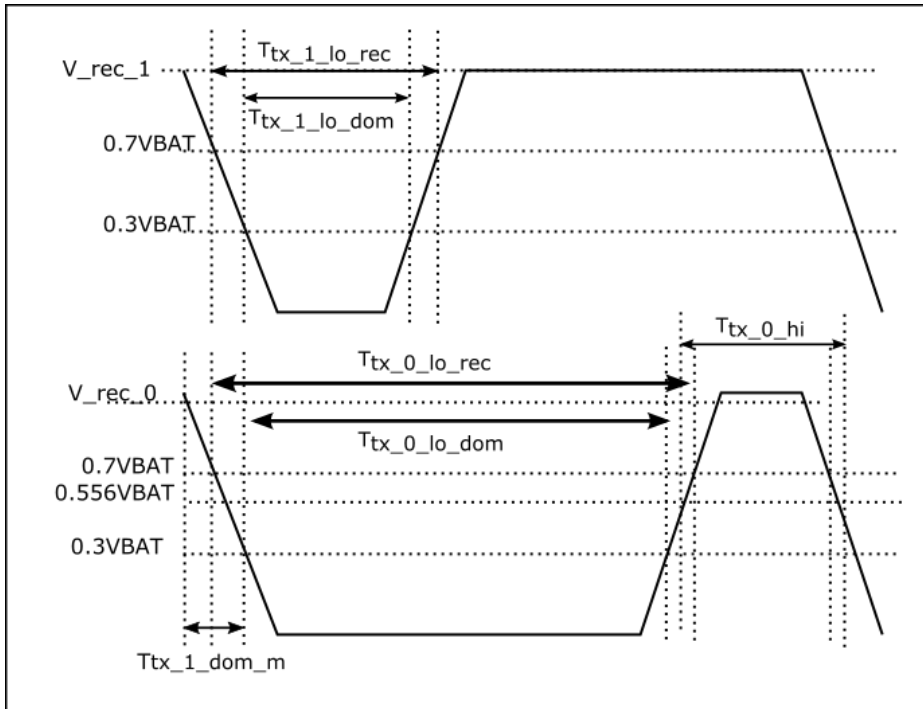
Figure 8-8. Receiver Delay Time
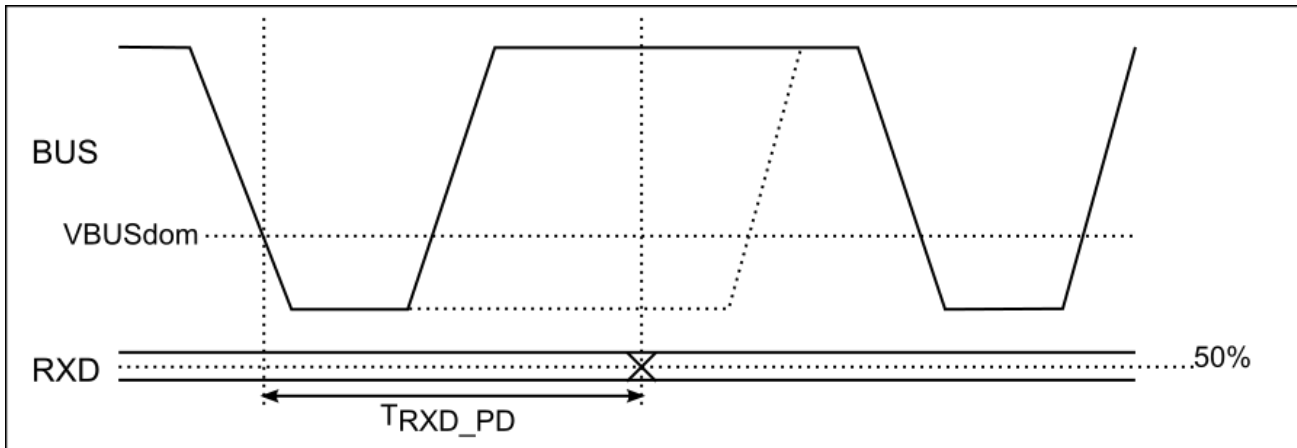
Figure 8-9. Logic Low Transmission Delay Time
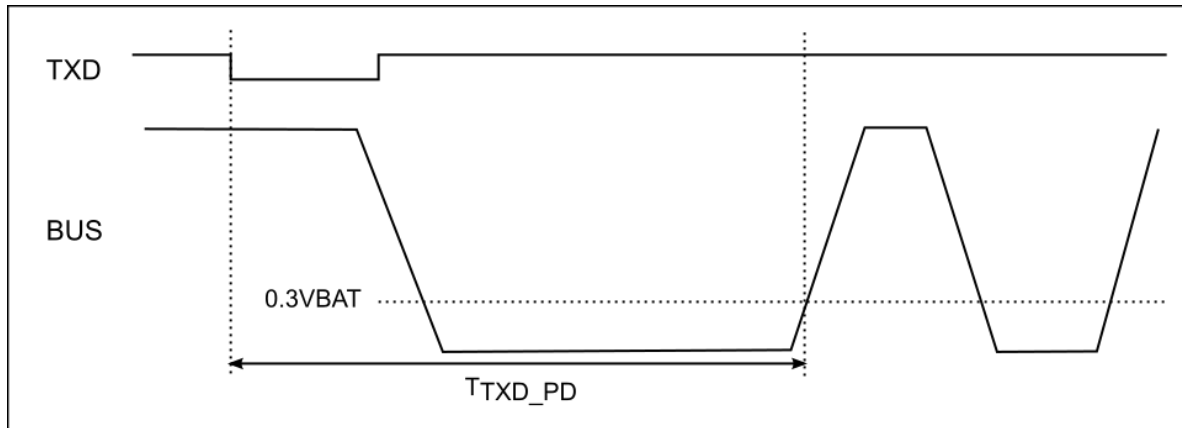
Figure 8-10. Wakeup Pulse Waveform
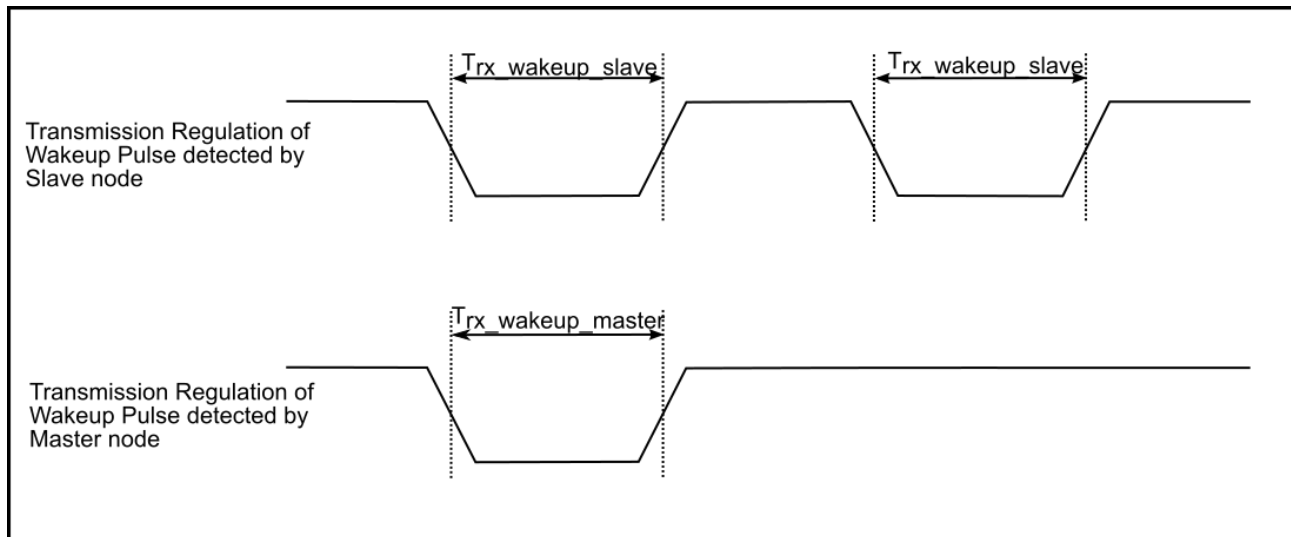
Figure 8-11. CXPI BUS Load Connection
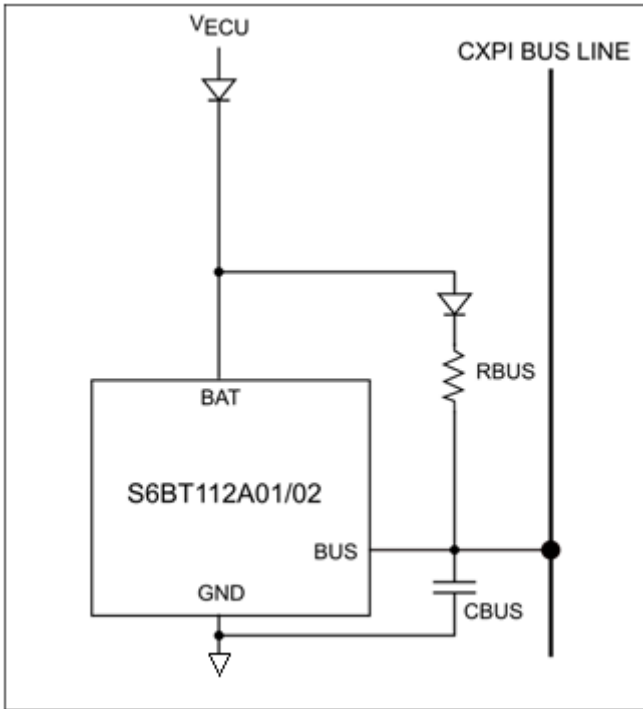
9. Ordering Information

Part Number	Package
S6BT112A01SSBB002	8-pin 150-mil SOIC Tape and Reel (SOA008)
S6BT112A02SSBB002	8-pin 150-mil SOIC Tape and Reel (SOA008)

10. Package Dimensions

Package Type	Package Code
SOP 8	SOA 008
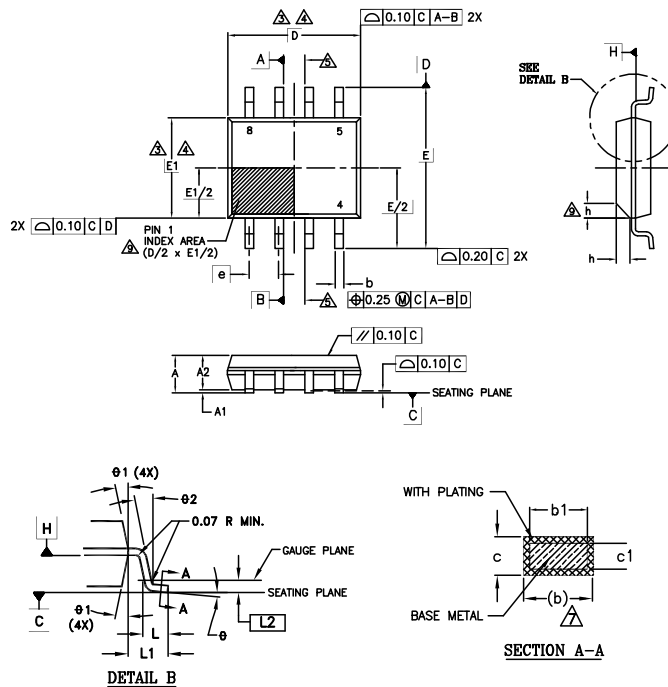
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.32	-	-
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	0.89
L1	1.04 REF		
L2	0.25 BSC		
N	8		
h	0.25	-	0.50
θ	0°	-	8°
θ 1	5°	-	15°
θ 2	0° REF		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.

3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.

4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

5. DATUMS A AND B TO BE DETERMINED AT DATUM H.

6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.

7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.

8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.

9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.

10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

002-18754 **

Document History

Document Title: S6BT112A01/S6BT112A02 ASSP CXPI Transceiver IC for Automotive Network

Document Number: 002-10203

Revision	ECN	Submission Date	Description of Change
**	5046456	12/11/2015	Initial release New Spec.
*A	5208207	04/06/2016	Revised the sentence style of the cover page Changed all section 5 for easy to understand. Changed figure of application. Changed Figure 4-1 and Figure 5-1. Removed "Driver recovery time when over-temperature detection is released."
*B	5528948	11/24/2016	Changed figure of application. Changed Figure 4-1 Block Diagram Changed Figure 5-12 Application example Secondary clock master Added the conditions of V_{BUSdom}/V_{BUSrec}/ V_{HYS}/$T_{tx\_1\_dom\_m}$. Removed the prameter of Receiver center level voltage (V_{BUS_CNT}). Changed Figure 8-11 CXPI BUS Load Connection Changed Ordering Information. Changed Package Dimensions.
*C	5547736	12/09/2016	Updated Introduction. Updated Note [3] (Page 8). Updated 5.2 Master Node. Updated 5.2.2 Sleep Mode.
*D	5757034	06/20/2017	Changed figure of 1. Applications Changed Figure 5-12 Application example Secondary Clock Master
*E	6397891	12/04/2018	Changed SOA 008 figure in Package Demensions
*F	6748976	12/23/2019	Added recommendation when stopping clock (Page 9). Corrected Figure 5-2, 5-3, 5-5, 5-6, 5-7, 5-10, 5-11, 5-13, 5-14 Changed Table 5-5 to Table 5-9, 20 kbps to 19.2 kbps. Added explanation (Page 10, 13). Added max. value for IBAT at Sleep mode, SELMS=5V, and TA=25 °C (Page 23). Changed max. value of T_{TXD_BT} to 66 (Page 27). Changed max. value of $T_{tx\_1\_lo\_rec}$ to 0.39Tbit+0.6т (Page 28). Changed max. value of T_{RXD_PD} to 1.0 (Page 28). Changed max. value of T_{TXD_PD} to 2.0 (Page 28).

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