# SLG59M1804V

## Dual 4.5A GreenFET 3 Load Switch

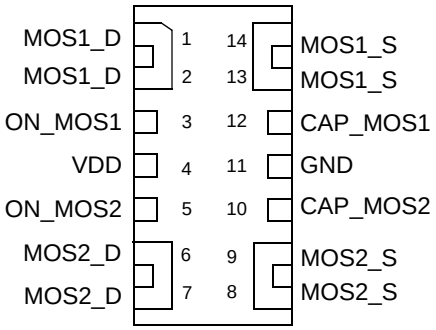
### General Description

The SLG59M1804V is designed for load switching application. The part comes with two 4.5 A rated MOSFETs switched on by two ON control pins. Each MOSFETs turn on time is independently adjusted by an external capacitor.

### Features

- UL2367 Certified - File Number E497808
- Two 4.5A independent MOSFETs
- Two Integrated VGS Charge Pumps
- Two internal discharges per channel for gate and source
- Independent Ramp Control
- Protected by thermal shutdown with current limit
- Pb-Free / RoHS Compliant
- Halogen-Free
- STDFN 14L, 1 x 3 x 0.55 mm

### Pin Configuration

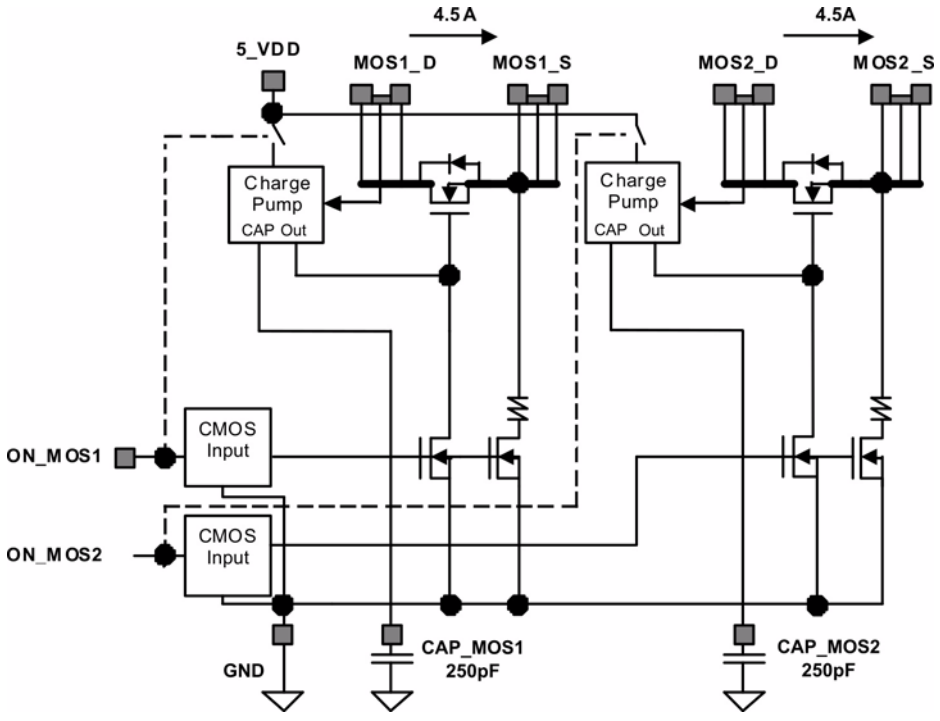



**14-pin STDFN**
(Top View)

### Applications

- Ideal for switching ON and OFF S0 +5.0 and 3.3V power rails with associated support circuitry discharges.
- Ideal for switching ON and OFF power rails 5V or less.
- Can use either channel up to 4.5A with combined maximum current of 8.5A
- Maximum load capacitance of 1000 µF for each Channel Source terminal.

### Block Diagram




**Do not probe CAP_MOS1 (PIN 12) or CAP_MOS2 (PIN 10) with low impedance probe.**

## Pin Description

| Pin # | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | MOS1_D | MOSFET | Drain of MOSFET1 |
| 2 | MOS1_D | MOSFET | Drain of MOSFET1 (fused with pin 1) |
| 3 | ON_MOS1 | Input | Turns on MOS1 (4 MΩ pull down resistor) |
| 4 | VDD | VDD | +5VDD Power |
| 5 | ON_MOS2 | Input | Turns on MOS2 (4 MΩ pull down resistor) |
| 6 | MOS2_D | MOSFET | Drain of MOSFET2 |
| 7 | MOS2_D | MOSFET | Drain of MOSFET2 (fused with pin 6) |
| 8 | MOS2_S | MOSFET | Source of MOSFET2 (fused with pin 9) |
| 9 | MOS2_S | MOSFET | Source of MOSFET2 |
| 10 | CAP_MOS2 | Input | Sets ramp and turn on time for MOSFET2 |
| 11 | GND | GND | Ground |
| 12 | CAP_MOS1 | Input | Sets ramp and turn on time for MOSFET1 |
| 13 | MOS1_S | MOSFET | Source of MOSFET1 (fused with pin 14) |
| 14 | MOS1_S | MOSFET | Source of MOSFET1 |

## Ordering Information

| Part Number | Type | Production Flow |
|---|---|---|
| SLG59M1804V | STDFN 14L | Industrial, -40 °C to 85 °C |
| SLG59M1804VTR | STDFN 14L (Tape and Reel) | Industrial, -40 °C to 85 °C |

## Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_D$ | Power Supply | | -- | -- | 6 | V |
| $T_S$ | Storage Temperature | | -65 | -- | 150 | °C |
| $ESD_{HBM}$ | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| $W_{DIS}$ | Package Power Dissipation | | -- | -- | 1.2 | W |
| $IDS_{MAX}$ | Max Operating Current | | | | 4.5 | A |
| MOSFET $IDS_{PK}$ | Peak Current from Drain to Source | Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle | -- | -- | 8 | A |

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

$T_A$ = -40 °C to 85 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 2.5 | -- | 5.0 | V |
| $I_{DD}$ | Power Supply Current when OFF | | -- | 0.1 | 1 | µA |
| | Power Supply Current ON_MOS_1 & ON_MOS_2 (Steady State) | | -- | 50 | 75 | µA |
| $RDS_{ON}$ | ON Resistance | $T_A$ 25°C MOSFET1 @100 mA | -- | 14.5 | 18 | mΩ |
| | | $T_A$ 70°C MOSFET1 @100 mA | -- | 17 | 22 | mΩ |
| | | $T_A$ 85°C MOSFET1 @100 mA | -- | 18 | 23 | mΩ |
| | | $T_A$ 85°C MOSFET1 @ 4.5 A | -- | 19.3 | 25.1 | mΩ |
| | | $T_A$ 25°C MOSFET2 @100 mA | -- | 14.5 | 18 | mΩ |
| | | $T_A$ 70°C MOSFET2 @100 mA | -- | 17 | 22 | mΩ |
| | | $T_A$ 85°C MOSFET2 @100 mA | -- | 18 | 23 | mΩ |
| | | $T_A$ 85°C MOSFET2 @ 4.5 A | -- | 19.3 | 25.1 | mΩ |
| MOSFET IDS | Current from Drain to Source for each MOSFET | Continuous | -- | -- | 4.5 | A |
| $V_D$ | Drain Voltage | | 0.9 | -- | $V_{DD}$ | V |
| $T_{ON\_Delay}$ | ON pin Delay Time | 50% ON to Ramp Begin | 0 | 300 | 500 | µs |
| $T_{Total\_ON}$ | Total Turn On Time | 50% ON to 90% $V_S$ | Configurable [1] | | | ms |
| | | Example: CAP = 4 nF, $V_{DD}$ = $V_D$ = 5 V, Source_Cap = 10 µF, $R_L$ = 20 Ω | -- | 2.0 | -- | ms |
| $T_{SLEWRATE}$ | Slew Rate | 10% $V_S$ to 90% $V_S$ | Configurable [1] | | | V/ms |
| | | Example: CAP = 4 nF, $V_{DD}$ = $V_D$ = 5 V, Source_Cap = 10 µF, $R_L$ = 20 Ω | -- | 3.0 | -- | V/ms |
| $CAP_{SOURCE}$ | Source Cap | Source to GND | -- | -- | 1000 | µF |
| $R_{DIS}$ | Discharge Resistance | | 100 | 150 | 300 | Ω |
| $ON\_V_{IH}$ | High Input Voltage on ON pin | | 0.85 | -- | $V_{DD}$ | V |
| $ON\_V_{IL}$ | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| $I_{LIMIT}$ | Active Current Limit | MOSFET will automatically limit current when $V_S$ > 250 mV | -- | 6.0 | 8 | A |
| $THERM_{ON}$ | Thermal shutoff turn-on temperature | | -- | 125 | -- | °C |

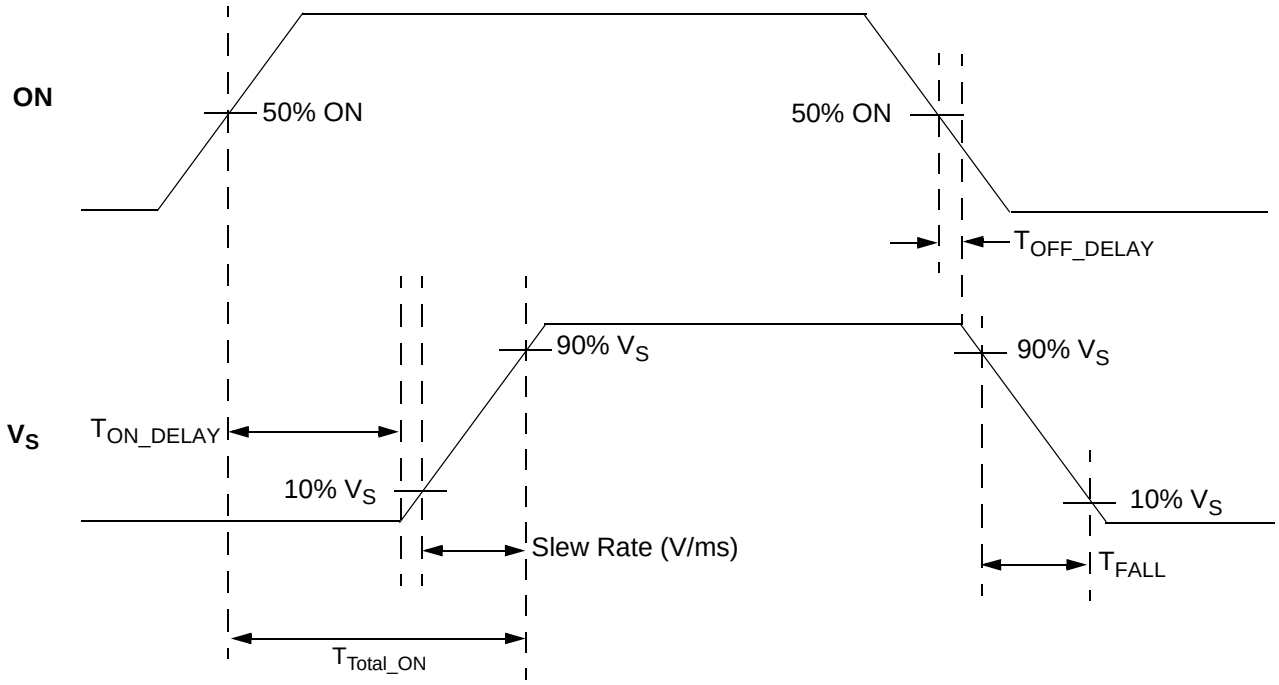
## Electrical Characteristics (continued)

$T_A$ = -40 °C to 85 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $THERM_{OFF}$ | Thermal shutoff turn-off temperature | | -- | 100 | -- | °C |
| $THERM_{TIME}$ | Thermal shutoff time | | -- | -- | 1 | ms |
| $T_{OFF\_Delay}$ | OFF Delay Time | 50% ON to $V_S$ Fall, $V_{DD}$ = $V_D$ = 5 V | -- | -- | 15 | µs |

Notes:
1. Refer to table for configuration details.

### $T_{Total\_ON}$, $T_{ON\_Delay}$ and Slew Rate Measurement



## Application NotesSLG59M1804V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply $V_{DD}$ first, followed by $V_D$ after $V_{DD}$ exceeds 1 V. Then allow $V_D$ to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If $V_{DD}$ and $V_D$ need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF $C_{LOAD}$ will prevent glitches for rise times of $V_{DD}$ and $V_D$ less than 2 ms.

If the ON pin is toggled HIGH before $V_{DD}$ and $V_D$ have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output $V_S$ follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

## SLG59M1804V Current Limiting

The SLG59M1804V has two forms of current limiting.

### Standard Current Limiting Mode

Current is measured by mirroring the current through the main MOSFET. The mirrored current is then sent through a resistor creating a voltage V(i) proportional to the MOSFET current. The V(i) is then compared with a Band Gap voltage V(BG). If V(i) exceeds the Band Gap voltage then the voltage V(g) on the gate of the main MOSFET is reduced. The V(g) continues to drop until V(i) < V(BG). This response is a closed loop response and is therefore very fast and current limits in less than a few micro-seconds. There is no difference between peak or constant current limit.

### Temperature Cutoff

However, as the V(g) drops the Rds(ON) of the main MOSFET will increase, thus limiting the current, but also increasing the power dissipation of the IC. The IC is very small and cannot dissipate much power. Therefore, if a current limit condition is sustained the IC will heat up. If the temperature exceeds approximately 120°C, then V(g) will be brought low completely shutting off the main MOSFET. As the die cools the MOSFET will be turned back on at 100°C.

If the current limiting condition has not been mitigated then the die will again heat up to 120°C and the process will repeat.

## Short Circuit Current Limiting Mode

When $V(V_S) < 250$ mV, which is the case if there is a solder bridge during the manufacturing process or a hard short on the power rail, then the current is limited to approximately 500 mA. This current limit is accomplished in the same manner as the Standard Current Limiting Mode with the exception that the current mirror is 12x greater. Because the current mirror is so much larger, a 15x smaller main MOSFET current is required to generate the same V(i). If $V(V_S)$ rises above approximately 250 mV, then this mode is automatically switched out.

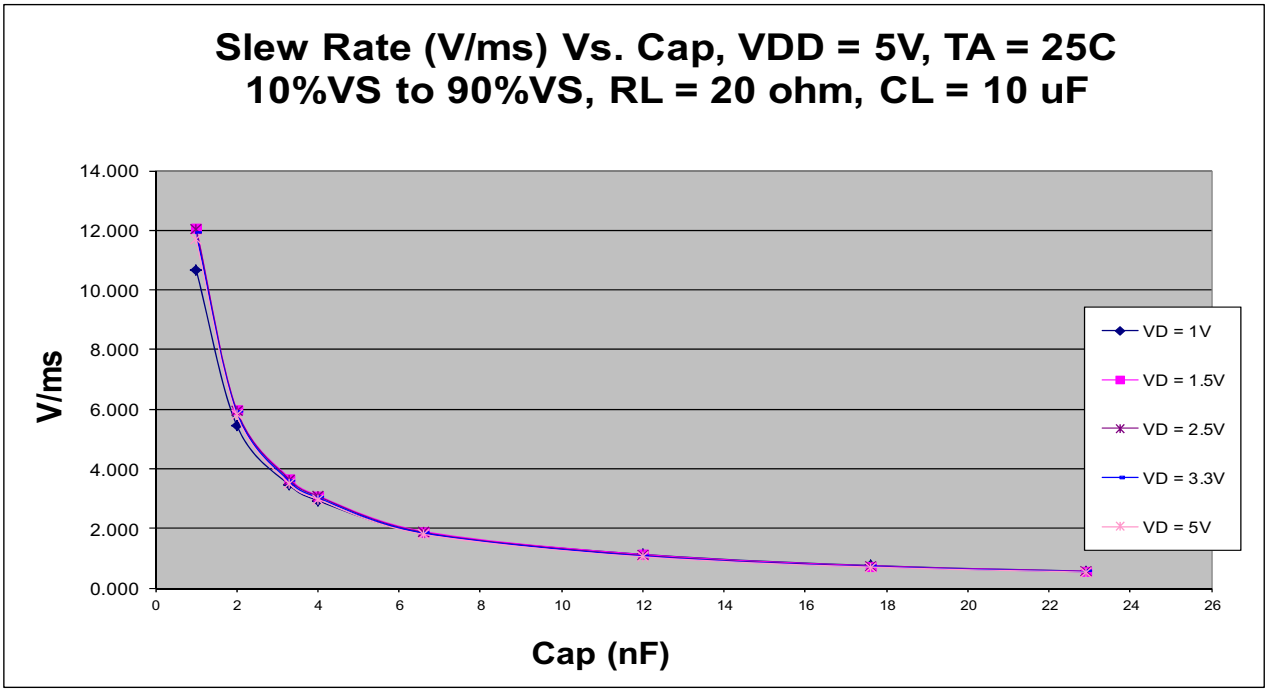
## Slew Rate Control

$V_S$ slew rate control, or in rush current control for each channel, is set by an external capacitor on pin 10 and pin 12. The charging current drawn from $V_D$ is commonly referred to as "$V_D$ Inrush Current" and can cause the input power source to collapse if the $V_D$ inrush current is too high. The expression relating $V_D$ inrush current, $V_S$ slew rate and COUT is:

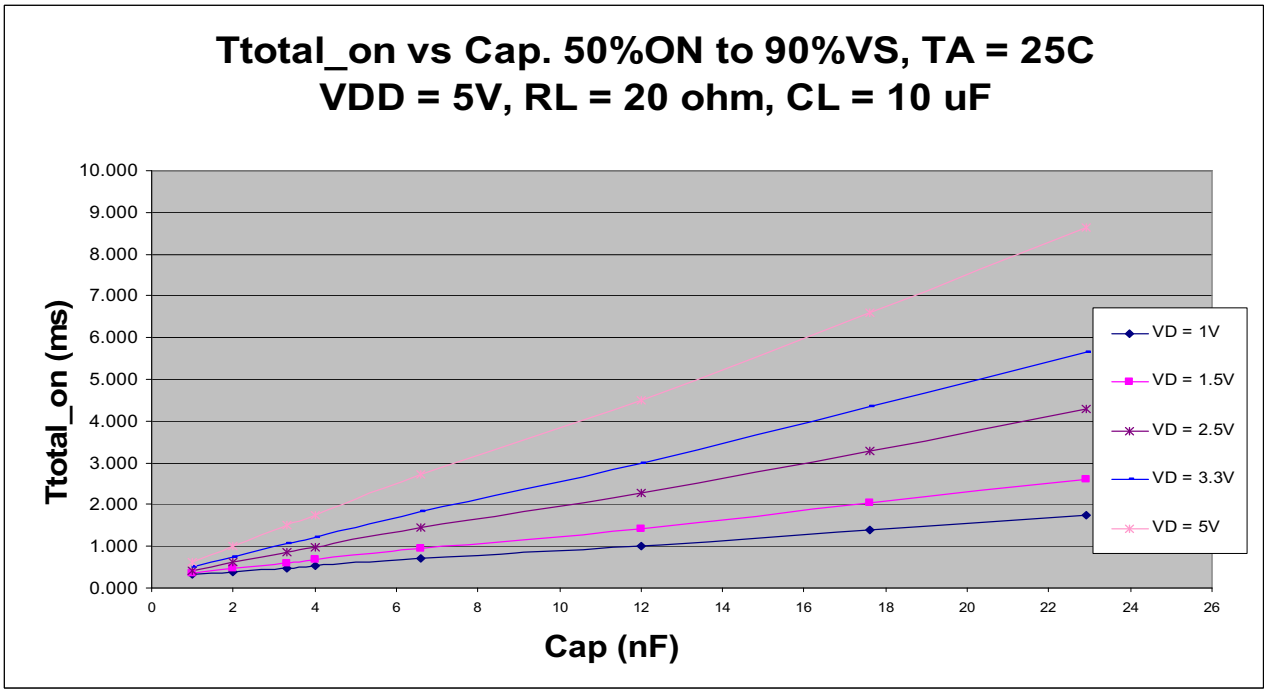
$V_D$ Inrush Current, A = COUT, µF x Slew Rate, V/ms

Dependence of Slew Rate from Cap on Pin 10 and pin 12 is illustrated on page 6. Since the IPS has some Ton Delay time before $V_S$ starts rising, the dependence of Total ON time vs Cap on pin 10 and pin 12 can be estimated and is illustrated on page 6.

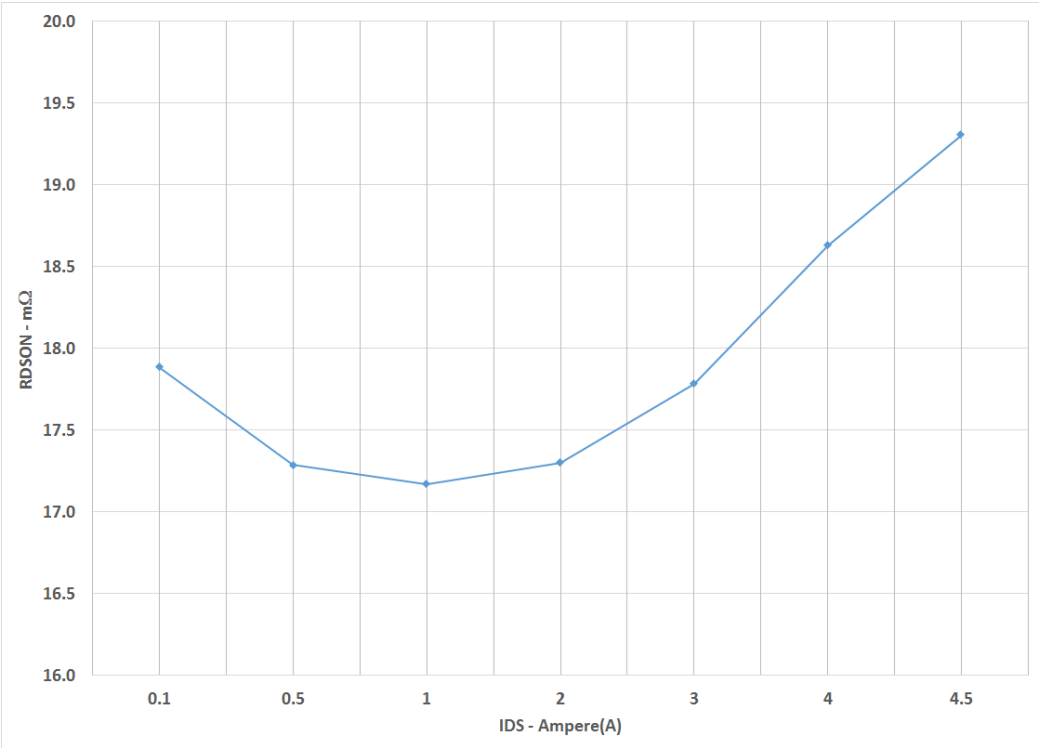
## $T_{SLEW}$ vs. CAP



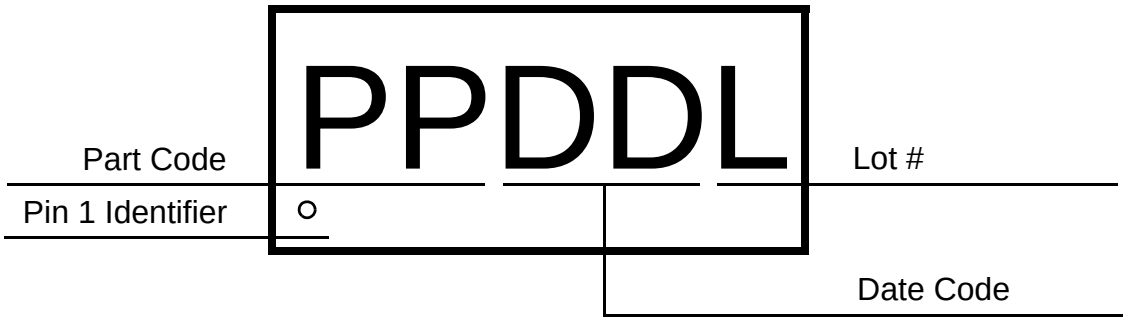

## $T_{TOTAL\_ON}$ vs. CAP



**$RDS_{ON}$ (typ) vs IDS @ $T_A$ = 85°C**



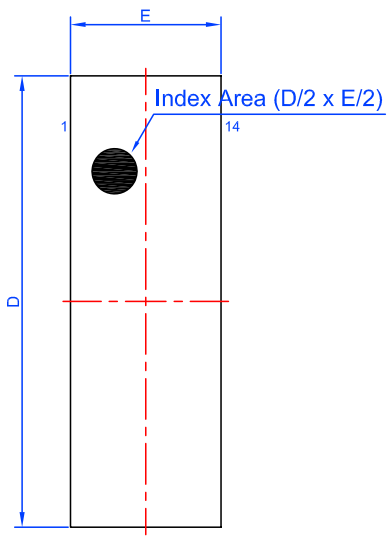
**Package Top Marking System Definition**



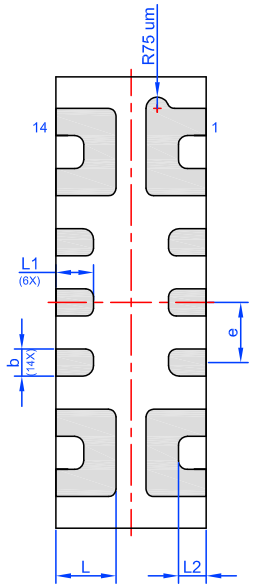

Part Number: SLG59M1804V
Production Part Code: CN

## Package Drawing and Dimensions

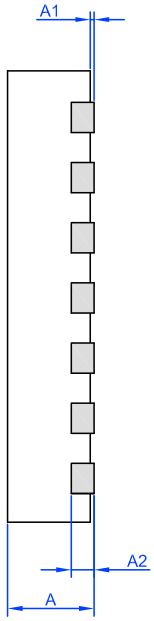
14 Lead STDFN Package 1 mm x 3 mm (Fused Lead)




Top View




BTM View




SIDE View

Unit: mm

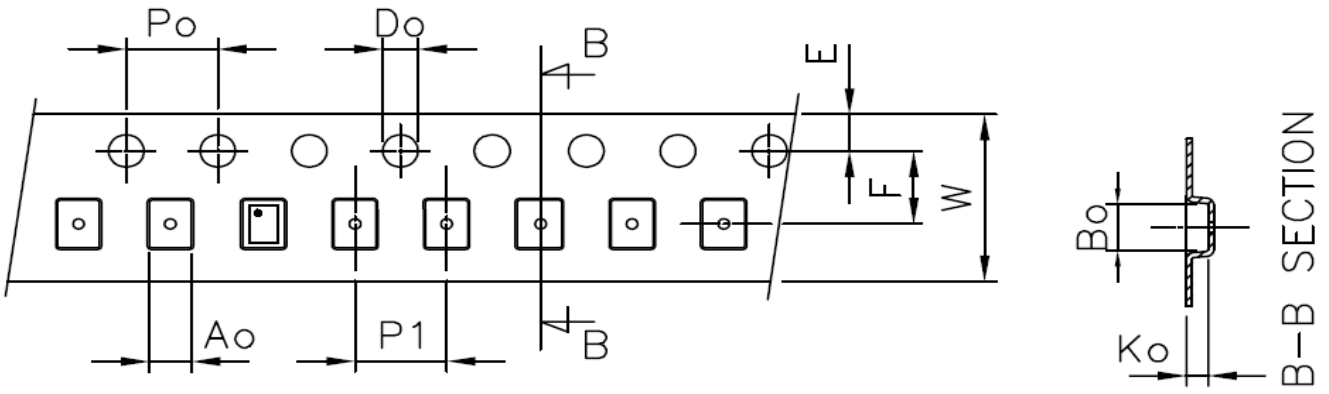
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.050 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.20 | 0.25 | 0.30 |
| e | 0.40 BSC | | | L2 | 0.06 | 0.11 | 0.16 |

## Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size | Units per Reel | Max Units per Box | Reel & Hub Size (mm) | Trailer A | | Leader B | | Pocket Tape (mm) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Pockets | Length (mm) | Pockets | Length (mm) | Width | Pitch |
| STDFN 14L | 14 | 1x3x0.55mm | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

## Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length [mm] | Pocket BTM Width [mm] | Pocket Depth [mm] | Index Hole Pitch [mm] | Pocket Pitch [mm] | Index Hole Diameter [mm] | Index Hole to Tape Edge [mm] | Index Hole to Pocket Center [mm] | Tape Width [mm] |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 14L | 1.15 | 3.15 | 0.7 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |




## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.65 $mm^3$ (nominal). More information can be found at www.jedec.org.

## Revision History

| Date | Version | Change |
|---|---|---|
| 2/16/2018 | 1.02 | Updated VDD Max to 5 V<br>Added UL certification |
| 10/26/2017 | 1.01 | Updated Part Code Marking<br>Fixed typos |
| 10/03/2017 | 1.00 | Production Release |