Single-Phase High-Performance Wide-Span Energy Metering IC 90E21/22/23/24

Version 6
January 10, 2012

6024 Silver Creek Valley Road, San Jose, CA 95138
Printed in U.S.A.

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FEATURES

Metering Features

- Metering features fully in compliance with the requirements of IEC62052-11, IEC62053-21 and IEC62053-23; applicable in class 1 or class 2 single-phase watt-hour meter or class 2 single-phase var-hour meter.
- Accuracy of 0.1% for active energy and 0.2% for reactive energy over a dynamic range of 5000:1.
- Temperature coefficient is 15 ppm/ ℃ (typical) for on-chip reference voltage
- Single-point calibration over a dynamic range of 5000:1 for active energy; no calibration needed for reactive energy.
- Energy Meter Constant doubling at low current to save verification time.
- Electrical parameters measurement: less than ±0.5% fiducial error for Vrms, Irms, mean active/ reactive/ apparent power, frequency, power factor and phase angle.
- Forward/ reverse active/ reactive energy with independent energy registers. Active/ reactive energy can be output by pulse or read through energy registers to adapt to different applications.
- Programmable startup and no-load power threshold.
- Dedicated ADC and different gains for L line and N line current sampling circuits. Current sampled over shunt resistor or current transformer (CT); voltage sampled over resistor divider network or potential transformer (PT).
- Programmable L line and N line metering modes: anti-tampering mode (larger power), L line mode (fixed L line), L+N mode (applicable for single-phase three-wire system) and flexible mode (configure through register).
- Programmable L line and N line power difference threshold in anti-tampering mode.

Other Features

- 3.3V single power supply. Operating voltage range: 2.8~3.6V. Metering accuracy guaranteed within 3.0V~3.6V. 5V compatible for digital input.
- Built-in hysteresis for power-on reset.
- Four-wire SPI interface or simplified three-wire SPI interface with fixed 24 cycles for all registers operation
- Parameter diagnosis function and programmable interrupt output of the IRQ interrupt signal and the WarnOut signal.
- Programmable voltage sag detection and zero-crossing output.
- Channel input range
  - Voltage channel (when gain is '1'): 120μVrms~600mVrms.
  - L line current channel (when gain is '24'): 5μVrms~25mVrms.
  - N line current channel (when gain is '1'): 120μVrms~600mVrms.
- Programmable L line current gain: 1, 4, 8, 16, 24; Programmable N line gain: 1, 2, 4.
- Support L line and N line offset compensation.
- CF1 and CF2 output active and reactive energy pulses respectively which can be used for calibration or energy accumulation.
- Crystal oscillator frequency: 8.192 MHz. On-chip 10pF capacitors and no need of external capacitors.
- Green SSOP28 package.
- Operating temperature: -40 ℃ ~ +85 ℃ .

APPLICATION

- The 90E21/22/23/24 series are used for active and reactive energy metering for single-phase two-wire, single-phase three-wire or anti-tampering energy meters. With the measurement function, the 90E21/22/23/24 series can also be used in power instruments which need to measure voltage, current, etc.

DESCRIPTION

The 90E21/22/23/24 series are high-performance wide-span energy metering chips. IDT's proprietary ADC and DSP technology ensure the chips' long-term stability over variations in grid and ambient environmental conditions.

Table-1 Function List

Part Number	Active Energy Metering	Reactive Energy Metering	N Line Metering	Electrical Parameters Measurement
90E21	√			√
90E22	√	√		√
90E23	√		√	√
90E24	√	√	√	√

90E21/22/23/24 are all of green SSOP28 package with the same pin alignment. In this datasheet, all reactive energy metering parts are only applicable for the 90E22/24, and all N line metering and measurement parts are only applicable for the 90E23/24.

BLOCK DIAGRAM

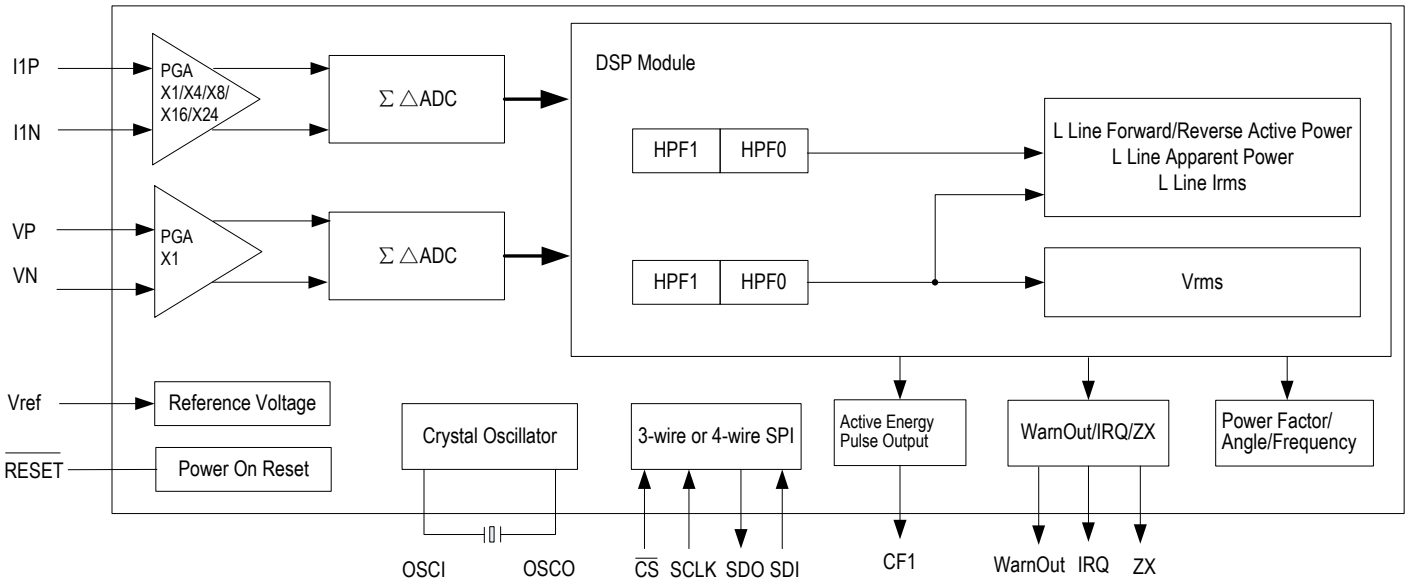


Figure-1 90E21 Block Diagram

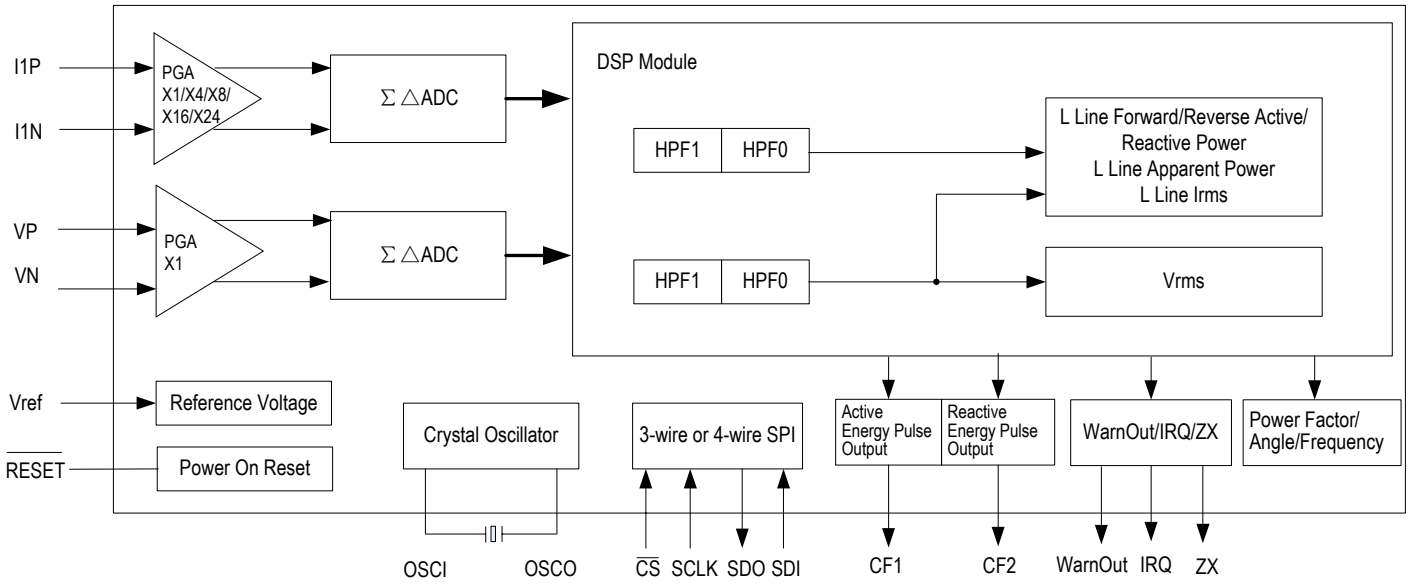


Figure-2 90E22 Block Diagram

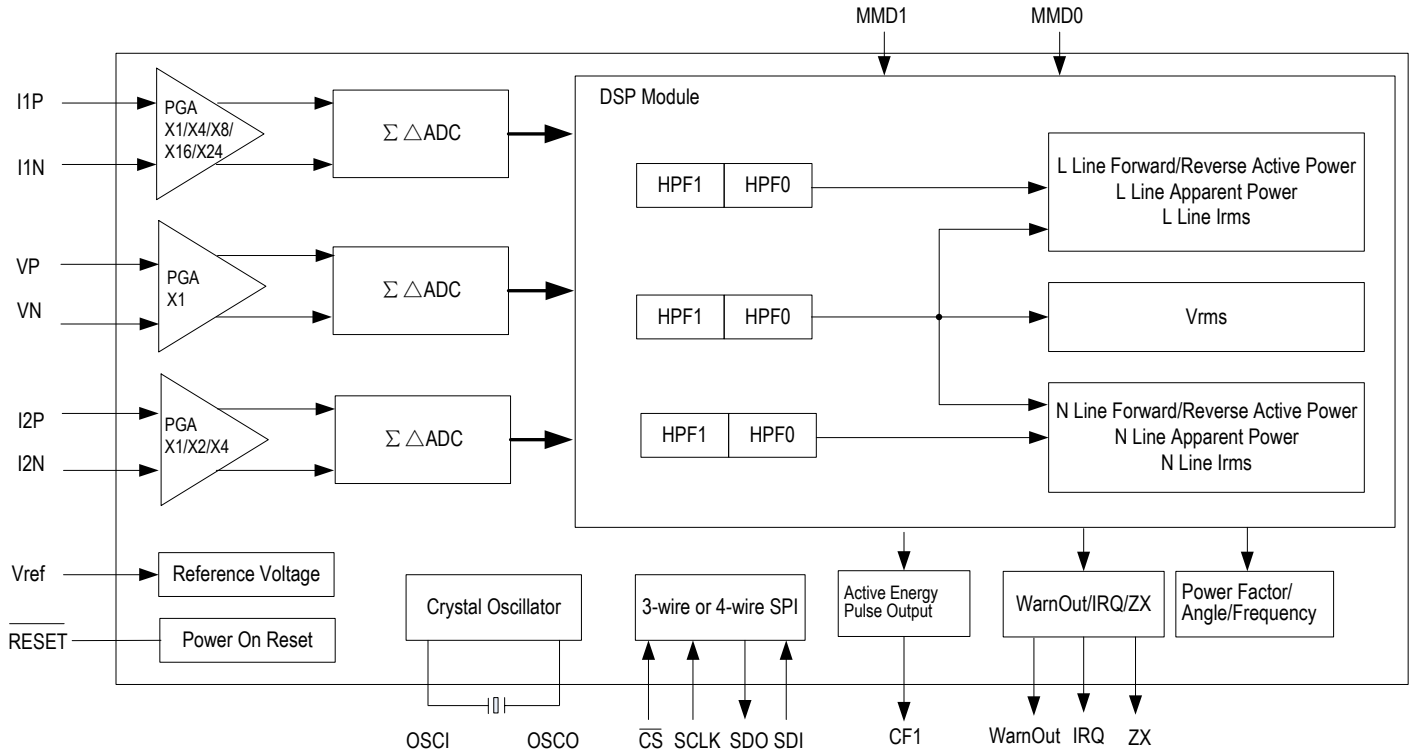


Figure-3 90E23 Block Diagram

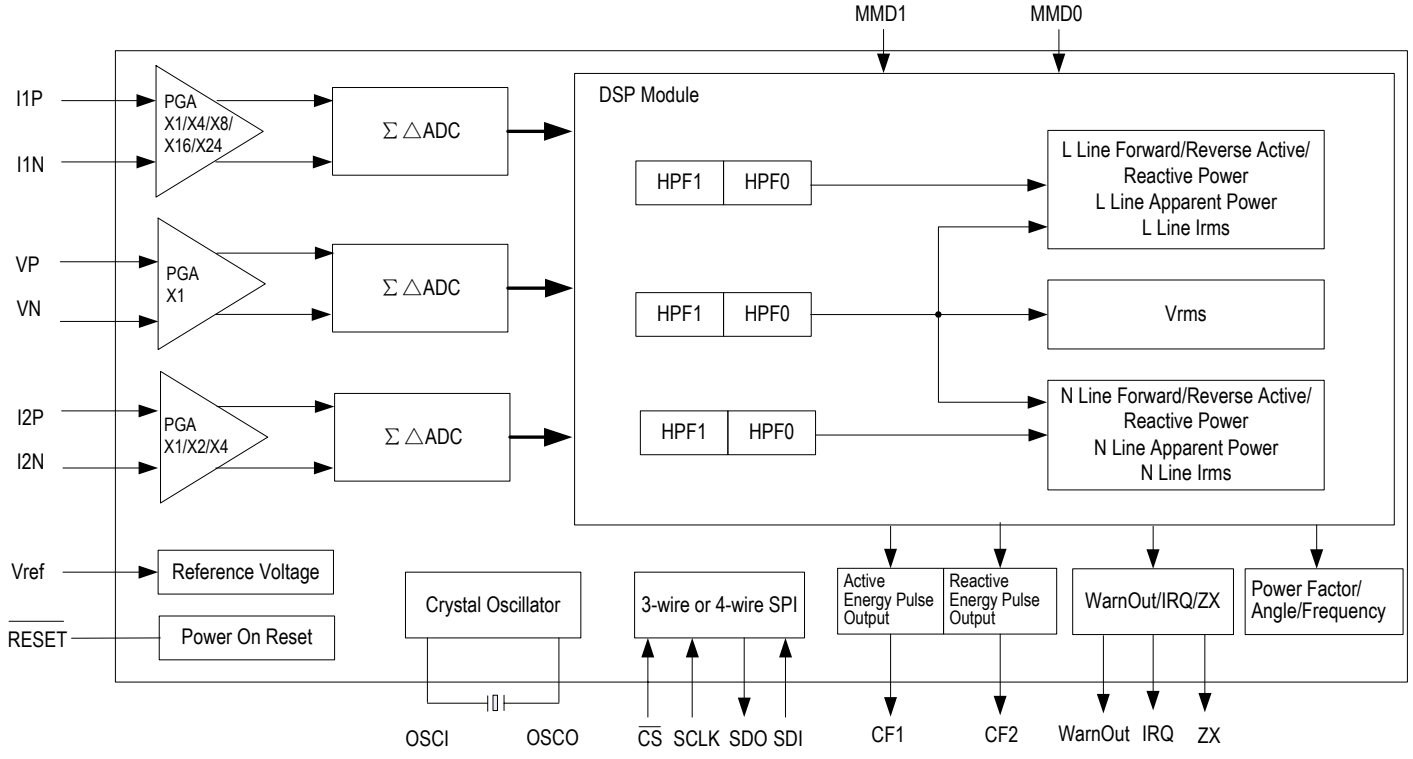


Figure-4 90E24 Block Diagram

1 PIN ASSIGNMENT

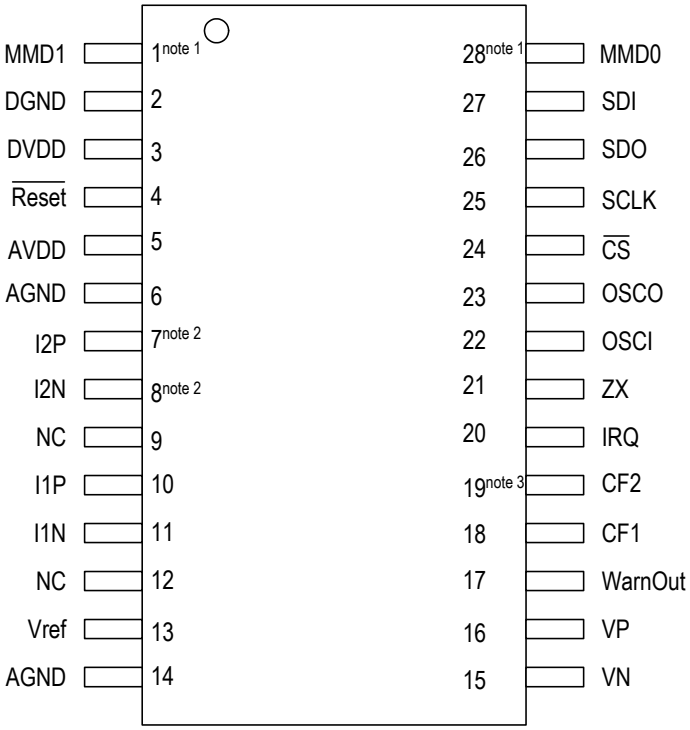


Figure-5 Pin Assignment (Top View)

Note 1: Pin 1 and 28 are dedicated for the 90E23/24. Pin 1 should connect to DGND and pin 28 should connect to DVDD for 90E21/22.

Note 2: Pin 7 and 8 are dedicated for the 90E23/24. They should be left open for the 90E21/22.

Note 3: Pin 19 is dedicated for the 90E22/24. It should be left open for the 90E21/23.

2 PIN DESCRIPTION

Table-2 Pin Description

Name	Pin No.	I/O [note 1]	Type	Description
$\overline{\text{Reset}}$	4	I	LVTTL	**$\overline{\text{Reset}}$: Reset Pin (active low)** This pin should connect to ground through a 0.1μF filter capacitor. In application it can also directly connect to one output pin from microcontroller (MCU).
DVDD	3	I	Power	**DVDD: Digital Power Supply** This pin provides power supply to the digital part. It should be decoupled with a 10μF electrolytic capacitor and a 0.1μF capacitor.
DGND	2	I	Power	**DGND: Digital Ground**
AVDD	5	I	Power	**AVDD: Analog Power Supply** This pin provides power supply to the analog part. This pin should connect to DVDD through a 10Ω resistor and be decoupled with a 0.1μF capacitor.
Vref	13	O	Analog	**Vref: Output Pin for Reference Voltage** This pin should be decoupled with a 1μF capacitor and a 1nF capacitor.
AGND	6, 14	I	Power	**AGND: Analog Ground**
I1P I1N	10 11	I	Analog	**I1P: Positive Input for L Line Current** **I1N: Negative Input for L Line Current** These pins are differential inputs for L line current. Input range is 5μVrms~25mVrms when gain is '24'.
I2P I2N	7 8	I	Analog	**I2P: Positive Input for N Line Current** **I2N: Negative Input for N Line Current** These pins are differential inputs for N line current. Input range is 120μVrms~600mVrms when gain is '1'. **Note:** I2P and I2N are dedicated for the 90E23/24. They should be left open for the 90E21/22.
VP VN	16 15	I	Analog	**VP: Positive Input for Voltage** **VN: Negative Input for Voltage** These pins are differential inputs for voltage. Input range is 120μVrms~600mVrms.
NC	9, 12			**NC: This pin should be left open.**
$\overline{\text{CS}}$	24	I	LVTTL	**$\overline{\text{CS}}$: Chip Select (Active Low)** In 4-wire SPI mode, this pin must be driven from high to low for each read/write operation, and maintain low for the entire operation. In 3-wire SPI mode, this pin must be low all the time. Refer to section 4.1.
SCLK	25	I	LVTTL	**SCLK: Serial Clock** This pin is used as the clock for the SPI interface. Data on SDI is shifted into the chip on the rising edge of SCLK while data on SDO is shifted out of the chip on the falling edge of SCLK.
SDO	26	OZ	LVTTL	**SDO: Serial Data Output** This pin is used as the data output for the SPI interface. Data on this pin is shifted out of the chip on the falling edge of SCLK.
SDI	27	I	LVTTL	**SDI: Serial Data Input** This pin is used as the data input for the SPI interface. Address and data on this pin is shifted into the chip on the rising edge of SCLK.
MMD1 MMD0	1 28	I	LVTTL	**MMD1/0: Metering Mode Configuration** 00: anti-tampering mode (larger power); 01: L line mode (fixed L line); 10: L+N mode (applicable for single-phase three-wire system); 11: flexible mode (line specified by the LNSel bit (MMode, 2BH)) **Note:** The MMD1/0 pins are dedicated for the 90E23/24. For the 90E21/22, the metering mode is fixed as L line mode, and MMD1 should connect to DGND and MMD0 should connect to DVDD.

Table-2 Pin Description (Continued)

Name	Pin No.	I/O note 1	Type	Description
OSCI	22	I	LVTTL	**OSCI: External Crystal Input** An 8.192 MHz crystal is connected between OSCI and OSCO. There is an on-chip 10pF capacitor, therefore no need of external capacitors.
OSCO	23	O	LVTTL	**OSCO: External Crystal Output** An 8.192 MHz crystal is connected between OSCI and OSCO. There is an on-chip 10pF capacitor, therefore no need of external capacitors.
CF1 CF2	18 19	O	LVTTL	**CF1: Active Energy Pulse Output** **CF2: Reactive Energy Pulse Output** These pins output active/reactive energy pulses. **Note:** CF2 is dedicated for the 90E22/24. It should be left open for the 90E21/23.
ZX	21	O	LVTTL	**ZX: Voltage Zero-Crossing Output** This pin is asserted when voltage crosses zero. Zero-crossing mode can be configured to positive zero-crossing, negative zero-crossing or all zero-crossing by the Zxcon[1:0] bits (MMode, 2BH).
IRQ	20	O	LVTTL	**IRQ: Interrupt Output** This pin is asserted when one or more events in the SysStatus register (01H) occur. It is deasserted when there is no bit set in the SysStatus register (01H).
WarnOut	17	O	LVTTL	**WarnOut: Fatal Error Warning** This pin is asserted when there is metering parameter calibration error or voltage sag. Refer to section 4.2.
Note 1: All digital inputs are 5V tolerant except for the OSCI pin.				

3 FUNCTIONAL DESCRIPTION

3.1 DYNAMIC METERING RANGE

Accuracy is 0.1% for active energy metering and 0.2% for reactive energy metering over a dynamic range of 5000:1 (typical). Refer to Table-3 and Table-4.

Table-3 Active Energy Metering Error

Current	Power Factor	Error (%)
20mA ⩽ I < 50mA	1.0	±0.2
50mA ⩽ I ⩽ 100A		±0.1
50mA ⩽ I < 100mA	0.5 (Inductive) 0.8 (Capacitive)	±0.2
100mA ⩽ I ⩽ 100A		±0.1
Note: Shunt resistor is 250 μΩ or CT ratio is 1000:1 and load resistor is 6Ω.		

Table-4 Reactive Energy Metering Error

Current	sinϕ (Inductive or Capacitive)	Error (%)
20mA ⩽ I < 50mA	1.0	±0.4
50mA ⩽ I ⩽ 100A		±0.2
50mA ⩽ I < 100mA	0.5	±0.4
100mA ⩽ I ⩽ 100A		±0.2
Note: Shunt resistor is 250 μΩ or CT ratio is 1000:1 and load resistor is 6Ω.		

3.2 STARTUP AND NO-LOAD POWER

Startup and no-load power thresholds are programmable, both for active and reactive power. The related registers are listed in Table-5.

Table-5 Threshold Configuration for Startup and No-Load Power

Threshold	Register
Threshold for Active Startup Power	PStartTh, 27H
Threshold for Active No-load Power	PNolTh, 28H
Threshold for Reactive Startup Power	QStartTh, 29H
Threshold for Reactive No-load Power	QNolTh, 2AH

The chip will start within 1.2 times of the theoretical startup time of the configured startup power, if startup power is less than the corresponding power of 20mA when power factor or sinϕ is 1.0.

The chip has no-load status bits, the Pnoload/Qnoload bit (EnStatus, 46H). The chip will not output any active pulse (CF1) in active no-load state. The chip will not output any reactive pulse (CF2) in reactive no-load state.

3.3 ENERGY REGISTERS

The 90E21/22/23/24 provides energy pulse output CFx (CF1/CF2) which is proportionate to active/reactive energy. Energy is usually accumulated by adding the CFx pulses in system applications. Alternatively, the 90E21/22/23/24 provides energy registers. There are forward (inductive), reverse (capacitive) and absolute energy registers for both active and reactive energy. Refer to Table-6.

Table-6 Energy Registers

Energy	Register
Forward Active Energy	APenergy, 40H
Reverse Active Energy	ANenergy, 41H
Absolute Active Energy	ATenergy, 42H
Forward (Inductive) Reactive Energy	RPenergy, 43H
Reverse (Capacitive) Reactive Energy	RNenergy, 44H
Absolute Reactive Energy	RTenergy, 45H

Each energy register is cleared after read. The resolution of energy registers is 0.1CF, i.e. one LSB represents 0.1 energy pulse.

3.4 N LINE METERING AND ANTI-TAMPERING

3.4.1 METERING MODE AND L/N LINE CURRENT SAMPLING GAIN CONFIGURATION

The 90E23 and 90E24 have two current sampling circuits with N line metering and anti-tampering functions. The MMD1 and MMD0 pins are used to configure the metering mode. Refer to Table-7.

Table-7 Metering Mode

MMD1	MMD0	Metering Mode	CFx (CF1 or CF2) Output
0	0	Anti-tampering Mode (larger power)	CFx represents the larger energy line. Refer to section 3.4.2.
0	1	L Line Mode (fixed L line)	CFx represents L line energy all the time.
1	0	L+N Mode (applicable for single-phase three-wire system)	CFx represents the arithmetic sum of L line and N line energy
1	1	Flexible Mode (line specified by the LNSel bit (MMode, 2BH))	CFx represents energy of the specified line.

The 90E23 and 90E24 have two current sampling circuits with different gain configurations. L line gain can be 1, 4, 8, 16 and 24, and N line gain can be 1, 2 and 4. The configuration is made by the MMode register (2BH). Generally L line can be sampled over shunt resistor or CT. N line can be sampled over CT for isolation consideration. Note that Rogowski coil is not supported.

3.4.2 ANTI-TAMPERING MODE

Threshold

In anti-tampering mode, the power difference threshold between L line and N line can be: 1%, 2%,... 12%, 12.5%, 6.25%, 3.125% and 1.5625%, altogether 16 choices. The configuration is made by the Pthresh[3:0] bits (MMode, 2BH) and the default value is 3.125%. The threshold is applicable for active energy. The metering line of the reactive energy follows that of the active energy.

Compare Method

In anti-tampering mode, the compare method is as follows:

If current metering line is L line and

$$\frac{\text{N Line Active Power - L Line Active Power}}{\text{L Line Active Power}} * 100\% > \text{Threshold}$$

N line is switched as the metering line, otherwise L line keeps as the metering line.

If current metering line is N line and

$$\frac{\text{L Line Active Power - N Line Active Power}}{\text{N Line Active Power}} * 100\% > \text{Threshold}$$

L line is switched as the metering line, otherwise N line keeps as the metering line.

This method can achieve hysteresis around the threshold automatically. L line is employed after reset by default.

Special Treatment at Low Power

When power is low, general factors such as the quantization error or calibration difference between L line and N line might cause the power difference to be exceeded. To ensure L line and N line to start up normally, special treatment as follows is adopted:

The line with higher power is selected as the metering line when both L line and N line power are lower than 8 times of the startup power but higher than the startup power.

3.5 MEASUREMENT AND ZERO-CROSSING

3.5.1 MEASUREMENT

The 90E21/22/23/24 has the following measurements:

- voltage rms
- current rms (L line/N line)
- mean active power (L line/N line)
- mean reactive power (L line/N line)
- voltage frequency
- power factor (L line/N line)
- phase angle between voltage and current (L line/N line)
- mean apparent power (L line/N line)

The above measurements are all calculated with fiducial error except for frequency. The frequency accuracy is 0.01Hz, and the other measurement accuracy is 0.5%. Fiducial error is calculated as follow:

$$\text{Fiducial\_Error} = \frac{U_{mea} - U_{real}}{U_{FV}} * 100\%$$

Where U_{mea} is the measured voltage, U_{real} is the actual voltage and U_{FV} is the fiducial value.

Table-8 The Measurement Format

Measurement	Fiducial Value (FV)	90E21/22/23/24 Defined Format	Range	Comment
Voltage rms	Un	XXX.XX	0~655.35V	
Current rms[note 1, note 2]	Imax as 4Ib	XX.XXX	0~65.535A	
Active/ Reactive Power[note 1]	maximum power as Un*4Ib	XX.XXX	-32.768~+32.767 kW/kvar	Complement, MSB as the sign bit
Apparent Power[note 1]	Un*4Ib	XX.XXX	0~+32.767 kVA	Complement, MSB always '0'
Frequency	fn	XX.XX	45.00~65.00 Hz	
Power Factor[note 3]	1.000	X.XXX	-1.000~+1.000	Signed, MSB as the sign bit
Phase Angle[note 4]	180°	XXX.X	-180°~+180°	Signed, MSB as the sign bit

Note 1: All registers are of 16 bits. For cases when the current and active/reactive/apparent power goes beyond the above range, it is suggested to be handled by microcontroller (MCU) in application. For example, register value can be calibrated to 1/2 of the actual value during calibration, then multiply 2 in application. Note that if the actual current is twice of that of the 90E21/22/23/24, the actual active/reactive/apparent power is also twice of that of the chip.
Note 2: The accuracy is not guaranteed when the current is lower than 15mA. Note that the tolerance is 25 mA at I_{FV} of 5A and fiducial accuracy of 0.5%.
Note 3: Power factor is obtained by active power dividing apparent power
Note 4: Phase angle is obtained when voltage/current crosses zero at the frequency of 256kHz. Precision is not guaranteed at small current.

3.5.2 ZERO-CROSSING

The ZX pin is asserted when the sampling voltage crosses zero. Zero-crossing mode can be configured to positive zero-crossing, negative zero-crossing and all zero-crossing by the Zxcon[1:0] bits (MMode, 2BH). Refer to section 6.4.

The zero-crossing signal can facilitate operations such as relay operation and power line carrier transmission in typical smart meter applications.

3.6 CALIBRATION

Metering Calibration

Only single-point calibration is needed over the entire dynamic range.

Metering calibration is realized by first calibrating gain at unity power factor and then calibrating phase angle compensation at 0.5 inductive power factor.

However, due to very small signal in L line current sampling circuits, any external interference, e.g., a tens of nano volts influence voltage on shunt resistor conducted by transformer in the energy meter's power supply may cause perceptible metering error, especially in low current state. For this nearly constant external interference, the 90E21/22/23/24 also provides power offset compensation.

L line and N line need to be calibrated sequentially. Reactive does not need to be calibrated.

Measurement Calibration

Measurement calibration is realized by calibrating the gains for voltage rms and current rms. Considering the possible nonlinearity around zero caused by external components, the chip also provides offset compensation for voltage rms, current rms, mean active power and mean reactive power.

Frequency, phase angle and power factor do not need calibration.

For more calibration details, please refer to Application Note AN-641.

3.7 RESET

The 90E21/22/23/24 has an on-chip power supply monitor circuit with built-in hysteresis. The 90E21/22/23/24 only works within the voltage range.

The 90E21/22/23/24 has three means of reset: power-on reset, hardware reset and software reset. All registers resume to their default value after reset.

Power-on Reset: Power-on reset is initiated during power-up. Refer to section 6.3.

Hardware Reset: Hardware Reset is initiated when the $\overline{\text{reset}}$ pin is pulled low. The width of the reset signal should be over 200μs.

Software Reset: Software Reset is initiated when '789AH' is written to the software reset register (SoftReset, 00H).

4 INTERFACE

4.1 SERIAL PERIPHERAL INTERFACE (SPI)

SPI is a full-duplex, synchronous channel. There are two SPI modes: four-wire mode and three-wire mode. In four-wire mode, four pins are used: $\overline{CS}$, SCLK, SDI and SDO. In three-wire mode, three pins are used: SCLK, SDI and SDO. Data on SDI is shifted into the chip on the rising edge of SCLK while data on SDO is shifted out of the chip on the falling edge of SCLK. The LastSPIData register (06H) stores the 16-bit data that is just read or written.

4.1.1 FOUR-WIRE MODE

In four-wire mode, the $\overline{CS}$ pin must be driven low for the entire read or write operation. The first bit on SDI defines the access type and the lower 7-bit is decoded as address.

Read Sequence

As shown in Figure-6, a read operation is initiated by a high on SDI followed by a 7-bit register address. A 16-bit data in this register is then shifted out of the chip on SDO. A complete read operation contains 24 cycles.

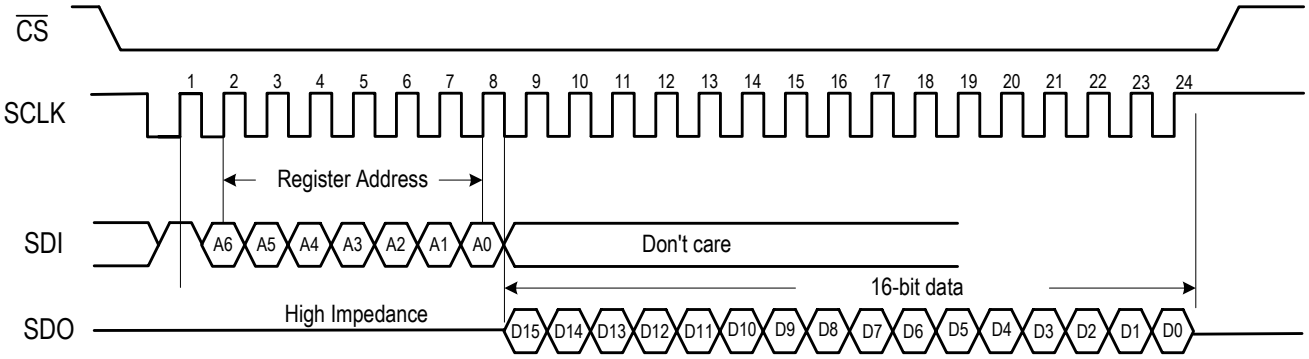


Figure-6 Read Sequence in Four-Wire Mode

Write Sequence

As shown in Figure-7, a write operation is initiated by a low on SDI followed by a 7-bit register address. A 16-bit data is then shifted into the chip on SDI. A complete write operation contains 24 cycles.

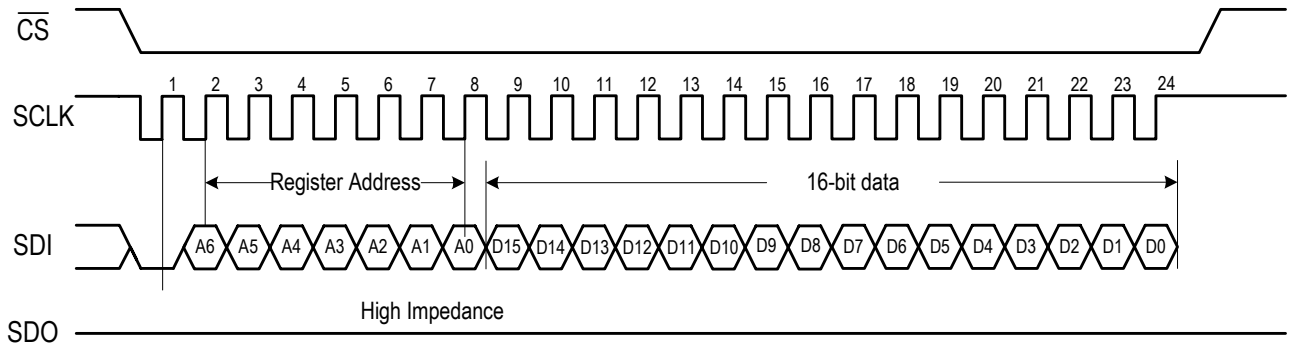


Figure-7 Write Sequence in Four-Wire Mode

4.1.2 THREE-WIRE MODE

In three-wire mode, $\overline{CS}$ is always at low level. When there is no operation, SCLK keeps at high level. The start of a read or write operation is triggered if SCLK is consistently low for at least 400μs. The subsequent read or write operation is similar to that in four-wire mode. Refer to Figure-8 and Figure-9.

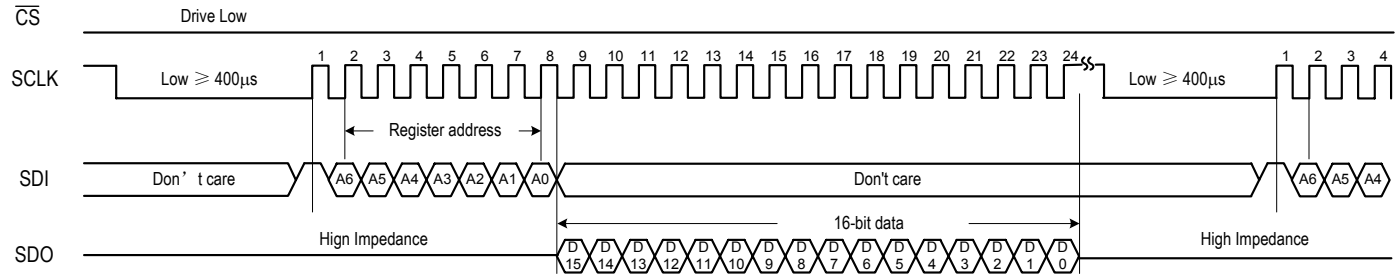


Figure-8 Read Sequence in Three-Wire Mode

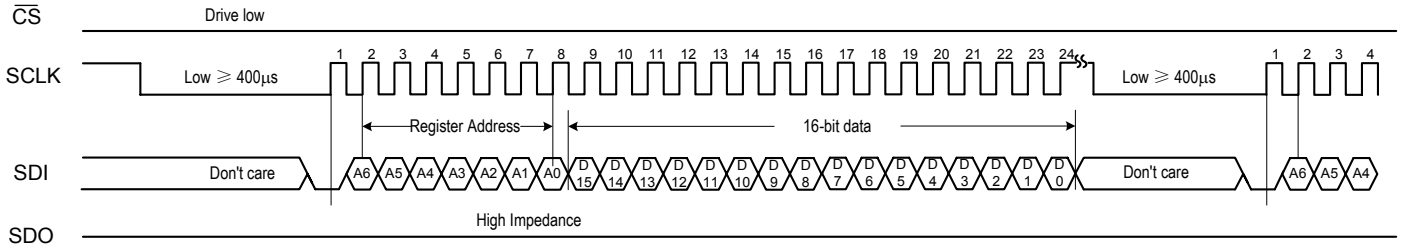


Figure-9 Write Sequence in Three-Wire Mode

4.1.3 TIMEOUT AND PROTECTION

Timeout occurs if SCLK does not toggle for 6ms in both four-wire and three-wire modes. When timeout, the read or write operation is aborted.

If there are more than 24 SCLK cycles when $\overline{CS}$ is driven low in four-wire mode or between two starts in three-wire mode, writing operation is prohibited while normal reading operation can be completed by taking the first 24 SCLK cycles as the valid ones. However, the reading result might not be the intended one.

A read access to an invalid address returns all zero. A write access to an invalid address is discarded.

Table-9 and Table-10 list the read or write result in different conditions.

Table-9 Read / Write Result in Four-Wire Mode

Condition			Result	
Operation	Timeout	SCLK Cycles[note 1]	Read/Write Status	LastSPIData Register Update
Read	-[note 2]	>=24	Normal Read	Yes
	-[note 2]	<24	Partial Read	No
Write	No	=24	Normal Write	Yes
	No	!=24	No Write	No
	Yes	-	No Write	No

Note 1: The number of SCLK cycles when $\overline{CS}$ is driven low or the number of SCLK cycles before timeout if any.
Note 2: '-' stands for Don't Care.

Table-10 Read / Write Result in Three-Wire Mode

Condition			Result	
Operation	Timeout	SCLK Cycles[note 1]	Read/Write Status	LastSPIData Register Update
Read	No	>=24[note 2]	Normal Read	Yes
	Timeout after 24 cycles	>24	Normal Read	Yes
	Timeout before 24 cycles	-[note 3]	Partial Read	No
	Timeout at 24 cycles	=24	Normal Read	Yes
Write	No	=24	Normal Write	Yes
	No	!=24	No Write	No
	Yes	-	No Write	No

Note 1: The number of SCLK cycles between 2 starts or the number of SCLK cycles before timeout if any.
Note 2: There is no such case of less than 24 SCLK cycles when there is no timeout in three-wire mode, because the first few SCLK cycles in the next operation is counted into this operation. In this case, data is corrupted.
Note 3: '-' stands for Don't Care.

4.2 WARNOUT PIN FOR FATAL ERROR WARNING

Fatal error warning is raised through the WarnOut pin in two cases: checksum calibration error and voltage sag.

Calibration Error

The 90E21/22/23/24 performs diagnosis on a regular basis for important parameters such as calibration parameters and metering configuration. When checksum is not correct, the CalErr[1:0] bits (SysStatus, 01H) are set, and both the WarnOut pin and the IRQ pin are asserted. When checksum is not correct, the metering part does not work to prevent a large number of pulses during power-on or any abnormal situation upon incorrect parameters.

Voltage Sag

Voltage sag is detected when voltage is continuously below the voltage sag threshold for one cycle which starts from any zero-crossing point. Voltage threshold is configured by the SagTh register (03H). Refer to section 6.5.

When voltage sag occurs, the SagWarn bit (SysStatus, 01H) is set and the WarnOut pin is asserted if the FuncEn register (02H) enables voltage sag warning through the WarnOut pin. This function helps reduce power-down detection circuit in system design. In addition, the method of judging voltage sag by detecting AC side voltage eliminates the influence of large capacitor in traditional rectifier circuit, and can detect voltage sag earlier.

4.3 LOW COST IMPLEMENTATION IN ISOLATION WITH MCU

The following functions can be achieved at low cost when the 90E21/22/23/24 is isolated from the MCU:

SPI: MCU can perform read and write operations through low speed optocoupler (e.g. NEC2501) when the 90E21/22/23/24 is isolated from the MCU. The SPI interface can be of 3-wire or 4-wire.

Energy Pulses CFx: Energy can be accumulated by reading values in corresponding energy registers. CFx can also connect to the optocoupler and the energy pulse light can be turned on by CFx.

Fatal Error WarnOut: Fatal error can be acquired by reading the CalErr[1:0] bits (SysStatus, 01H).

IRQ: IRQ interrupt can be acquired by reading the SysStatus register (01H).

Reset: The 90E21/22/23/24 is reset when '789AH' is written to the software reset register (SoftReset, 00H).

5 REGISTER

5.1 REGISTER LIST

Table-11 Register List

Register Address	Register Name	Read/Write Type	Functional Description	Comment[note 1]	Page
Status and Special Register					
00H	SoftReset	W	Software Reset		P 21
01H	SysStatus	R/C	System Status	different for various chips[note 2, note 3]	P 22
02H	FuncEn	R/W	Function Enable	different for various chips[note 2]	P 23
03H	SagTh	R/W	Voltage Sag Threshold		P 23
04H	SmallPMod	R/W	Small-Power Mode		P 24
06H	LastSPIData	R	Last Read/Write SPI Value		P 24
Metering Calibration and Configuration Register					
20H	CalStart	R/W	Calibration Start Command		P 25
21H	PLconstH	R/W	High Word of PL_Constant		P 25
22H	PLconstL	R/W	Low Word of PL_Constant		P 26
23H	Lgain	R/W	L Line Calibration Gain		P 26
24H	Lphi	R/W	L Line Calibration Angle		P 26
25H	Ngain	R/W	N Line Calibration Gain	Not applicable to the 90E21/22[note 3]	P 27
26H	Nphi	R/W	N Line Calibration Angle	Not applicable to the 90E21/22[note 3]	P 27
27H	PStartTh	R/W	Active Startup Power Threshold		P 27
28H	PNolTh	R/W	Active No-Load Power Threshold		P 28
29H	QStartTh	R/W	Reactive Startup Power Threshold	Not applicable to the 90E21/23[note 2]	P 28
2AH	QNolTh	R/W	Reactive No-Load Power Threshold	Not applicable to the 90E21/23[note 2]	P 28
2BH	MMode	R/W	Metering Mode Configuration	different for various chips[note 2, note 3]	P 29
2CH	CS1	R/W	Checksum 1		P 31
Measurement Calibration Register					
30H	AdjStart	R/W	Measurement Calibration Start Command		P 32
31H	Ugain	R/W	Voltage rms Gain		P 32
32H	IgainL	R/W	L Line Current rms Gain		P 33
33H	IgainN	R/W	N Line Current rms Gain	Not applicable to the 90E21/22[note 3]	P 33
34H	Uoffset	R/W	Voltage Offset		P 33
35H	IoffsetL	R/W	L Line Current Offset		P 34
36H	IoffsetN	R/W	N Line Current Offset	Not applicable to the 90E21/22[note 3]	P 34
37H	PoffsetL	R/W	L Line Active Power Offset		P 34
38H	QoffsetL	R/W	L Line Reactive Power Offset	Not applicable to the 90E21/23[note 2]	P 35
39H	PoffsetN	R/W	N Line Active Power Offset	Not applicable to the 90E21/22[note 3]	P 35
3AH	QoffsetN	R/W	N Line Reactive Power Offset	Not applicable to the 90E21/22/23[note 2, note 3]	P 35
3BH	CS2	R/W	Checksum 2		P 36
Energy Register					
40H	APenergy	R/C	Forward Active Energy		P 37

Table-11 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment[note 1]	Page
41H	ANenergy	R/C	Reverse Active Energy		P 37
42H	ATenergy	R/C	Absolute Active Energy		P 38
43H	RPenergy	R/C	Forward (Inductive) Reactive Energy	Not applicable to the 90E21/23[note 2]	P 38
44H	RNenergy	R/C	Reverse (Capacitive) Reactive Energy	Not applicable to the 90E21/23[note 2]	P 39
45H	RTenergy	R/C	Absolute Reactive Energy	Not applicable to the 90E21/23[note 2]	P 39
46H	EnStatus	R	Metering Status	different for various chips[note 2, note 3]	P 40
Measurement Register					
48H	Irms	R	L Line Current rms		P 41
49H	Urms	R	Voltage rms		P 41
4AH	Pmean	R	L Line Mean Active Power		P 42
4BH	Qmean	R	L Line Mean Reactive Power	Not applicable to the 90E21/23[note 2]	P 42
4CH	Freq	R	Voltage Frequency		P 43
4DH	PowerF	R	L Line Power Factor		P 43
4EH	Pangle	R	Phase Angle between Voltage and L Line Current		P 43
4FH	Smean	R	L Line Mean Apparent Power		P 44
68H	Irms2	R	N Line Current rms	Not applicable to the 90E21/22[note 3]	P 44
6AH	Pmean2	R	N Line Mean Active Power	Not applicable to the 90E21/22[note 3]	P 45
6BH	Qmean2	R	N Line Mean Reactive Power	Not applicable to the 90E21/22/23[note 2, note 3]	P 45
6DH	PowerF2	R	N Line Power Factor	Not applicable to the 90E21/22[note 3]	P 46
6EH	Pangle2	R	Phase Angle between Voltage and N Line Current	Not applicable to the 90E21/22[note 3]	P 46
6FH	Smean2	R	N Line Mean Apparent Power	Not applicable to the 90E21/22[note 3]	P 47

Note:
1. This register list shows all registers for the 90E24.
2. This register is related to reactive energy metering. Part of this register is invalid for the 90E21/23 which does not have reactive metering. Reading these registers always return 0000H and writing these registers always take no effect.
3. This register is related to N line metering. Part of this register is invalid for the 90E21/22 which does not have N line metering. Reading these registers always return 0000H and writing these registers always have no effect.

5.2 STATUS AND SPECIAL REGISTER

SoftReset
Software Reset

Address: 00H
Type: Write
Default Value: 0000H

15	14	13	12	11	10	9	8
SoftReset15	SoftReset14	SoftReset13	SoftReset12	SoftReset11	SoftReset10	SoftReset9	SoftReset8
7	6	5	4	3	2	1	0
SoftReset7	SoftReset6	SoftReset5	SoftReset4	SoftReset3	SoftReset2	SoftReset1	SoftReset0

Bit	Name	Description
15 - 0	SoftReset[15:0]	Software reset register. The 90E21/22/23/24 resets if only 789AH is written to this register.

SysStatus
System Status

Address: 01H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
CalErr1	CalErr0	AdjErr1	AdjErr0	-	-	-	-
7	6	5	4	3	2	1	0
LNchange	RevQchg	RevPchg	-	-	-	SagWarn	-

Bit	Name	Description
15 - 14	CalErr[1:0]	These bits indicate CS1 checksum status. 00: CS1 checksum correct (default) 11: CS1 checksum error. At the same time, the WarnOut pin is asserted.
13 - 12	AdjErr[1:0]	These bits indicate CS2 checksum status. 00: CS2 checksum correct (default) 11: CS2 checksum error.
11 - 8	-	Reserved.
7	LNchange	This bit indicates whether there is any change of the metering line (L line and N line). 0: metering line no change (default) 1: metering line changed
6	RevQchq	This bit indicates whether there is any change with the direction of reactive energy. 0: direction of reactive energy no change (default) 1: direction of reactive energy changed This status is enabled by the RevQEn bit(FuncEn, 02H).
5	RevPchg	This bit indicates whether there is any change with the direction of active energy. 0: direction of active energy no change (default) 1: direction of active energy changed This status is enabled by the RevPEn bit (FuncEn, 02H).
4 - 2	-	Reserved.
1	SagWarn	This bit indicates the voltage sag status. 0: no voltage sag (default) 1: voltage sag Voltage sag is enabled by the SagEn bit (FuncEn, 02H). Voltage sag status can also be reported by the WarnOut pin. It is enabled by the SagWo bit(FuncEn, 02H).
0	-	Reserved.

Note: Any of the above events will prompt the IRQ pin to be asserted, which can be supplied to external MCU as an interrupt.

FuncEn
Function Enable

Address: 02H
Type: Read/Write
Default Value: 000CH

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	SagEn	SagWo	RevQEn	RevPEn	-	-

Bit	Name	Description
15 - 6	-	Reserved.
5	SagEn	This bit determines whether to enable the voltage sag interrupt. 0: disable (default) 1: enable
4	SagWo	This bit determines whether to enable voltage sag to be reported by the WarnOut pin. 0: disable (default) 1: enable
3	RevQEn	This bit determines whether to enable the direction change interrupt of reactive energy. 0: disable 1: enable (default)
2	RevPEn	This bit determines whether to enable the direction change interrupt of active energy. 0: disable 1: enable (default)
1 - 0	-	Reserved.

SagTh
Voltage Sag Threshold

Address: 03H
Type: Read/Write
Default Value: 1D6AH

15	14	13	12	11	10	9	8
SagTh15	SagTh14	SagTh13	SagTh12	SagTh11	SagTh10	SagTh9	SagTh8
7	6	5	4	3	2	1	0
SagTh7	SagTh6	SagTh5	SagTh4	SagTh3	SagTh2	SagTh1	SagTh0

Bit	Name	Description
15 - 0	SagTh[15:0]	Voltage sag threshold configuration. Data format is XXX.XX. Unit is V. The power-on value of SagTh is 1D6AH, which is calculated by 22000*sqrt(2)*0.78/(4*Ugain/32768) For details, please refer to IDT application note AN-641.

SmallPMod
Small-Power Mode

Address: 04H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
SmallPMod15	SmallPMod14	SmallPMod13	SmallPMod12	SmallPMod11	SmallPMod10	SmallPMod9	SmallPMod8
7	6	5	4	3	2	1	0
SmallPMod7	SmallPMod6	SmallPMod5	SmallPMod4	SmallPMod3	SmallPMod2	SmallPMod1	SmallPMod0

Bit	Name	Description
15 - 0	SmallPMod[15:0]	Small-power mode command. A987H: small-power mode. The relationship between the register value of L line and N line active/reactive power in small-power mode and normal mode is: power in normal mode = power in small-power mode *10*Igain*Ugain /2^42 Others: Normal mode. Small-power mode is mainly used in the power offset calibration.

LastSPIData
Last Read/Write SPI Value

Address: 06H
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
LastSPIData15	LastSPIData14	LastSPIData13	LastSPIData12	LastSPIData11	LastSPIData10	LastSPIData9	LastSPIData8
7	6	5	4	3	2	1	0
LastSPIData7	LastSPIData6	LastSPIData5	LastSPIData4	LastSPIData3	LastSPIData2	LastSPIData1	LastSPIData0

Bit	Name	Description
15 - 0	LastSPI-Data[15:0]	This register stores the data that is just read or written through the SPI interface. Refer to Table-9 and Table-10.

5.3 METERING/ MEASUREMENT CALIBRATION AND CONFIGURATION

5.3.1 METERING CALIBRATION AND CONFIGURATION REGISTER

CalStart
Calibration Start Command

Address: 20H
Type: Read/Write
Default Value: 6886H

15	14	13	12	11	10	9	8
CalStart15	CalStart14	CalStart13	CalStart12	CalStart11	CalStart10	CalStart9	CalStart8
7	6	5	4	3	2	1	0
CalStart7	CalStart6	CalStart5	CalStart4	CalStart3	CalStart2	CalStart1	CalStart0

Bit	Name	Description
15 - 0	CalStart[15:0]	Metering calibration start command: 6886H: Power-on value. Metering function is disabled. 5678H: Metering calibration startup command. After 5678H is written to this register, registers 21H-2BH resume to their power-on values. The 90E21/22/23/24 starts to meter and output energy pulses regardless of the correctness of diagnosis. The CalErr[1:0] bits (SysStatus, 01H) are not set and the WarnOut/IRQ pins do not report any warning/interrupt. 8765H: Check the correctness of the 21H-2BH registers. If correct, normal metering. If not correct, metering function is disabled, the CalErr[1:0] bits (SysStatus, 01H) are set and the WarnOut/IRQ pins report warning/interrupt. Others: Metering function is disabled. The CalErr[1:0] bits (SysStatus, 01H) are set and the WarnOut/IRQ pins report warning/interrupt.

PLconstH
High Word of PL_Constant

Address: 21H
Type: Read/Write
Default Value: 0015H

15	14	13	12	11	10	9	8
PLconstH15	PLconstH14	PLconstH13	PLconstH12	PLconstH11	PLconstH10	PLconstH9	PLconstH8
7	6	5	4	3	2	1	0
PLconstH7	PLconstH6	PLconstH5	PLconstH4	PLconstH3	PLconstH2	PLconstH1	PLconstH0

Bit	Name	Description
15 - 0	PLconstH[15:0]	The PLconstH[15:0] and PLconstL[15:0] bits are high word and low word of PL_Constant respectively. PL_Constant is a constant which is proportional to the sampling ratios of voltage and current, and inversely proportional to the Meter Constant. PL_Constant is a threshold for energy calculated inside the chip, i.e., energy larger than PL_Constant will be accumulated in the corresponding energy registers and then output on CFx. It is suggested to set PL_constant as a multiple of 4 so as to double or redouble Meter Constant in low current state to save verification time. Note: PLconstH takes effect after PLconstL are configured. For details, please refer to IDT application note AN-641.

PLconstL
Low Word of PL_Constant

Address: 22H
Type: Read/Write
Default Value: D174H

15	14	13	12	11	10	9	8
PLconstL15	PLconstL14	PLconstL13	PLconstL12	PLconstL11	PLconstL10	PLconstL9	PLconstL8
7	6	5	4	3	2	1	0
PLconstL7	PLconstL6	PLconstL5	PLconstL4	PLconstL3	PLconstL2	PLconstL1	PLconstL0

Bit	Name	Description
15 - 0	PLconstL[15:0]	The PLconstH[15:0] and PLconstL[15:0] bits are high word and low word of PL_Constant respectively. It is suggested to set PL_constant as a multiple of 4. For details, please refer to IDT application note AN-641.

Lgain
L Line Calibration Gain

Address: 23H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
Lgain15	Lgain14	Lgain13	Lgain12	Lgain11	Lgain10	Lgain9	Lgain8
7	6	5	4	3	2	1	0
Lgain7	Lgain6	Lgain5	Lgain4	Lgain3	Lgain2	Lgain1	Lgain0

Bit	Name	Description
15 - 0	Lgain[15:0]	L line calibration gain. For details, please refer to IDT application note AN-641.

Lphi
L Line Calibration Angle

Address: 24H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
Lphi15	-	-	-	-	-	Lphi9	Lphi8
7	6	5	4	3	2	1	0
Lphi7	Lphi6	Lphi5	Lphi4	Lphi3	Lphi2	Lphi1	Lphi0

Bit	Name	Description
15 - 0	Lphi[15:0]	L line calibration phase angle. For details, please refer to IDT application note AN-641.

Ngain
N Line Calibration Gain

Address: 25H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
Ngain15	Ngain14	Ngain13	Ngain12	Ngain11	Ngain10	Ngain9	Ngain8
7	6	5	4	3	2	1	0
Ngain7	Ngain6	Ngain5	Ngain4	Ngain3	Ngain2	Ngain1	Ngain0

Bit	Name	Description
15 - 0	Ngain[15:0]	N line calibration gain. For details, please refer to IDT application note AN-641.

Nphi
N Line Calibration Angle

Address: 26H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
Nphi15	-	-	-	-	-	Nphi9	Nphi8
7	6	5	4	3	2	1	0
Nphi7	Nphi6	Nphi5	Nphi4	Nphi3	Nphi2	Nphi1	Nphi0

Bit	Name	Description
15 - 0	Nphi[15:0]	N line calibration phase angle. For details, please refer to IDT application note AN-641.

PStartTh
Active Startup Power Threshold

Address: 27H
Type: Read/Write
Default Value: 08BDH

15	14	13	12	11	10	9	8
PStartTh15	PStartTh14	PStartTh13	PStartTh12	PStartTh11	PStartTh10	PStartTh9	PStartTh8
7	6	5	4	3	2	1	0
PStartTh7	PStartTh6	PStartTh5	PStartTh4	PStartTh3	PStartTh2	PStartTh1	PStartTh0

Bit	Name	Description
15 - 0	PStartTh[15:0]	Active startup power threshold. For details, please refer to IDT application note AN-641.

PNolTh
Active No-Load Power Threshold

Address: 28H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
PNolTh15	PNolTh14	PNolTh13	PNolTh12	PNolTh11	PNolTh10	PNolTh9	PNolTh8
7	6	5	4	3	2	1	0
PNolTh7	PNolTh6	PNolTh5	PNolTh4	PNolTh3	PNolTh2	PNolTh1	PNolTh0

Bit	Name	Description
15 - 0	PNolTh[15:0]	Active no-load power threshold. For details, please refer to IDT application note AN-641.

QStartTh
Reactive Startup Power Threshold

Address: 29H
Type: Read/Write
Default Value: 0AECH

15	14	13	12	11	10	9	8
QStartTh15	QStartTh14	QStartTh13	QStartTh12	QStartTh11	QStartTh10	QStartTh9	QStartTh8
7	6	5	4	3	2	1	0
QStartTh7	QStartTh6	QStartTh5	QStartTh4	QStartTh3	QStartTh2	QStartTh1	QStartTh0

Bit	Name	Description
15 - 0	QStartTh[15:0]	Reactive startup power threshold. For details, please refer to IDT application note AN-641.

QNolTh
Reactive No-Load Power Threshold

Address: 2AH
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
QNolTh15	QNolTh14	QNolTh13	QNolTh12	QNolTh11	QNolTh10	QNolTh9	QNolTh8
7	6	5	4	3	2	1	0
QNolTh7	QNolTh6	QNolTh5	QNolTh4	QNolTh3	QNolTh2	QNolTh1	QNolTh0

Bit	Name	Description
15 - 0	QNolTh[15:0]	Reactive no-load power threshold. For details, please refer to IDT application note AN-641.

MMode
Metering Mode Configuration

Address: 2BH
Type: Read/Write
Default Value: 9422H

15	14	13	12	11	10	9	8
Lgain2	Lgain1	Lgain0	Ngain1	Ngain0	LNSel	DisHPF1	DisHPF0
7	6	5	4	3	2	1	0
Amod	Rmod	ZXCon1	ZXCon0	Pthresh3	Pthresh2	Pthresh1	Pthresh0

Bit	Name	Description
15 - 13	Lgain[2:0]	L line current gain, default value is '100'. Lgain2 / Lgain1 / Lgain0 / Current Channel Gain 1 / X / X / 1 0 / 0 / 0 / 4 0 / 0 / 1 / 8 0 / 1 / 0 / 16 0 / 1 / 1 / 24
12 - 11	Ngain[1:0]	N line current gain 00: 2 01: 4 10: 1 (default) 11: 1
10	LNSel	This bit specifies metering as L line or N line when metering mode is set to flexible mode by MMD1 and MMD0 pins. 0: N line 1: L line (default)
9 - 8	DisHPF[1:0]	These bits configure the High Filter Pass (HPF) after ADC. There are two first-order HPF in serial: HPF1 and HPF0. The configuration are applicable to all channels: DisHPF1 / DisHPF 0 / HPF Configuration 0 / 0 / enable HPF1 and HPF0 (default) 0 / 1 / enable HPF1, disable HPF0; 1 / 0 / disable HPF1, enable HPF0; 1 / 1 / disable HPF1 and HPF0
7	Amod	CF1 output for active power: 0: forward or reverse energy pulse output (default) 1: absolute energy pulse output
6	Rmod	CF2 output for reactive power: 0: forward (inductive) or reverse (capacitive) energy pulse output (default) 1: absolute energy pulse output

<table>
<tr><td>5 - 4</td><td>Zxcon[1:0]</td><td>These bits configure zero-crossing mode. The ZX pin outputs 5ms-width high level when voltage crosses zero.
00: positive zero-crossing
01: negative zero-crossing
10: all zero-crossing: both positive and negative zero-crossing (default)
11: no zero-crossing output</td></tr>
<tr><td>3 - 0</td><td>Pthresh[3:0]</td><td>These bits configure the L line and N line power difference threshold in anti-tampering mode.
<table>
<tr><th>Pthresh3</th><th>Pthresh2</th><th>Pthresh1</th><th>Pthresh0</th><th>Threshold</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>12.5%</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>6.25%</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>3.125% (default)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1.5625%</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1%</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>2%</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3%</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>4%</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5%</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>6%</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>7%</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8%</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>9%</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>10%</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>11%</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>12%</td></tr>
</table>
</td></tr>
</table>

CS1
Checksum 1

Address: 2CH
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
CS1_15	CS1_14	CS1_13	CS1_12	CS1_11	CS1_10	CS1_9	CS1_8
7	6	5	4	3	2	1	0
CS1_7	CS1_6	CS1_5	CS1_4	CS1_3	CS1_2	CS1_1	CS1_0

Bit	Name	Description
15 - 0	CS1[15:0]	The CS1 register should be written after the 21H-2BH registers are written. Suppose the high byte and the low byte of the 21H-2BH registers are shown in below table.

Register Address	High Byte	Low Byte
21H	H_{21}	L_{21}
22H	H_{22}	L_{22}
23H	H_{23}	L_{23}
24H	H_{24}	L_{24}
25H	H_{25}	L_{25}
26H	H_{26}	L_{26}
27H	H_{27}	L_{27}
28H	H_{28}	L_{28}
29H	H_{29}	L_{29}
2AH	H_{2A}	L_{2A}
2BH	H_{2B}	L_{2B}

The calculatiion of the CS1 register is as follows:

The low byte of 2CH register is: $\mathbf{L_{2C}}$=MOD($\mathbf{H_{21}}$+$\mathbf{H_{22}}$+...+$\mathbf{H_{2B}}$+$\mathbf{L_{21}}$+$\mathbf{L_{22}}$+...+$\mathbf{L_{2B}}$, 2^8)
The high byte of 2CH register is: $\mathbf{H_{2C}}$=$\mathbf{H_{21}}$ XOR $\mathbf{H_{22}}$ XOR ... XOR $\mathbf{H_{2B}}$ XOR $\mathbf{L_{21}}$ XOR $\mathbf{L_{22}}$ XOR ... XOR $\mathbf{L_{2B}}$
For 90E21/22/23, a part of registers are not used. These registers can be dealed as 0000H in CS calculation.

The 90E21/22/23/24 calculates CS1 regularly. If the value of the CS1 register and the calculation by the 90E21/22/23/24 is different when CalStart=8765H, the CalErr[1:0] bits (SysStatus, 01H) are set and the WarnOut and IRQ pins are asserted.
Note: The readout value of the CS1 register is the calculation by the 90E21/22/23/24, which is different from what is written.

5.3.2 MEASUREMENT CALIBRATION REGISTER

AdjStart
Measurement Calibration Start Command

Address: 30H
Type: Read/Write
Default Value: 6886H

15	14	13	12	11	10	9	8
AdjStart15	AdjStart14	AdjStart13	AdjStart12	AdjStart11	AdjStart10	AdjStart9	AdjStart8
7	6	5	4	3	2	1	0
AdjStart7	AdjStart6	AdjStart5	AdjStart4	AdjStart3	AdjStart2	AdjStart1	AdjStart0

Bit	Name	Description
15 - 0	AdjStart[15:0]	Measurement Calibration Start Command 6886H: Power-on value. No measurement. 5678H: Measurement calibration startup command. After 5678H is written to this register, registers 31H-3AH resume to their power-on values. The 90E21/22/23/24 starts to measure regardless of the correctness of diagnosis. The AdjErr[1:0] bits (SysStatus, 01H) are not set and the IRQ pin does not report any interrupt. 8765H: Check the correctness of the 31H-3AH registers. If correct, normal measurement. If not correct, measurement function is disabled, the AdjErr[1:0] bits (SysStatus, 01H) are set and the IRQ pin reports interrupt. Others: No measurement. The AdjErr[1:0] bits (SysStatus, 01H) are set and the IRQ pin reports interrupt.

Ugain
Voltage rms Gain

Address: 31H
Type: Read/Write
Default Value: 6720H

15	14	13	12	11	10	9	8
Ugain15	Ugain14	Ugain13	Ugain12	Ugain11	Ugain10	Ugain9	Ugain8
7	6	5	4	3	2	1	0
Ugain7	Ugain6	Ugain5	Ugain4	Ugain3	Ugain2	Ugain1	Ugain0

Bit	Name	Description
15 - 0	Ugain[15:0]	Voltage rms Gain. For details, please refer to IDT application note AN-641. **Note:** the Ugain15 bit should only be '0'

IgainL
L Line Current rms Gain

Address: 32H
Type: Read/Write
Default Value: 7A13H

15	14	13	12	11	10	9	8
IgainL15	IgainL14	IgainL13	IgainL12	IgainL11	IgainL10	IgainL9	IgainL8
7	6	5	4	3	2	1	0
IgainL7	IgainL6	IgainL5	IgainL4	IgainL3	IgainL2	IgainL1	IgainL0

Bit	Name	Description
15 - 0	IgainL[15:0]	L Line Current rms Gain, For details, please refer to IDT application note AN-641.

IgainN
N Line Current rms Gain

Address: 33H
Type: Read/Write
Default Value: 7530H

15	14	13	12	11	10	9	8
IgainN15	IgainN14	IgainN13	IgainN12	IgainN11	IgainN10	IgainN9	IgainN8
7	6	5	4	3	2	1	0
IgainN7	IgainN6	IgainN5	IgainN4	IgainN3	IgainN2	IgainN1	IgainN0

Bit	Name	Description
15 - 0	IgainN[15:0]	N Line Current rms Gain. For details, please refer to IDT application note AN-641.

Uoffset
Voltage Offset

Address: 34H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
Uoffset15	Uoffset14	Uoffset13	Uoffset12	Uoffset11	Uoffset10	Uoffset9	Uoffset8
7	6	5	4	3	2	1	0
Uoffset7	Uoffset6	Uoffset5	Uoffset4	Uoffset3	Uoffset2	Uoffset1	Uoffset0

Bit	Name	Description
15 - 0	Uoffset[15:0]	Voltage offset. For calculation method, please refer to IDT application note AN-641.

IoffsetL
L Line Current Offset

Address: 35H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
IoffsetL15	IoffsetL14	IoffsetL13	IoffsetL12	IoffsetL11	IoffsetL10	IoffsetL9	IoffsetL8
7	6	5	4	3	2	1	0
IoffsetL7	IoffsetL6	IoffsetL5	IoffsetL4	IoffsetL3	IoffsetL2	IoffsetL1	IoffsetL0

Bit	Name	Description
15 - 0	IoffsetL[15:0]	L line current offset. For calculation method, please refer to IDT application note AN-641.

IoffsetN
N Line Current Offset

Address: 36H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
IoffsetN15	IoffsetN14	IoffsetN13	IoffsetN12	IoffsetN11	IoffsetN10	IoffsetN9	IoffsetN8
7	6	5	4	3	2	1	0
IoffsetN7	IoffsetN6	IoffsetN5	IoffsetN4	IoffsetN3	IoffsetN2	IoffsetN1	IoffsetN0

Bit	Name	Description
15 - 0	IoffsetN[15:0]	N line current offset. For calculation method, please refer to IDT application note AN-641.

PoffsetL
L Line Active Power Offset

Address: 37H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
PoffsetL15	PoffsetL14	PoffsetL13	PoffsetL12	PoffsetL11	PoffsetL10	PoffsetL9	PoffsetL8
7	6	5	4	3	2	1	0
PoffsetL7	PoffsetL6	PoffsetL5	PoffsetL4	PoffsetL3	PoffsetL2	PoffsetL1	PoffsetL0

Bit	Name	Description
15 - 0	PoffsetL[15:0]	L line active power offset. Complement, MSB is the sign bit. For calculation method, please refer to IDT application note AN-641.

QoffsetL
L Line Reactive Power Offset

Address: 38H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
QoffsetL15	QoffsetL14	QoffsetL13	QoffsetL12	QoffsetL11	QoffsetL10	QoffsetL9	QoffsetL8
7	6	5	4	3	2	1	0
QoffsetL7	QoffsetL6	QoffsetL5	QoffsetL4	QoffsetL3	QoffsetL2	QoffsetL1	QoffsetL0

Bit	Name	Description
15 - 0	QoffsetL[15:0]	L line reactive power offset. Complement, MSB is the sign bit. For calculation method, please refer to IDT application note AN-641.

PoffsetN
N Line Active Power Offset

Address: 39H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
PoffsetN15	PoffsetN14	PoffsetN13	PoffsetN12	PoffsetN11	PoffsetN10	PoffsetN9	PoffsetN8
7	6	5	4	3	2	1	0
PoffsetN7	PoffsetN6	PoffsetN5	PoffsetN4	PoffsetN3	PoffsetN2	PoffsetN1	PoffsetN0

Bit	Name	Description
15 - 0	PoffsetN[15:0]	N line active power offset. Complement, MSB is the sign bit. For calculation method, please refer to IDT application note AN-641.

QoffsetN
N Line Reactive Power Offset

Address: 3AH
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
QoffsetN15	QoffsetN14	QoffsetN13	QoffsetN12	QoffsetN11	QoffsetN10	QoffsetN9	QoffsetN8
7	6	5	4	3	2	1	0
QoffsetN7	QoffsetN6	QoffsetN5	QoffsetN4	QoffsetN3	QoffsetN2	QoffsetN1	QoffsetN0

Bit	Name	Description
15 - 0	QoffsetN[15:0]	N line reactive power offset. Complement, MSB is the sign bit. For calculation method, please refer to IDT application note AN-641.

CS2
Checksum 2

Address: 3BH
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
CS2_15	CS2_14	CS2_13	CS2_12	CS2_11	CS2_10	CS2_9	CS2_8
7	6	5	4	3	2	1	0
CS2_7	CS2_6	CS2_5	CS2_4	CS2_3	CS2_2	CS2_1	CS2_0

Bit	Name	Description
15 - 0	CS2[15:0]	The CS2 register should be written after the 31H-3AH registers are written. Suppose the high byte and the low byte of the 31H-3AH registers are shown in below table.

Register Address	High Byte	Low Byte
31H	H_{31}	L_{31}
32H	H_{32}	L_{32}
33H	H_{33}	L_{33}
34H	H_{34}	L_{34}
35H	H_{35}	L_{35}
36H	H_{36}	L_{36}
37H	H_{37}	L_{37}
38H	H_{38}	L_{38}
39H	H_{39}	L_{39}
3AH	H_{3A}	L_{3A}

The calculatiion of the CS2 register is as follows:

The low byte of 3BH register is: $\mathbf{L_{3B}}$=MOD($\mathbf{H_{31}}$+$\mathbf{H_{32}}$+...+$\mathbf{H_{3A}}$+$\mathbf{L_{31}}$+$\mathbf{L_{32}}$+...+$\mathbf{L_{3A}}$, 2^8)
The high byte of 3BH register is: $\mathbf{H_{3B}}$=$\mathbf{H_{31}}$ XOR $\mathbf{H_{32}}$ XOR ... XOR $\mathbf{H_{3A}}$ XOR $\mathbf{L_{31}}$ XOR $\mathbf{L_{32}}$ XOR ... XOR $\mathbf{L_{3A}}$
For 90E21/22/23, a part of registers are not used. These registers can be dealed as 0000H in CS calculation.

The 90E21/22/23/24 calculates CS2 regularly. If the value of the CS2 register and the calculation by the 90E21/22/23/24 is different when AdjStart=8765H, the AdjErr[1:0] bits (SysStatus, 01H) are set.
Note: The readout value of the CS2 register is the calculation by the 90E21/22/23/24, which is different from what is written.

5.4 ENERGY REGISTER

Theory of Energy Registers

The internal energy resolution is 0.01 pulse. Within 0.01 pulse, forward and reverse energy are counteracted. When energy exceeds 0.01 pulse, the respective forward/reserve energy is increased. The forward and reverse energy are not counteracted in absolute energy registers. Take the example of active energy, suppose:

T0: Forward energy is 12.34 pulses and reverse energy is 1.23 pulses;

From T0 to T1: 0.005 forward pulse appeared

From T1 to T2: 0.004 reverse pulse appeared

From T2 to T3: 0.003 reverse pulse appeared

	T0	T1	T2	T3
Forward Active Pulse	12.34	12.345	12.341	12.34
Reserve Active Pulse	1.23	1.23	1.23	1.232
Absolute Active Pulse	13.57	13.575	13.579	13.582

When forward/reverse energy or absolute energy reaches 0.1 pulse, the respective register is updated. When forward/reverse energy or absolute energy reaches 1 pulse, CFx pins output pulse and the REVP/REVQ bits (EnStatus, 46H) are updated.

Absolute energy might be more than the sum of forward and reverse energies. If "consistency" is required between absolute energy and forward/reverse energy in system application, absolute energy can be obtained by calculating the readout of the forward and reverse energy registers.

APenergy
Forward Active Energy

Address: 40H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
APenergy15	APenergy14	APenergy13	APenergy12	APenergy11	APenergy10	APenergy9	APenergy8
7	6	5	4	3	2	1	0
APenergy7	APenergy6	APenergy5	APenergy4	APenergy3	APenergy2	APenergy1	APenergy0

Bit	Name	Description
15 - 0	APenergy[15:0]	Forward active energy; cleared after read. Data format is XXXX.X pulses. Resolution is 0.1 pulse. Maximum is 6553.5 pulses. When the accumulation of this register has achieved FFFFH, the continuation accumulation will return to 0000H.

ANenergy
Reverse Active Energy

Address: 41H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
ANenergy15	ANenergy14	ANenergy13	ANenergy12	ANenergy11	ANenergy10	ANenergy9	ANenergy8
7	6	5	4	3	2	1	0
ANenergy7	ANenergy6	ANenergy5	ANenergy4	ANenergy3	ANenergy2	ANenergy1	ANenergy0

Bit	Name	Description
15 - 0	ANenergy[15:0]	Reverse active energy, cleared after read. Data format is XXXX.X pulses. Resolution is 0.1 pulse. Maximum is 6553.5 pulses. When the accumulation of this register has achieved FFFFH, the continuation accumulation will return to 0000H.

ATenergy
Absolute Active Energy

Address: 42H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
ATenergy15	ATenergy14	ATenergy13	ATenergy12	ATenergy11	ATenergy10	ATenergy9	ATenergy8
7	6	5	4	3	2	1	0
ATenergy7	ATenergy6	ATenergy5	ATenergy4	ATenergy3	ATenergy2	ATenergy1	ATenergy0

Bit	Name	Description
15 - 0	ATenergy[15:0]	Absolute active energy, cleared after read. Data format is XXXX.X pulses. Resolution is 0.1 pulse. Maximum is 6553.5 pulses. When the accumulation of this register has achieved FFFFH, the continuation accumulation will return to 0000H.

RPenergy
Forward (Inductive) Reactive Energy

Address: 43H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
RPenergy15	RPenergy14	RPenergy13	RPenergy12	RPenergy11	RPenergy10	RPenergy9	RPenergy8
7	6	5	4	3	2	1	0
RPenergy7	RPenergy6	RPenergy5	RPenergy4	RPenergy3	RPenergy2	RPenergy1	RPenergy0

Bit	Name	Description
15 - 0	RPenergy[15:0]	Forward (inductive) reactive energy, cleared after read. Data format is XXXX.X pulses. Resolution is 0.1 pulse. Maximum is 6553.5 pulses. When the accumulation of this register has achieved FFFFH, the continuation accumulation will return to 0000H.

RNenergy
Reverse (Capacitive) Reactive Energy

Address: 44H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
RNenergy15	RNenergy14	RNenergy13	RNenergy12	RNenergy11	RNenergy10	RNenergy9	RNenergy8
7	6	5	4	3	2	1	0
RNenergy7	RNenergy6	RNenergy5	RNenergy4	RNenergy3	RNenergy2	RNenergy1	RNenergy0

Bit	Name	Description
15 - 0	RNenergy[15:0]	Reverse (capacitive) reactive energy, cleared after read. Data format is XXXX.X pulses. Resolution is 0.1 pulse. Maximum is 6553.5 pulses. When the accumulation of this register has achieved FFFFH, the continuation accumulation will return to 0000H.

RTenergy
Absolute Reactive Energy

Address: 45H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
RTenergy15	RTenergy14	RTenergy13	RTenergy12	RTenergy11	RTenergy10	RTenergy9	RTenergy8
7	6	5	4	3	2	1	0
RTenergy7	RTenergy6	RTenergy5	RTenergy4	RTenergy3	RTenergy2	RTenergy1	RTenergy0

Bit	Name	Description
15 - 0	RTenergy[15:0]	Absolute reactive energy, cleared after read. Data format is XXXX.X pulses. Resolution is 0.1 pulse. Maximum is 6553.5 pulses. When the accumulation of this register has achieved FFFFH, the continuation accumulation will return to 0000H.

EnStatus
Metering Status

Address: 46H
Type: Read
Default Value After Power On: C800H

15	14	13	12	11	10	9	8
Qnoload	Pnoload	RevQ	RevP	Lline	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	LNMode1	LNMode0

Bit	Name	Description
15	Qnoload	This bit indicates whether the chip is in reactive no-load status. 0: not reactive no-load state 1: reactive no-load state
14	Pnoload	This bit indicates whether the 90E21/22/23/24 is in active no-load status. 0: not active no-load state 1: active no-load state
13	RevQ	This bit indicates the direction of the last CF2 (reactive output). 0: reactive forward 1: reactive reverse **Note:** This bit is always '0' when the CF2 output is configured to be absolute energy.
12	RevP	This bit indicates the direction of the last CF1 (active output). 0: active forward 1: active reverse **Note:** This bit is always '0' when the CF1 output is configured to be absolute energy.
11	Lline	This bit indicates the current metering line in anti-tampering mode. 0: N line 1: L line
10 - 2	-	Reserved.
1 - 0	LNMode[1:0]	These bits indicate the configuration of MMD1 and MMD0 pins. Their relationship is as follows:

MMD1	MMD0	LNmod1	LNmod0	L/N Metering Mode
0	0	0	0	anti-tampering mode (larger power)
0	1	0	1	L line mode (fixed L line)
1	0	1	0	L+N mode (applicable for single-phase three-wire system)
1	1	1	1	Flexible mode (Line specified by the LNSel bit (MMode, 2BH))

5.5 MEASUREMENT REGISTER

Irms
L Line Current rms

Address: 48H
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Irms15	Irms14	Irms13	Irms12	Irms11	Irms10	Irms9	Irms8
7	6	5	4	3	2	1	0
Irms7	Irms6	Irms5	Irms4	Irms3	Irms2	Irms1	Irms0

Bit	Name	Description
15 - 0	Irms[15:0]	L line current rms. Data format is XX.XXX, which corresponds to 0 ~ 65.535A. For cases when the current exceeds 65.535A, it is suggested to be handled by MCU in application. For example, the register value can be calibrated to 1/2 of the actual value during calibration, then multiplied by 2 in application.

Urms
Voltage rms

Address: 49H
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Urms15	Urms14	Urms13	Urms12	Urms11	Urms10	Urms9	Urms8
7	6	5	4	3	2	1	0
Urms7	Urms6	Urms5	Urms4	Urms3	Urms2	Urms1	Urms0

Bit	Name	Description
15 - 0	Urms[15:0]	Voltage rms. Data format is XXX.XX, which corresponds to 0 ~ 655.35V.

Pmean
L Line Mean Active Power

Address: 4AH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Pmean15	Pmean14	Pmean13	Pmean12	Pmean11	Pmean10	Pmean9	Pmean8
7	6	5	4	3	2	1	0
Pmean7	Pmean6	Pmean5	Pmean4	Pmean3	Pmean2	Pmean1	Pmean0

Bit	Name	Description
15 - 0	Pmean[15:0]	L line mean active power. Complement, MSB is the sign bit. Data format is XX.XXX, which corresponds to -32.768~+32.768kW. If current is specially handle by MCU, the power of the 90E21/22/23/24 and the actual power have the same multiple relationship as the current.

Qmean
L Line Mean Reactive Power

Address: 4BH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Qmean15	Qmean14	Qmean13	Qmean12	Qmean11	Qmean10	Qmean9	Qmean8
7	6	5	4	3	2	1	0
Qmean7	Qmean6	Qmean5	Qmean4	Qmean3	Qmean2	Qmean1	Qmean0

Bit	Name	Description
15 - 0	Qmean[15:0]	L line mean reactive power. Complement, MSB is the sign bit. Data format is XX.XXX, which corresponds to -32.768~+32.768kvar. If current is specially handled by MCU, the power of the 90E22/24 and the actual power have the same multiple relationship as the current.

Freq
Voltage Frequency

Address: 4CH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Freq15	Freq14	Freq13	Freq12	Freq11	Freq10	Freq9	Freq8
7	6	5	4	3	2	1	0
Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0

Bit	Name	Description
15 - 0	Freq[15:0]	Voltage frequency. Data format is XX.XX. Frequency measurement range is 45.00~65.00Hz. For example, 1388H corresponds to 50.00Hz.

PowerF
L Line Power Factor

Address: 4DH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
PowerF15	PowerF14	PowerF13	PowerF12	PowerF11	PowerF10	PowerF9	PowerF8
7	6	5	4	3	2	1	0
PowerF7	PowerF6	PowerF5	PowerF4	PowerF3	PowerF2	PowerF1	PowerF0

Bit	Name	Description
15 - 0	PowerF[15:0]	L line power factor. Signed, MSB is the sign bit. Data format is X.XXX. Power factor range: -1.000~+1.000. For example, 03E8H corresponds to the power factor of 1.000, and 83E8H corresponds to the power factor of -1.000.

Pangle
Phase Angle between Voltage and L Line Current

Address: 4EH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Pangle15	Pangle14	Pangle13	Pangle12	Pangle11	Pangle10	Pangle9	Pangle8
7	6	5	4	3	2	1	0
Pangle7	Pangle6	Pangle5	Pangle4	Pangle3	Pangle2	Pangle1	Pangle0

Bit	Name	Description
15 - 0	Pangle[15:0]	L line voltage current angle. Signed, MSB is the sign bit. Data format is XXX.X. Angle range: -180.0~+180.0 degree.

Smean
L Line Mean Apparent Power

Address: 4FH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Smean15	Smean14	Smean13	Smean12	Smean11	Smean10	Smean9	Smean8
7	6	5	4	3	2	1	0
Smean7	Smean6	Smean5	Smean4	Smean3	Smean2	Smean1	Smean0

Bit	Name	Description
15 - 0	Smean[15:0]	L line mean apparent power. Complement, MSB is always '0'. Data format is XX.XXX, which corresponds to 0~+32.767kVA. If current is specially handled by MCU, the power of the 90E21/22/23/24 and the actual power have the same multiple relationship as the current.

Irms2
N Line Current rms

Address: 68H
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Irms2_15	Irms2_14	Irms2_13	Irms2_12	Irms2_11	Irms2_10	Irms2_9	Irms2_8
7	6	5	4	3	2	1	0
Irms2_7	Irms2_6	Irms2_5	Irms2_4	Irms2_3	Irms2_2	Irms2_1	Irms2_0

Bit	Name	Description
15 - 0	Irms2[15:0]	N line current rms. Data format is XX.XXX, which corresponds to 65.535A. For cases when the current exceeds 65.535A, it is suggested to be handled by MCU in application. For example, the register value can be calibrated to 1/2 of the actual value during calibration, then multiplied by 2 in application.

Pmean2
N Line Mean Active Power

Address: 6AH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Pmean2_15	Pmean2_14	Pmean2_13	Pmean2_12	Pmean2_11	Pmean2_10	Pmean2_9	Pmean2_8
7	6	5	4	3	2	1	0
Pmean2_7	Pmean2_6	Pmean2_5	Pmean2_4	Pmean2_3	Pmean2_2	Pmean2_1	Pmean2_0

Bit	Name	Description
15 - 0	Pmean2[15:0]	N line mean active power. Complement, MSB is the sign bit. Data format is XX.XXX, which corresponds to -32.768~+32.767kW. If current is specially handled by MCU, the power of the 90E21/22/23/24 and the actual power have the same multiple relationship as the current.

Qmean2
N Line Mean Reactive Power

Address: 6BH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Qmean2_15	Qmean2_14	Qmean2_13	Qmean2_12	Qmean2_11	Qmean2_10	Qmean2_9	Qmean2_8
7	6	5	4	3	2	1	0
Qmean2_7	Qmean2_6	Qmean2_5	Qmean2_4	Qmean2_3	Qmean2_2	Qmean2_1	Qmean2_0

Bit	Name	Description
15 - 0	Qmean2[15:0]	N line mean reactive power. Complement, MSB is the sign bit. Data format is XX.XXX, which corresponds to -32.768~+32.767kvar. If current is specially handled by MCU, the power of 90E22/24 and the actual power have the same multiple relationship as the current.

PowerF2
N Line Power Factor

Address: 6DH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
PowerF2_15	PowerF2_14	PowerF2_13	PowerF2_12	PowerF2_11	PowerF2_10	PowerF2_9	PowerF2_8
7	6	5	4	3	2	1	0
PowerF2_7	PowerF2_6	PowerF2_5	PowerF2_4	PowerF2_3	PowerF2_2	PowerF2_1	PowerF2_0

Bit	Name	Description
15 - 0	PowerF2[15:0]	N line power factor. Signed, MSB is the sign bit. Data format is X.XXX. Power factor range: -1.000~+1.000. For example, 03E8H corresponds to the power factor of 1.000, and 83E8H corresponds to the power factor of -1.000.

Pangle2
Phase Angle between Voltage and N Line Current

Address: 6EH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Pangle2_15	Pangle2_14	Pangle2_13	Pangle2_12	Pangle2_11	Pangle2_10	Pangle2_9	Pangle2_8
7	6	5	4	3	2	1	0
Pangle2_7	Pangle2_6	Pangle2_5	Pangle2_4	Pangle2_3	Pangle2_2	Pangle2_1	Pangle2_0

Bit	Name	Description
15 - 0	Pangle2[15:0]	N line voltage current angle Signed, MSB is the sign bit. Data format is XXX.X. Angle range: -180.0~+180.0 degree.

Smean2
N Line Mean Apparent Power

Address: 6FH
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
Smean2_15	Smean2_14	Smean2_13	Smean2_12	Smean2_11	Smean2_10	Smean2_9	Smean2_8
7	6	5	4	3	2	1	0
Smean2_7	Smean2_6	Smean2_5	Smean2_4	Smean2_3	Smean2_2	Smean2_1	Smean2_0

Bit	Name	Description
15 - 0	Smean2[15:0]	N line mean apparent power Complement, MSB is always '0'. Data format is XX.XXX, which corresponds to 0~+32.767kVA. If current is specially handled by MCU, the power of 90E21/22/23/24 and the actual power have the same multiple relationship as the current.

6 ELECTRICAL SPECIFICATION

6.1 ELECTRICAL SPECIFICATION

Parameters and Description	Min.	Typical	Max.	Unit	Test Conditions and Comments
Accuracy					
DC Power Supply Rejection Ratio (PSRR)			±0.1	%	VDD=3.3V±0.3V, 100Hz, I=5A, V=220V, L line shunt resistor 150μΩ, N line CT 1000:1, sampling resistor 4.8Ω
AC Power Supply Rejection Ratio (PSRR)			±0.1	%	VDD=3.3V superimposes 400mVrms, 100Hz Sinusoidal signal, I=5A, V=220V, L line shunt resistor 150μΩ, N line CT 1000:1, sampling resistor 4.8Ω
Active Energy Error (Dynamic Range 5000:1)			±0.1	%	L line current gain is '24'; N line current gain is '1'
Channel Characteristics					
Sampling Frequency		8		kHz	
L Line Current Channel Equivalent Input Noise			19.1	nV/√Hz	Single side band noise (measured at 50Hz, and PGA gain is '24')
N Line Current Channel Equivalent Input Noise			458.4	nV/√Hz	Single side band noise (measured at 50Hz, and PGA gain is '1')
Voltage Channel Equivalent Input Noise			458.4	nV/√Hz	Single side band noise (measured at 50Hz, and PGA gain is '1')
Total Harmonic Distortion for Each Channel	80			dB	25°C, PGA gain is '1', 500mVrms input
Reactive Energy Metering Bandwidth		4		kHz	
Active Energy Metering Bandwidth		4		kHz	
Irms and Vrms Measurement Bandwidth		4		kHz	
Measurement Error			±0.5	%	
Analog Input					
L Line Current Channel Differential Input	5μ		25m	Vrms	PGA gain is '24'
	7.5μ		37.5m		PGA gain is '16'
	15μ		75m		PGA gain is '8'
	30μ		150m		PGA gain is '4'
	120μ		600m		PGA gain is '1'
N Line Current Channel Differential Input	30μ		150m	Vrms	PGA gain is '4'
	60μ		300m		PGA gain is '2'
	120μ		600m		PGA gain is '1'
Voltage Channel Differential Input	120μ		600m	Vrms	PGA gain is '1'
L Line Current Channel Input Impedance		1		KΩ	
N Line Current Channel Input Impedance		50		KΩ	
Voltage Channel Input Impedance		50		KΩ	
L Line Current Channel DC Offset			10	mV	PGA gain is '24'
N Line Current Channel DC Offset			10	mV	PGA gain is '1'
Voltage Channel DC Offset			10	mV	PGA gain is '1'
Reference					
On-Chip Reference (90E21/22/23/24)	1.398	1.417	1.440	V	Reference voltage test mode
Reference Voltage Temperature Coefficient		±15	±40	ppm/°C	
Clock					
Crystal or External Clock		8.192		MHz	The Accuracy of crystal or external clock is ±100 ppm
SPI Interface					
SPI Interface Bit Rate	200		160k	bps	
Pulse Width					
CFx Pulse Width		80		ms	If T ≥ 160 ms, width=80ms; if T<160 ms, width = 0.5T. Refer to Section 6.6
ESD					
Machine Model (MM)	400			V	JESD22-A115
Charged Device Model (CDM)	1000			V	JESD22-C101

Human Body Model (HBM)	4000			V	JESD22-A114
Latch Up			±100	mA	JESD78A
Latch Up			4.95	V	JESD78A
Operating Conditions					
AVDD, Analog Power Supply	2.8	3.3	3.6	V	Metering precision guaranteed within 3.0V~3.6V.
DVDD, Digital Power Supply	2.8	3.3	3.6	V	Metering precision guaranteed within 3.0V~3.6V.
I_{AVDD}, Analog Current (90E21/22)		3.00		mA	L line current channel and voltage channel are open
I_{AVDD}, Analog Current (90E23/24)		3.75		mA	L line/ N line current channel and voltage channel are open
I_{DVDD}, Digital Current		2.75		mA	VDD=3.3V
DC Characteristics					
Digital Input High Level (all digital pins except OSCI)	2.0		VDD+2.6	V	VDD=3.3V±10%,
Digital Input High Level (OSCI)	2.0		VDD+0.3	V	VDD=3.3V±10%
Digital Input Low Level			0.8	V	VDD=3.3V±10%
Digital Input Leakage Current			±1	μA	VDD=3.6V, VI=VDD or GND
Digital Output Low Level (CF1, CF2)			0.4	V	VDD=3.3V, I_{OL}=10mA
Digital Output Low Level (IRQ, WarnOut, ZX, SDO)			0.4	V	VDD=3.3V, I_{OL}=5mA
Digital Output High Level (CF1, CF2)	2.4			V	VDD=3.3V, I_{OH}=-10mA
Digital Output High Level (IRQ, WarnOut, ZX, SDO)	2.4			V	VDD=3.3V, I_{OH}=-5mA
Digital Output Low Level (OSCO)			0.4	V	VDD=3.3V, I_{OL}=1mA
Digital Output High Level (OSCO)	2.4			V	VDD=3.3V, I_{OH}=-1mA

6.2 SPI INTERFACE TIMING

The SPI interface timing is as shown in Figure-10, Figure-11 and Table-12.

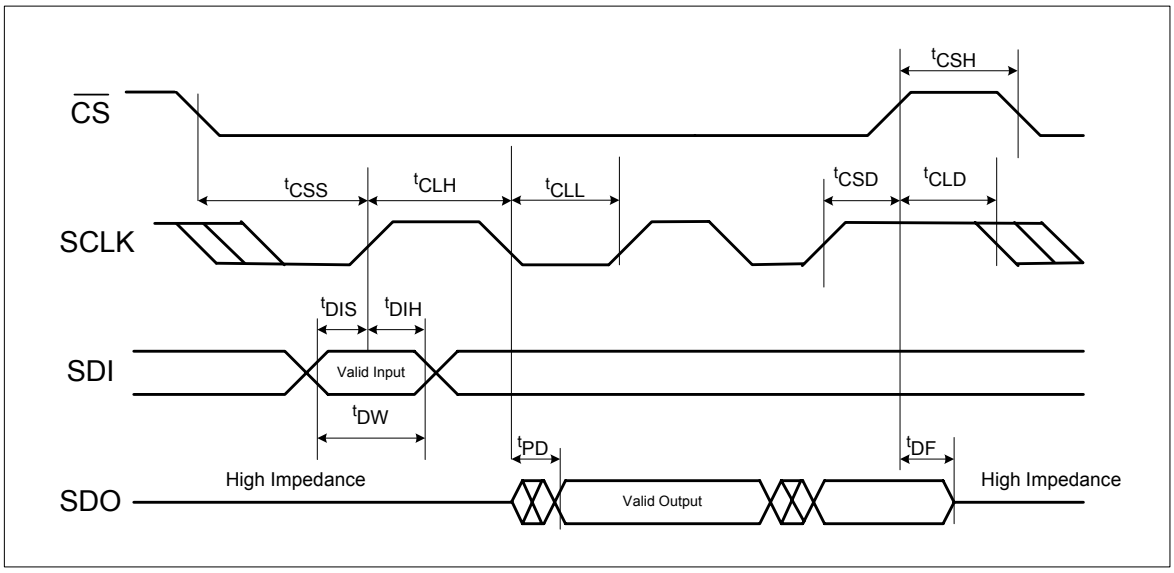


Figure-10 4-Wire SPI Timing Diagram

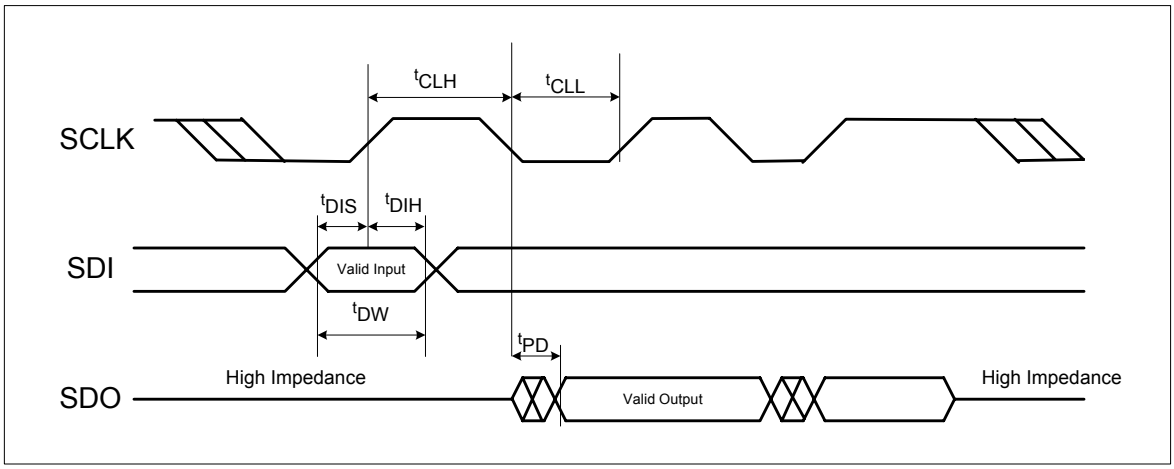


Figure-11 3-Wire SPI Timing Diagram

Table-12 SPI Timing Specification

Symbol	Description	Min.	Typical	Max.	Unit
t_{CSH} note 1	Minimum $\overline{CS}$ High Level Time	30T note 2+10			ns
t_{CSS} note 1	$\overline{CS}$ Setup Time	3T+10			ns
t_{CSD} note 1	$\overline{CS}$ Hold Time	30T+10			ns
t_{CLD} note 1	Clock Disable Time	1T			ns
t_{CLH}	Clock High Level Time	30T+10			ns
t_{CLL}	Clock Low Level Time	16T+10			ns
t_{DIS}	Data Setup Time	3T+10			ns
t_{DIH}	Data Hold Time	22T+10			ns

Table-12 SPI Timing Specification (Continued)

t_{DW}	Minimum Data Width	30T+10			ns
t_{PD}	Output Delay	14T		15T+20	ns
t_{DF} note 1	Output Disable Time			16T+20	ns

Note:
1. Not applicable for three-wire SPI.
2. T means SCLK cycle. T=122ns. (Typical value for four-wire SPI)

6.3 POWER ON RESET TIMING

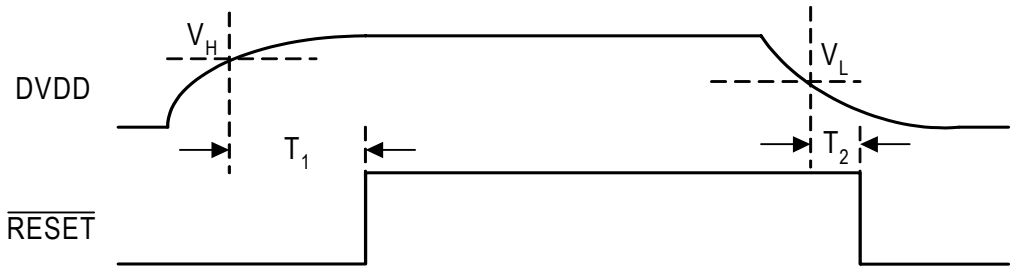


Figure-12 Power On Reset Timing Diagram

Table-13 Power On Reset Specification

Symbol	Description	Min.	Typical	Max.	Unit
V_H	Power On Trigger Voltage	2.47	2.6	2.73	V
V_L	Power Off Trigger Voltage	2.185	2.3	2.415	V
V_H-V_L	Hysteretic Voltage Difference	0.285	0.3	0.315	V
T_1	Delay Time After Power On	5			ms
T_2	Delay Time After Power Off	10			μs

6.4 ZERO-CROSSING TIMING

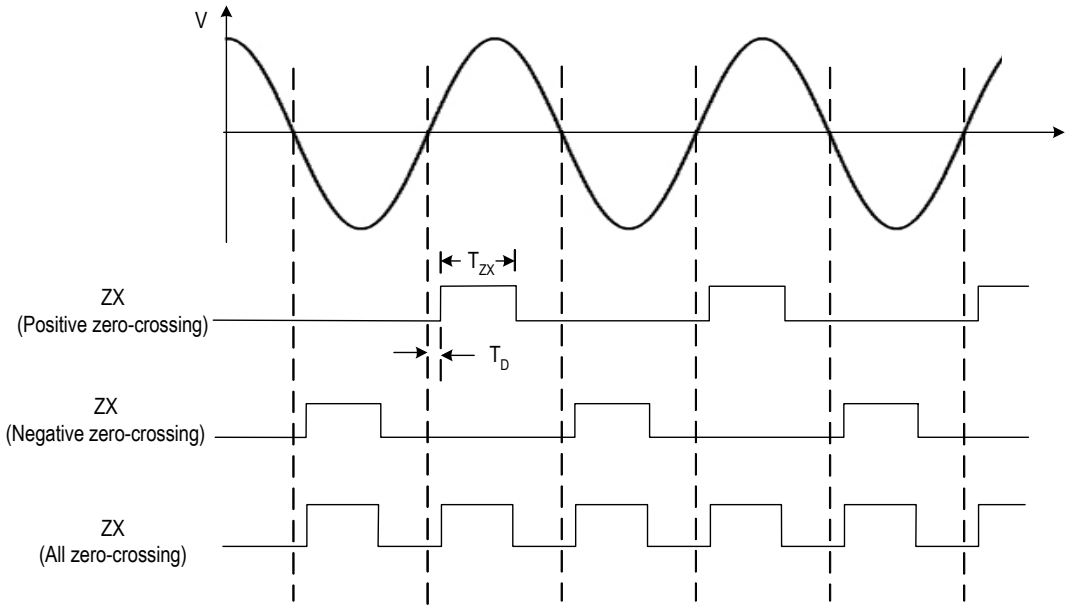


Figure-13 Zero-Crossing Timing Diagram

Table-14 Zero-Crossing Specification

Symbol	Description	Min.	Typical	Max.	Unit
T_{ZX}	High Level Width		5		ms
T_D	Delay Time			0.5	ms

6.5 VOLTAGE SAG TIMING

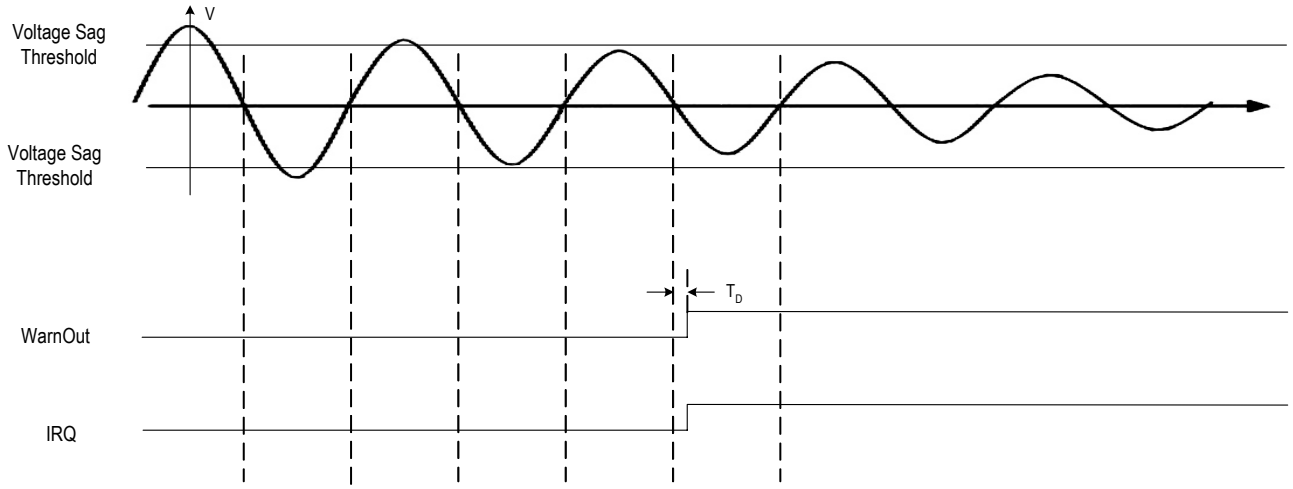


Figure-14 Voltage Sag Timing Diagram

Table-15 Voltage Sag Specification

Symbol	Description	Min.	Typical	Max.	Unit
T_D	Delay Time			0.5	ms

6.6 PULSE OUTPUT

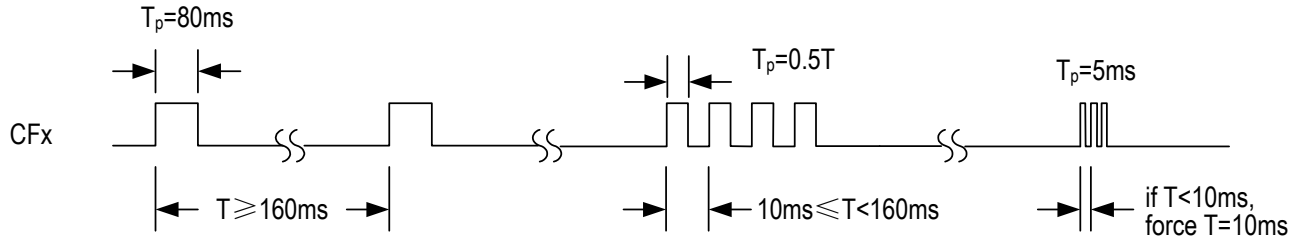


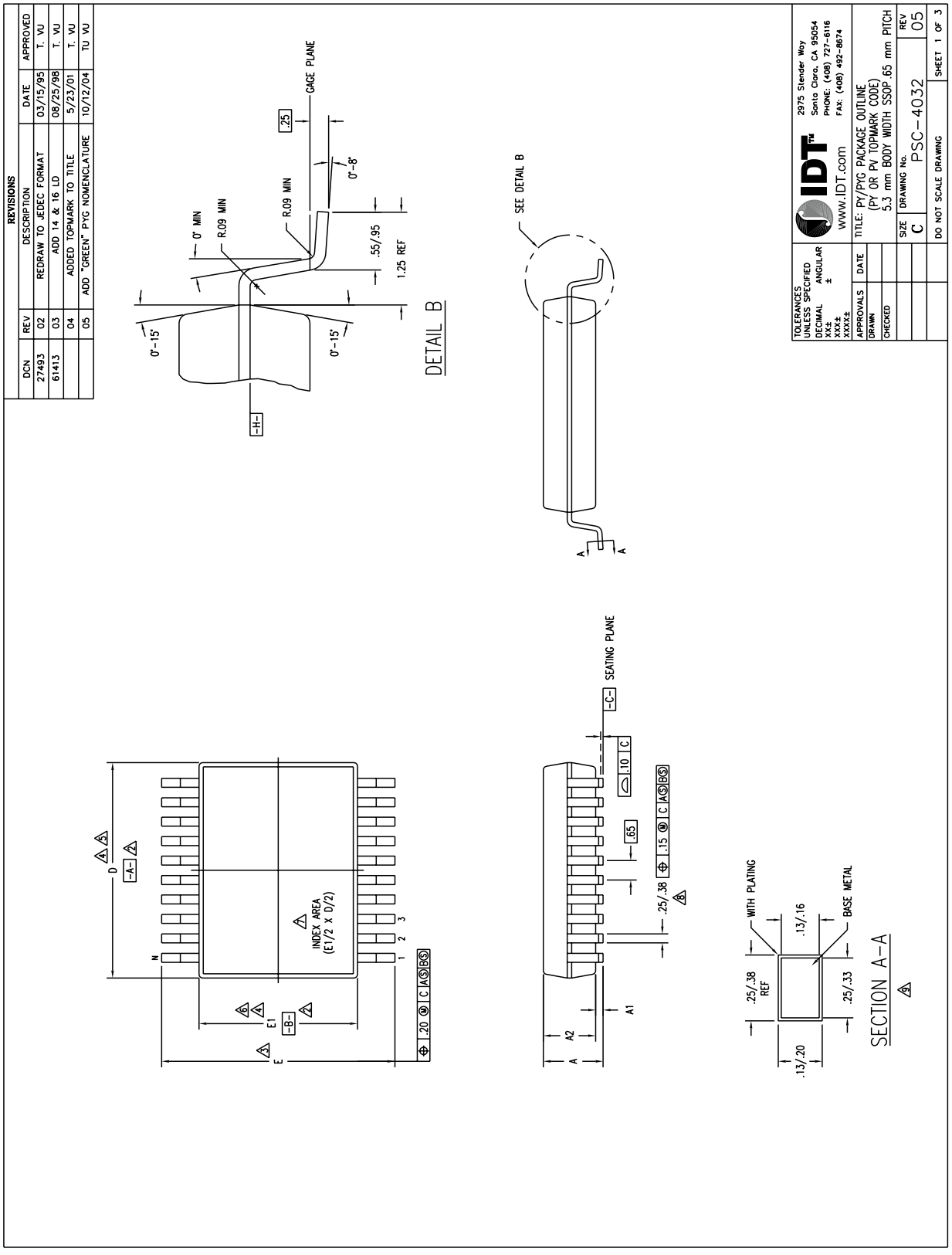
Figure-15 Output Pulse Width

6.7 ABSOLUTE MAXIMUM RATING

Parameter	Maximum Limit
Relative Voltage Between AVDD and AGND	-0.3V~3.7V
Relative Voltage Between DVDD and DGND	-0.3V~3.7V
Analog Input Voltage (I1P, I1N, I2P, I2N, VP, VN)	-1V~VDD
Digital Input Voltage	-0.3V~VDD+2.6V
Operating Temperature Range	-40~85 °C
Maximum Junction Temperature	150 °C

Package Type	Thermal Resistance θ_{JA}	Unit	Condition
Green SSOP28[note 1]	63.2	°C/W	No Airflow
Note 1: Refer to http://www.idt.com/package/pyg28.			

PACKAGE DIMENSIONS



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27493	02	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
61413	03	ADD 14 & 16 LD	08/25/98	T. VU
	04	ADDED TOPMARK TO TITLE	5/23/01	T. VU
	05	ADD "GREEN" PYG NOMENCLATURE	10/12/04	TU VU

SYMBOL	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AG			NOTE	JEDEC VARIATION AH			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99	
A1	.05	.13	.21		.05	.13	.21		.05	.13	.21		.05	.13	.21		.05	.13	.21	
A2	1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78	
D	5.90	6.20	6.50	4,5	5.90	6.20	6.50	4,5	7.07	7.20	7.33	4,5	8.07	8.20	8.33	4,5	10.07	10.20	10.33	4,5
E	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3
E1	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6
N	14				16				20				24				28			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .20 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .20 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .13 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

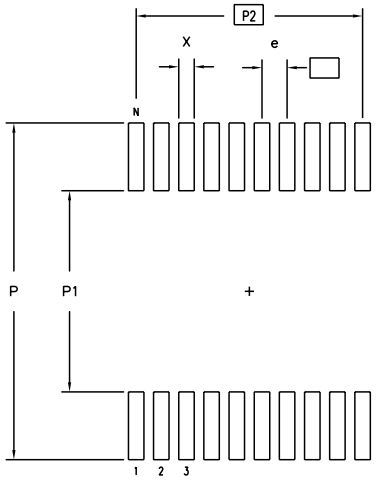
10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-150, VARIATION AB, AC, AE, AG & AH

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE PY/PYG PACKAGE OUTLINE (PY OR PV TOPMARK CODE) 5.3 mm BODY WIDTH SSOP .65 mm PITCH	
DRAWN			
CHECKED			
		SIZE C / DRAWING No. PSC-4032 / REV 05	
		DO NOT SCALE DRAWING	SHEET 2 OF 3

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20286	00	INITIAL RELEASE	04/15/91	T. VU
24536	01	ADD 28 LD	07/27/93	T. VU
27493	02	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
61413	03	ADD 14 & 16 LD	08/25/98	T. VU
	04	ADDED TOPMARK TO TITLE	5/23/01	T. VU
	05	ADD "GREEN" PYG NOMENCLATURE	10/12/04	TU VU

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	8.60	8.80	8.60	8.80	8.60	8.80	8.60	8.80	8.60	8.80
P1	5.10	5.30	5.10	5.30	5.10	5.30	5.10	5.30	5.10	5.30
P2	3.90 BSC		4.55 BSC		5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.40	.30	.40	.30	.40	.30	.40	.30	.40
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	14		16		20		24		28	

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DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS | DATE
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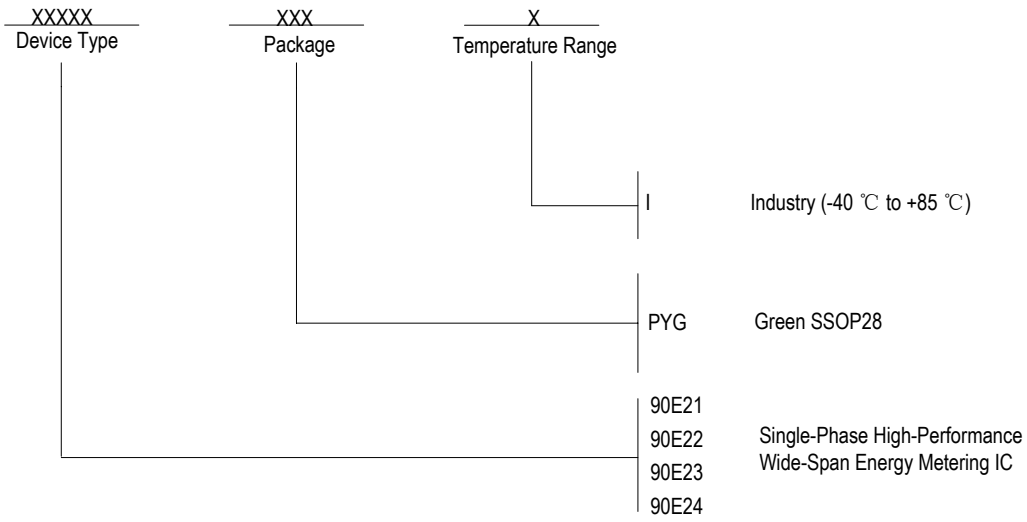
(PY OR PV TOPMARK CODE)
5.3 mm BODY WIDTH SSOP .65 mm PITCH

SIZE C | DRAWING No. PSC-4032 | REV 05

DO NOT SCALE DRAWING | SHEET 3 OF 3

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

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03/22/2011 pg. 53

01/10/2012 pg. 48, 52, 54, 55, 56

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