

## Four Output Differential Buffer for PCIe Gen 1 and Gen 2

## ICS9DB403D

## Description

The ICS9DB403 is compatible with the Intel DB400v2 Differential Buffer Specification. This buffer provides 4 PCI-Express Gen2 clocks. The ICS9DB403 is driven by a differential output pair from a CK410B+, CK505 or CK509B main clock generator.

## **Output Features**

- 4 0.7V current-mode differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available
- 50-100 MHz operation in PLL mode
- 50-400 MHz operation in Bypass mode

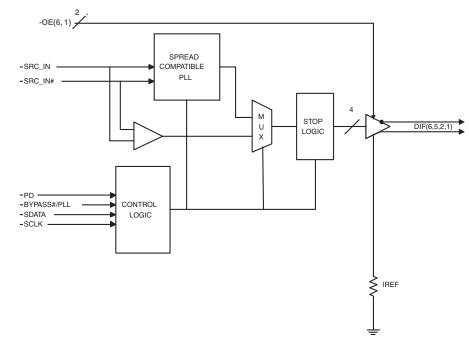
## Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread.
- Supports undriven differential outputs in PD# and SRC\_STOP# modes for power management.

## **Key Specifications**

- Outputs cycle-cycle jitter < 50ps
- Outputs skew: 50ps
- Phase jitter: PCIe Gen1 < 86ps peak to peak
- Phase jitter: PCIe Gen2 < 3.0/3.1ps rms
- 28-pin SSOP/TSSOP pacakge
- Available in RoHS compliant packaging
- Supports Commercial (0 to +70°C) and Industrial (-40 to +85°C) temperature ranges

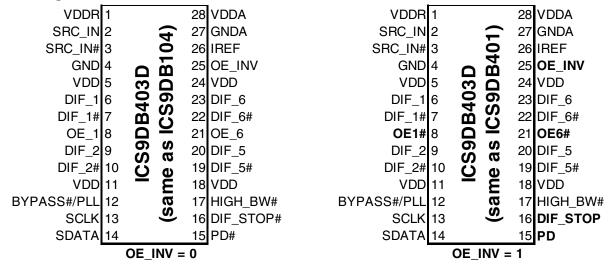
## **Functional Block Diagram**



## Note: Polarities shown for $OE_INV = 0$ .

IDT® Four Output Differential Buffer for PCIe and Gen 1 and Gen 2

## Pin Configuration



## 28-pin SSOP & TSSOP

#### **Polarity Inversion Pin List Table**

	OE_INV					
Pins	0	1				
8	OE_1	OE1#				
15	PD#	PD				
16	DIF_STOP#	DIF_STOP				
21	OE_6	OE6#				

#### **Power Groups**

Pin N	lumber	Description			
VDD	GND				
1	4	SRC_IN/SRC_IN#			
5,11,18, 24	4	DIF(1,2,5,6)			
N/A	27	IREF			
28	27	Analog VDD & GND for PLL core			

#### Pin Decription When OE\_INV = 0

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
			3.3V power for differential input clock (receiver). This VDD should be treated
1	VDDR	PWR	as an analog power rail and filtered appropriately.
2	SRC_IN	IN	0.7 V Differential SRC TRUE input
3	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
4	GND	PWR	Ground pin.
5	VDD	PWR	Power supply, nominal 3.3V
6	DIF 1	OUT	0.7V differential true clock output
7	DIF_1#	OUT	0.7V differential Complementary clock output
	_		Active high input for enabling output 1.
8	OE_1	IN	0 =disable outputs, 1= enable outputs
9	DIF_2	OUT	0.7V differential true clock output
10	DIF_2#	OUT	0.7V differential Complementary clock output
11	VDD	PWR	Power supply, nominal 3.3V
			Input to select Bypass(fan-out) or PLL (ZDB) mode
12	BYPASS#/PLL	IN	0 = Bypass mode, 1 = PLL mode
13	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
14	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
	00/11/1	., 0	Asynchronous active low input pin used to power down the device. The
15	PD#	IN	internal clocks are disabled and the VCO and the crystal osc. (if any) are
			stopped.
16	DIF_STOP#	IN	Active low input to stop differential output clocks.
			3.3V input for selecting PLL Band Width
17	HIGH_BW#	IN	0 = High, 1 = Low
18	VDD	PWR	Power supply, nominal 3.3V
19	DIF_5#	OUT	0.7V differential Complementary clock output
20	DIF_5	OUT	0.7V differential true clock output
			Active high input for enabling output 6.
21	OE_6	IN	0 =disable outputs, 1= enable outputs
22	DIF_6#	OUT	0.7V differential Complementary clock output
23	DIF_6	OUT	0.7V differential true clock output
24	VDD	PWR	Power supply, nominal 3.3V
			This latched input selects the polarity of the OE pins.
25	OE_INV	IN	0 = OE pins active high, $1 = OE$ pins active low (OE#)
			This pin establishes the reference for the differential current-mode output
			pairs. It requires a fixed precision resistor to ground. 4750hm is the standard
26	IREF	OUT	value for 1000hm differential impedance. Other impedances require different
			values. See data sheet.
27	GNDA	PWR	Ground pin for the PLL core.
			- · · · · · · · · · · · · · · · · · · ·

#### Pin Decription When OE\_INV = 1

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1 111 #			3.3V power for differential input clock (receiver). This VDD should be
1	VDDR	PWR	treated as an analog power rail and filtered appropriately.
2	SRC IN	IN	0.7 V Differential SRC TRUE input
3	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
4	GND	PWR	Ground pin.
5	VDD	PWR	Power supply, nominal 3.3V
6	DIF_1	OUT	0.7V differential true clock output
7	 DIF_1#	OUT	0.7V differential Complementary clock output
/		001	Active low input for enabling DIF pair 1.
8	OE1#	IN	1 =disable outputs, 0 = enable outputs
9	DIF 2	OUT	0.7V differential true clock output
9 10	DIF_2#	OUT	0.7V differential Complementary clock output
11	VDD	PWR	Power supply, nominal 3.3V
	VDD		Input to select Bypass(fan-out) or PLL (ZDB) mode
12	BYPASS#/PLL	IN	
10	SCLK	INI	0 = Bypass mode, 1 = PLL mode
13		IN I/O	Clock pin of SMBus circuitry, 5V tolerant.
14	SDATA	1/0	Data pin for SMBus circuitry, 5V tolerant.
15	PD	IN	Asynchronous active high input pin used to power down the device.
10		INI	The internal clocks are disabled and the VCO is stopped.
16	DIF_STOP	IN	Active High input to stop differential output clocks.
17	HIGH_BW#	IN	3.3V input for selecting PLL Band Width
10		DWD	0 = High, 1= Low
18	VDD	PWR	Power supply, nominal 3.3V
19	DIF_5#	OUT	0.7V differential Complementary clock output
20	DIF_5	OUT	0.7V differential true clock output
21	OE6#	IN	Active low input for enabling DIF pair 6.
			1 =disable outputs, 0 = enable outputs
22	DIF_6#	OUT	0.7V differential Complementary clock output
23	DIF_6	OUT	0.7V differential true clock output
24	VDD	PWR	Power supply, nominal 3.3V
25	OE_INV	IN	This latched input selects the polarity of the OE pins.
	_		0 = OE pins active high, 1 = OE pins active low (OE#)
			This pin establishes the reference for the differential current-mode
26	IREF	OUT	output pairs. It requires a fixed precision resistor to ground. 475ohm is
			the standard value for 100ohm differential impedance. Other
			impedances require different values. See data sheet.
27	GNDA	PWR	Ground pin for the PLL core.
28	VDDA	PWR	3.3V power for the PLL core.

## Absolute Max

Symbol	Parameter	Min	Max	Units
VDDA/R	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Supply Voltage		4.6	V
V <sub>IL</sub>	Input Low Voltage	GND-0.5		V
V <sub>IH</sub>	Input High Voltage		$V_{DD}$ +0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Commerical Operating Range	0	70	°C
Tampient	Industrial Operating Range	-40	85	°C
Tcase	Case Temperature		115	°C
	Input ESD protection			
ESD prot	human body model	2000		V

## **Electrical Characteristics - Clock Input Parameters**

 $T_A$  = Tambient for the desired operating range, Supply Voltage  $V_{DD}$  = 3.3 V +/-5%

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	VIHDIF	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	VILDIF	Differential inputs (single-ended measurement)	V <sub>SS</sub> - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V <sub>COM</sub>	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V <sub>SWING</sub>	Peak to Peak value (single-ended measurement)	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I <sub>IN</sub>	$V_{IN} = V_{DD}, V_{IN} = GND$	-5		5	uA	1
Input Duty Cycle	d <sub>tin</sub>	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	$J_{DIFIn}$	Differential Measurement	0		125	ps	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through Vswing min centered around differential zero

#### ICS9DB403D Four Output Differential Buffer for PCIe for Gen 1 and Gen 2

#### Electrical Characteristics - Input/Supply/Common Output Parameters

 $T_A$  = Tambient for the desired operating range. Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%

PARAMETERSYMBOLCONDITIONSInput High Voltage $V_{IHSE}$ Single Ended Inputs, 3.3 V +/-5Input Low Voltage $V_{ILSE}$ Single Ended Inputs, 3.3 V +/-5Input Low Current $I_{IL1}$ $V_{IN} = 0$ V; Inputs with no pull-up resistenceInput Low Current $I_{IL2}$ $V_{IN} = 0$ V; Inputs with null-up resistence9DB803 Supply Current $I_{DD3.3PDC}$ Full Active, $C_L = Full load; Industria9DB803 PowerdownI_{DD3.3PDC}all diff pairs driven, C-Temp9DB403 PowerdownI_{DD3.3PDC}all diff pairs driven, C-Temp9DB403 Supply CurrentI_{DD3.3PDC}all diff pairs driven, C-Temp9DB403 PowerdownI_{DD3.3PDC}all diff ential pairs tri-stated, I-T1nput FrequencyF_{IPLL}PCIe Mode (Bypass#/PLL=1Pin InductanceL_{pin}all diff erential pairs tri-stated, I-T1nput S ModulationC_{IN}Logic Inputs, except SRC_INCik StabilizationT_{STAB}SRC_IN differential clock inputCik Stabilizationf_{MODIN}Allowable FrequencyCik Stabilizationf_{MODIN}Allowable FrequencyCik Stabilizationf_{MODIN}Allowable FrequencyCik Stabilizationf_{MODIN}Allowable FrequencyCik Stabilizationf_{MODIN}Allowable Frequency$	/-5%		-	•	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	MIN	TYP	MAX	UNITS	NOTES
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	2		V <sub>DD</sub> + 0.3	V	1
$ \begin{array}{ c c c c c c } &  I_{IL1} &  V_{IN} = V_{DD} \\ \hline \\ Input Low Current \\ Input Low Current \\ Input Low Current \\ \hline \\ Input Low Current \\ \hline \\ Inpus Supply Current \\ \hline \\ Inpus Frequency \\ \hline \\ Input Frequency \\ PLL Bandwidth \\ PLL Bandwidth \\ PLL Bandwidth \\ PLL Supply Current \\ \hline \\ Input S Modulation \\ PLL Bandwidth \\ PLL Supply Current \\ \hline \\ Input S Modulation \\ Frequency \\ PLL Bandwidth \\ PLL Supply Current \\ \hline \\ \\ Input S Modulation \\ Frequency \\ PLL Bandwidth \\ PLL Supply Current \\ \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ $	% GND - 0	.3	0.8	V	1
$\begin{tabular}{ c                                   $	-5		5	uA	1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	sistors -5			uA	1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	stors -200			uA	1
9DB803 Supply CurrentIemp Hange $I_{DD3.30PI}$ Full Active, CL = Full load; Industria Range9DB803 Powerdown Current $I_{DD3.3PDC}$ all diff pairs driven, C-Temp all diff pairs driven, I-temp all differential pairs tri-stated, C-19DB403 Supply Current $I_{DD3.3PDC}$ Full Active, CL = Full load; Comm Temp Range9DB403 Supply Current $I_{DD3.3OPC}$ Full Active, CL = Full load; Industria Range9DB403 Powerdown Current $I_{DD3.3OPC}$ Full Active, CL = Full load; Industria Range9DB403 Powerdown Current $I_{DD3.3PDC}$ all differential pairs tri-stated, L-T Range9DB403 Powerdown Current $I_{DD3.3PDC}$ all differential pairs tri-stated, L-T Powers9DB403 Powerdown Current Inductance $I_{DD1.2D}$ <tr< td=""><td></td><td>475</td><td>000</td><td></td><td></td></tr<>		475	000		
$\frac{ _{\text{DD3.3OPI}} _{\text{BD3.3PDC}} = \frac{ _{\text{Int}} \text{Active}, C_L = \text{Purricat, misstriar}}{\text{Range}}$ $\frac{ _{\text{DD3.3PDC}} _{\text{I}_{\text{DD3.3PDC}}} = \frac{\text{all diff pairs driven, C-Temp}}{\text{all diff pairs driven, L-temp}} \\ \frac{ _{\text{DD3.3PDI}} _{\text{I}_{\text{DD3.3PDI}}} = \frac{\text{all diff pairs driven, L-temp}}{\text{all differential pairs tri-stated, L-tr}} \\ \frac{ _{\text{DD3.3OPI}} _{\text{I}_{\text{DD3.3OPI}}} = \frac{\text{All Active}, C_L = \text{Full load; moments}}{\text{Full Active, C_L = Full load; comm}} \\ \frac{ _{\text{DD3.3OPI}} _{\text{I}_{\text{DD3.3OPI}}} = \frac{\text{Full Active, C_L = Full load; moments}}{\text{Range}} \\ \frac{ _{\text{DD3.3OPI}} _{\text{I}_{\text{DD3.3OPI}}} = \frac{\text{All diff pairs driven, C-Temp}}{\text{all diff pairs driven, C-Temp}} \\ \frac{ _{\text{DD3.3PDI}} _{\text{I}_{\text{DD3.3PDI}}} = \frac{\text{all diff pairs driven, C-Temp}}{\text{all diff pairs driven, 1-Temp}} \\ \frac{ _{\text{I}_{\text{DD3.3PDI}} _{\text{I}_{\text{DD3.3PDI}}} = \frac{\text{all diff pairs driven, 1-Temp}}{\text{all differential pairs tri-stated, C-T}} \\ \frac{ _{\text{I}_{\text{DD3.3PDI}} _{\text{I}_{\text{I}_{\text{N}_{\text{T}}}}} = \frac{\text{All diff pairs driven, 1-Temp}}{\text{all differential pairs tri-stated, C-T}} \\ \frac{ _{\text{I}_{\text{DD3.3PDI}} _{\text{I}_{\text{D}_{\text{D}}}} = \frac{\text{All differential pairs tri-stated, C-T}}{\text{all differential pairs tri-stated, C-T}} \\ \frac{ _{\text{I}_{\text{DD3.3PDI}} _{\text{I}_{\text{D}}}} = \frac{\text{All diff pairs driven, 1-Temp}}{\text{all differential pairs tri-stated, C-T}} \\ \frac{ _{\text{I}_{\text{D}}} = \frac{1}{\text{I}_{\text{D}}} = \frac{1}{\text{I}_{\text{D}}} \\ \frac{ _{\text{I}_{\text{D}}} = \frac{1}{\text{I}_{\text{D}}} = \frac{1}{\text{I}_{\text{B}}} \\ \frac{ _{\text{D}}} = \frac{1}{\text{I}_{\text{D}}} \\ \frac{ _{\text{D}}} = \frac{1}{\text{I}_{\text$		175	200	mA	1
$\begin{array}{ c c c c } & & & & & & & & & & & & & & & & & & &$	Temp	190	225	mA	1
9DB803 Powerdown Current $^{1DD3.3PDC}$ all differential pairs tri-stated, C-1 all diff pairs driven, 1-temp all differential pairs tri-stated, 1-t Full Active, $C_L = Full load; Comm$ $Temp Range9DB403 Supply Current1_{DD3.3PDI}Full Active, C_L = Full load; CommTemp Range9DB403 PowerdownCurrent1_{DD3.3PDI}Full Active, C_L = Full load; IndustriaRange9DB403 PowerdownCurrent1_{DD3.3PDI}all differential pairs tri-stated, C-1Range9DB403 PowerdownCurrent1_{DD3.3PDI}all differential pairs tri-stated, C-1Range9DB403 PowerdownCurrentF_{iPLL}PCle Mode (Bypass#/PLL=1PCle Mode (Bypass#/PLL=11nput FrequencyF_{iPLL}PCle Mode (Bypass#/PLL=1FigsPASSPin InductanceL_{pin}CinCapacitanceC_{IN}Logic Inputs, except SRC_INGOUTPLL BandwidthBW-3dB point in High BW Mode-3dB point in Low BW ModePLL Jitter Peakingt_{JPEAK}Peak Pass band GainclockPLL StabilizationT_{STAB}From V_{DD} Power-Up and after inpuclockInput SS ModulationFrequencyf_{MODIN}Allowable Frequency(Triangular Modulation)OE# Latencyt_{DRVSTP}DIF stap after OE# deassertionSRC Stop# de-assertionTdrive_SRC_STOP#t_{DRVSTP}DIF output enable afterPD# and SRC_STCTfallt_FFall time of PD# and SRC_STCTriset_RRise time of PD# and SRC_STCSMBus VoltageV_{MAX}Maximum input voltageLow-level $					
SDB00 POWerdown Currentand differential pairs tri-stated, C-1 all diff pairs driven, 1-temp all differential pairs tri-stated, L-t all differential pairs tri-stated, L-t Full Active, $C_L = Full load; CommRange9DB403 Supply CurrentIbD3.30PCFull Active, C_L = Full load; IndustriaRange9DB403 PowerdownCurrentIbD3.30PCFull Active, C_L = Full load; IndustriaRange9DB403 PowerdownCurrentIbD3.30PCall differential pairs tri-stated, C-1all differential pairs tri-stated, C-11Input FrequencyFiPLLPCle Mode (Bypass#/PLL=1FiBYPASSPin InductanceLpinPCle Mode (Bypass#/PLL=1CINCapacitanceCINLogic Inputs, except SRC_INCOUTPLL BandwidthBW-3dB point in High BW Mode-3dB point in Low BW ModePLL Jitter Peakingt_{JPEAK}Peak Pass band GainFrom VDD Power-Up and after inpuclockInput SS ModulationFrequencyftuatoe#From VDD Power-Up and after inpuclockClk Stabilizationftuatoe#DIF start after OE# assertionOE# LatencyTdrive_SRC_STOP#tborvsrPDIF start after OE# deassertionDIF stor after OE# deassertionDIF output enable afterSRC Stop# de-assertionTfallTdrive_PD#tborvsrPPD# de-assertionPD# de-assertionTfalltFFall time of PD# and SRC_STOSMBus VoltageVMAXMaximum input voltageLow-level Output VoltageVolu\ell_{PULLUP}$		50	60	mA	1
$\frac{ ^{1DD3.3PDI} }{PDB403 Supply Current} + \frac{ _{DD3.3OPC} }{ _{DD3.3OPC}} + \frac{PUII Active, C_{L} = FuII load; CommTemp Range}{FuII Active, C_{L} = FuII load; CommTemp Range} + FuII Active, C_{L} = FuII load; IndustriaRange} + \frac{PUI Active, C_{L} = FuII IndustriaRange} + \frac{PUI Active, C_{L} = FuII IndustriaRange} + \frac{PUI Active, C_{L} = FuII Industria Range} + PUI Active, PUI Active,$	emp	4	6	mA	1
$\begin{array}{ c c c c c } & \label{eq:generalized_scalar} \\ & eq:generalized$		55	65	mA	1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		6	8	mA	1
	illai	105	125	mA	1
$\begin{tabular}{ c c c c c } \hline I_{DD3.3PPC} & I_{DD3.3PDC} & all diff pairs driven, C-Temp \\ \hline all diff pairs driven, C-Temp \\ \hline all diff pairs driven, C-Temp \\ all diff pairs driven, I-Temp \\ all diff pairs driven, I-Te$	Temp		1		
$\begin{array}{c} \label{eq:posterior} & \label{eq:posterior} \\ \begin{tabular}{ l                                   $	lonp	115	150	mA	1
$\begin{array}{c} \end{tabular}{ \begin{tabular}{ c c c c } \hline \end{tabular} \\ tabula$		25	30	mA	1
$\frac{I_{DD3.3PDI}}{Input Frequency} \qquad \frac{F_{iPLL}}{F_{iBYPASS}} \qquad \frac{PCle Mode (Bypass#/PLL= 1)}{Bypass Mode ((Bypass#/PLL= 1)} \\ \frac{F_{iBYPASS}}{Input Capacitance} \qquad \frac{C_{IN}}{C_{IN}} \qquad \frac{Logic Inputs, except SRC_IN}{SRC_IN differential clock input} \\ \frac{C_{OUT}}{C_{OUT}} \qquad \frac{C_{IN} Input Capacitance}{Input Court} \qquad \frac{C_{IN} Input Capacitance}{Input Court} \\ \frac{C_{INSRC_IN}}{Input Capacitance} \qquad \frac{C_{IN}}{Input Capacitance} \qquad \frac{C_{IN} Input Capacitance}{Input Capacitance} \\ \frac{C_{INSRC_IN}}{Input Capacitance} \qquad \frac{C_{IN} Input Capacitance}{Input Clk Stabilization} \qquad \frac{T_{STAB}}{Input SS Modulation} \\ \frac{f_{MODIN}}{Input SS Modulation} \\ \frac{C_{INT} Input SS Modulation}{Input SS Modulation} \\ \frac{C_{INT} Input SS Modulation}{Input Clk Capacitance} \qquad \frac{C_{IN} Input SS Modulation}{Input SS Modulation} \\ \frac{C_{INT} Input SS Modulation}{Input SS Modulatio} \\ \frac{C_{INT} Input SS Modulatio}{Input SS Modulatio} \\ \frac{C_{INT} Inp$	emp	2	3	mA	1
		30	35	mA	1
$ \begin{array}{ c c c c c c c } \hline F_{\text{IBYPASS}} & Bypass Mode ((Bypass#/PLL= \\ \hline Pin Inductance & L_{pin} & \\ \hline C_{IN} & Logic Inputs, except SRC_IN \\ \hline Capacitance & \hline C_{INSRC_IN} & SRC_IN differential clock input \\ \hline C_{OUT} & Output pin capacitance & \\ \hline PLL Bandwidth & BW & \\ \hline -3dB point in High BW Mode & \\ \hline -3dB point in Low BW Mode & \\ \hline -3dB point & \\ \hline -3dB point in Low BW Mode & \\ \hline -3dB point & \\ \hline -3dB point & \\ \hline -3dB & \\ \hline -$	mp	3	4	mA	1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	50	100.00	110	MHz	1
$\begin{array}{ c c c } \mbox{Pin Inductance} & $L_{pin}$ & $L_{ogic Inputs, except SRC_IN}$ \\ \hline C_{INSRC_IN} & $SRC_IN differential clock input cloc$	0) 33		400	MHz	1
$ \begin{array}{ c c c } \hline C_{\rm IN} & Logic Inputs, except SRC_IN \\ \hline C_{\rm INSRC_IN} & SRC_IN differential clock input \\ \hline C_{\rm OUT} & Output pin capacitance \\ \hline Output pin capacitance \\ \hline C_{\rm OUT} & Output pin capacitance \\ \hline C_{\rm STAB} & Peak Pass band Gain \\ \hline From V_{DD} Power-Up and after input \\ stabilization or de-assertion of PD# \\ \hline C_{\rm Input SS Modulation \\ Frequency & f_{\rm MODIN} & Allowable Frequency \\ \hline T_{\rm Requency} & f_{\rm MODIN} & OIF start after OE# assertior \\ \hline D_{\rm F stop after OE# deassertior \\ D_{\rm F stop after OE# deassertior \\ D_{\rm IF stop after OE# deassertion \\ D_{\rm IF output enable after \\ SRC_Stop# de-assertion \\ D_{\rm F output enable after \\ SRC_Stop# de-assertion \\ \hline T_{\rm drive_PD# & t_{DRVPD} & DIF output enable after \\ PD# de-assertion \\ \hline T_{\rm Trise} & t_{\rm R} & Rise time of PD# and SRC_STO \\ \hline T_{\rm rise} & t_{\rm R} & Rise time of PD# and SRC_STO \\ \hline C_{\rm NBUS Voltage} & V_{\rm MAX} & Maximum input voltage \\ \hline C_{\rm OUTPUT Voltage } & V_{OL} & @I_{\rm PULLUP} \\ \hline \end{array}$			7	nH	1
$\begin{array}{c c c c c } \mbox{Capacitance} & \hline C_{\rm INSRC_IN} & SRC_IN differential clock input \\ \hline C_{\rm OUT} & Output pin capacitance \\ \hline -3dB point in High BW Mode \\ \hline -3dB point in Low BW Mode \\ \hline -3dB point in High BW Mode \\ \hline -3dB point in Low BW Mode \\ \hline -3dB point in Low BW Mode \\ \hline -3dB point in Low BW Mode \\ \hline -3dB point in High BW Mode \\ \hline -3dB point in Low BW Mode \\ \hline -3de point \\ \hline$	1.5		5	pF	1
$ \begin{array}{c c c c c } \hline C_{OUT} & Output pin capacitance \\ \hline C_{OUT} & Output pin capacitance \\ \hline PLL Bandwidth & BW & -3dB point in High BW Mode \\ \hline -3dB point in Low BW mode \\ \hline -3dB point $	s 1.5		2.7	pF	1,4
$\begin{array}{c c c c c c } \mbox{PLL Bandwidth} & \mbox{BW} & \begin{array}{r} -3dB \mbox{point in High BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & -3dB \mbox{point in Low BW Mode} \\ \hline & Frequency \\ \hline & Clex \\ \hline & Stabilization or de-assertion of PD# \\ \hline & clock \\ \hline & clock \\ \hline & Input SS Modulation \\ \hline & Frequency \\ \hline & OE# \mbox{Latency} \\ \hline & f_{MODIN} \\ \hline & f_{MODIN} \\ \hline & f_{MODIN} \\ \hline & Clock \\ \hline & Frequency \\ \hline & (Triangular Modulation) \\ \hline & OE# \mbox{Latency} \\ \hline & f_{MODIN} \\ \hline & f_{MODIN} \\ \hline & OIF start after OE# assertion \\ \hline & DIF \mbox{start after OE# assertion \\ \hline & DIF \mbox{start of PD# de-assertion \\ \hline & PD# \mbox{de-assertion \\ \hline &$			6	pF	1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	2	3	4	MHz	1
$ \begin{array}{c} \mbox{Clk Stabilization} & \mbox{T}_{STAB} & \mbox{From V}_{DD} \mbox{Power-Up and after input stabilization or de-assertion of PD# clock} \\ \mbox{Input SS Modulation} & \mbox{f}_{MODIN} & \mbox{Allowable Frequency} & \mbox{(Triangular Modulation)} & \mbox{(Triangular Modulation)} & \mbox{(Triangular Modulation)} & \mbox{OE# Latency} & \mbox{t}_{LATOE#} & \mbox{DIF start after OE# assertion} & \mbox{DIF stop after OE# deassertion} & \mbox{DIF stop after OE# deassertion} & \mbox{DIF output enable after} & \mbox{SRC Stop# de-assertion} & \mbox{DIF output enable after} & \mbox{SRC Stop# de-assertion} & \mbox{DIF output enable after} & \mbox{SRC Stop# de-assertion} & \mbox{DIF output enable after} & \mbox{PD# de-assertion} & PD# de-asse$	0.7	1	1.4	MHz	1
$ \begin{array}{c} \mbox{Clk Stabilization} & \mbox{T}_{STAB} & \mbox{From V}_{DD} \mbox{Power-Up and after input stabilization or de-assertion of PD# clock} \\ \mbox{Input SS Modulation} & \mbox{f}_{MODIN} & \mbox{Allowable Frequency} & \mbox{(Triangular Modulation)} & \mbox{(Triangular Modulation)} & \mbox{(Triangular Modulation)} & \mbox{OE# Latency} & \mbox{t}_{LATOE#} & \mbox{DIF start after OE# assertion} & \mbox{DIF stop after OE# deassertion} & \mbox{DIF stop after OE# deassertion} & \mbox{DIF output enable after} & \mbox{SRC Stop# de-assertion} & \mbox{DIF output enable after} & \mbox{SRC Stop# de-assertion} & \mbox{DIF output enable after} & \mbox{SRC Stop# de-assertion} & \mbox{DIF output enable after} & \mbox{PD# de-assertion} & PD# de-asse$		1.5	2	dB	1
$\begin{tabular}{ c c c c } \hline line & line &$	clock				
$\begin{array}{ c c c c c c } \mbox{Input SS Modulation} & f_{MODIN} & Allowable Frequency & (Triangular Modulation) & \\ \hline Frequency & t_{LATOE\#} & DIF start after OE# assertion & \\ \hline DIF stop after OE# deassertion & \\ \hline Tdrive_SRC_STOP# & t_{DRVSTP} & DIF output enable after & \\ \hline Tdrive_PD# & t_{DRVPD} & DIF output enable after & \\ \hline Tfall & t_F & Fall time of PD# and SRC_STO & \\ \hline Trise & t_R & Rise time of PD# and SRC_STO & \\ \hline SMBus Voltage & V_{MAX} & Maximum input voltage & \\ \hline Low-level Output Voltage & V_{OL} & @ I_{PULLUP} & \\ \hline \end{array}$	to 1st		1	ms	1,2
$\begin{tabular}{ c c c c c } \hline Frequency & $^{I_{MODIN}}$ & (Triangular Modulation) \\ \hline (Triangular Modulation) & (Triangular Modulation) \\ \hline (Triangular Modulation) & DIF start after OE# assertion \\ DIF stop after OE# deassertion \\ DIF output enable after \\ SRC Stop# de-assertion \\ \hline (Tdrive_PD#) & $t_{DRVPD}$ & DIF output enable after \\ PD# de-assertion \\ \hline (Tfall tree of PD# and SRC_STO) \\ \hline (Trise) & $t_R$ & Rise time of PD# and SRC_STO \\ \hline (Trise) & $t_R$ & Rise time of PD# and SRC_STO \\ \hline (SMBus Voltage) & $V_{MAX}$ & Maximum input voltage \\ \hline (Low-level Output Voltage) & $V_{OL}$ & $(PULLUP$ & $V_{DLLUP}$ & $V_{DLLUP}$ & $V_{DLLUP}$ & $V_{DL}$ & $V_{DLLUP}$ & $V_{DL}$ & $V_{D$					
Frequency     (Triangular Modulation)       OE# Latency     t <sub>LATOE#</sub> DIF start after OE# assertion       Tdrive_SRC_STOP#     t <sub>DRVSTP</sub> DIF output enable after       Tdrive_PD#     t <sub>DRVPD</sub> DIF output enable after       Tfall     t <sub>F</sub> Fall time of PD# and SRC_STOP       Trise     t <sub>R</sub> Rise time of PD# and SRC_STOP       SMBus Voltage     V <sub>MAX</sub> Maximum input voltage       Low-level Output Voltage     V <sub>OL</sub> @ I <sub>PULLUP</sub>	30		33	kHz	1
OE# Latency     t <sub>LATOE#</sub> DIF stop after OE# deassertio       Tdrive_SRC_STOP#     t <sub>DRVSTP</sub> DIF output enable after SRC Stop# de-assertion       Tdrive_PD#     t <sub>DRVPD</sub> DIF output enable after PD# de-assertion       Tfall     t <sub>F</sub> Fall time of PD# and SRC_STO       Trise     t <sub>R</sub> Rise time of PD# and SRC_STO       SMBus Voltage     V <sub>MAX</sub> Maximum input voltage       Low-level Output Voltage     V <sub>OL</sub> @ I <sub>PULLUP</sub>				KI IZ	'
Tdrive_SRC_STOP#     t <sub>DRVSTP</sub> DIF stop after OL# deassertion       Tdrive_PD#     t <sub>DRVPD</sub> DIF output enable after       Tfall     t <sub>R</sub> DIF output enable after       Trise     t <sub>R</sub> Fall time of PD# and SRC_STO       SMBus Voltage     V <sub>MAX</sub> Maximum input voltage       Low-level Output Voltage     V <sub>OL</sub> @ I <sub>PULLUP</sub>	1 1		3	cycles	1,3
Idrive_SRC_STOP#     IDRVSTP     SRC Stop# de-assertion       Tdrive_PD#     tDRVPD     DIF output enable after       Tfall     tF     Fall time of PD# and SRC_STO       Trise     tR     Rise time of PD# and SRC_STO       SMBus Voltage     VMAX     Maximum input voltage       Low-level Output Voltage     VOL     @ IPULLUP	<u>1                                    </u>		, , , , , , , , , , , , , , , , , , ,	0,0100	1,0
Tdrive_PD#     t_DRVPD     DIF output enable after       Tfall     t <sub>F</sub> Fall time of PD# and SRC_STC       Trise     t <sub>R</sub> Rise time of PD# and SRC_STC       SMBus Voltage     V <sub>MAX</sub> Maximum input voltage       Low-level Output Voltage     V <sub>OL</sub> @ I <sub>PULLUP</sub>			10	ns	1,3
Tdrive_PD#         t <sub>DRVPD</sub> PD# de-assertion           Tfall         t <sub>F</sub> Fall time of PD# and SRC_STC           Trise         t <sub>R</sub> Rise time of PD# and SRC_STC           SMBus Voltage         V <sub>MAX</sub> Maximum input voltage           Low-level Output Voltage         V <sub>OL</sub> @ I <sub>PULLUP</sub>					,
Tfall         t <sub>F</sub> Fall time of PD# and SRC_STC           Trise         t <sub>R</sub> Rise time of PD# and SRC_STC           SMBus Voltage         V <sub>MAX</sub> Maximum input voltage           Low-level Output Voltage         V <sub>OL</sub> @ I <sub>PULLUP</sub> Current sinking at V <sub>OL</sub> I <sub>PULLUP</sub>			300	us	1,3
Trise         t <sub>R</sub> Rise time of PD# and SRC_STO           SMBus Voltage         V <sub>MAX</sub> Maximum input voltage           Low-level Output Voltage         V <sub>OL</sub> @ I <sub>PULLUP</sub> Current sinking at V <sub>OL</sub> I <sub>PULLUP</sub>	P#	_	5	ns	1
SMBus Voltage         V <sub>MAX</sub> Maximum input voltage           Low-level Output Voltage         V <sub>OL</sub> @ I <sub>PULLUP</sub> Current sinking at V <sub>OL</sub> I <sub>PULLUP</sub>		_	5	ns	2
Low-level Output Voltage         V <sub>OL</sub> @ I <sub>PULLUP</sub> Current sinking at V <sub>OL</sub> I <sub>PULLUP</sub>	<u>F#</u>		5.5	V	1
Current sinking at V <sub>OL</sub> I <sub>PULLUP</sub>			1	V	
			0.4		1
	4			mA	1
SCLK/SDATA (Max VIL - 0.15) to			1000	ns	1
Clock/Data Rise Time (Min VIH + 0.15)	<u> </u>	-		<del> </del>	
TEOND			300	ns	1
SMBus Operating				1.	
Frequency f <sub>MAXSMB</sub> Maximum SMBus operating frequ	ency		100	kHz	1,5
Clock/Data Rise Time         Image: RSMB         (Min VIH + 0.15)           SCLK/SDATA         (Min VIH + 0.15) to         (Min VIH + 0.15) to           Clock/Data Fall Time         t <sub>FSMB</sub> (Max VIL - 0.15)			300	ns	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>SRC\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

IDT® Four Output Differential Buffer for PCIe Gen 1 and Gen 2

## Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

 $T_A$  =Tambient;  $V_{DD}$  = 3.3 V +/-5%;  $C_L$  =2pF,  $R_S$ =33 $\Omega$ ,  $R_P$ =49.9 $\Omega$ ,  $R_{REF}$ =475 $\Omega$ 

PARAMETER	SYMBOL	$\begin{array}{c} \text{CONDITIONS} \\ \end{array}$	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo <sup>1</sup>		3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660		850	mV	1,2
Voltage Low	VLow	math function.	-150		150		1,2
Max Voltage	Vovs	Measurement on single ended			1150	mV	1
Min Voltage	Vuds	signal using absolute value.	-300			111.0	1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Rise Time	t <sub>r</sub>	$V_{OL} = 0.175V, V_{OH} = 0.525V$	175		700	ps	1
Fall Time	t <sub>f</sub>	$V_{OH} = 0.525 V V_{OL} = 0.175 V$	175		700	ps	1
<b>Rise Time Variation</b>	d-t <sub>r</sub>				125	ps	1
Fall Time Variation	d-t <sub>f</sub>				125	ps	1
Duty Cycle	d <sub>t3</sub>	Measurement from differential wavefrom	45		55	%	1
Skew, Input to Output	t <sub>pdBYP</sub>	Bypass Mode, V <sub>T</sub> = 50%	2500		5000	ps	1
Skew, input to Output	t <sub>pdPLL</sub>	PLL Mode $V_T = 50\%$	-250		250	ps	1
Skew, Output to Output	t <sub>sk3</sub>	V <sub>T</sub> = 50%			50	ps	1
litter Ovele to evele		PLL mode			50	ps	1,3
Jitter, Cycle to cycle	t <sub>jcyc-cyc</sub>	Additive Jitter in Bypass Mode			50	ps	1,3
		PCIe Gen1 phase jitter (Additive in Bypass Mode)		7	10	ps (pk2pk)	1,4,5
	t <sub>jphaseBYP</sub>	PCIe Gen 2 Low Band phase jitter (Additive in Bypass Mode)		0	0.1	ps (rms)	1,4,5
Jitter, Phase		PCIe Gen 2 High Band phase jitter (Additive in Bypass Mode)		0.3	0.5	ps (rms)	1,4,5
		PCIe Gen 1 phase jitter		40	86	ps (pk2pk)	1,4,5
	t <sub>jphasePLL</sub>	PCIe Gen 2 Low Band phase jitter		1.5	3	ps (rms)	1,4,5
		PCIe Gen 2 High Band phase jitter		2.7/ 2.2	3.1	ps (rms)	1,4,5,6

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

 $^{2}$  I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475 $\Omega$  (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50 $\Omega$ .

3 Measured from differential waveform

<sup>4</sup> See http://www.pcisig.com for complete specs

<sup>5</sup> Device driven by 932S421C or equivalent.

<sup>6</sup> First number is High Bandwidth Mode, second number is Low Bandwidth Mode

Meas	urement									
Wi	indow	1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Sy	/mbol	Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
Det	finition	Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
	<b>DIF 100</b>	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2,3
e	<b>DIF 133</b>	7.41425	7.49925	7.49925	7.50000	7.50075	7.53845	7.62345	ns	1,2,4
Signal Name	<b>DIF 166</b>	5.91440	5.99940	5.99940	6.00000	6.00060	6.03076	6.11576	ns	1,2,4
al N	<b>DIF 200</b>	4.91450	4.99950	4.99950	5.00000	5.00050	5.02563	5.11063	ns	1,2,4
gn	<b>DIF 266</b>	3.66463	3.74963	3.74963	3.75000	3.75038	3.76922	3.85422	ns	1,2,4
N.	DIF 333	2.91470	2.99970	2.99970	3.00000	3.00030	3.01538	3.10038	ns	1,2,4
	<b>DIF 400</b>	2.41475	2.49975	2.49975	2.50000	2.50025	2.51282	2.59782	ns	1,2,4

### **Clock Periods Differential Outputs with Spread Spectrum Enabled**

## **Clock Periods Differential Outputs with Spread Spectrum Disabled**

Meas	urement									
Wi	ndow	1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Sy	mbol	Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
Def	inition	Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
	DIF 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2,3
е	DIF 133	7.41425		7.49925	7.50000	7.50075		7.62345	ns	1,2,4
Signal Name	DIF 166	5.91440		5.99940	6.00000	6.00060		6.11576	ns	1,2,4
	DIF 200	4.91450		4.99950	5.00000	5.00050		5.11063	ns	1,2,4
gn	DIF 266	3.66463		3.74963	3.75000	3.75038		3.85422	ns	1,2,4
S	DIF 333	2.91470		2.99970	3.00000	3.00030		3.10038	ns	1,2,4
	DIF 400	2.41475		2.49975	2.50000	2.50025		2.59782	ns	1,2,4

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.

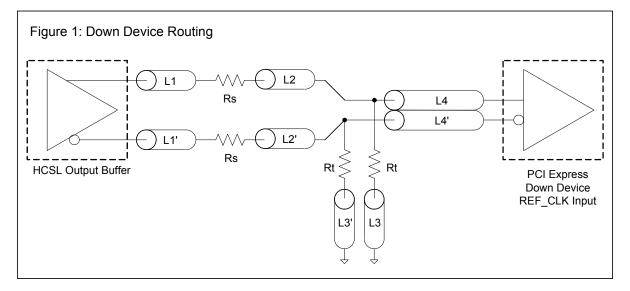
<sup>3</sup> Driven by SRC output of main clock, PLL or Bypass mode

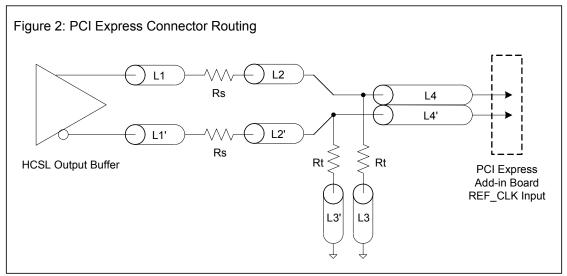
<sup>4</sup> Driven by CPU output of CK410/CK505 main clock, **Bypass mode only** 

SRC Reference Clock									
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure						
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1						
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1						
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1						
Rs	33	ohm	1						
Rt	49.9	ohm	1						

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

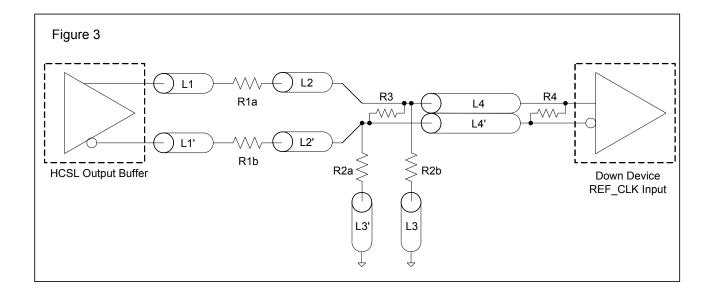




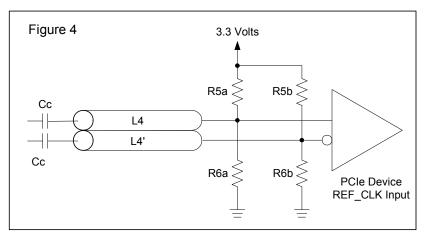
#### ICS9DB403D Four Output Differential Buffer for PCIe for Gen 1 and Gen 2

	Alternative Termination for LVDS and other Common Differential Signals (figure 3)									
Vdiff	Vp-р	Vcm	R1	R2	R3	R4	Note			
0.45v	0.22v	1.08	33	150	100	100				
0.58	0.28	0.6	33	78.7	137	100				
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible			
0.60	0.3	1.2	33	174	140	100	Standard LVDS			
R1a = R	R1a = R1b = R1									

R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)							
Component	Value	Note					
R5a, R5b	8.2K 5%						
R6a, R6b	1K 5%						
Сс	0.1 µF						
Vcm	0.350 volts						



## General SMBus serial interface information for the ICS9DB403D

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC (h)
- ICS clock will *acknowledge*
- Controller (host) sends the begining byte location = N
- ICS clock will *acknowledge*
- Controller (host) sends the data byte count = X
- ICS clock will acknowledge
- Controller (host) starts sending Byte N through Byte N + X -1
- ICS clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC (h)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD (h)
- ICS clock will acknowledge
- ICS clock will send the data byte count = X
- ICS clock sends Byte N + X -1
- ICS clock sends Byte 0 through byte X (if X<sub>(n)</sub> was written to byte 8).
- · Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Ind	ex Block V	Vrit	e Operation
Сог	ntroller (Host)		ICS (Slave/Receiver)
Т	starT bit		
Slav	e Address DC <sub>(h)</sub>		
WR	WRite		
			ACK
Begi	inning Byte = N		
			ACK
Data	Byte Count = X		
			ACK
Begir	nning Byte N		
			ACK
	$\diamond$	te [	
	$\diamond$	X Byte	$\diamond$
	$\diamond$	×	<b>O</b>
			0
Byt	e N + X - 1		
			ACK
Р	stoP bit		

Ind	Index Block Read Operation								
Con	troller (Host)	IC	S (Slave/Receiver)						
Т	starT bit								
Slave	e Address DC <sub>(h)</sub>								
WR	WRite								
		ACK							
Begii	nning Byte = N								
			ACK						
RT	Repeat starT								
Slave	e Address DD <sub>(h)</sub>								
RD	ReaD								
			ACK						
		Data Byte Count = X							
	ACK								
			Beginning Byte N						
	ACK								
		X Byte	$\diamond$						
	$\diamond$	B	$\diamond$						
	$\diamond$	$ \times $	<b>O</b>						
	<b>O</b>								
			Byte N + X - 1						
N	Not acknowledge								
Р	stoP bit								

Byt	te 0	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-		PD_Mode	PD# drive mode	RW	driven	Hi-Z	0
Bit 6	-		STOP_Mode	DIF_Stop# drive mode	RW	driven	Hi-Z	0
Bit 5	-		Reserved	Reserved	RW	Reserved		Х
Bit 4	-		Reserved	Reserved	RW	Reserved		Х
Bit 3	-		Reserved	Reserved	RW	Reserved		Х
Bit 2	-		PLL_BW#	Select PLL BW	RW	High BW	Low BW	1
Bit 1	-		BYPASS#	BYPASS#/PLL	RW	fan-out	ZDB	1
Bit 0	-		SRC_DIV#	SRC Divide by 2 Select	RW	x/2	1x	1

#### SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

#### SMBus Table: Output Control Register

Byt	te 1	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	t7 -		Reserved	Reserved	RW	RW Reserved		1
Bit 6	22,2	23	DIF_6	Output Enable	RW	Disable	Enable	1
Bit 5	19,2	20	DIF_5	Output Enable	RW	Disable	Enable	1
Bit 4	-		Reserved	Reserved	RW	Reserved		1
Bit 3	-		Reserved	Reserved	RW	Reserved		1
Bit 2	9,1	0	DIF_2	Output Enable	RW	Disable	Enable	1
Bit 1	6,7	7	DIF_1	Output Enable	RW	Disable	Enable	1
Bit 0			Reserved	Reserved	RW	Rese	erved	1

NOTE: The SMBus Output Enable Bit must be '1' AND the respective OE pin must be active for the output to run!

### SMBus Table: OE Pin Control Register

By	te 2	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	it 7 -		Reserved	rved Reserved RW Reserved		erved	0	
Bit 6	22	,23	DIF_6	DIF_6 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 5	19	,20	DIF_5	DIF_5 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 4		-	Reserved	Reserved	RW	Reserved		0
Bit 3		-	Reserved	Reserved	RW	Rese	erved	0
Bit 2	9	.1	DIF_2	DIF_2 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 1	6	,7	DIF_1	DIF_1 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 0		-	Reserved	Reserved	RW	Rese	erved	0

#### SMBus Table: Reserved Register

By	te 3	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7				Reserved				Х
Bit 6				Reserved				Х
Bit 5				Reserved				Х
Bit 4				Reserved				Х
Bit 3				Reserved				Х
Bit 2				Reserved				Х
Bit 1				Reserved				Х
Bit 0				Reserved				Х

By	te 4	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7		-	RID3		R	-	-	0
Bit 6		-	RID2	<b>REVISION ID</b>	R	-	-	0
Bit 5		-	RID1		R	-	-	1
Bit 4		-	RID0		R	-	-	1
Bit 3		-	VID3		R	-	-	0
Bit 2		-	VID2	VENDOR ID	R	-	-	0
Bit 1	-		VID1	VENDORID	R	-	-	0
Bit 0		-	VID0		R	-	-	1

#### SMBus Table: Vendor & Revision ID Register

#### SMBus Table: DEVICE ID

Byt	te 5	Pin #	Name	Control Function		Туре	0	1	Default				
Bit 7		-		Device ID 7 (MSB)		RW			0				
Bit 6	-		-		Bit 6 -			Device ID 6		RW			Х
Bit 5		-		Device ID 5		RW	Davias ID	is 83 Hex	Х				
Bit 4		-		Device ID 4		RW			0				
Bit 3		-		Device ID 3		RW	for 9DB803 and 43 Hex for 9DB403		0				
Bit 2	-			Device ID 2		RW		900403	0				
Bit 1		-	Device ID 1						1				
Bit 0		-		Device ID 0		RW			1				

#### SMBus Table: Byte Count Register

By	te 6	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-		BC7		RW	-	-	0
Bit 6	-		BC6		RW	-	-	0
Bit 5	-		BC5		RW	-	-	0
Bit 4	-		BC4	Writing to this register configures how	RW	-	-	0
Bit 3	-		BC3	many bytes will be read back.	RW	-	-	0
Bit 2	-		BC2		RW	-	-	1
Bit 1	-		BC1		RW	-	-	1
Bit 0	-		BC0		RW	-	-	1

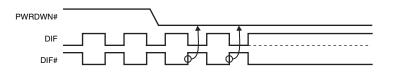
Note: Polarities in timing diagrams are shown  $OE_INV = 0$ . They are similar to  $OE_INV = 1$ .

#### PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

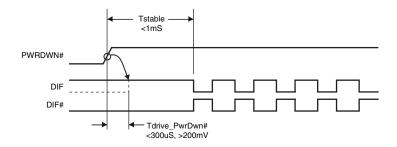
#### **PD# Assertion**

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with 2 x I<sub>REF</sub> and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.



#### **PD# De-assertion**

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC\_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.



#### SRC\_STOP#

The SRC\_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC\_IN for this input to work properly. The SRC\_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

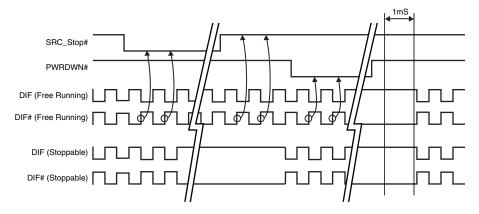
#### SRC\_STOP# - Assertion

Asserting SRC\_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC\_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with  $6x_{REF}$  DIF# is not driven, but pulled low by the termination. When the SRC\_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

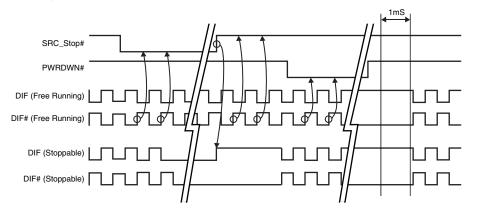
#### SRC\_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC\_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

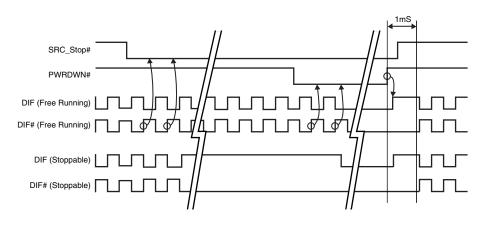
#### SRC\_STOP\_1 (SRC\_Stop = Driven, PD = Driven)



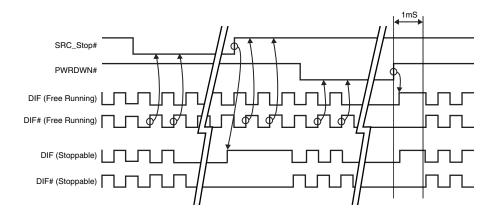
#### SRC\_STOP\_2 (SRC\_Stop =Tristate, PD = Driven)



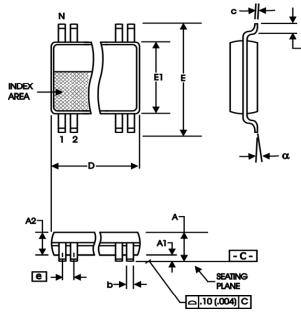
## SRC\_STOP\_3 (SRC\_Stop = Driven, PD = Tristate)



### SRC\_STOP\_4 (SRC\_Stop = Tristate, PD = Tristate)



## 28-pin SSOP Package Dimensions



		209 mil SSOP		
	In Milli	meters	In Inches	
SYMBOL	COMMON D	COMMON DIMENSIONS		IMENSIONS
	MIN	MAX	MIN	MAX
А		2.00		.079
A1	0.05		.002	
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
С	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
е	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
Ν	SEE VARIATIONS		SEE VAF	RIATIONS
α	0°	8°	0°	8°

#### VARIATIONS

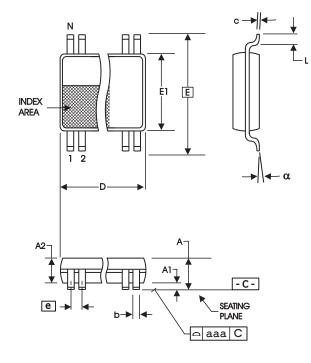
	N	D mm.		D (inch)	
IN	MIN	MAX	MIN	MAX	
	28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

209 mil SSOP

## 28-pin TSSOP Package Dimensions



(173 mil) (25.6 mil)					
	In Millimeters COMMON DIMENSIONS		In Inches		
SYMBOL			COMMON DIMENSIONS		
	MIN	MAX	MIN	MAX	
Α		1.20		.047	
A1	0.05	0.15	.002	.006	
A2	0.80	1.05	.032	.041	
b	0.19	0.30	.007	.012	
С	0.09	0.20	.0035	.008	
D	SEE VARIATIONS		SEE VARIATIONS		
E	6.40 BASIC		0.252 BASIC		
E1	4.30	4.50	.169	.177	
е	0.65 BASIC		0.0256 BASIC		
L	0.45	0.75	.018	.030	
N	SEE VARIATIONS		SEE VARIATIONS		
α	0°	8°	0°	8°	
aaa		0.10		.004	

## 4.40 mm. Body, 0.65 mm. Pitch TSSOP

#### VARIATIONS

N	D mm.		D (inch)		
	N	MIN	MAX	MIN	MAX
	28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

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## **Ordering Information**

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
9DB403DGLF	9DB403DGLF	Tubes	28-pin TSSOP	0 to +70° C
9DB403DGLFT	9DB403DGLF	Tape and Reel	28-pin TSSOP	0 to +70° C
9DB403DGILF	9DB403DGILF	Tubes	28-pin TSSOP	-40 to +85° C
9DB403DGILFT	9DB403DGILF	Tape and Reel	28-pin TSSOP	-40 to +85° C
9DB403DFLF	9DB403DFLF	Tubes	28-pin SSOP	0 to +70° C
9DB403DFLFT	9DB403DFLF	Tape and Reel	28-pin SSOP	0 to +70° C
9DB403DFILF	9DB403DFILF	Tubes	28-pin SSOP	-40 to +85° C
9DB403DFILFT	9DB403DFILF	Tape and Reel	28-pin SSOP	-40 to +85° C

#### "LF" denotes Pb-free package, RoHS compliant

#### "D" is the revision designator (will not correlate to datasheet revision)

#### **Revision History**

Rev.	Issue Date	Description	Page #
	11/26/2008	Updated SMBus table - Byte0:Byte3.	11
J	2/6/2009	Added Industrial temp. specs and ordering information.	Various
K	7/13/2009	Updated general description and block diagram	1
		1. Clarified that Vih and Vil values were for Single ended inputs	
		2. Added separate Idd values for the 9DB403	
L	10/7/2009	3. Added Differential Clock input parameters.	Various
М	1/27/2011	Updated Termination Figure 4	10
		1. Update pin 1 pin-name and pin description from VDD to VDDR. This	
		highlights that optimal peformance is obtained by treating VDDR as in analog	
Ν	5/6/2011	pin. This is a document update only, there is no silicon change.	Various
Р	8/27/2012	Updated Vswing conditions to include "single-ended measurement"	5
Q	9/18/2012	Updated Byte 2, bits 1, 2, 5 and 6 per char review. Outputs can be programmed with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE pins.	12
R	11/1/2012	Updated Input-to-Output Skew max value (Bypass Mode condition only) from 4500ps to 5000ps per latest characterization data.	7

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#### **Corporate Headquarters**

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138 United States 800 345 7015 +408 284 8200 (outside U.S.)

#### Asia Pacific and Japan

Integrated Device Technology Singapore (1997) Pte. Ltd. Reg. No. 199707558G 435 Orchard Road #20-03 Wisma Atria Singapore 238877 +65 6 887 5505

#### Europe

IDT Europe, Limited Prime House Barnett Wood Lane Leatherhead, Surrey United Kingdom KT22 7DE +44 1372 363 339



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