

150mA Dual LDO with Low Noise, High PSRR, and Low I_Q

ISL9016

ISL9016 is a high performance dual LDO capable of providing up to 150mA current on each channel. It features a low standby current and very high PSRR and is stable with output capacitance of 1μF to 4.7μF with an ESR of up to 200mΩ.

The device integrates a separate enable function for each output. The quiescent current is typically 49μA when only one LDO is enabled and typically 80μA when both LDOs are enabled. When both LDOs are under shutdown condition, the drawing current is typically less than 1μA.

ISL9016 provides a wide input voltage range from 1.8V to 6.5V. It also has a high PSRR of 80dB at 1kHz and 45dB at 1MHz. ISL9016 also provides output current limit, overheat protection, reverse current protection, as well as excellent load transient response.

ISL9016 is offered in a tiny 1.6mmx1.6mm 6 Ld μTDFN package. Output voltage options are available from 1.2V to 3.3V. Several combinations of voltage outputs are standard and others may be available upon request.

Features

- Dual Integrated 150mA High Performance LDOs
- High PSRR: 80dB @ 1kHz and 45dB @ 1MHz
- Reverse Current Protection
- Low Quiescent Current
 - 49μA (Single LDO Enabled)/80μA (Dual LDOs Enabled)
- Excellent Load Transient Response
- Typically ±0.8% Output Voltage Accuracy
- Low Output Noise: Typically 25μV_{RMS}
- Wide Input Voltage Capability: 1.8V to 6.5V
- Low Dropout Voltage: Typically 120mV @ 150mA
- Separate Enable Control for each LDO
- Stable with 1μF to 4.7μF Ceramic Output Capacitors
- Soft-start to Limit Input Current Surge During Enable
- Current Limit and Overheat Protection
- Tiny 6 Ld 1.6mmx1.6mm μTDFN package
- Pb-free (RoHS Compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3/4 Players, PMP, DSC
- Handheld Devices including Medical Handhelds

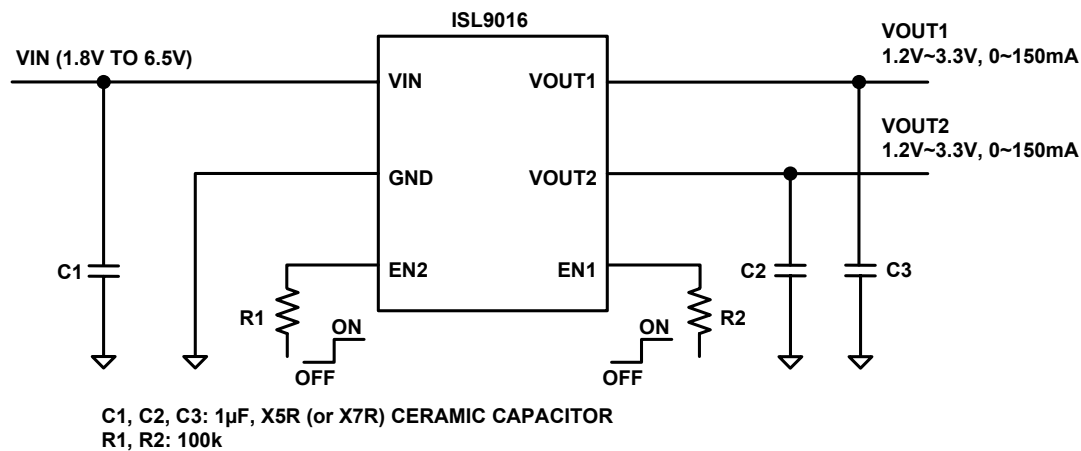
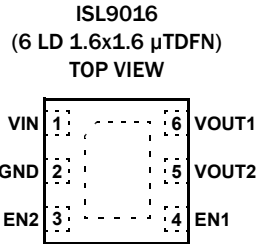


FIGURE 1. TYPICAL APPLICATION DIAGRAM

ISL9016

Pin Configuration



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	VIN	Supply Voltage/LDO Input. Connect a 1 μ F capacitor to GND.
2	GND	GND is the connection to system ground. Connect to PCB Ground plane.
3	EN2	LDO2 Enable pin. Enable = High, Disable = Low. A 100k resistor should be connected between EN2 and the control voltage rail. Do NOT leave it floating.
4	EN1	LDO1 Enable pin. Enable = High, Disable = Low. A 100k resistor should be connected between EN1 and the control voltage rail. Do NOT leave it floating.
5	VOUT2	LDO2 Output. Connect capacitor with a value from 1 μ F to 4.7 μ F to GND (1 μ F recommended).
6	VOUT1	LDO1 Output. Connect capacitor with a value from 1 μ F to 4.7 μ F to GND (1 μ F recommended).
-	E-Pad	Connect the e-pad to the system ground.

Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	VO1 VOLTAGE (V) (Note 2)	VO2 VOLTAGE (V) (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL9016IRUWCZ-T	N7	1.2	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUWGZ-T	N6	1.2	2.7	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUWJZ-T	N2	1.2	2.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUWKZ-T	N1	1.2	2.85	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUBWZ-T	R7	1.5	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUBBZ-T	R6	1.5	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUCWZ-T	R5	1.8	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUCBZ-T	R4	1.8	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUCCZ-T	U7	1.8	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUFWZ-T	R3	2.5	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUFBZ-T	N8	2.5	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUFCZ-T	N9	2.5	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUFFZ-T	P0	2.5	2.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUGWZ-T	P1	2.7	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUGCZ-T	R2	2.7	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUGGZ-T	N3	2.7	2.7	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUJWZ-T	P2	2.8	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUJBZ-T	P3	2.8	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUJCZ-T	N4	2.8	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUJJZ-T	N0	2.8	2.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUKWZ-T	P5	2.85	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUKFZ-T	P4	2.85	2.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUKKZ-T	N5	2.85	2.85	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUMWZ-T	P6	3.0	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUMBZ-T	P7	3.0	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUMCZ-T	P8	3.0	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUMKZ-T	P9	3.0	2.85	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUNWZ-T	R0	3.3	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9016IRUNCZ-T	R1	3.3	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. For other output voltages, contact Intersil marketing or local sales office.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and Tin Bismuth plate - e6 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for [ISL9016](#). For more information on MSL please see techbrief [TB363](#).

ISL9016

Absolute Maximum Ratings

V_{IN} to GND	-0.3V to +7.1V
All Other Pins to GND	-0.3 to ($V_{IN} + 0.3$)V

Recommended Operating Conditions

Supply Voltage (V_{IN})	1.8V to 6.5V
Each LDO Load Current	up to 150mA
Ambient Temperature Range (T_A)	-40 °C to +85 °C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
6 Ld μ TDFN Package (Note 5)	117.5
Junction Temperature Range	-40 °C to +125 °C
Operating Temperature Range	-40 °C to +85 °C
Storage Temperature Range	-65 °C to +150 °C
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications Typical specifications are measured at the following conditions: $T_A = +25$ °C; $V_{IN} = (V_O + 0.5V)$ to 6.5V with a minimum V_{IN} of 1.8V; $C_{IN} = 1\mu F$; $C_O = 1\mu F$. **Boldface limits apply over the operating temperature range, -40 °C to +85 °C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		1.8		6.5	V
UVLO Threshold	V_{UV+}			1.710	1.775	V
	V_{UV-}		1.55	1.62		
Input Quiescent Current		Quiescent condition: $I_{O1} = 0\mu A$; $I_{O2} = 0\mu A$				
	I_{DD1}	One LDO active		49	67	μA
	I_{DD2}	Both LDO active		80	100	μA
Shutdown Current	I_{DSD}	@ +25 °C		0.1	1.0	μA
Regulation Voltage Accuracy		$V_{IN} = V_O + 0.5V$ to 6.5V, $I_O = 10\mu A$ to 150mA, $T_A = +25$ °C	-0.8		+0.8	%
		$V_{IN} = V_O + 0.5V$ to 6.5V, $I_O = 10\mu A$ to 150mA, $T_A = -40$ °C to +85 °C	-1.8		+1.8	%
Maximum Output Current	I_{MAX}	Each LDO, Continuous	150			mA
Internal Current Limit	I_{LIM}		175	265	355	mA
Dropout Voltage (Note 6)	V_{D01}	$I_O = 150mA$; $1.2V \leq V_O \leq 2.1V$		250	425	mV
	V_{D02}	$I_O = 150mA$; $2.1V \leq V_O \leq 2.8V$		200	325	mV
	V_{D03}	$I_O = 150mA$; $2.8V \leq V_O$		120	200	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection		$I_O = 10mA$, $V_{IN} = 3.7V(\text{min})$, $V_O = 2.7V$, $T_A = +25$ °C				
		@ 1kHz		80		dB
		@ 10kHz		60		dB
		@ 100kHz		50		dB
		@ 1MHz		45		dB
Output Noise Voltage		$V_{IN} = 4.2V$, $I_O = 10mA$, $T_A = +25$ °C, BW = 10Hz to 100kHz		25		μV_{RMS}
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the $V_O(\text{nom})$		400	600	μs
LDO Soft-Start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	$\mu s/V$

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Electrical Specifications Typical specifications are measured at the following conditions: $T_A = +25^\circ\text{C}$; $V_{IN} = (V_O + 0.5\text{V})$ to 6.5V with a minimum V_{IN} of 1.8V; $C_{IN} = 1\mu\text{F}$; $C_O = 1\mu\text{F}$. **Boldface limits apply over the operating temperature range, -40°C to $+85^\circ\text{C}$. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
EN PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}	$T_A = -20^\circ\text{C}$ to $+85^\circ$	-0.3		0.4	V
Input High Voltage	V_{IH}		1.1		$V_{IN} + 0.3$	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	μA
REVERSE CURRENT CHARACTERISTICS						
Output Reverse Leakage Current (Note 7)	I_{ORLC}	$V_{IN} = 0\text{V}, V_{OUT} = 5.5\text{V}$		8	15	μA

NOTES:

- $V_{OX} = 0.98 \cdot V_{OX(NOM)}$; Valid for V_{OX} greater than 1.80V.
- Output reverse leakage current is measured with V_{IN} pin grounded and V_{OUT} pin connected to 5.5V.
- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ\text{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Operating Performance

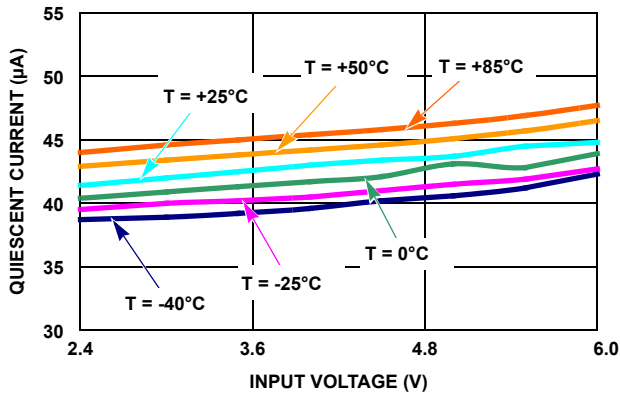


FIGURE 2. QUIESCENT CURRENT vs INPUT VOLTAGE ($V_{OUT1} = 2.1V$, ONLY LDO1 ENABLED)

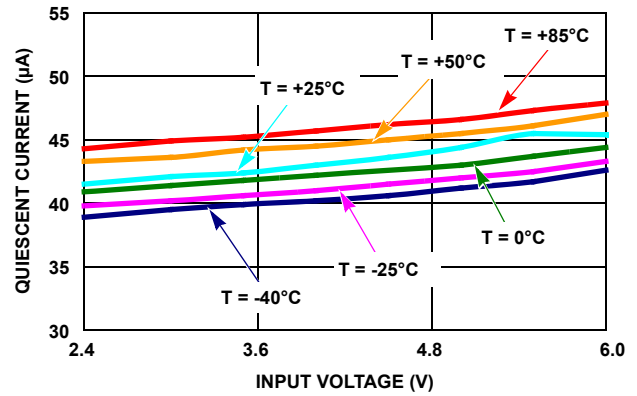


FIGURE 3. QUIESCENT CURRENT vs INPUT VOLTAGE ($V_{OUT2} = 2.1V$, ONLY LDO2 ENABLED)

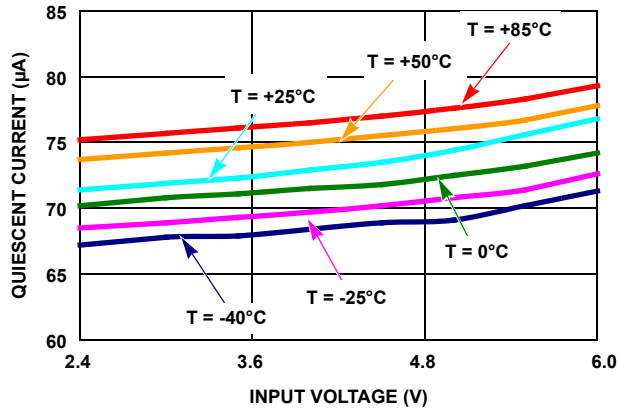


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE ($V_{OUT1} = V_{OUT2} = 2.1V$, LDO1 AND LDO2 ENABLED)

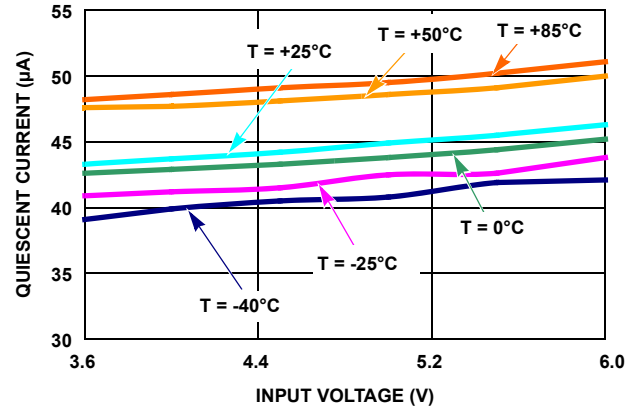


FIGURE 5. QUIESCENT CURRENT vs INPUT VOLTAGE ($V_{OUT1} = 3.3V$, ONLY LDO1 ENABLED)

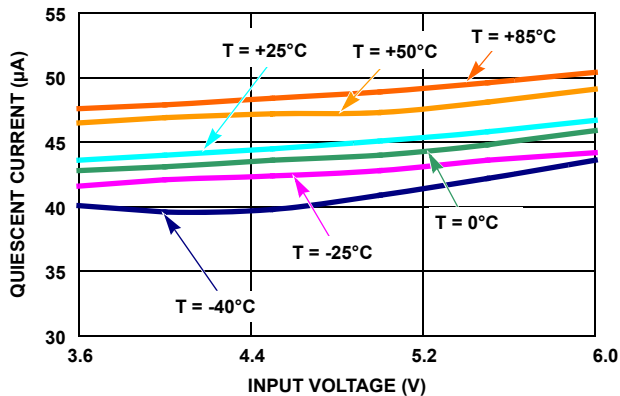


FIGURE 6. QUIESCENT CURRENT vs INPUT VOLTAGE ($V_{OUT2} = 3.3V$, ONLY LDO2 ENABLED)

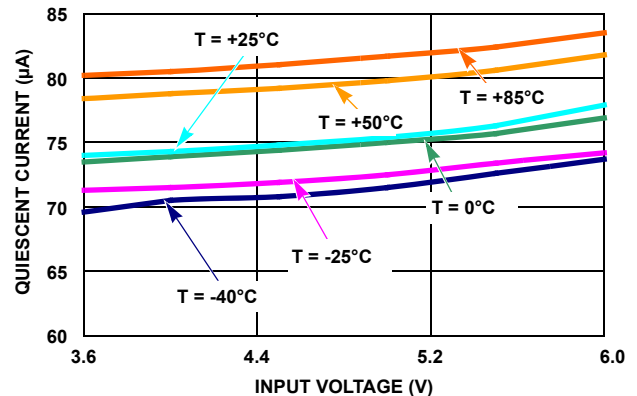


FIGURE 7. QUIESCENT CURRENT vs INPUT VOLTAGE ($V_{OUT1} = V_{OUT2} = 3.3V$, LDO1 AND LDO2 ENABLED)

Typical Operating Performance (Continued)

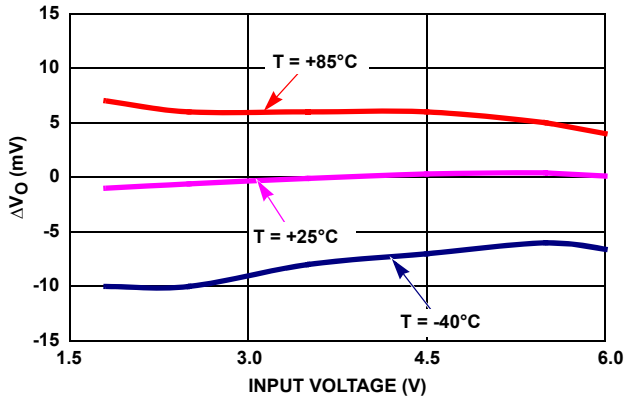


FIGURE 8. ΔV_{OUT} vs INPUT VOLTAGE ($V_{OUT_NOMINAL} = 1.2V$, $I_{OUT} = 50mA$)

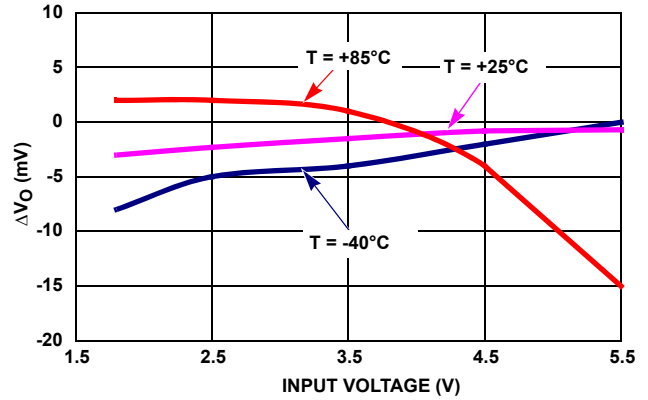


FIGURE 9. ΔV_{OUT} vs INPUT VOLTAGE ($V_{OUT_NOMINAL} = 1.2V$, $I_{OUT} = 150mA$)

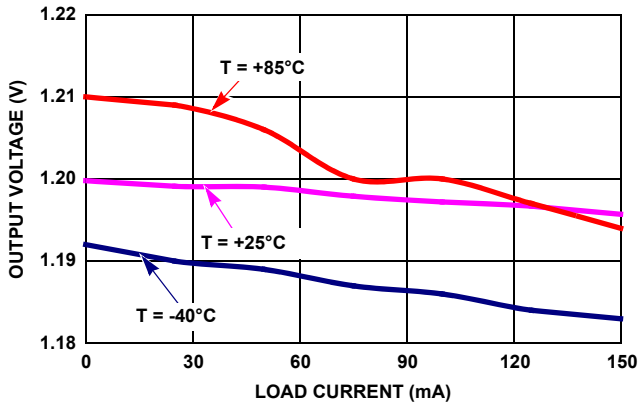


FIGURE 10. LOAD REGULATION ($V_{IN} = 1.8V$, $V_{OUT} = 1.2V$)

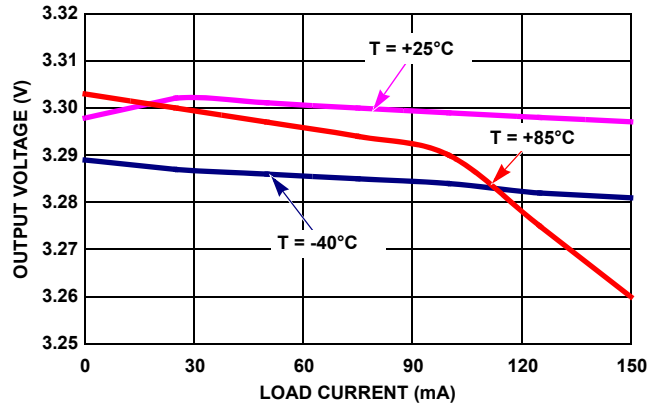


FIGURE 11. LOAD REGULATION ($V_{IN} = 4.5V$, $V_{OUT} = 3.3V$)

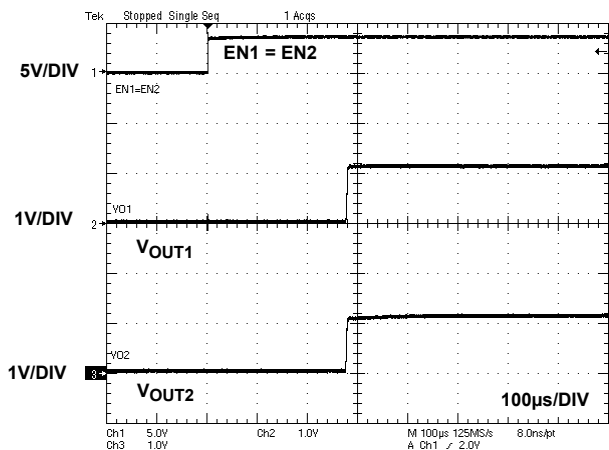


FIGURE 12. ENABLE OPERATION ($V_{IN} = 3.6V$, $V_{OUT1} = V_{OUT2} = 1.2V$)

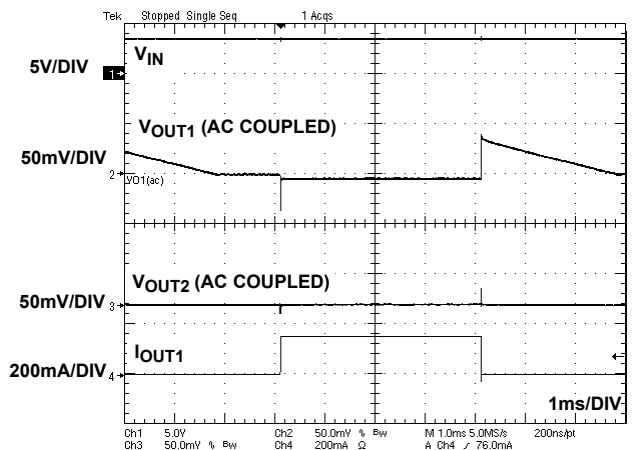


FIGURE 13. LOAD TRANSIENT RESPONSE ($V_{IN} = 3.6V$, $V_{OUT1} = V_{OUT2} = 1.2V$, $I_{OUT1} 0.01mA$ TO $150mA$)

Typical Operating Performance (Continued)

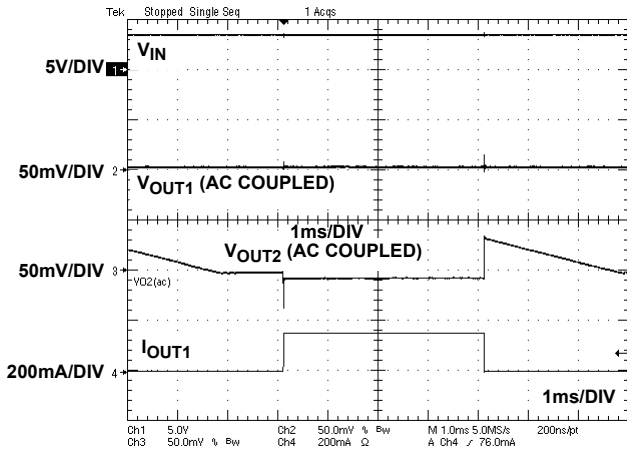


FIGURE 14. LOAD TRANSIENT RESPONSE ($V_{IN} = 3.6V$, $V_{OUT1} = V_{OUT2} = 1.2V$, I_{OUT2} 0.01mA TO 150mA)

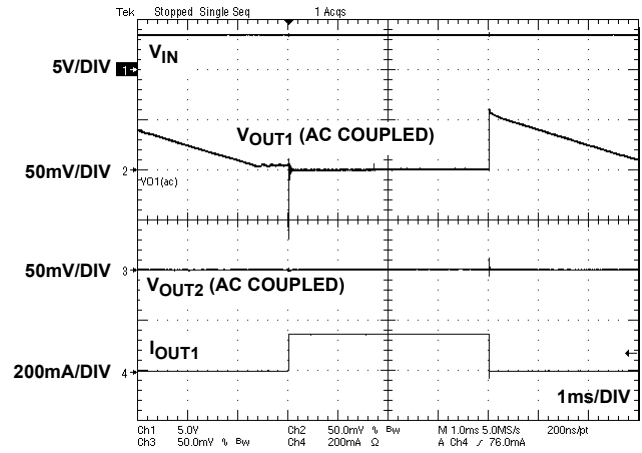


FIGURE 15. LOAD TRANSIENT RESPONSE ($V_{IN} = 3.6V$, $V_{OUT1} = V_{OUT2} = 3.3V$, I_{OUT1} 0.01mA TO 150mA)

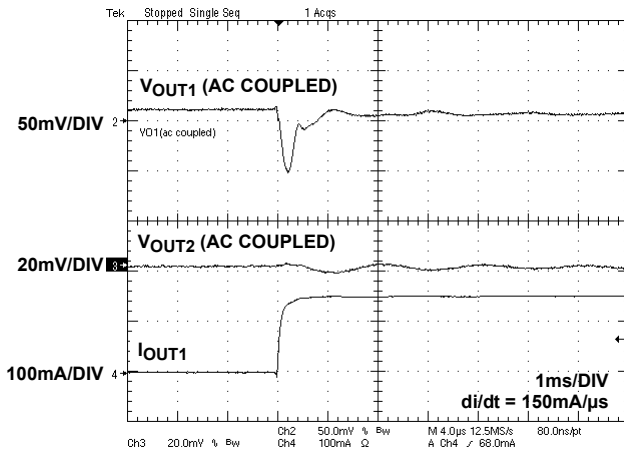


FIGURE 16. LOAD TRANSIENT RESPONSE ($V_{IN} = 1.8V$, $V_{OUT1} = V_{OUT2} = 1.2V$, I_{OUT1} 0.01mA TO 150mA)

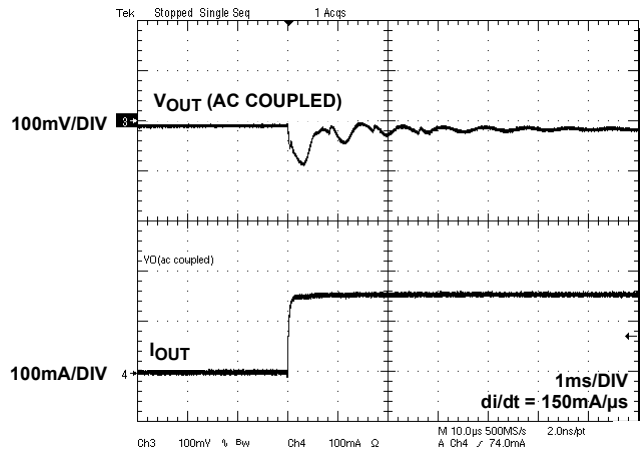


FIGURE 17. LOAD TRANSIENT RESPONSE ($V_{IN} = 3.3V$, $V_{OUT1} = V_{OUT2} = 1.2V$, I_{OUT1} 0.01mA TO 150mA)

ISL9016

Input and Output Capacitors

The ISL9016 provides a linear regulator that has low quiescent current, fast transient response, and overall stability across the recommended operating conditions. A ceramic capacitor (X5R or X7R) with a capacitance of 1 μ F to 4.7 μ F with an ESR up to 200m Ω is suitable for the ISL9016 to maintain its output stability. The ground connection of the output capacitor should be connected directly to the GND pin of the device, and also placed close to the device. Similarly for the input capacitor, usually a 1 μ F ceramic capacitor (X5R or X7R) is suitable for most cases, but if large, fast rising-time load transient condition is expected, a higher value input capacitor may be necessary to achieve better performance.

Board Layout Recommendations

A good PCB layout will be an important step to achieve good performance. It is recommended to design the board with separate ground planes for input and output, and connect both ground planes at the GND pin of the device. Consideration should be taken when placing the components and route the trace to minimize the ground impedance, as well as keep the parasitic inductance low. Usually the input/output capacitors should be placed close to the device with good ground connection.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
April 26, 2011	FN6832.1	Added ISL9016IRUCCZ-T to Ordering Information table.
January 22, 2009	FN6832.0	Initial release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL9016](http://www.intersil.com/ISL9016)

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: <http://rel.intersil.com/reports/sear>

For additional products, see www.intersil.com/product_tree

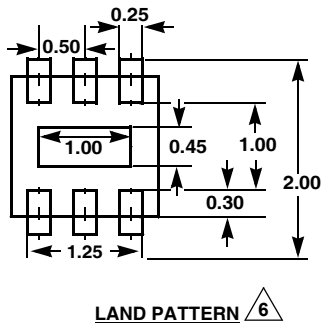
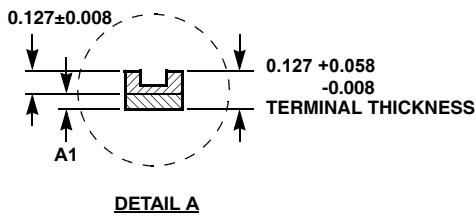
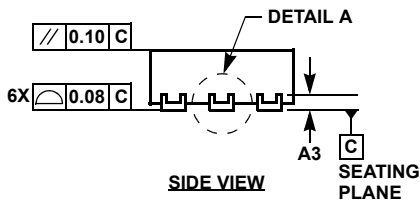
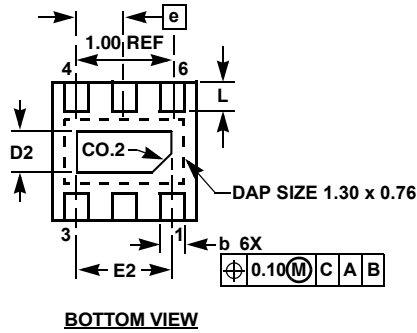
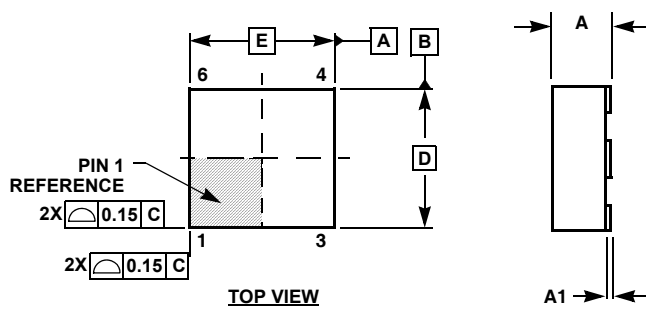
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ISL9016

Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e	0.50 BSC			-
L	0.25	0.30	0.35	-

Rev. 1 6/06

NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.