Single Phase Core Controller for VR12.6

ISL95813

The ISL95813 single-phase controller provides a fully compliant VR12.6 power supply solution for Intel™ microprocessors. It provides a tightly regulated output voltage that is programmed through a high speed serial bus interface with the CPU. This interface also allows the CPU to acquire real-time information from the voltage regulator (VR), which includes load current and VR temperature.

Based on Intersil's Robust Ripple Regulator (R3™) technology, the PWM modulator provides faster transient response and settling time when compared against traditional modulation schemes. Its variable frequency topology also allows for natural period stretching discontinuous conduction mode (DCM) for increased efficiency and power savings in light load situations.

The ISL95813 has several other key features that include: DCR current sensing with single NTC thermal compensation; discrete resistor current sensing; differential remote voltage feedback; and user-programmable boot voltage, I_{MAX}, T_{MAX}, voltage transition slew rate, and switching frequency.

Features

- Full VR12.6 specification compliance
- Wide input voltage range: 4.6V to 25V
- R3™ control architecture delivers excellent transient response and power state mode transitions
- Current monitor (IMON) with temperature compensation
- VRHOT# indicator for CPU protection
- Digitally selectable switching frequency:
  - 425kHz, 550kHz, 700kHz with ECO and PRO options
- Enhanced light-load efficiency discontinuous conduction mode operation
- Ultra-small 20 lead 3mmx4mm QFN package
- Enable and power-good monitor

Applications

- Notebook Computers
- Tablets, Ultrabooks™, and AIO

Related Literature

- AN1846 Designer's Guide to the ISL95813 Evaluation Board

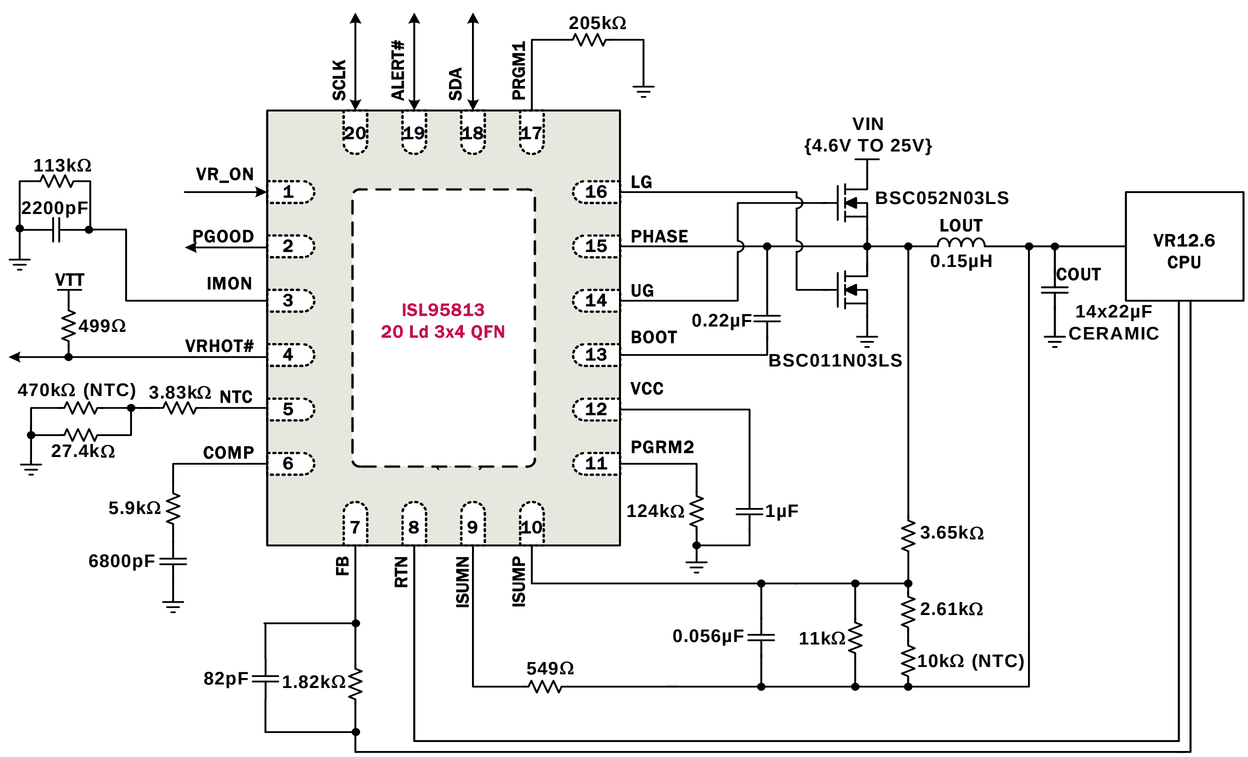


FIGURE 1. TYPICAL 40Amax, 12.6, APPLICATION DIAGRAM

Ordering Information

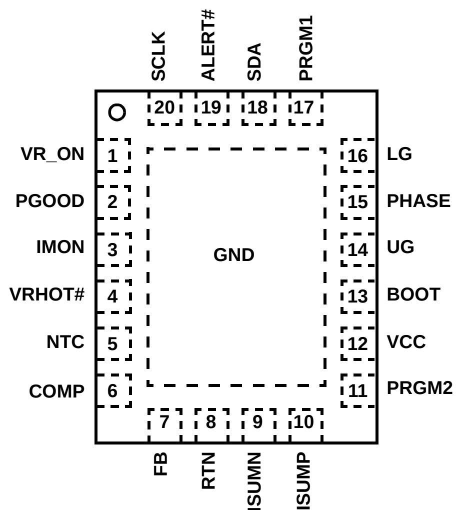
PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95813HRZ	813H	-10 to +100	20 LD 3x4 QFN	L20.3x4
ISL95813IRZ	813I	-40 to +100	20 LD 3x4 QFN	L20.3x4
ISL95813EV1Z	Evaluation Board			

NOTES:

1. Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95813. For more information on MSL, please see tech brief TB363.

Pin Configuration

ISL95813
(20 LD 3X4 QFN)
TOP VIEW



Pin Descriptions

PIN	NAME	FUNCTION	
1	VR_ON	Digital Input	Enable input for controller. Connect to ground to disable the part. Connect to VCC to initiate soft-start and regulation.
2	PGOOD	Digital Output	Power-Good open-drain output indicating when VR is in regulation with no faults detected. Pull up externally with a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.
3	IMON	Analog Output: [Small-signal]	VR output current monitor. IMON pin sources a current proportional to the regulator output current. A resistor connected from this pin to ground will set a voltage that is proportional to the load current. This voltage is sampled with an internal ADC to produce a digital IMON signal that can be read through the serial communications bus.
4	VRHOT#	Digital Output	Open drain thermal overload output indicator. Can be considered part of communication bus with CPU.
5	NTC	Analog Input: [Small-Signal]	Thermistor input to VR_HOT# circuit. Used to monitor VR temperature.
6	COMP	Analog Output: [Small-signal]	Output of the gm error-amplifier for loop control. Connect to ground through the compensation network.

Pin Descriptions (Continued)

PIN	NAME	FUNCTION	
7	FB	Analog Input: [Small-signal]	Output voltage feedback sensing input for regulation. Connect via resistor to VCC_{SENSE} on CPU.
8	RTN	Analog Input: [Small-signal]	Ground return for differential remote output voltage sensing.Connect via resistor to VCC_{SENSE} on CPU.
9	ISUMN	Analog Input: [Small-signal]	VR Loadline, Droop, and DCR sensing input.
10	ISUMP	Analog Input: [Small-signal]	VR Loadline, Droop, and DCR sensing input.
11	PRGM2	Analog Input: [Small-signal]	ADC input to program switching frequency and boot voltage using a resistor to ground. See "PROGRAM 2 Pin" on page 13 for all programming options.
12	VCC	Analog Input: [Small-signal]	5V IC bias supply input. Bypass to ground with a high-quality 0.1µF ceramic capacitor.
13	BOOT	Analog Input: [Power]	Floating high-side gate drive voltage supply. Connect to PHASE with a 0.1µF to 0.22µF high-quality ceramic capacitor.
14	UG	Analog Output: [Power]	Upper MOSFET gate drive. Connect with a wide trace to the gate of the upper switching MOSFET.
15	PHASE	Analog I/O: [Power]	Switching node and upper MOSFET gate drive return path. Connect with a wide trace to the source of the upper switching MOSFET, the drain of the lower switching MOSFET, and the output inductor.
16	LG	Analog Output: [Power]	Lower MOSFET gate drive. Connect with a wide trace to the gate of the lower switching MOSFET.
17	PRGM1	Analog Input: [Small-signal]	ADC input to program I_{CCMAX} and FSEL bit using a resistor to ground. See "PROGRAM 1 Pin" on page 13 for all programming options.
18	SDA	Digital I/O	Data input/output for CPU serial interface.
19	ALERT#	Digital Output	Alert signal for CPU serial interface.
20	SCLK	Digital Input	Clock input for CPU serial interface.
e-pad	GND	Analog Input: [Power]	Ground reference for IC as well as gate drive power ground return path. Connect to system ground plane with multiple vias.

Absolute Maximum Ratings

Supply Voltage, VCC . . . . -0.3V to +7V
Battery Voltage, VIN . . . . +28V
Boot Voltage (BOOT). . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . -0.3V to +7V(DC)
. . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . PHASE-0.3V (DC) to BOOT
. . . . PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage
. . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . -0.3V to (VDD + 0.3V)
Open Drain Outputs, PGOOD, VR_HOT#, ALERT#. . . . . -0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5)	44	6

Maximum Junction Temperature . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VCC . . . . +5V ±5%
Battery Voltage, VIN . . . . 4.6V to 25V
Ambient Temperature
HRZ. . . . . -10°C to +100°C
IRZ . . . . -40°C to +100°C
Junction Temperature
HRZ. . . . . -10°C to +125°C
IRZ . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VDD = 5V, T_A = -10°C to +100°C or -40°C to +100°C, f_{SW} = 700kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range for High Temp Commercial at -10°C to +100°C or Industrial Temp at -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 1V		3.5	**5**	mA
		VR_ON = 0V			**1**	µA
		PS4 State		90	**150**	µA
POWER-ON-RESET THRESHOLDS						
VDD Power-On-Reset Threshold	$VDDPOR_r$	V_{DD} rising		4.35	**4.5**	V
	$VDDPOR_f$	V_{DD} falling	**4.00**	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	HRZ %Error (V_{OUT})	VID = 1.50V to 2.30V	**-0.5**		**+0.5**	%
		VID = 1.00V to 1.49V	**-8**		**+8**	mV
		VID = 0.50V to 0.99V	**-10**		**+10**	mV
	IRZ %Error (V_{OUT})	VID = 1.50V to 2.30V	**-1**		**+1**	%
		VID = 1.00V to 1.49V	**-15**		**+15**	mV
		VID = 0.50V to 0.99V	**-20**		**+20**	mV
Internal V_{BOOT}		HRTZ (Set by R_PROG2)	**1.683**	1.7	**1.717**	V
		IRTZ (Set by R_PROG2)	**1.675**	1.7	**1.725**	V
Maximum Output Voltage	$V_{OUT(MAX)}$	VID = [11111111]		2.3		V
Minimum Output Voltage	$V_{OUT(MIN)}$	VID = [00000001]		0.5		V

Electrical Specifications

Operating Conditions: VDD = 5V, T_A = -10°C to +100°C or -40°C to +100°C, f_{SW} = 700kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range for High Temp Commercial at -10°C to +100°C or Industrial Temp at -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CHANNEL FREQUENCY						
425kHz Configuration	f_{SW_425k}	Set by R_PROG1	**395**	425	**455**	kHz
550kHz Configuration	f_{SW_550k}		**510**	550	**590**	kHz
700kHz Configuration	f_{SW_700k}		**650**	700	**750**	kHz
1000kHz Configuration	f_{SW_1000k}	Set by R_PROG1 (PRO PS2/PS3 only)	**915**	985	**1055**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I_{FB} = 0A, HRZ	**-0.2**		**+0.2**	mV
		I_{FB} = 0A, IRZ	**-0.3**		**+0.3**	mV
Error Amp DC Gain (Note 7)	A_{V0}			90		dB
Error Amp Gain-Bandwidth Product (Note 7)	GBW	C_L = 20pF		18		MHz
POWER-GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.15	**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V			**1**	µA
PGOOD Delay	tpgd	V_{BOOT} = 1.7V		1.2		ms
ALERT# Low Voltage (Note 6)				7	**12**	Ω
VR_HOT# Low Voltage (Note 6)				7	**12**	Ω
ALERT# Leakage Current					**1**	µA
VR_HOT# Leakage Current					**1**	µA
GATE DRIVER						
UGATE Pull-Up Resistance (Note 7)	R_{UGPU}	200mA Source Current		1.0	**1.5**	Ω
UGATE Source Current (Note 7)	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance (Note 7)	R_{UGPD}	250mA Sink Current		1.0	**1.5**	Ω
UGATE Sink Current (Note 7)	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance (Note 7)	R_{LGPU}	250mA Source Current		1.0	**1.5**	Ω
LGATE Source Current (Note 7)	I_{LGSRC}	LGATE - GND= 2.5V		2.0		A
LGATE Sink Resistance (Note 7)	R_{LGPD}	250mA Sink Current		0.5	**0.9**	Ω
LGATE Sink Current (Note 7)	I_{LGSNK}	LGATE - GND = 2.5V		4.0		A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load		17		ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load		29		ns
BOOTSTRAP DIODE						
ON-Resistance	R_F			22		Ω
Reverse Leakage	I_R	V_R = 25V		0.2		µA
PROTECTION						
Overvoltage Threshold	OV_H	ISUMN rising above setpoint for >1µs	**240**	300	**360**	mV
Overcurrent Threshold			**56**	60	**64**	µA
LOGIC THRESHOLDS						
VR_ON Input Low	V_{IL}				**0.3**	V
VR_ON Input High	V_{IH}	HRZ	**0.7**			V
	V_{IH}	IRZ	**0.75**			V
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	**58**	60	**62**	µA
VR_HOT# Trip Voltage		Falling	**0.881**	0.893	**0.905**	V
VR_HOT# Reset Voltage		Rising	**0.924**	0.936	**0.948**	V

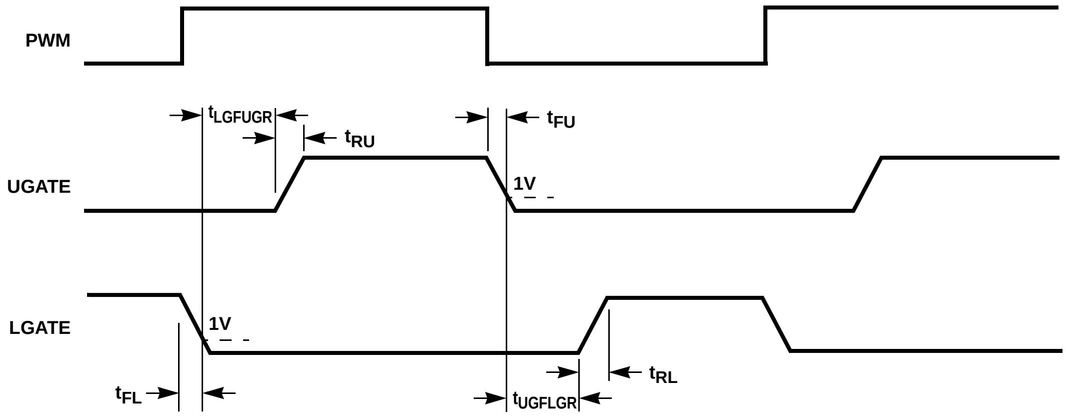
Electrical Specifications Operating Conditions: VDD = 5V, T_A = -10°C to +100°C or -40°C to +100°C, f_{SW} = 700kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range for High Temp Commercial at -10°C to +100°C or Industrial Temp at -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Therm_Alert Trip Voltage		Falling	**0.92**	0.932	**0.944**	V
Therm_Alert Reset Voltage		Rising	**0.962**	0.974	**0.986**	V
CURRENT MONITOR						
IMON Output Current	I_{IMON}	ISUMN pin current = 40µA	**9.7**	10	**10.3**	µA
		ISUMN pin current = 20µA	**4.8**	5	**5.2**	µA
		ISUMN pin current = 4µA	**0.875**	1	**1.125**	µA
I_{CCMAX} Alert Trip Voltage	$V_{IMONMAX}$	Rising	1.185	1.2	**1.215**	V
I_{CCMAX} Alert Reset Voltage		Falling	1.122	1.14	1.152	V
INPUTS						
VR_ON Leakage Current	I_{VR_ON}	VR_ON = 0V	**-1**	0	1	µA
		VR_ON = 1V		3	**5**	µA
SCLK, SDA Leakage		VR_ON = 0V, SCLK & SDA = 0V & 1V	**-1**		**1**	µA
		VR_ON = 1V, SCLK & SDA = 1V	**-5**		**1**	µA
		VR_ON = 1V, SCLK & SDA = 0V, SCLK		-42		µA
		VR_ON = 1V, SCLK & SDA = 0V, SDA		-21		µA
SLEW RATE (For VID Change)						
Fast Slew Rate		Set by R_PROG2	**12**			mV/µs
Slow Slew Rate		Default setting Fast Slew divided by 4	**3**			mV/µs

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.

Gate Driver Timing Diagram



Typical Performance Waveforms (V_{IN} = 19V, 700kHz, PRO)

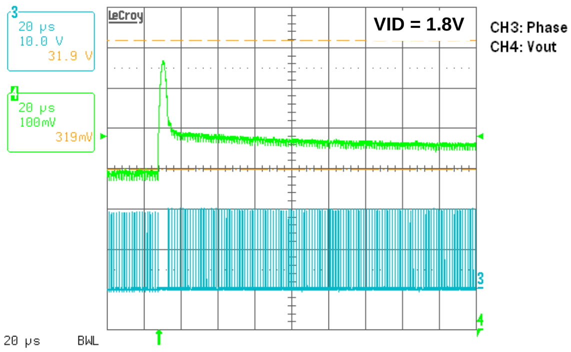


FIGURE 2. PS0, 1-35A LOAD RELEASE

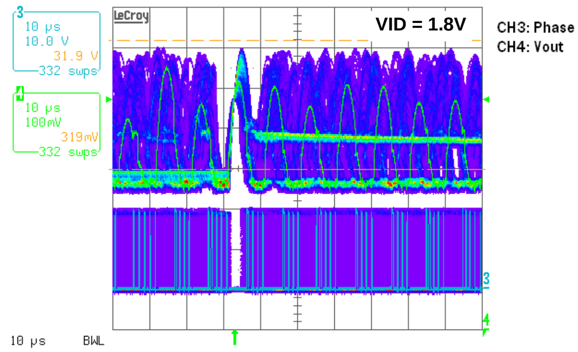


FIGURE 3. PS0, 1-35A HIGH REP LOAD TRANSIENT

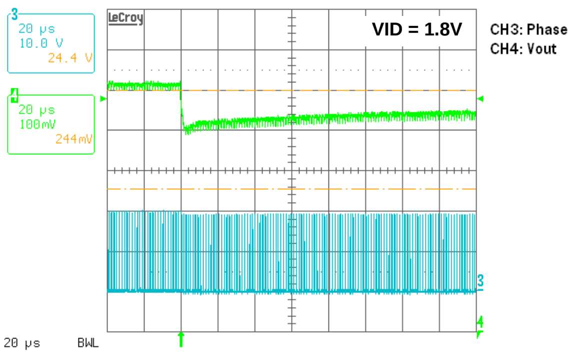


FIGURE 4. PS0, 1-35A LOAD INSERTION

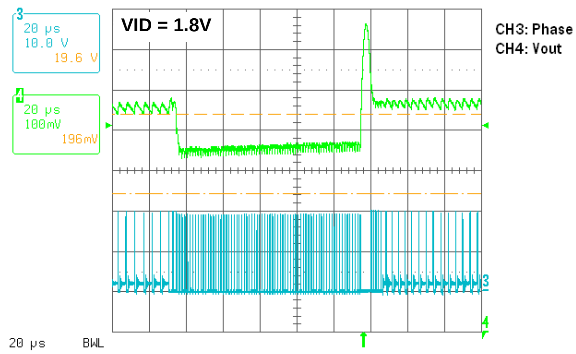


FIGURE 5. PS3 TO PS0, 1-35A TRANSIENT

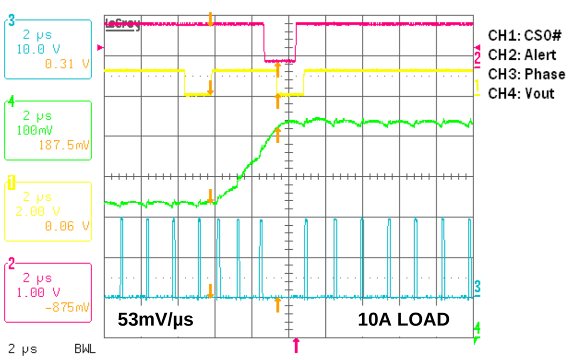


FIGURE 6. PS0, SET VID FAST FROM 1.6V TO 1.8V

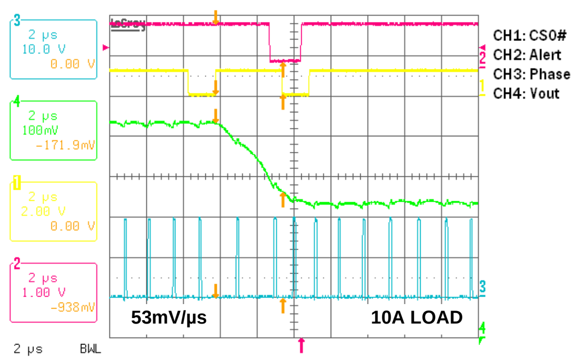


FIGURE 7. PS0, SET VID FAST FROM 1.8V TO 1.6V

Typical Performance Waveforms (V_{IN} = 19V, 700kHz, PRO)

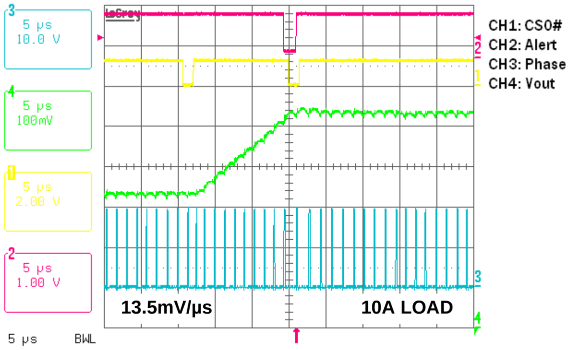


FIGURE 8. PS0, SET VID FAST FROM 1.6V TO 1.8V

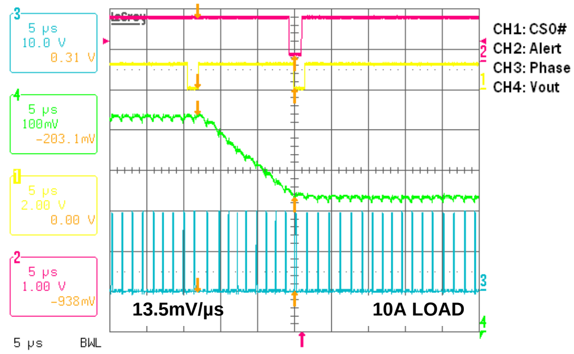


FIGURE 9. PS0, SET VID FAST FROM 1.8V TO 1.6V

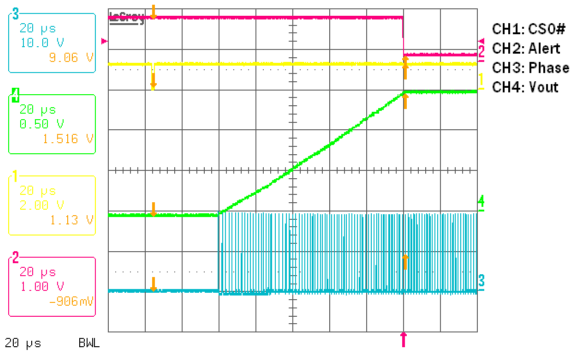


FIGURE 10. PS4 EXIT TO 1.6V, IO = 1A, SLEWRATE = 53mV/µs

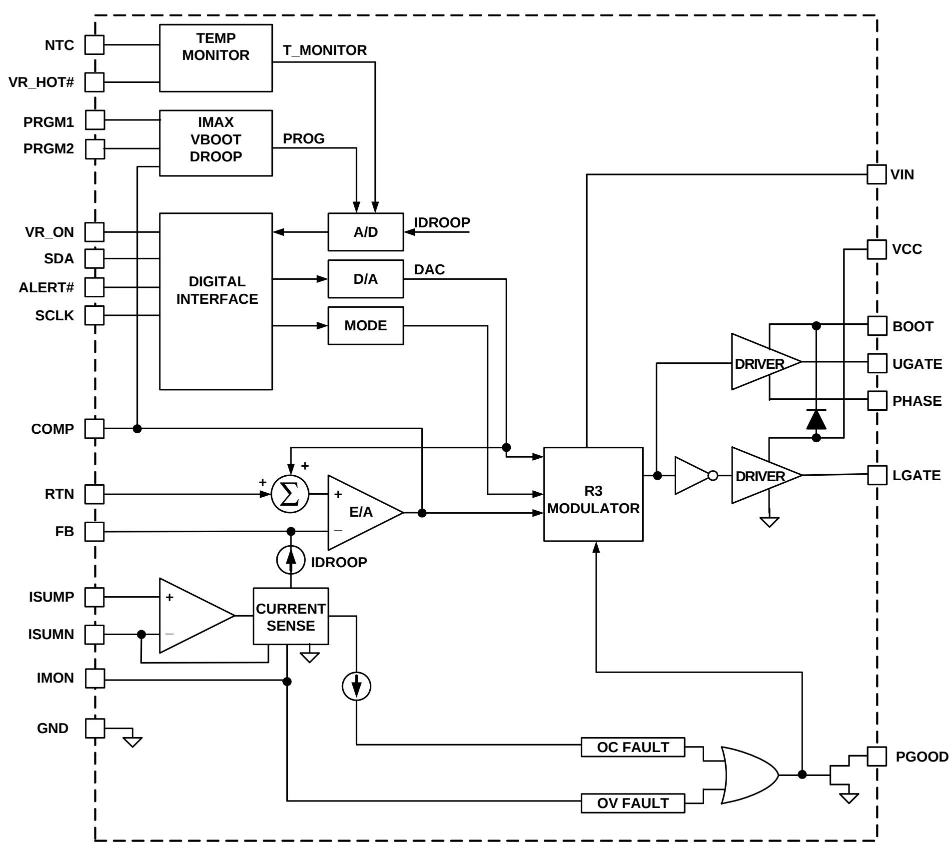


FIGURE 11. BLOCK DIAGRAM

Theory of Operation

R^3™ Modulator

The R^3™ Modulator is Intersil's proprietary synthetic current-mode hysteretic controller and is a blend of fixed frequency PWM and variable frequency hysteretic control technology. This modulator topology offers high noise immunity and a rapid transient response to dynamic load scenarios. Under static conditions the desired switching frequency is maintained within the entire specified range of input voltages, output voltages, and load currents. During load transients the controller will increase or decrease the PWM pulses and switching frequency to maintain output voltage regulation. Figure 12 illustrates this effect during a load insertion. As the window voltage starts to climb from a load step the time between PWM pulses decreases as f_{SW} increases to keep the output within regulation.

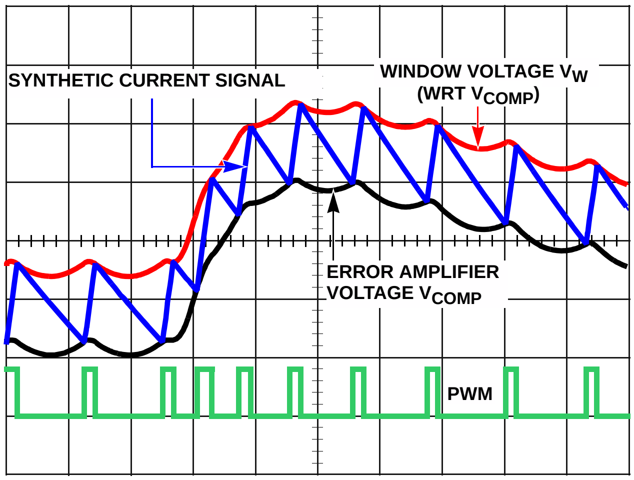


FIGURE 12. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

Diode Emulation and Period Stretching

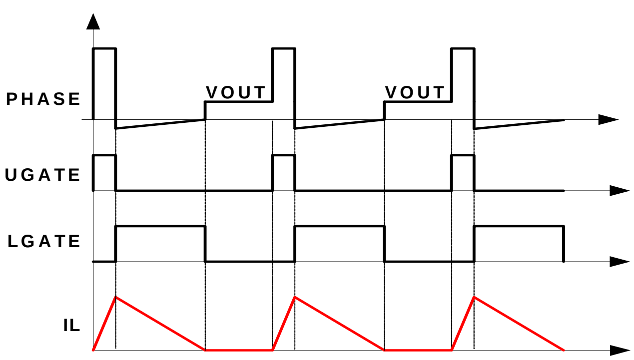


FIGURE 13. DIODE EMULATION

The ISL95813 can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts only when the current is flowing from source to drain and does not allow reverse current, emulating a diode like a standard buck regulator. As Figure 13 shows, when LGATE is on, the low-side MOSFET conducts, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The controller monitors the current through monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing direction.

If the load current reaches the critical conduction point the inductor current will reach and stay at zero before the next phase node pulse and the regulator is in discontinuous conduction mode (DCM). Should the load current rise above the critical conduction point, the inductor current will not cross 0A in a switching cycle, and the regulator is in CCM although the controller is in DE mode.Equation 1 below gives the formula for critical conduction, where $I_{critical}$ is the load current for critical conduction and ΔI_L is the ripple on the inductor current.

$$I_{critical} = \frac{\Delta I_L}{2} \quad \text{(EQ. 1)}$$

Figure 14 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the peak inductor current the same in the three cases. The controller clamps the synthetic current DE mode to make it mimic the inductor current. It takes the synthesized current longer to hit the lower window voltage, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. By reducing the switching frequency in DE mode switching losses are decreased and light load efficiency is improved.

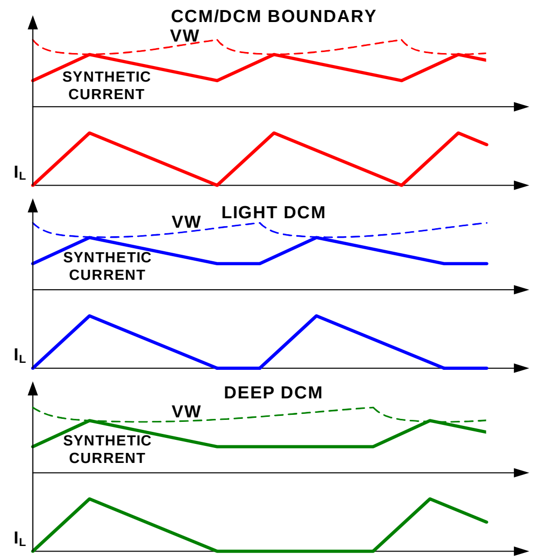


FIGURE 14. PERIOD STRETCHING

ECO and PRO Mode DCM

The ISL95813 has the ability to set both ECO and PRO mode DCM options for 700kHz switching applications. In ECO mode the time from Upper Gate On to Lower Gate Off is set to $^1/_{700kHz}$ or 1.43µs. When PRO mode is selected the UG On to LG Off time is reduced to $^1/_{1MHz}$ or 1.0µs. For applications where efficiency is important ECO mode should be implemented as the longer switching times reduce the amount of switching loss in the FETs. PRO mode is ideal for applications that require lower DCM ripple as the shorter gate times reduce the amount of output ripple. Because of the reduced ripple in PRO mode the amount of output capacitance can be reduced, saving both board space and BOM costs.

See “PROGRAM 1 RESISTOR VALUES” on page 13 for the ECO/PRO programming resistor options.

Start-up Timing

With the controller's V_{DD} voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the logic high threshold. Figure 15 shows the typical start-up timing. The controller uses digital soft-start to ramp-up DAC to the voltage programmed by the SetVID command. PGOOD is asserted high and ALERT# is asserted low at the end of the ramp up. Similar results occur if VR_ON is tied to V_{DD}, with the soft-start sequence starting 1.1ms after V_{DD} crosses the POR threshold.

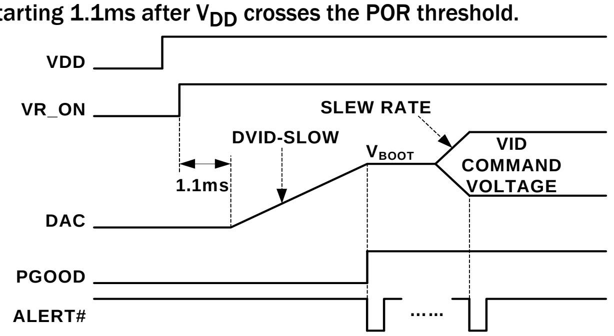


FIGURE 15. SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the start-up sequence, the controller regulates the output voltage to the value set by the VID information in Table 1. The controller will control the no-load output voltage to an accuracy of ±0.5% over the VID voltage range. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die. Current silicon maximum VID is set as 2.3V, and any VID command above 2.3V will be rejected.

TABLE 1. VID TABLE

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			VR12.6
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.50000
0	0	0	0	0	0	1	0	0	2	0.51000
0	0	0	0	0	0	1	1	0	3	0.52000
0	0	0	0	0	1	0	0	0	4	0.53000
0	0	0	0	0	1	0	1	0	5	0.54000
0	0	0	0	0	1	1	0	0	6	0.55000
0	0	0	0	0	1	1	1	0	7	0.56000
0	0	0	0	1	0	0	0	0	8	0.57000
0	0	0	0	1	0	0	1	0	9	0.58000
0	0	0	0	1	0	1	0	0	A	0.59000
0	0	0	0	1	0	1	1	0	B	0.60000
0	0	0	0	1	1	0	0	0	C	0.61000

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			VR12.6
0	0	0	0	1	1	0	1	0	D	0.62000
0	0	0	0	1	1	1	0	0	E	0.63000
0	0	0	0	1	1	1	1	0	F	0.64000
0	0	0	1	0	0	0	0	1	0	0.65000
0	0	0	1	0	0	0	1	1	1	0.66000
0	0	0	1	0	0	1	0	1	2	0.67000
0	0	0	1	0	0	1	1	1	3	0.68000
0	0	0	1	0	1	0	0	1	4	0.69000
0	0	0	1	0	1	0	1	1	5	0.70000
0	0	0	1	0	1	1	0	1	6	0.71000
0	0	0	1	0	1	1	1	1	7	0.72000
0	0	0	1	1	0	0	0	1	8	0.73000
0	0	0	1	1	0	0	1	1	9	0.74000
0	0	0	1	1	0	1	0	1	A	0.75000
0	0	0	1	1	0	1	1	1	B	0.76000
0	0	0	1	1	1	0	0	1	C	0.77000
0	0	0	1	1	1	0	1	1	D	0.78000
0	0	0	1	1	1	1	0	1	E	0.79000
0	0	0	1	1	1	1	1	1	F	0.80000
0	0	1	0	0	0	0	0	2	0	0.81000
0	0	1	0	0	0	0	1	2	1	0.82000
0	0	1	0	0	0	1	0	2	2	0.83000
0	0	1	0	0	0	1	1	2	3	0.84000
0	0	1	0	0	1	0	0	2	4	0.85000
0	0	1	0	0	1	0	1	2	5	0.86000
0	0	1	0	0	1	1	0	2	6	0.87000
0	0	1	0	0	1	1	1	2	7	0.88000
0	0	1	0	1	0	0	0	2	8	0.89000
0	0	1	0	1	0	0	1	2	9	0.90000
0	0	1	0	1	0	1	0	2	A	0.91000
0	0	1	0	1	0	1	1	2	B	0.92000
0	0	1	0	1	1	0	0	2	C	0.93000
0	0	1	0	1	1	0	1	2	D	0.94000
0	0	1	0	1	1	1	0	2	E	0.95000
0	0	1	0	1	1	1	1	2	F	0.96000
0	0	1	1	0	0	0	0	3	0	0.97000
0	0	1	1	0	0	0	1	3	1	0.98000
0	0	1	1	0	0	1	0	3	2	0.99000
0	0	1	1	0	0	1	1	3	3	1.00000

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0	Hex		VR12.6
0	0	1	1	0	1	0	0	3	4	1.01000
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0	0	1	1	0	1	1	0	3	6	1.03000
0	0	1	1	0	1	1	1	3	7	1.04000
0	0	1	1	1	0	0	0	3	8	1.05000
0	0	1	1	1	0	0	1	3	9	1.06000
0	0	1	1	1	0	1	0	3	A	1.07000
0	0	1	1	1	0	1	1	3	B	1.08000
0	0	1	1	1	1	0	0	3	C	1.09000
0	0	1	1	1	1	0	1	3	D	1.10000
0	0	1	1	1	1	1	0	3	E	1.11000
0	0	1	1	1	1	1	1	3	F	1.12000
0	1	0	0	0	0	0	0	4	0	1.13000
0	1	0	0	0	0	0	1	4	1	1.14000
0	1	0	0	0	0	1	0	4	2	1.15000
0	1	0	0	0	0	1	1	4	3	1.16000
0	1	0	0	0	1	0	0	4	4	1.17000
0	1	0	0	0	1	0	1	4	5	1.18000
0	1	0	0	0	1	1	0	4	6	1.19000
0	1	0	0	0	1	1	1	4	7	1.20000
0	1	0	0	1	0	0	0	4	8	1.21000
0	1	0	0	1	0	0	1	4	9	1.22000
0	1	0	0	1	0	1	0	4	A	1.23000
0	1	0	0	1	0	1	1	4	B	1.24000
0	1	0	0	1	1	0	0	4	C	1.25000
0	1	0	0	1	1	0	1	4	D	1.26000
0	1	0	0	1	1	1	0	4	E	1.27000
0	1	0	0	1	1	1	1	4	F	1.28000
0	1	0	1	0	0	0	0	5	0	1.29000
0	1	0	1	0	0	0	1	5	1	1.30000
0	1	0	1	0	0	1	0	5	2	1.31000
0	1	0	1	0	0	1	1	5	3	1.32000
0	1	0	1	0	1	0	0	5	4	1.33000
0	1	0	1	0	1	0	1	5	5	1.34000
0	1	0	1	0	1	1	0	5	6	1.35000
0	1	0	1	0	1	1	1	5	7	1.36000
0	1	0	1	1	0	0	0	5	8	1.37000
0	1	0	1	1	0	0	1	5	9	1.38000
0	1	0	1	1	0	1	0	5	A	1.39000

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0	Hex		VR12.6
0	1	0	1	1	0	1	1	5	B	1.40000
0	1	0	1	1	1	0	0	5	C	1.41000
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0	1	0	1	1	1	1	1	5	F	1.44000
0	1	1	0	0	0	0	0	6	0	1.45000
0	1	1	0	0	0	0	1	6	1	1.46000
0	1	1	0	0	0	1	0	6	2	1.47000
0	1	1	0	0	0	1	1	6	3	1.48000
0	1	1	0	0	1	0	0	6	4	1.49000
0	1	1	0	0	1	0	1	6	5	1.50000
0	1	1	0	0	1	1	0	6	6	1.51000
0	1	1	0	0	1	1	1	6	7	1.52000
0	1	1	0	1	0	0	0	6	8	1.53000
0	1	1	0	1	0	0	1	6	9	1.54000
0	1	1	0	1	0	1	0	6	A	1.55000
0	1	1	0	1	0	1	1	6	B	1.56000
0	1	1	0	1	1	0	0	6	C	1.57000
0	1	1	0	1	1	0	1	6	D	1.58000
0	1	1	0	1	1	1	0	6	E	1.59000
0	1	1	0	1	1	1	1	6	F	1.60000
0	1	1	1	0	0	0	0	7	0	1.61000
0	1	1	1	0	0	0	1	7	1	1.62000
0	1	1	1	0	0	1	0	7	2	1.63000
0	1	1	1	0	0	1	1	7	3	1.64000
0	1	1	1	0	1	0	0	7	4	1.65000
0	1	1	1	0	1	0	1	7	5	1.66000
0	1	1	1	0	1	1	0	7	6	1.67000
0	1	1	1	0	1	1	1	7	7	1.68000
0	1	1	1	1	0	0	0	7	8	1.69000
0	1	1	1	1	0	0	1	7	9	1.70000
0	1	1	1	1	0	1	0	7	A	1.71000
0	1	1	1	1	0	1	1	7	B	1.72000
0	1	1	1	1	1	0	0	7	C	1.73000
0	1	1	1	1	1	0	1	7	D	1.74000
0	1	1	1	1	1	1	0	7	E	1.75000
0	1	1	1	1	1	1	1	7	F	1.76000
1	0	0	0	0	0	0	0	8	0	1.77000
1	0	0	0	0	0	0	1	8	1	1.78000

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			VR12.6
1	0	0	0	0	0	1	0	8	2	1.79000
1	0	0	0	0	0	1	1	8	3	1.80000
1	0	0	0	0	1	0	0	8	4	1.81000
1	0	0	0	0	1	0	1	8	5	1.82000
1	0	0	0	0	1	1	0	8	6	1.83000
1	0	0	0	0	1	1	1	8	7	1.84000
1	0	0	0	1	0	0	0	8	8	1.85000
1	0	0	0	1	0	0	1	8	9	1.86000
1	0	0	0	1	0	1	0	8	A	1.87000
1	0	0	0	1	0	1	1	8	B	1.88000
1	0	0	0	1	1	0	0	8	C	1.89000
1	0	0	0	1	1	0	1	8	D	1.90000
1	0	0	0	1	1	1	0	8	E	1.91000
1	0	0	0	1	1	1	1	8	F	1.92000
1	0	0	1	0	0	0	0	9	0	1.93000
1	0	0	1	0	0	0	1	9	1	1.94000
1	0	0	1	0	0	1	0	9	2	1.95000
1	0	0	1	0	0	1	1	9	3	1.96000
1	0	0	1	0	1	0	0	9	4	1.97000
1	0	0	1	0	1	0	1	9	5	1.98000
1	0	0	1	0	1	1	0	9	6	1.99000
1	0	0	1	0	1	1	1	9	7	2.00000
1	0	0	1	1	0	0	0	9	8	2.01000
1	0	0	1	1	0	0	1	9	9	2.02000
1	0	0	1	1	0	1	0	9	A	2.03000
1	0	0	1	1	0	1	1	9	B	2.04000
1	0	0	1	1	1	0	0	9	C	2.05000
1	0	0	1	1	1	0	1	9	D	2.06000
1	0	0	1	1	1	1	0	9	E	2.07000
1	0	0	1	1	1	1	1	9	F	2.08000
1	0	1	0	0	0	0	0	A	0	2.09000
1	0	1	0	0	0	0	1	A	1	2.10000
1	0	1	0	0	0	1	0	A	2	2.11000
1	0	1	0	0	0	1	1	A	3	2.12000
1	0	1	0	0	1	0	0	A	4	2.13000
1	0	1	0	0	1	0	1	A	5	2.14000
1	0	1	0	0	1	1	0	A	6	2.15000
1	0	1	0	0	1	1	1	A	7	2.16000
1	0	1	0	1	0	0	0	A	8	2.17000

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			VR12.6
1	0	1	0	1	0	0	1	A	9	2.18000
1	0	1	0	1	0	1	0	A	A	2.19000
1	0	1	0	1	0	1	1	A	B	2.20000
1	0	1	0	1	1	0	0	A	C	2.21000
1	0	1	0	1	1	0	1	A	D	2.22000
1	0	1	0	1	1	1	0	A	E	2.23000
1	0	1	0	1	1	1	1	A	F	2.24000
1	0	1	1	0	0	0	0	B	0	2.25000
1	0	1	1	0	0	0	1	B	1	2.26000
1	0	1	1	0	0	1	0	B	2	2.27000
1	0	1	1	0	0	1	1	B	3	2.28000
1	0	1	1	0	1	0	0	B	4	2.29000
1	0	1	1	0	1	0	1	B	5	2.30000

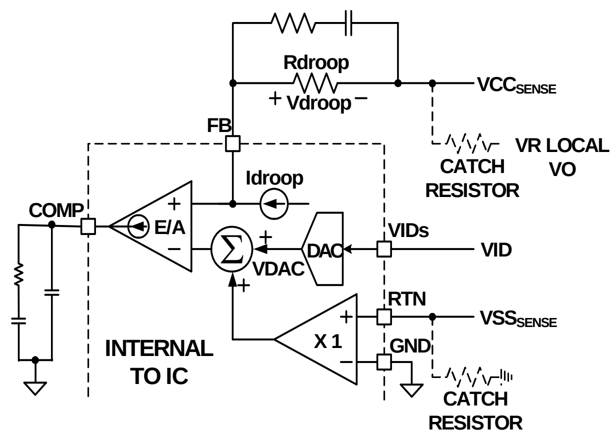


FIGURE 16. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to the load current to achieve the load line. The controller can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors as shown in the Typical Applications Diagram or through a current sense resistor in series with the inductor (Figure 24). In both methods, the capacitor C_n voltage represents the inductor total current. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for load line implementation, current monitor and overcurrent protection.

$$I_{droop} = \frac{V_{Cn}}{R_i} \qquad \text{(EQ. 2)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 3.

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 3)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can both change the load line slope. Since I_{droop} also sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Voltage Sensing

Figure 16 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and add it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal as shown in Equation 4:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 4)}$$

Rewriting Equation 4 and substitution of Equation 3 gives

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 5)}$$

Equation 5 is the exact equation required for load line implementation.

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback will be open circuit in the absence of the processor. As Figure 16 shows, it is recommended to add a “catch” resistor to feed the VR local output voltage back to the compensator, and add another “catch” resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

CCM Switching Frequency

The PROG2 pin configures the CCM switching frequency. When the ISL95813 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R^3™ modulator. Section “R3™ Modulator” on page 9 explains that the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. On the other hand, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and doesn’t have any significant effect on output voltage ripple magnitude.

PROGRAM 1 Pin

PRGM1 programs I_{CCMAX} register and switching frequency. For proper operation, it is recommended the 1% resistor value called out in the table be used in the final application.

TABLE 2. PROGRAM 1 RESISTOR VALUES

R_PROG1 (±3%, kΩ)	I_{CCMAX} (A)	f_{SW} (kHz)
1.0	17	425
5.76	21	
9.31	28	
13.3	33	
17.4	35	
21	40	
24.9	17	550
28.7	21	
33	28	
42.2	33	
49.9	35	
57.6	40	
64.9	17	700 ECO
73.2	21	
80.6	28	
90.9	33	
102	35	
113	40	
124	17	700 PRO
137	21	
154	28	
169	33	
187	35	
205	40	

PROGRAM 2 Pin

PRGM2 pin programs the both boot up voltage V_{BOOT}, and the VID Slew Rate. For proper operation, it is recommended the 1% resistor value called out in the table be used in the final application.

TABLE 3. PROGRAM 2 RESISTOR VALUES

R_PROG2 (±3%, kΩ)	V_{BOOT} (V)	VID Slew (mV/µs)
1.0	0	12
5.76	1.65	
9.31	1.7	
13.3	1.75	

TABLE 3. PROGRAM 2 RESISTOR VALUES (Continued)

R_PROG2 (±3%, kΩ)	V_{BOOT} (V)	VID Slew (mV/µs)
17.4	1.75	24
21	1.7	
24.9	1.65	
28.7	0	
33	0	40
42.2	1.65	
49.9	1.7	
57.6	1.75	
64.9	1.75	45
73.2	1.7	
80.6	1.65	
90.9	0	
102	0	53
113	1.65	
124	1.7	
137	1.75	
154	1.75	80
169	1.7	
187	1.65	
205	0	

Power State Modes

Table 4 shows the power state operation mode.

TABLE 4. POWER STATE OPERATION MODE

POWER STATE	CONFIGURATION
PS0	1-phase CCM
PS1	1-phase CCM
PS2	1-phase DE
PS3	1-phase DE
PS4	Very low power state

For PS0 and PS1, the ISL95813 operates in CCM while in PS2 and PS3 the device enters DCM.

In PS4, ISL95813 enters a very low power state and shuts down all the drivers and internal circuits. In this mode the controller only accepts SetVID-fast and SetVID-slow commands, all other SVID commands will be rejected. ISL95813 quiescent power is about 0.5mW in PS4.

Dynamic Operation

The ISL95813 responds to VID changes by slewing to the new voltage at a slew rate indicated in the SetVID command. There are three SetVID slew rates, namely SetVID_fast, SetVID_slow and SetVID_decay.

SetVID_fast command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 12mV/µs slew rate or the fast slew rate set by R_PROG2.

SetVID_slow command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 3mV/µs slew rate.

SetVID_decay command prompts the controller to enter DE mode. The output voltage, V_{core}, will decay down to the new VID value at a slew rate determined by the load as shown in Equation 6.

$$\frac{dV_{core}}{dt} = \frac{I_{out}}{C_{out}} \quad \text{(EQ. 6)}$$

Overvoltage protection is blanked during VID down transition in DE mode until the output voltage is within 60mV of the VID value. If the voltage decay rate is too fast, the controller will limit the voltage slew rate at SetVID_slow slew rate.

ALERT# will be asserted low at the end of SetVID_fast and SetVID_slow VID transitions.

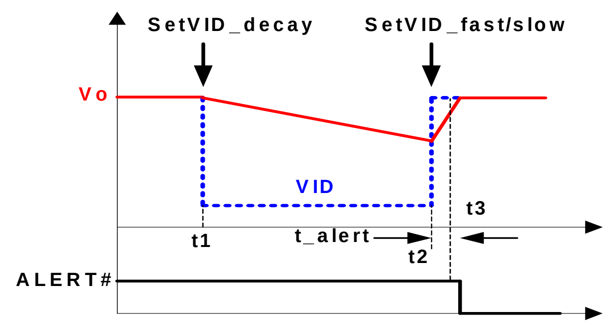


FIGURE 17. SETVID DECAY PRE-EMPTIVE BEHAVIOR

Figure 17 shows SetVID Decay Pre-Emptive behavior. The controller receives a SetVID_decay command at t1. The VR enters DE mode and the output voltage Vo decays down slowly. At t2, before Vo reaches the intended VID target of the SetVID_decay command, the controller receives a SetVID_fast (or SetVID_slow) command to go to a voltage higher than the actual Vo. The controller will react immediately and slew Vo to the new target voltage at the slew rate specified by the SetVID command. At t3, Vo reaches the new target voltage and the controller asserts the ALERT# signal.

The R$^{3™}$ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

Current Monitor

The controller provides the current monitor function. IMON pin reports the inductor current.

The IMON pin outputs a high-speed analog current source that is 1/4 of the droop current flowing out of the FB pin. Thus becoming Equation 7:

$$I_{IMON} = 0.25 \times I_{droop} \quad \text{(EQ. 7)}$$

As the Typical Applications Diagram shows in Figure 1, a resistor R_{imon} is connected to the IMON pin to convert the IMON pin current to voltage. A capacitor should be paralleled with R_{imon} to filter the voltage information. This voltage is sampled with an internal ADC to produce a digital IMON signal that can be read through the serial communications bus.

The IMON pin voltage range is 0V to 1.2V. The controller monitors the IMON pin voltage and considers that ISL95813 has reached I_{CCMAX} when IMON pin voltage is 1.2V.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, the phase node sits at a negative voltage equal to the MOSFET r_{DSON} voltage drop. A phase comparator inside the controller monitors the phase voltage during the on-time of the low-side MOSFET and compares it against a threshold to determine the zero-crossing point of the inductor current. Should the inductor current not reach zero when the lower FET turns off, it will then flow through the low-side MOSFET body diode, decreasing the voltage on the phase node until the inductor current completely decays to zero. When the inductor current finally reaches 0A phase is considered to be in tri-state mode and its voltage floats to the set V_{OUT} value.

If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, current will then flow through the high-side MOSFET body diode, causing a voltage spike on phase which will decay to the set V_{OUT} voltage as phase tri-states.

The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 30ns to minimize the body diode-related loss.

Protection

The ISL95813 provides the designer with overcurrent, overvoltage, and over-temperature protection.

The controller determines overcurrent protection (OCP) by comparing the average value of the droop current I_{droop} with an internal current source threshold as Table 5 shows. It declares OCP when I_{droop} is above the threshold for 120µs.

For over temperature and overcurrent faults, the controller takes the same actions: de-assertion of PGOOD and turn-off of all the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes or load.

The controller will declare an overvoltage fault and de-assert PGOOD if the output voltage exceeds the VID set value by +300mV. The controller will immediately declare an OV fault, toggle PGOOD to ground. The low-side power MOSFET remains on until the output voltage is pulled down below the VID set value before being shut off, and placing phase into tri-state. If the output voltage rises above the VID set value +300mV again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

All the above fault conditions can be reset by toggling VR_ON low. When VR_ON is brought back to its high operating levels a soft-start will occur.

Table 5 summarizes the fault protections.

TABLE 5. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Overvoltage +300mV	Immediately	PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	

Supported Data And Configuration Registers

The controller supports the following data and configuration registers.

TABLE 6. SUPPORTED DATA AND CONFIGURATION REGISTERS

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
00h	Vendor ID	Uniquely identifies the VR vendor. Assigned by Intel.	12h
01h	Product ID	Uniquely identifies the VR product. Intersil assigns this number.	0Ch
02h	Product Revision	Uniquely identifies the revision of the VR control IC. Intersil assigns this data.	04h
05h	Protocol ID	Identifies what revision of SVID protocol the controller supports.	03h
06h	Capability	Identifies the SVID VR capabilities and which of the optional telemetry registers are supported.	81h
10h	Status_1	Data register read after ALERT# signal. Indicating if a VR rail has settled, has reached VR_HOT# condition or has reached I_{CCMAX}.	00h
11h	Status_2	Data register showing Status_2 communication.	00h
12h	Temperature Zone	Data register showing temperature zones that have been entered.	00h
1Ch	Status_2_ LastRead	This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command.	00h
21h	I_{CCMAX}	Data register containing the I_{CCMAX} the platform supports, set at start-up by resistors R_PROG1. The platform design engineer programs this value during the design process. Binary format in amps, i.e., 100A = 64h	Set by R_PROG1
24h	SR-fast	Slew Rate Normal. The fastest slew rate the platform VR can sustain. Binary format in mV/µs. i.e., 0Ch = 12mV/µs.	Set by R_PROG2

TABLE 6. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
25h	SR-slow	Default is 4x slower than normal. Binary format in mV/us. i.e., 03h = 3mV/µs. Can be configured by register 2Ah.	Set by R_PROG2 and Register 2Ah
26h	V_{BOOT}	If programmed by the platform, the VR supports V_{BOOT} voltage during start-up ramp. The VR will ramp to V_{BOOT} and hold at V_{BOOT} until it receives a new SetVID command to move to a different voltage.	Set by R_PROG2
2Ah	Slow slew rate selector	01h = 1/2 of fast slew rate 02h = 1/4 of fast slew rate 04h = 1/8 of fast slew rate 08h = 1/16 of fast slew rate	02h
2Bh	PS4 exit latency	Report 48µs	76h
2Ch	PS3 exit latency		38h
2Dh	Enable to VR_Ready latency		C2h
30h	V_{OUT} max	This register is programmed by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with “not supported” acknowledge.	B5h
31h	VID Setting	Data register containing currently programmed VID voltage. VID data format.	00h
32h	Power State	Register containing the current programmed power state.	00h

33h	Voltage Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is a sign bit, 0 = positive margin,
		1 = negative margin. Remaining 7 bits are # VID steps for the margin.
		00h = no margin,
		01h = +1 VID step
		02h = +2 VID steps...
			00h

34h	Multi VR Config	Data register that configures multiple VRs behavior on the same SVID bus.	00h
35h	SetRegADR	Serial data bus communication address	00h

Key Component Selection

Inductor DCR Current-Sensing Network

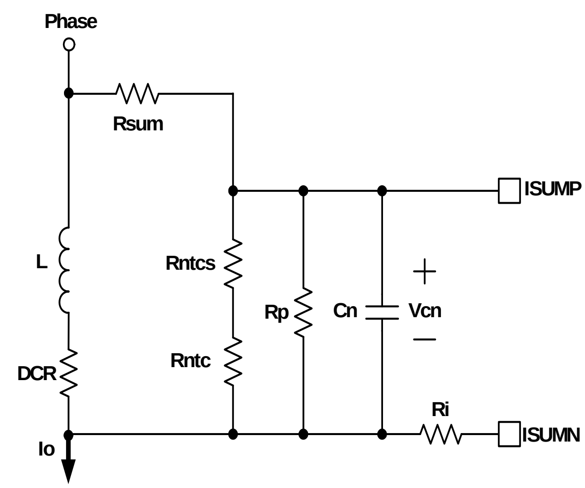


FIGURE 18. DCR CURRENT-SENSING NETWORK

Figure 18 shows the inductor DCR current-sensing network for a single phase solution. This loop monitors the voltage drop across the DCR creating by current flowing in the inductor and feeds that information to the ISL95813 for I_{MON} and load line purposes.

The summed inductor current information is presented to the capacitor C_n. Equations 8 thru 12 describe the frequency-domain relationship between inductor total current $I_o(s)$ and C_n voltage$V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet}+R_{sum}} \times DCR\right) \times I_o(s) \times A_{cs}(s) \qquad \textbf{(EQ. 8)}$$

$$R_{ntcnet} = \frac{(R_{ntcs}+R_{ntc}) \times R_p}{R_{ntcs}+R_{ntc}+R_p} \qquad \textbf{(EQ. 9)}$$

$$A_{cs}(s) = \frac{1+\frac{s}{\omega_L}}{1+\frac{s}{\omega_{sns}}} \qquad \textbf{(EQ. 10)}$$

$$\omega_L = \frac{DCR}{L} \qquad \textbf{(EQ. 11)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times R_{sum}}{R_{ntcnet}+R_{sum}} \times C_n} \qquad \textbf{(EQ. 12)}$$

In the DCR network, transfer function $A_c(s)$ has unity gain at DC. As winding temperature increases, the DCR of the inductor increases which causes a higher reading of the DC current flowing through the inductor. To compensate for this effect, the resistance of the NTC R_{ntc} decreases as its temperature increases. Choosing the remaining components of the DCR network correctly ensures that the capacitor voltage V_{cn} accurately represents the total DC current through the inductor over the entire operating temperature range.

It is recommended when designing the DCR network to maintain V_{cn} as the highest feasible fraction of the voltage that is dropped across the inductor's DCR in order to ensure the droop circuitry on chip has a high signal level to operate with.

While final component values should be fine tuned for a given application, a good starting point for the DCR temperature compensation network is as follows: Rsum = 3.65kΩ, Rp = 11kΩ, Rntcs = 2.61kΩ, and Rntc = 10kΩ (ERT-J1VR103J). To check the operation of the compensation network apply the full load DC current and record the output voltage both immediately and once the circuit has reached its thermal equilibrium. A well designed NTC network can limit the amount of drift on the output voltage to within 2 mV.

In order to achieve proper transient response it is also crucial that $V_{Cn}(s)$ represents real-time $I_o(s)$ of the controller. This is done by matching the pole and zero present in $A_{cs}(s)$ to one another which sets the transfer function to unity gain for all frequencies. To ensure unity gain force ω_L equal to ω_{sns} and solve for C_n as seen in Equation 13.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times R_{sum}}{R_{ntcnet} + R_{sum}} \times DCR} \quad \text{(EQ. 13)}$$

For example, with R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 1mΩ, and L = 0.2µH, Equation 13 gives C_n = 0.088µF.

With proper compensator design, Figure 19 shows the expected load transient response waveforms. When the load current i_o has a square change, the output voltage V_o also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ will not accurately represent real-time $i_o(s)$ and the transient response of the controller will degrade. When C_n is too small, V_o will sag excessively as seen in Figure 20 and potentially trigger a system failure. Figure 21 shows the transient response when C_n is sized too large. In this case V_o will reach its expected droop voltage much too slowly with respect to the load insertion. Should a load release occur during this time there will be excessive overshoot on V_o which may potentially hurt CPU reliability.

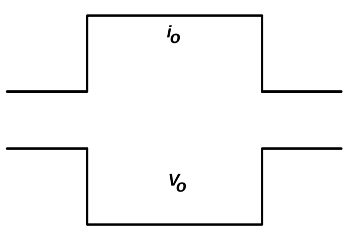


FIGURE 19. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

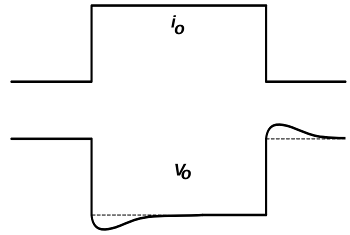


FIGURE 20. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

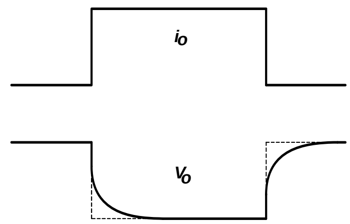


FIGURE 21. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

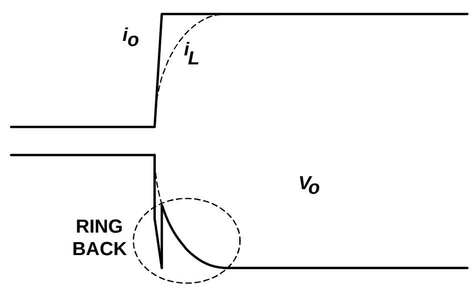


FIGURE 22. OUTPUT VOLTAGE RING BACK PROBLEM

Figure 22 gives an example of ring back on the output voltage during load transient response. Ring back occurs when the load current i_o has a fast step change, but the inductor current i_L cannot accurately track it. Instead, i_L responds in a first order fashion due to the nature of current loop. Instead of the output accurately responding to the load insertion the parasitic ESR and ESL properties of the output capacitors cause an abrupt dip in the voltage. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore it pulls V_o back to the level dictated by i_L, introducing the ring back into the response. This phenomenon can be mitigated through the use of very low ESR and ESL ceramic capacitors for the output filter.

Figure 23 shows two circuits for ring back reduction that can be used in conjunction with low parasitic output filter components if need be. Normally C_n, the capacitor used to match the inductor time constant, is implemented through the parallel combination of two or more capacitors shown in Figure 23 as $C_{n.1}$ and $C_{n.2}$. The first option to reduce ring back is to add resistor R_n in series to $C_{n.1}$. At steady state operation $C_{n.1}$ + $C_{n.2}$ provide the desired C_n capacitance calculated from Equation 11. At the beginning of i_o change however, the effective capacitance of the matching network is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 20 explains, V_o tends to dip when C_n is too small which will reduce the amount of ring back seen during load transients. This effect is more pronounced when $C_{n.1}$ is larger than $C_{n.2}$ as well as when the value of R_n is increased. However, when designing the final circuit, care should be taken not to make R_n larger than necessary or make $C_{n.1}$ much larger than $C_{n.2}$ or else excessive ripple will be seen on V_{cn}. It is recommended to keep $C_{n.2}$ greater than 2200pF and R_n in the range of only few ohms. The final values of $C_{n.1}$, $C_{n.2}$ and R_n should be determined through tuning the load transient response waveforms on an actual board to be used in the end application.

The second method for ring back reduction is to add the series combination of R_{ip} and C_{ip} in parallel with R_i. These components should be sized to provide a lower impedance path than R_i alone at the beginning of an i_o transient. During steady state operation R_{ip} and C_{ip} do not have any effect on the controller's operation. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can more closely resemble i_o rather than i_L, and ring back on the output voltage will not be seen. The recommended value for R_{ip} is 100Ω. while the recommended range for C_{ip} is 100pF to 2000pF though final values should be tuned to the final end product board. It should be noted that the R_{ip} -C_{ip} branch may distort the i_{droop} signal by introducing sharp spikes to the normally triangular waveform which may adversely affect the average value detection and therefore may affect OCP accuracy. Discretion is recommended when implementing this second ring back reduction method in order to maintain a robust system.

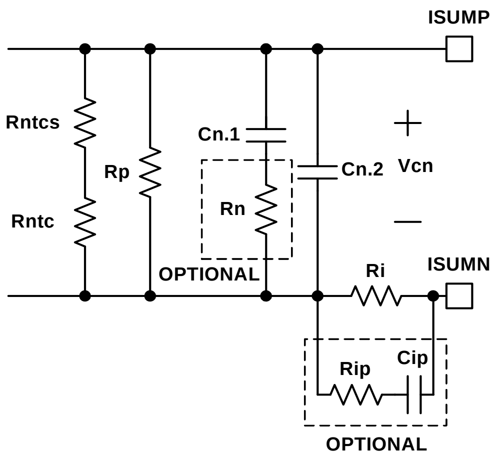


FIGURE 23. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Resistor Current-Sensing Network

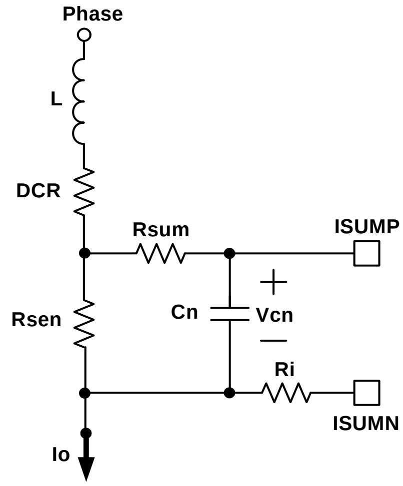


FIGURE 24. RESISTOR CURRENT-SENSING NETWORK

Above is an example of using a resistor sense method of sensing load current instead of SCR sensing. In this method, the inductor current creates a voltage across R_{sen} which is then filters and averaged by the RC filter composed of R_{sum} and C_n. The results voltage, V_{cn}, is then fed into the current sense amplifier on chip through the ISUMP and ISUMN pins. No NTC network is needed in this scenario because the value of the current sensing resistor, R_{sen}, will not vary appreciably over temperature. The design equations for this method of current sensing are given in Equations 14 through 16.

$$V_{Cn}(s) = R_{sen} \times I_o(s) \times A_{Rsen}(s) \qquad \text{(EQ. 14)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{Rsen}}} \qquad \text{(EQ. 15)}$$

$$\omega_{Rsen} = \frac{1}{R_{sum} \times C_n} \qquad \text{(EQ. 16)}$$

Recommended values for R_{sum} and C_n are 1kΩ and 5600pF respectively. As with the DCR method, final values should be tuned in on the actual application board.

Overcurrent Protection

Refer to Equation 2 on page 12 and Figures 18, 22 and 25; resistor R_i sets the droop current I_{droop}. Table 5 shows the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, assume the OCP threshold is 60µA for 1-phase solution. We will design I_{droop} to be 48µA at full load.

From Equation 8 in inductor DCR sensing applications assuming DC conditions gives the relationship of $V_{cn}(s)$ to $I_o(s)$ in Equation 17.

$$V_{Cn} = \frac{R_{ntcnet}}{R_{ntcnet} + R_{sum}} \times DCR \times I_o \qquad \text{(EQ. 17)}$$

Substituting of Equation 17 into Equation 2 yields Equation 18 which can then be solved for R_i.

$$I_{droop} = \frac{1}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + R_{sum}} \times DCR \times I_o \quad \text{(EQ. 18)}$$

$$R_i = \frac{R_{ntcnet} \times DCR \times I_o}{(R_{ntcnet} + R_{sum}) \times I_{droop}} \quad \text{(EQ. 19)}$$

Expanding the R_{ntcnet} term using Equation 9 and applying of the OCP condition in Equation 19 gives the final expression for R_i in Equation 20.

$$R_i = \frac{\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{\left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + R_{sum}\right) \times I_{droopmax}} \quad \text{(EQ. 20)}$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.9mΩ, I_{omax} = 33A and $I_{droopmax}$ = 48µA, Equation 20 gives R_i = 381Ω.

When resistor sensing methods are used, assuming DC conditions in Equation 14 gives the following relationship between V_{cn} and I_o.

$$V_{Cn} = R_{sen} \times I_o \quad \text{(EQ. 21)}$$

Substituting Equation 21 into Equation 2 gives Equation 22:

$$I_{droop} = \frac{1}{R_i} \times R_{sen} \times I_o \quad \text{(EQ. 22)}$$

Therefore

$$R_i = \frac{R_{sen} \times I_o}{I_{droop}} \quad \text{(EQ. 23)}$$

Assuming the OCP conditions put in place previously in Equation 23 gives Equation 24:

$$R_i = \frac{R_{sen} \times I_{omax}}{I_{droopmax}} \quad \text{(EQ. 24)}$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given R_{sen} = 1mΩ, I_{omax} = 33A and $I_{droopmax}$ = 48µA, Equation 24 gives R_i = 687Ω.

As before, with the DCR and R_{sense} components, the final value of Ri should be tuned to fit the final application.

Load Line Slope

For this section please refer to Figure 16 on page 12.

In order to calculate the load line in DCR sense applications start by substituting Equation 8 into Equation 2 to give a more detailed expression for I_{droop}. Next, substitute the new expression for I_{droop} into Equation 3 and solve for the DC load line, shown in Equation 25:

$$LL = \frac{V_{droop}}{I_o} = \frac{R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + R_{sum}} \times DCR \quad \text{(EQ. 25)}$$

For resistor sensing, substitute Equation 22 into Equation 3 to get the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{R_{sen} \times R_{droop}}{R_i} \quad \text{(EQ. 26)}$$

To find the value of R_{droop}, substitute Equation 19 into Equation 25 and solve for R_{droop}, or substitute Equation 23 into Equation 26 and solve for R_{droop}. Both methods give the same result, which is shown in Equation 27:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 27)}$$

One can use the full load condition to calculate R_{droop}. For example, given I_{omax} = 33A, $I_{droopmax}$ = 48µA and LL = 2.0mΩ, Equation 27 gives R_{droop} = 1.37kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 27 and fine tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Compensator

Figure 19 shows the desired load transient response waveforms while Figure 25 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e. constant output impedance, in the entire frequency range, V_o will have square response when I_o has a square change.

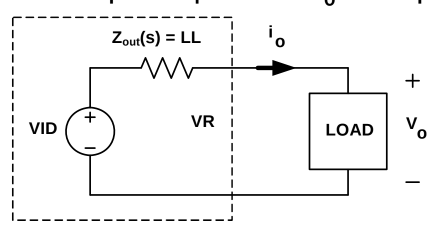


FIGURE 25. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

A voltage regulator with an active droop function is a dual-loop system consisting of a voltage loop and a current based droop loop, of which neither is sufficient to describe the entire system alone.

Figure 26 conceptually shows T1(s) measurement set-up and Figure 27 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T(1) is measured after the summing node, and T2(s) is measured in the voltage loop before the summing node.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more meaning of system stability. T2(s) is the voltage loop gain with closed droop loop. It has more meaning of output voltage response. Only T2(s) can be actually measured in a laboratory setting on the ISL95813 regulator.

Typically, one should design the compensator to get stable T1(s) and T2(s) with sufficient phase margin, and output impedance equal or smaller than the load line slope.

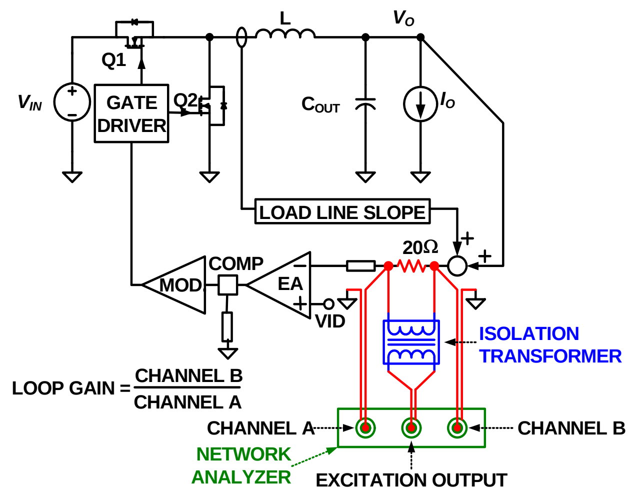


FIGURE 26. LOOP GAIN T1(s) MEASUREMENT SET-UP

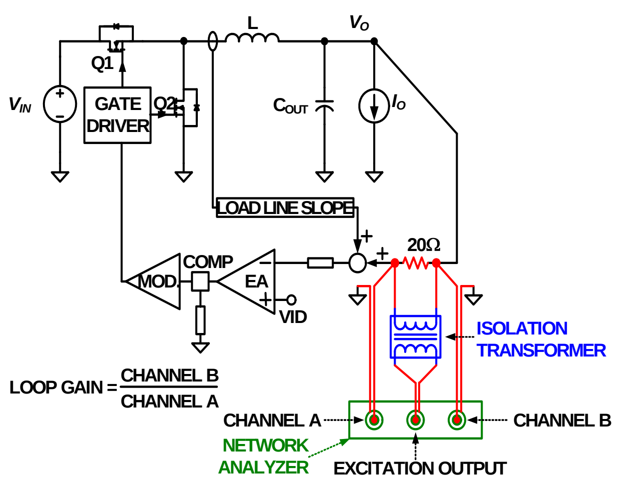


FIGURE 27. LOOP GAIN T2(s) MEASUREMENT SET-UP

Current Monitor

Refer to Equation 7 on page 14 for the IMON pin current expression.

Looking at the "TYPICAL 40Amax, 12.6, APPLICATION DIAGRAM" on page 1, the current flowing from the IMON pin goes through R_{imon} creating a voltage V_{Rimon}. The expression for voltage is expressed in Equation 28:

$$V_{Rimon} = 0.25 \times I_{droop} \times R_{imon} \qquad \text{(EQ. 28)}$$

To expand this expression, first solve Equation 27 for I_{droop} giving Equation 29:

$$I_{droop} = \frac{I_O}{R_{droop}} \times LL \qquad \text{(EQ. 29)}$$

Next, substitute Equation 29 into Equation 28 giving the final expression for V_{Rimon}.

$$V_{Rimon} = \frac{0.25 I_O \times LL}{R_{droop}} \times R_{imon} \qquad \text{(EQ. 30)}$$

Assuming $I_O = I_{omax}$ and rewriting Equation 30 gives Equation 31 for choosing the value of R_{imon}.

$$R_{imon} = \frac{V_{Rimon} \times R_{droop}}{0.25 I_O \times LL} \qquad \text{(EQ. 31)}$$

For example, given LL = 2.0mΩ, R_{droop} = 1.37kΩ, V_{Rimon} = 1.2V at I_{omax} = 33A, Equation 31 gives R_{imon} = 100kΩ. The results from Equation 29 should be treated as a starting point for the design and the resistor value should be finalized on an actual application board.

A capacitor C_{imon} should be but in parallel with R_{imon} to filter the IMON pin voltage. It is recommended to have a time constant long enough to remove any switching frequency ripples from the IMON signal.

Slew Rate Compensation Circuit For VID Transition

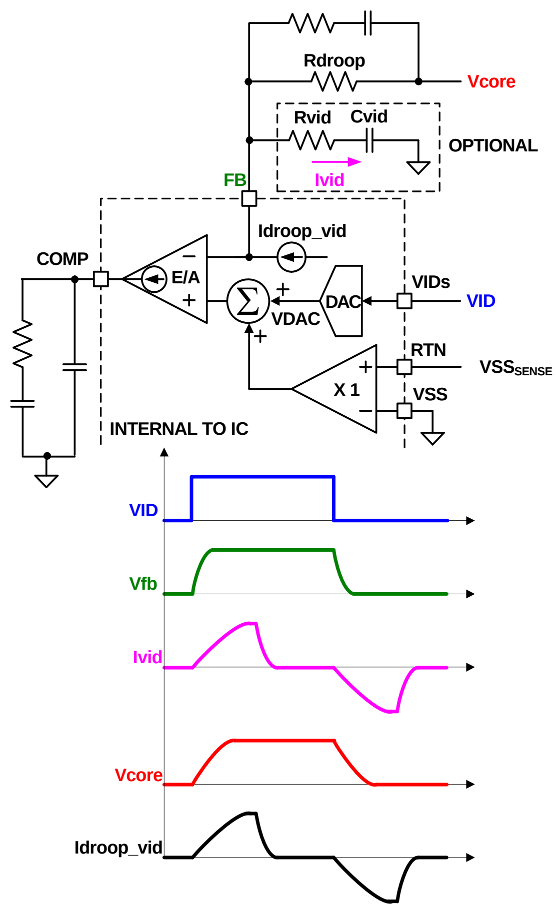


FIGURE 28. SLEW RATE COMPENSATION CIRCUIT FOR VID TRANSITION

During a large VID transition, the DAC steps through the VIDs at a controlled slew rate while maintaining an output voltage, V_{core}, slew rate of 10mV/µs.

Figure 28 shows the waveforms of VID transition. During VID transition, the output capacitor is being charged and discharged, causing C_{out} x dV_{core}/dt current on the inductor. The controller senses the inductor current increase during the up transition (as the I_{droop_vid} waveform shows) and will droop the output voltage V_{core} accordingly, making V_{core} slew rate slow. Similar behavior occurs during the down transition. To get the correct V_{core} slew rate during VID transition, one can add the R_{vid} to C_{vid} branch, whose current I_{vid} cancels I_{droop_vid}.

It's recommended to choose the R_{vid} and C_{vid} values from the reference design as a starting point. Then tweak the actual values on the board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The R_{vid} to C_{vid} network is between the virtual ground and the real ground, and hence has no effect on transient response.

VR_HOT#/ALERT# Behavior

The ISL95813 sources 60µA of current out of the NTC pin at 1kHz with a 50% duty cycle. The current source flows through the respective NTC resistor network on the pin and creates a voltage that is monitored by the controller through an A/D converter (ADC) to generate the T_{ZONE} value. Table 7 shows the programming table for T_{ZONE}. The user needs to scale the NTC resistor network such that it generates the NTC pin voltage that corresponds to the left-most column. Do not use any capacitor to filter the voltage.

TABLE 7. T_{ZONE} VALUES

VNTC (V)	TMAX (%)	T_{ZONE}
0.84	>100	FFh
0.88	100	FFh
0.92	97	7Fh
0.96	94	3Fh
1.00	91	1Fh
1.04	88	0Fh
1.08	85	07h
1.12	82	03h
1.16	79	01h
1.2	76	01h
>1.2	<76	00h

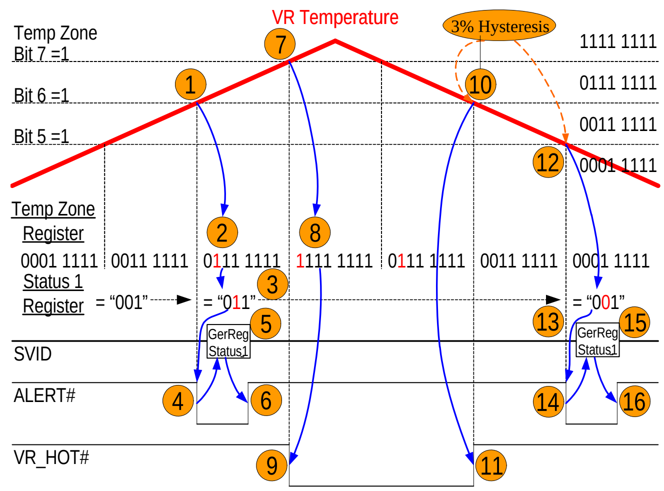
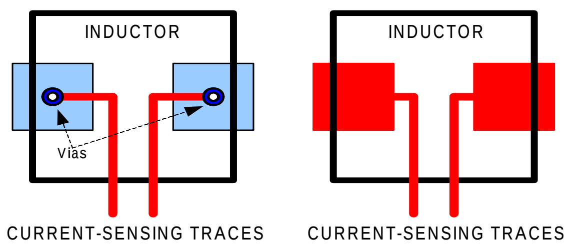


FIGURE 29. VR_HOT#/ALERT# BEHAVIOR

Figure 29 shows how the NTC and the NTCG network should be designed to get correct VR_HOT#/ALERT# behavior when the system temperature rises and falls which is manifested as the NTC pin voltage rising and falling. The series of events are:

1. The temperature rises so the NTC pin voltage drops. T_{ZONE} value changes accordingly.
2. The temperature crosses the threshold where T_{ZONE} register Bit 6 changes from 0 to 1.
3. The controller changes Status_1 register bit 1 from 0 to 1.
4. The controller asserts ALERT#.
5. The CPU reads Status_1 register value to know that the alert assertion is due to T_{ZONE} register bit 6 flipping.
6. The controller clears ALERT#.
7. The temperature continues rising.
8. The temperature crosses the threshold where T_{ZONE} register Bit 7 changes from 0 to 1.
9. The controllers asserts VR_HOT# signal. The CPU throttles back and the system temperature starts dropping eventually.
10. The temperature crosses the threshold where T_{ZONE} register Bit 6 changes from 1 to 0. This threshold is 1 ADC step lower than the one when VR_HOT# gets asserted, to provide 3% hysteresis.
11. The controllers de-asserts VR_HOT# signal.
12. The temperature crosses the threshold where T_{ZONE} register bit 5 changes from 1 to 0. This threshold is 1 ADC step lower than the one when ALERT# gets asserted during the temperature rise to provide 3% hysteresis.
13. The controller changes Status_1 register Bit 1 from 1 to 0.
14. The controller asserts ALERT#.
15. The CPU reads Status_1 register value to know that the alert assertion is due to T_{ZONE} register Bit 5 flipping.
16. The controller clears ALERT#.

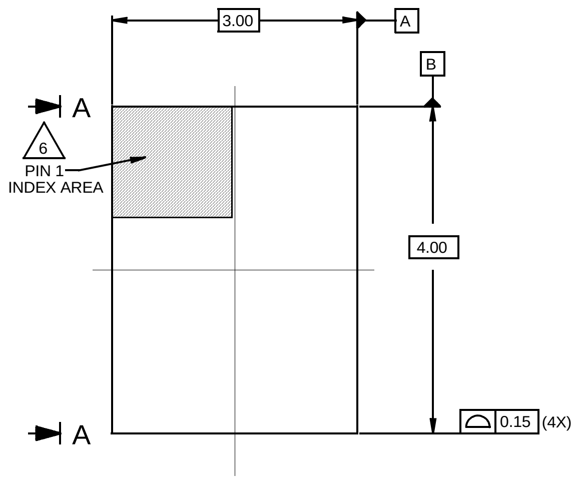
Layout Guidelines

<table>
<tr><th>ISL95813</th><th>SYMBOL</th><th>LAYOUT GUIDELINES</th></tr>
<tr><td>BOTTOM PAD</td><td>GND</td><td>Connect this ground pad to the ground plane through low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers.</td></tr>
<tr><td>18, 19, 20</td><td>SCLK,
SDA,
ALERT#</td><td>Follow Intel recommendation.</td></tr>
<tr><td>1</td><td>VR_ON</td><td>No special consideration.</td></tr>
<tr><td>2</td><td>PGOOD</td><td>No special consideration.</td></tr>
<tr><td>3</td><td>IMON</td><td>No special consideration.</td></tr>
<tr><td>4</td><td>VR_HOT#</td><td>No special consideration.</td></tr>
<tr><td>5</td><td>NTC</td><td>The NTC thermistor needs to be placed close to the thermal source that is monitored to determine CPU Vcore thermal throttling. Recommend placing it at the hottest spot of the CPU Vcore VR.</td></tr>
<tr><td>6</td><td>COMP</td><td rowspan="2">Place the compensator components in general proximity of the controller.</td></tr>
<tr><td>7</td><td>FB</td></tr>
<tr><td>10</td><td>ISUMN</td><td rowspan="2">Place the current sensing circuit in general proximity of the controller.
Place capacitor Cn very close to the controller.
Place the NTC thermistor next to the inductor so it senses the inductor temperature correctly.
The power stage requires a pair of VSUMP and VSUMN signals to the controller. These two signal traces should run in a parallel fashion with decent width (>20mil).
IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces.
</td></tr>
<tr><td>9</td><td>ISUMP</td></tr>
<tr><td>13</td><td>BOOT1</td><td>Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.</td></tr>
<tr><td>14</td><td>UG</td><td rowspan="2">Run these two traces in parallel fashion with a decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE trace to high-side MOSFET source pins instead of general copper.</td></tr>
<tr><td>15</td><td>PHASE</td></tr>
<tr><td>16</td><td>LG</td><td>Use a decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.</td></tr>
<tr><td>12</td><td>VCC</td><td>A capacitor decouples it to GND. Place it in close proximity of the controller.</td></tr>
<tr><td>17</td><td>PROG1</td><td>Connect a resistor to GND. Place it in close proximity of the controller.</td></tr>
<tr><td>11</td><td>PROG2</td><td>Connect a resistor to GND. Place it in close proximity of the controller.</td></tr>
<tr><td>8</td><td>RTN</td><td>Place the RTN filter in close proximity of the controller for good decoupling.</td></tr>
</table>

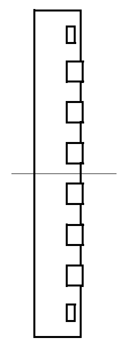
Package Outline Drawing

L20.3x4

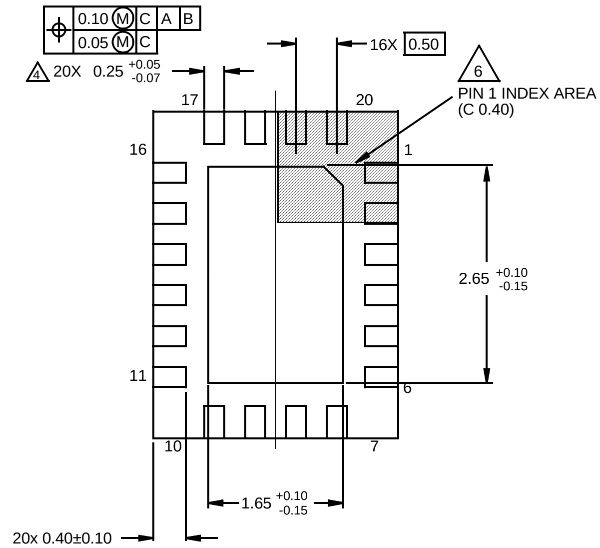
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



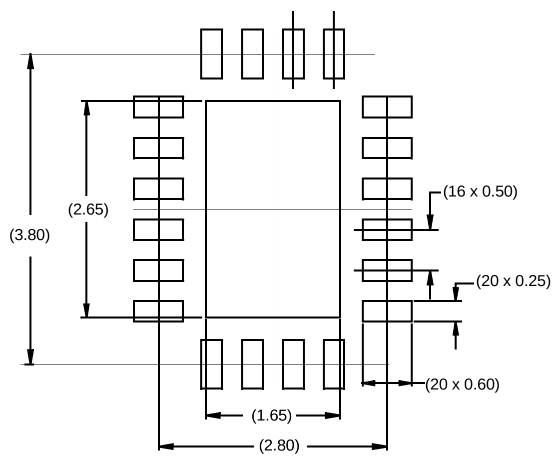
TOP VIEW



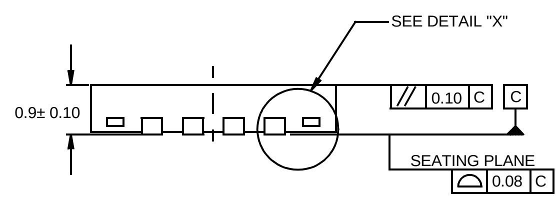
VIEW "A-A"



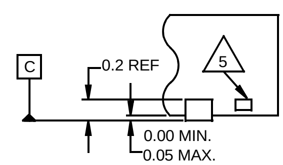
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 15, 2013	FN8449.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability