Freescale Semiconductor
Application Note

Document Number: AN4624
Rev. 1, 11/2012

Migrating from MPC5643L to MPC5744P

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Contents

1 Introduction

The Qorivva MPC5643L 32-bit MCU built on Freescale's Power Architecture® technology is the first MCU to achieve ISO 26262 ASIL D functional safety standard certification. It targets chassis and safety applications that require a high safety integrity level, such as electric power steering, radar and electronic stability control. The MPC5744P is the 55 nm successor to the MPC5643L. The MPC5744P is built around a safety concept targeting an ISO 26262 ASIL D integrity level and is part of the SafeAssure program. Its peripheral set is compatible with the MPC5643L to allow a high degree of re-use.

This application note provides a summary of the significant differences between the MPC5643L and MPC5744P devices, and may be used as a reference for planning a migration to the MPC5744P. This document covers the architectural differences between the two devices and highlights the software and hardware considerations for migrating an existing MPC5643L-based design to the MPC5744P.

2 Overview

The following table summarizes the key feature differences between the MPC5643L and the MPC5744P.

Table 1. Key feature comparison

Feature	MPC5643L	MPC5744P
Process	C90	C55
Core	Dual-core e200z4d	e200z4201n3 and e200z419 (cut 1) e200z4251n3 and e200z424 (cut 2)
Lock-step mode	Yes	Yes (delayed lock-step)
Decoupled parallel mode	Yes	No
Execution speed	Up to 120 MHz	Up to 180 MHz
SPE	Yes	No
LSP	No	Yes
EFPU	Scalar/Vector	Scalar
MMU	16 regions	No
MPU	No	24 regions
Instruction set PCC Book E	Yes	No
Instruction set VLE	Yes	Yes
Instruction cache	4 KB	8 KB
Data cache	No	4 KB
Data local memory	No	64 KB on e200z4201n3 and e200z4251n3
Core bus	AHB 32-bit address, 64-bit data	AHB 32-bit address, 64-bit data e2eECC
Internal periphery bus	32-bit address, 32-bit data	32-bit address, 32-bit data
Master x slave ports	4 x 3 in lock-step mode 6 x 3 in decoupled parallel mode	4 x 5
Code/data flash memory	1 MB	2.5 MB
SRAM	128 KB	384 KB
System MPU	16 regions	16 regions
Error correction status mode	Yes	No
Memory error management unit	No	Yes
Fault control and collection unit	Yes	Yes
Interrupt controller • Priority levels • SW settable interrupts • Latency monitor	 • 16 • 8 • No	 • 32 • 16 • Yes
Periodic interrupt timer	1 module x 4 channels	
System timer module	4 channels, replicated module	

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Table 1. Key feature comparison (continued)

Feature	MPC5643L	MPC5744P
eTimer	eTimer_0: 6 channels eTimer_1: 6 channels eTimer_2: 6 channels (257MAPBGA)	eTimer_0: 6 channels eTimer_1: 6 channels eTimer_2: 4 channels (144LQFP) 6 channels (257MAPBGA)
Enhanced DMA	16 channels, replicated module	32 channels in delayed lock-step
DMA channel mux	1 module 27 peripheral sources	2 modules 23 peripheral sources on DMAMUX_0 27 peripheral sources on DMAMUX_1
FlexRay	1 module x 64 message buffers, dual channel	
FlexCAN	2 modules x 32 message buffers	3 modules x 64 message buffers Error detection/correction
LINFlexD	2 modules	
FlexPWM	2 modules x 4 channels	
Analog-to-digital converter	12-bit ADC ADC0, ADC1 22 analog pads	12-bit ADC ADC0, ADC1, ADC3 (144LQFP) ADC0, ADC1, ADC2, ADC3 (257MAPBGA) 22 analog pads (144LQFP) 25 analog pads (257MAPBGA)
Analog-to-digital self-tests	Supply Capacitive Resistive-Capacitive	Supply Capacitive
Cross triggering unit	1 module	2 modules Dual conversion mode Interleaved triggering
Sine-wave generator	32 point	
Deserial serial peripheral interface	3 modules	3 modules (144LQFP cut 1) 4 modules (144LQFP cut 2) 4 modules (257MAPBGA)
Cyclic redundancy checker	Yes	Yes
Single edge nibble transmission	No	2 modules x 2 channels
Peripheral register protection	Yes	Yes
Interprocessor serial link interface	No	Yes (257MAPBGA)
Device power supply	3.3 V with external ballast transistor 3.3 V with internal ballast transistor	3.3 V with external ballast transistor 3.3 V with 1.25 V low drop-out regulator

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Table 1. Key feature comparison (continued)

Feature	MPC5643L	MPC5744P
Analog reference voltage	3.30 V to 5.5 V	
Phase-locked loop	2 frequency modulated PLL	1 PLL and 1 frequency-modulated PLL
Internal RC oscillator	16 MHz	
External crystal oscillator	4 – 40 MHz	
LBIST and MBIST	Available at startup	
Low power modes: • HALT • STOP	 • Yes • Yes	 • Yes • Yes
Debug/trace: • JTAG • Class • MDO • Aurora	 • Yes • Level 3+ • RPM and FPM • No	 • Yes • Level 3+ • RPM • Yes (257MAPBGA)
LQFP	144 pins, 0.5 mm pitch, 20 mm x 20 mm outline	
MAPBGA	257 balls, 0.8 mm pitch, 14 mm x 14 mm outline	

3 Software considerations

3.1 Flash memory

Both the MPC5643L and MPC5744P provide an electrically programmable/erasable, non-volatile flash memory for instruction and/or data storage.

However, the C55 flash memory of the MPC5744P has different electrical characteristics from the C90 flash memory of the MPC5643L. For optimum performance, software must configure the correct number of wait states and address pipeline control in the flash memory controller.

The linker file must be updated to reflect the increased flash memory size and different flash memory partitioning.

3.2 Core complex

Operating mode

The MPC5643L supports both lock-step mode (LSM) and decoupled parallel mode (DPM). In LSM, the two redundant e200z4d cores execute the same operations or transactions in synchronicity. In DPM, each core runs independently from the other core and redundancy checkers are disabled.

The MPC5744P master and checker cores (e200z420n3/e200z419 cut 1 or e200z425n3/e200z424 cut 2) run in delayed LSM, in which the checker core follows the execution of the main core with a delay of two cycles. The delayed lock-step mechanism minimizes common cause failures and simplifies timing. DPM mode is not supported.

From a software perspective, the main and checker cores behave as a single core. The MPC5744P software must be re-compiled to have the same code run on both cores for delayed LSM operation.

Signal processing extension unit

The MPC5643L supports the Signal processing extension (SPE) unit for real-time single instruction, multiple data (SIMD) fixed-point and single-precision embedded numeric operations.

The MPC5744P does not implement an SPE unit. Instead, the lightweight signal processing extension (LSP) APU on the e200z4251n3 is provided to support real-time SIMD fixed-point embedded numeric operations, including fixed-point multiply/accumulate and integer/fixed point SIMD operations.

Software must be updated to use the LSP if the SPE feature was used on the MPC5643L.

Floating point instructions

The MPC5643L supports the embedded floating-point unit (EFPU) which implements scalar and vector single-precision floating-point instructions.

The MPC5744P EFPU supports scalar single-precision floating-point instructions. It does not support vector single-precision floating-point instructions, therefore, the MPC5744P software must be updated if this feature was used on the MPC5643L.

General purpose registers

The MPC5643L e200z4d cores implement 64-bit general-purpose registers (GPRs) to support vector instructions defined by the SPE category.

The MPC5744P cores implement 32-bit GPRs that are accessed through instruction operands. EFPU and LSP instructions operate on the 32-bit GPRs.

Instruction set architecture

The MPC5643L e200z4 cores use the 32-bit PowerPC™ Book E instruction set architecture (ISA) as well as the variable-length encoding (VLE) which uses the 16-bit versions of the standard Book E ISA for reduced code footprint.

The MPC5744P cores implement the VLE ISA. Software must be updated to ensure the fixed-length 32-bit instruction set is not used.

Core memory management

The MPC5643L core Memory Management Unit (MMU) provides a 16-entry translation lookaside buffer (TLB) to define virtual to physical address translation.

The MPC5744P does not implement an MMU, so there is no address translation. Instead, the Core MPU (CMPU) is supported to provide access protection to specified memory regions. Software should configure the region descriptors with the address ranges, access protections and memory attributes for each protected region. Software instructions are also implemented for reading and writing MPU entries and special purpose registers for the MPU assist registers.

Local data memory

The MPC5643L does not include local memory in the core complex.

The MPC5744P linker file must be updated to add the main core's 64 KB of local data memory (DMEM). Software should use DMEM for critical data to take advantage of its zero wait-state latency.

3.3 Flash ECC testing

The MPC5643L flash memory has a user-test (UTEST) mode ECC logic check feature which can be utilized for ECC logic testing.

The software test applies walking 0 patterns to data and ECC parity bits to perform the ECC logic check during run-time.

In the MPC5744P, the flash ECC is supervised by hardware. The MPC5744P implements end-to-end ECC (e2eECC) error detection and correction in hardware for improved fault tolerance and detection. While traditional ECC-protected memories generate the ECC checkbits and store the data and checkbits in the memory, with e2eECC all bus masters generate the single error correcting and double error detecting (SECDED) code for every bus transaction. ECC is stored in memories on write operations and validated by the master on read operations.

The flash ECC testing in software is no longer required on the MPC5744P.

3.4 RAM

Both the MPC5643L and MPC5744P provide an on-chip SRAM with ECC.

The linker file must be updated to reflect the MPC5744P's increased SRAM size to 384 KB.

ECC protection in the MPC5744P is extended for all memories, including the FlexRay, FlexCAN and DMA RAM arrays. Software must take into consideration the changes in the mapping of the FCCU fault sources related to the system RAM and peripheral RAM ECC errors.

3.5 System memory protection

The MPC5643L memory protection unit (MPU) supports 16 memory region descriptors.

Each crossbar master can be assigned different access rights to each region. The optional process identifier (ID) from the current bus master is checked against the descriptor's attributes for region hit determination.

In addition to the MPC5744P core MPU, the system MPU (SMPU) provides another layer of memory protection. The SMPU splits the physical memory map into 16 different regions. Unlike the MPC5643L MPU which is process ID-aware, the MPC5744P SMPU uses the master ID, privilege level, and access type to determine whether an access violated the protected region. The SMPU also uses the memory region's cacheability attributes to determine whether references to a region can be cached.

Software must be updated to define the memory spaces and configure each crossbar master's access rights to each region.

3.6 Peripheral bridges

The peripheral bridge (PBRIDGE) is the interface between the system bus and the on-chip peripherals.

Accesses that fall within the address space of the PBRIDGE are decoded to provide individual module selects for the peripherals. The MPC5643L PBRIDGE is duplicated and a checker is applied on the PBRIDGE outputs toward the peripherals. In contrast, the MPC5744P includes two instances of PBRIDGEs belonging to two different peripheral lakes. The arrangement of the MPC5744P I/O peripherals onto the two PBRIDGEs allows redundant use of the peripherals while limiting possible common cause failures (CCFs).

The MPC5744P header file must be updated to reflect the new memory mapping of the peripherals. Peripheral access control to restrict read and write accesses to individual peripherals must be updated to reflect changes in the implemented peripherals.

3.7 Direct memory access

The MPC5643L and MPC5744P enhanced direct memory access (eDMA) allows complex data transfers with minimal intervention from the core processor.

The MPC5643L implements a replicated 16-channel eDMA controller. The MPC5643L eDMA channel mux (DMAMUX) allows the 27 DMA peripheral sources to be routed to the 16 DMA channels.

The MPC5744P implements two 32-channel eDMA controllers in which the second eDMA module operates with a delay of two cycles compared to the first eDMA module. It also implements two DMAMUX modules: DMAMUX_0 connects 23 peripheral sources channel 0 through 15, and DMAMUX_1 connects 27 peripheral sources to channels 16 through 31.

Software should be updated to take advantage of the additional DMA channels and the split of the DMA channel muxes.

3.8 Clock architecture

The MPC5643L implements two independent frequency-modulated phase-locked loop (FMPLL) modules to generate the system and peripheral clocks.

The MPC5744P C55 dual-PLL architecture drives the peripherals from the PLL0 output while the core and platform clocks are driven by the PLL1 frequency-modulated output. Software must update the drivers for the MPC5744P PLLs, which require a different programming model from the MPC5643L PLLs.

The clock distribution on the MPC5744P is also changed from the MPC5643L. Software must update the assignment of clock sources as well as the system and auxiliary clock dividers. It must also take into account the frequency limits of these clocks. Refer to the MPC5744P Reference Manual for the clock assignments and maximum frequencies for each module.

3.9 Interrupt controller

The MPC5643L interrupt controller (INTC) provides 16 interrupt priority levels and 8 software settable interrupt sources.

The MPC5744P doubles the number of interrupt priority levels to 32 and the number of software settable interrupt sources to 16. Software should take these enhancements into consideration.

Differences in implemented peripherals between the MPC5643L and MPC5744P affect the interrupt vector assignments. Software must update the interrupt vector table to define the implemented interrupt sources on the MPC5744P.

The MPC5744P adds the interrupt controller monitor (INTCM) to provide a safety mechanism to monitor the latency of up to 4 interrupt sources to ensure that these interrupts execute within the expected window of time. Safety-critical applications should use the INTCM select IRQs to monitor and to set the maximum interrupt latency for the selected IRQs.

3.10 Pad control and I/O multiplexing

The system integration unit lite (SIUL) provides control over the electrical configuration of the pads, general-purpose functionality, external interrupts and I/O multiplexing.

Although a similar I/O multiplexing between the MPC5643L and MPC5744P is maintained, the C55 devices implement a different SIUL programming model. Software must take into consideration the new SIUL memory map and updated pad control capabilities of the MPC5744P.

The MPC5744P SIUL also adds a DMA request interface. The REQ input pins are sources for interrupt or DMA requests. Four DMA request channels are available on the MPC5744P.

3.11 ECC error reporting

The MPC5643L error correction status module (ECSM) provides information about the platform configuration and revision.

It also provides registers for capturing information on memory errors. The ECSM is not supported on the MPC5744P. Software must be updated to remove ECC error reporting and error injection functions using the ECSM. Instead, software should check the reported ECC errors in SRAM, flash and peripheral RAM in the memory error management unit (MEMU).

Additionally, software should configure the reaction to the ECC error events in the fault collection and control unit (FCCU).

3.12 Failure handling

The MPC5643L and the MPC5744P implement the fault collection and control unit (FCCU), which offers a hardware channel to collect errors and to place the device into a safe state when a failure in the device is detected.

Whereas the MPC5643L classifies faults as either critical or non-critical based on the criticality and the related fault reactions, the MPC5744P classifies all faults as non-critical to provide maximum configurability of the fault reactions.

Software should be updated to reflect changes in fault configuration as well as the FCCU input mapping of the non-critical faults.

3.13 Low- and high-voltage detection and self-test

The MPC5643L and MPC5744P provides several low- and high-voltage detectors (LVD/HVD) which provide information if voltage is not in the proper range. The MPC5643L provides LVDs for the 3.3 V I/O, regulator, and flash supplies. It also provides both LVDs and HVDs for the 1.2 V core supply. The MPC5744P power management controller (PMC) provides LVDs for the 3.3V oscillator, ADC, I/O, flash and regulator supplies as well as HVD and LVD for the 1.25 V core supply. Software should be updated to configure the LVDs and HVDs accordingly.

The MPC5744P PMC implements an LVD/HVD self-test mechanism which is automatically performed at power-up. Software has the option to trigger the LVD/HVD self-test. In this case, software must configure the self-test time window before initiating the self-test.

3.14 Clock and temperature monitoring

The MPC5643L and MPC5744P provide clock monitoring units (CMUs) to detect missing clocks or incorrect clock frequencies.

The MPC5643L provides clock monitors for the system clock, XOSC clock, motor control clock and FlexRay clock. Additional clock monitoring on the MPC5744P is provided for the IRCOSC clock, checker clock, PBRIDGE clock, ADC clock and SENT clock. Software should configure the clock monitoring accordingly.

Both MPC5643L and MPC5744P are equipped with two temperature sensors (TSENS). Each TSENS module provides an analog voltage that is proportional to the internal junction temperature of the device. Software should update control of the MPC5744P TSENS, which is done via the PMC register space.

3.15 Logic and memory built-in self-tests

The MPC5643L performs the built-in self-test (BIST) every time a destructive or external reset occurs.

The BIST is performed while the device is still under reset. The MPC5643L provides memory BIST (MBIST) for all RAMs and ROMs. It also provides logic a scan-based BIST (LBIST).

The MPC5744P MBIST and LBIST are performed every time the device boots. It also allows the MBIST and LBIST to be performed during shutdown. The shutdown self-test sequence is user-programmable and can be executed at less critical times in the application. A long functional reset is initiated after the self-test is executed during shutdown. Software needs to configure the self-test control unit (STCU2) to prepare the device for the shutdown self-test.

3.16 Analog-to-digital converter self-test

The MPC5643L and MPC5744P implement the analog-to-digital converter (ADC) self-test to check the internal analog circuitry of the ADC.

The MPC5643L supports supply (Algorithm S), resistive-capacitive (Algorithm RC) and capacitive (Algorithm C) self-tests. The MPC5744P does not support a separate Algorithm RC test. Instead, it merges the Algorithm RC and Algorithm C into a single algorithm.

The MPC5744P also supports a high-accuracy calibration mode. In this mode, all the steps of the ADC built-in-self-test (BIST) are run in succession and with averaging. The ADC calibration registers get updated based on the measured values from the corresponding tests. Software should perform the ADC calibration after power-up, after an error situation, or when the operating conditions change, particularly a change in the ADC reference voltage.

3.17 Low power modes

Both the MPC5643L and MPC5744P provide peripheral clock gating control during low-power modes.

Software must be updated to reflect the changes in peripheral assignments when configuring the Mode Entry Peripheral Control registers (MC_ME_PCTLn).

3.18 Cyclic redundancy checking

The cyclic redundancy checker (CRC) unit is a dedicated module for the computation of CRC, off-loading the CPU.

The MPC5643L and MPC5744P support CRC generation for CRC-8, CRC-16-CCITT, and CRC-32 (Ethernet) polynomials.

For CRC-32, both the MPC5643L and the cut 1 version of the MPC5744P CRC engine expect the CRC input to be byte-swapped. For example, software must enter 0x98EFCDAB in the input data register for a given input data of 0xABCDEF98. The BYTE_SWAP, inversion (INV) and swap (SWAP) selection bits in the configuration register (CRC_CFG) must be set to 1.

For CRC-16, both the MPC5643L and the cut 1 version of the MPC5744P CRC engine expect the CRC input to be bit-reversed. For example, software must enter 0x19F7B3D5 in the input data register for a given input data of 0xABCDEF98. The BIT_SWAP, INV and SWAP bits in the CRC_CFG are set to 0.

For cut 2 of the MPC5744P, it is no longer necessary to perform the byte-swapping for CRC-32 or the bit-reversal for CRC-16.

3.19 Cross-triggering unit

The cross-triggering unit (CTU) allows automatic generation of ADC conversion requests without CPU load.

The MPC5743L implements one CTU module to control ADC0 and ADC1, while the MPC5744P has two CTU modules: CTU_0 controls ADC0 and ADC1 and CTU_1 controls ADC2 and ADC3 modules.

The MPC5744P adds support for dual conversion mode in which the conversion command is sent to both ADCs at the same time. If dual conversion mode is used, software must ensure that the same physical channel is not assigned to both ADCs.

Another CTU enhancement is the support for interleaved triggering in the MPC5744P. In this mode, two ADCs control the execution of command lists with their triggers independently. The completion of one of the command lists does not require acknowledgement by both ADCs. Software can configure the CTU for interleaved triggering to improve system performance.

3.20 FlexRay

The MPC5743L and MPC5744P both support a dual channel FlexRay communication controller that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev. A.

The FlexRay module implements 64 message buffers. The MPC5744P FlexRay module adds the Message Buffer Data Field Offset Registers (FR_MBDOR0:67) and the Receive FIFO Start Data Offset Register (FR_RFSDOR). Software must configure the data field offset values for all used message buffers.

The MPC5744P also adds the LRAM ECC Test Error Registers (FR_LEETR0:5) which contain the LRAM ECC test data. Software must take into consideration the layout changes to the controller host interface lookup-table memory (CHI LRAM) which now includes the new registers.

The message buffer search engine runs on the CHI clock and evaluates one individual message buffer per CHI clock cycle. The MPC5744P search duration requires an additional 27 CHI clock cycles instead of 10 CHI clock cycles for the MPC5643L to ensure correct search engine operation. Application software must take into consideration the additional clock cycle requirements in the search duration.

The minimum CHI clock frequency for the MPC5744P is different from the MPC5643L requirements. The timing requirements are defined in the MPC5744P Reference Manual. The minimum CHI frequency must be met, otherwise, a message buffer search error flag is set.

3.21 FlexCAN

The MPC5643L and MPC5744P FlexCAN module implements the CAN protocol according to Version 2.0B specification, which supports both standard and extended message frames.

The message buffers are stored in the embedded FlexCAN RAM.

The MPC5643L implements 2 FlexCAN modules, each with 32 message buffers, while the MPC5644P has 3 FlexCAN modules, each 64 message buffers. The increase in message buffers requires the implementation of additional registers, so the MPC5744P FlexCAN memory map and programming model are different from the MPC5643L. Software should take into account the new registers related to interrupts and masking for the additional message buffers.

The MPC5744P also adds error detection and correction to the FlexCAN memory in read accesses. Each byte of FlexCAN memory is associated with 5 parity bits. The error correction mechanism assures that in the 13-bit word, errors in one bit can be corrected and errors in two bits can be detected but not corrected. Software should enable error correction in the Memory Error Control Register (CAN_MECR) and check the error reporting registers to obtain the address, data and syndrome of the detected error.

3.22 Single Edge Nibble Transmission Receiver

The single edge nibble transmission (SENT) module receives serial data frames from a sensor that implements the SENT encoding scheme.

The SENT protocol is intended for use in applications where high resolution data needs to be communicated from a sensor to an engine control unit (ECU).

Although the MPC5643L does not support a dedicated SENT interface, it can implement the interface using the eTimer channels. An improvement over the MPC5643L is the addition of two dedicated SENT modules on the MPC5744P. Each SENT module supports two channels. The application software has the option to utilize the dedicated SENT modules or the eTimers implementation used on the MPC5643L.

3.23 Periodic Interrupt Timer

The MPC5643L and MPC5744P support a periodic interrupt timer (PIT).

The PIT contains four 32-bit timer channels which can generate interrupts and trigger DMA channels.

The MPC5744P adds a lifetime counter for applications that require Timer 0 and Timer 1 to be chained to build a 64-bit lifetime counter. To use this feature, software must first read the PIT Upper Lifetime Timer Register (PIT_LTMR64H) and then the PIT Lower Lifetime Timer Register (PIT_LTMR64L).

3.24 Sine wave generator

The MPC5643L and MPC5744P both support a sine wave generator (SWG) which generates an analog sine wave signal that can range from 1 KHz up to 50 KHz.

The normal output of the SWG is a free running sine wave of a specified amplitude and frequency.

As an enhancement to the MPC5643L SWG, the MPC5744P SWG adds support for two trigger signals to enable the user to phase-align the sine wave output to the activation of the trigger input. Software can enable this feature in the SWG Control Register (SWG_CTRL). When the sine wave is started, the trigger signal will be continuously checked for a phase offset. If there is a phase offset, the SWG will re-align the sine wave output so that the phase difference becomes zero.

4 Hardware considerations

4.1 Device packages

The MPC5643L and MPC5744P are both available in 144-pin LQFP and 257-ball MAPBGA production packages.

Because package pitch and case outline are maintained, the same socket type can be reused on the MPC5744P.

Package	MPC5643L	MPC5744P
144-pin LQFP	0.5 mm pitch 20 mm x 20 mm outline	
257-ball MAPBGA	0.8 mm pitch 14 mm x 14 mm outline	

4.2 Pin compatibility

Three pins differ in functionality between the 144LQFP package of the MPC5643L and MPC5744P.

The MPC5643L VDD_HV_REG_0:1 pins are replaced with port pins J[9] and J[8] on the MPC5744P. Since these pins are now GPIOs, the MPC5744P can be installed on existing MPC5643L designs that connect these pins to VDD. In this case, it must be ensured that these GPIOs are not configured as outputs.

The VDD_HV_REG_2 is now the external power-on reset pin EXT_POR on the MPC5744P. The EXT_POR is an optional pin that can be used to delay the start of the reset sequence progression until the supplies are stable. It is not mandatory for start-up, therefore, there is no issue when this pin is connected to VDD in existing MPC5643L designs.

Pin	MPC5643L	MPC5744P
16	VDD_HV_REG_0	J[9]
95	VDD_HV_REG_1	J[8]
130	VDD_HV_REG_2	EXT_POR

Compatibility between the 257BGA package of the MPC5643L and MPC5744P is not maintained. Hardware must be redesigned to use the 257BGA package.

4.3 Power supply

The power supply concept between the MPC5643L and MPC5744P share several commonalities.

The voltage regulator, I/O, flash, oscillator and ADC supply voltages remain 3.3 V (nominal). However, while the MPC5643L voltage range is 3.0 V to 3.6 V, the MPC5744P requires a narrower range of 3.15 V to 3.6 V. Both devices support ADC reference voltages of either 3.3 V or 5 V. Both devices also support internal regulation mode when using an external ballast transistor. The internal regulation mode allows a single 3.3 V supply to be input to the MPC5744P when an external ballast transistor is present.

However, the MPC5744P adds an external regulation option that allows 1.25 V ± 5% to be input to the core supply pins. This mode removes the requirement for an external ballast transistor. While the MPC5643L supports an internal ballast transistor, the MPC5744P does not support it.

The MPC5744P adds the Nexus Aurora and LFAST modules in the 257BGA package. These blocks require 1.25 V voltage supplies.

Supply	MPC5643L	MPC5744P
Voltage regulator supply voltage	3.0 V to 3.6 V	3.15 V to 3.6 V
I/O supply voltage		
Flash supply voltage		
Oscillator supply voltage		
ADC supply voltage		
ADC reference voltage	3.3 V or 5 V	3.3 V or 5 V
Core supply	Internal regulation with external ballast transistor or Internal ballast transistor	Internal regulation with external ballast transistor or 1.25 V ± 5% external regulation
Aurora supply voltage	N/A	1.25 V
LFAST supply voltage		

4.4 Operating temperature

The MPC5744P supports an extended junction temperature of up to 165°C.

The printed circuit board (PCB) and board components must meet the extended temperature requirements when exposing the MPC5744P to high temperature testing.

Feature	MPC5643L	MPC5744P
Junction temperature range	-40°C to 150°C	-40°C to 150°C with 165°C option
Ambient temperature range	-40°C to 125°C	-40°C to 125°C with option for higher Ta (TBD)

4.5 I/O multiplexing

Hardware design must take into consideration the changes in pin multiplexing from the MPC5643L to MPC5744P.

Most of the port pins' functionality remains the same, however, some pins now have added alternate functions. The addition of new modules also affects some pins' supported functionality.

Port pin	Changes to MPC5744P
A[4]	Adds FlexPWM_1 A2 alternate function
A[7]	Adds eTimer_2 ETC3 alternate function
A[8]	Adds eTimer_2 ETC4 alternate function
A[9]	Adds eTimer_2 ETC5 alternate function
C[13]	Adds FlexPWM_1 A0 alternate function
C[14]	Adds FlexPWM_1 B0 alternate function
D[5]	Adds SENT0 SENT_RX[0] alternate function
D[7]	Adds SENT1 SENT_RX[0] alternate function
E[13]	Adds DSPI1 CS4 alternate function
E[14]	Adds DSPI1 CS5 and FlexPWM_1 B2 alternate functions
F[12]	Adds FlexPWM_1 A1 alternate function
F[13]	Adds FlexPWM_1 B1 alternate function
F[14]	Adds FlexCAN2 TXD alternate function
F[15]	Adds FlexCAN2 RXD alternate function
G[12:15]	Not implemented on MPC5744P. On MPC5643L these pins were Nexus data out MDO8:11. The MPC5744P only supports MDO0:3.
H[0:3]	Not implemented on MPC5744P. On MPC5643L these pins were Nexus data out MDO4:7. The MPC5744P only supports MDO0:3.
I[4:15]	New on MPC5744P BGA. Adds DSPI3, SENT0, SENT1, FlexCAN2, CTU_0 and LFAST functionality.
J[0:9]	New on MPC5744P BGA. Adds DSPI3, SENT0, SENT1, FlexCAN2, CTU_1, eTimer_2 and ADC functionality.

5 Summary

Freescale's MPC5744P offers some changes and enhancements over the MPC5643L.

This document provides information on how to migrate existing MPC5643L designs to the MPC5744P. Software and hardware must address these major feature changes:

- Delayed lock-step mode only
- VLE instruction set only
- 32-bit general-purpose core registers
- End-to-end ECC protection for all memories
- External regulation for the core supply
- Core and system-level memory protection
- Option for extended junction temperature
- Enhanced pad control capabilities
- Additional port pin functionality in I/O multiplexing
- MBIST and LBSIT at startup and shutdown
- MEMU for ECC error collection and reporting
- Increased configurability of FCCU fault reactions
- Changes in FCCU input mapping
- 55 nm-based Flash memory controller
- Larger SRAM and Flash memory
- Clock distribution changes
- Additional clock monitors
- Trigger signals in the SWG
- ADC high calibration mode
- ADC self-test algorithm changes
- Dual conversion mode and interleaved triggering in the CTUs
- More DMA channels
- Changes in interrupt vector assignments

6 References

For additional information, refer to the following documentation:

- MPC5744P Reference Manual
- MPC5643L Reference Manual

7 Revision history

Revision	Description of changes
0	Initial release.
1	• In Overview section, changed latency monitor to "Yes" in MPC5744P column. • Updated Cyclic redundancy checking section to reflect cut 2 features.

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Document Number: AN4624
Rev. 1, 11/2012