



# **MX29GL256E DATASHEET**

The MX29GL256E product family is not recommended for new designs, while MX29GL256F family is suggested to replace it. Please refer to MX29GL256F datasheet for specifications and ordering information, or contact your local sales representative for additional support.

P/N:PM1499 REV. 1.4, JUL. 26, 2011



# SINGLE VOLTAGE 3V ONLY FLASH MEMORY

The MX29GL256E product family is not recommended for new designs, while MX29GL256F family is suggested to replace it. Please refer to MX29GL256F datasheet for specifications and ordering information, or contact your local sales representative for additional support.

#### **FEATURES**

# **GENERAL FEATURES**

- · Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
  - MX29GL256E H/L: VI/O=VCC=2.7V~3.6V, VI/O voltage must tight with VCC
  - MX29GL256E U/D: VI/O=1.65V~3.6V for Input/Output
- · Byte/Word mode switchable
- 33,554,432 x 8 / 16,777,216 x 16
- 64KW/128KB uniform sector architecture
- 256 equal sectors
- 16-byte/8-word page read buffer
- 64-byte/32-word write buffer
- Extrá 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced sector protection function (Solid and Password Protect)
- Latch-up protected to 100mA from -1V to 1.5xVcc
   Low Vcc write inhibit: Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode

#### **PERFORMANCE**

- High Performance
- Fast access time:
  - MX29GL256E H/L: 100ns (VCC=2.7~3.6V), 90ns (VCC=3.0~3.6V)
  - MX29GL256E U/D: 110ns (VCC=2.7~3.6V, V I/O=1.65 to Vcc)
- Page access time:
  - MX29GL256E H/L: 25ns
- MX29GL256E U/D: 30ns Fast program time: 11us/word
- Fast erase time: 0.6s/sector
- Low Power Consumption
- Low active read current: 30mA (typical) at 5MHz
- Low standby current: 30uA (typical)
- Typical 100,000 erase/program cyclé
- 20 years data retention

#### **SOFTWARE FEATURES**

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Status Reply
- Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

### HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
- Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
- Hardware write protect pin/Provides accelerated program capability



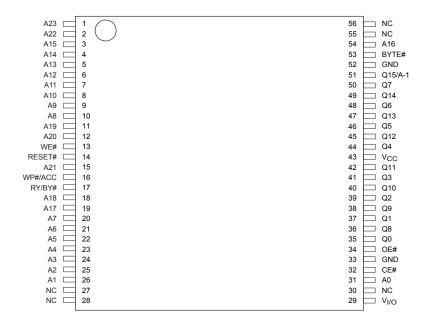


#### **PACKAGE**

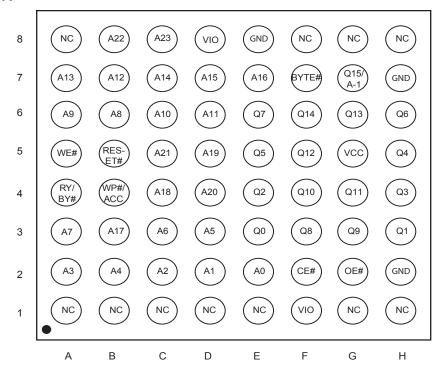
- 56-Pin TSOP
- 64-Ball FBGA (10mm x 13mm)
- 64-Ball LFBGA (11mm x 13mm)
- 70-Pin SSOP
- All devices are RoHS Compliant

### **PIN CONFIGURATION**

### **56 TSOP**

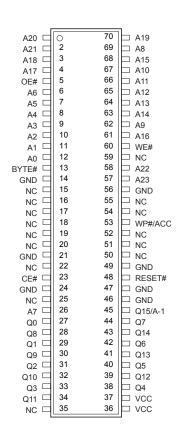


### 64 FBGA/64 LFBGA





### **70 SSOP**



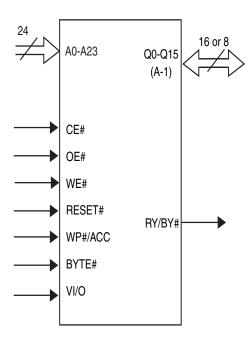
### **PIN DESCRIPTION**

CE# Chip Enable Input WE# Write Enable Input OE# Output Enable Input RESET# Hardware Reset Pin, Active Low		
Q0~Q14 Data Inputs/Outputs Q15/A-1 Q15(Word Mode)/LSB addr(Byte Mode) CE# Chip Enable Input WE# Write Enable Input OE# Output Enable Input RESET# Hardware Reset Pin, Active Low WP#/ACC* Hardware Write Protect/Programming Acceleration input RY/BY# Ready/Busy Output BYTE# Selects 8 bits or 16 bits mode VCC +3.0V single power supply GND Device Ground NC Pin Not Connected Internally	SYMBOL	PIN NAME
Q15/A-1 Q15(Word Mode)/LSB addr(Byte Mode) CE# Chip Enable Input WE# Write Enable Input OE# Output Enable Input RESET# Hardware Reset Pin, Active Low WP#/ACC* Hardware Write Protect/Programming Acceleration input RY/BY# Ready/Busy Output BYTE# Selects 8 bits or 16 bits mode VCC +3.0V single power supply GND Device Ground NC Pin Not Connected Internally	A0~A23	Address Input
CE# Chip Enable Input  WE# Write Enable Input  OE# Output Enable Input  RESET# Hardware Reset Pin, Active Low  WP#/ACC* Hardware Write Protect/Programming Acceleration input  RY/BY# Ready/Busy Output  BYTE# Selects 8 bits or 16 bits mode  VCC +3.0V single power supply  GND Device Ground  NC Pin Not Connected Internally	Q0~Q14	Data Inputs/Outputs
WE# Write Enable Input OE# Output Enable Input RESET# Hardware Reset Pin, Active Low WP#/ACC* Hardware Write Protect/Programming Acceleration input RY/BY# Ready/Busy Output BYTE# Selects 8 bits or 16 bits mode VCC +3.0V single power supply GND Device Ground NC Pin Not Connected Internally	Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
OE# Output Enable Input  RESET# Hardware Reset Pin, Active Low  WP#/ACC* Hardware Write Protect/Programming Acceleration input  RY/BY# Ready/Busy Output  BYTE# Selects 8 bits or 16 bits mode  VCC +3.0V single power supply  GND Device Ground  NC Pin Not Connected Internally	CE#	Chip Enable Input
RESET# Hardware Reset Pin, Active Low  WP#/ACC* Hardware Write Protect/Programming Acceleration input  RY/BY# Ready/Busy Output  BYTE# Selects 8 bits or 16 bits mode  VCC +3.0V single power supply  GND Device Ground  NC Pin Not Connected Internally	WE#	Write Enable Input
WP#/ACC* Hardware Write Protect/Programming Acceleration input  RY/BY# Ready/Busy Output  BYTE# Selects 8 bits or 16 bits mode  VCC +3.0V single power supply  GND Device Ground  NC Pin Not Connected Internally	OE#	Output Enable Input
Acceleration input  RY/BY# Ready/Busy Output  BYTE# Selects 8 bits or 16 bits mode  VCC +3.0V single power supply  GND Device Ground  NC Pin Not Connected Internally	RESET#	Hardware Reset Pin, Active Low
BYTE# Selects 8 bits or 16 bits mode  VCC +3.0V single power supply  GND Device Ground  NC Pin Not Connected Internally	WP#/ACC*	Hardware Write Protect/Programming Acceleration input
VCC +3.0V single power supply GND Device Ground NC Pin Not Connected Internally	RY/BY#	Ready/Busy Output
GND Device Ground  NC Pin Not Connected Internally	BYTE#	Selects 8 bits or 16 bits mode
NC Pin Not Connected Internally	VCC	+3.0V single power supply
-	GND	Device Ground
VI/O Power Supply for Input/Output	NC	Pin Not Connected Internally
	VI/O	Power Supply for Input/Output

### Notes:

- 1. WP#/ACC has internal pull up.
- 2. For MX29GL256E H/L VI/O voltage must tight with VCC. VI/O = VCC =2.7V~3.6V.

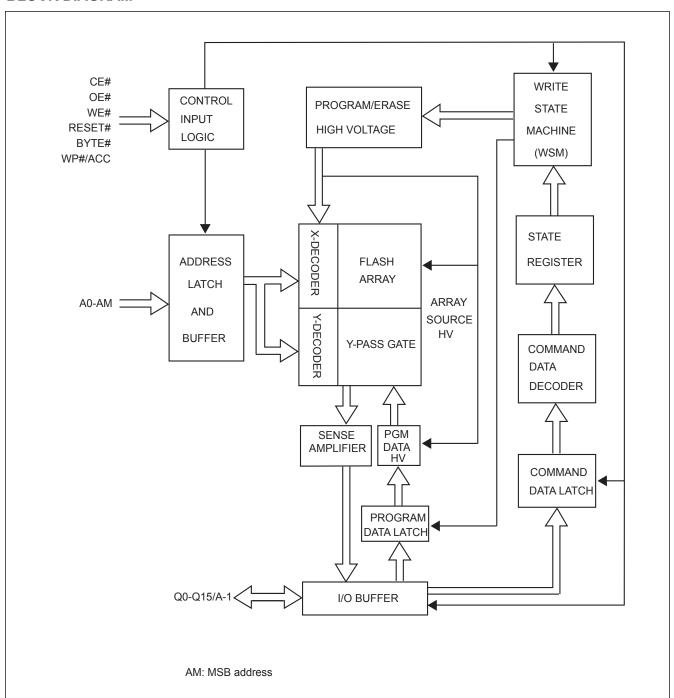
### LOGIC SYMBOL







# **BLOCK DIAGRAM**





# **BLOCK DIAGRAM DESCRIPTION**

The *block diagram* on Page 5 illustrates a simplified architecture of this device. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(A23). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

### **ARRAY ARCHITECTURE**

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in *Table 1*.





# **BLOCK STRUCTURE**

Table 1. MX29GL256E SECTOR ARCHITECTURE

Secto	or Size	Sector	Sector Address	(x16)
Kbytes	Kwords	Sector	A23-A16	Address Range
128	64	SA0	00000000	000000h-00FFFFh
128	64	SA1	0000001	010000h-01FFFFh
128	64	SA2	00000010	020000h-02FFFFh
128	64	SA3	00000011	030000h-03FFFFh
128	64	SA4	00000100	040000h-04FFFFh
128	64	SA5	00000101	050000h-05FFFFh
128	64	SA6	00000110	060000h-06FFFFh
128	64	SA7	00000111	070000h-07FFFh
128	64	SA8	00001000	080000h-08FFFFh
128	64	SA9	00001001	090000h-09FFFh
128	64	SA10	00001010	0A0000h-0AFFFFh
128	64	SA11	00001011	0B0000h-0BFFFFh
128	64	SA12	00001100	0C0000h-0CFFFFh
128	64	SA13	00001101	0D0000h-0DFFFFh
128	64	SA14	00001110	0E0000h-0EFFFFh
128	64	SA15	00001111	0F0000h-0FFFFh
128	64	SA16	00010000	100000h-10FFFFh
128	64	SA17	00010001	110000h-11FFFFh
128	64	SA18	00010010	120000h-12FFFFh
128	64	SA19	00010011	130000h-13FFFFh
128	64	SA20	00010100	140000h-14FFFFh
128	64	SA21	00010101	150000h-15FFFFh
128	64	SA22	00010110	160000h-16FFFFh
128	64	SA23	00010111	170000h-17FFFFh
128	64	SA24	00011000	180000h-18FFFFh
128	64	SA25	00011001	190000h-19FFFFh
128	64	SA26	00011010	1A0000h-1AFFFFh
128	64	SA27	00011011	1B0000h-1BFFFFh
128	64	SA28	00011100	1C0000h-1CFFFFh
128	64	SA29	00011101	1D0000h-1DFFFFh
128	64	SA30	00011110	1E0000h-1EFFFFh
128	64	SA31	00011111	1F0000h-1FFFFFh
128	64	SA32	00100000	200000h-20FFFFh
128	64	SA33		
128	64			220000h-22FFFFh
128	64	SA35	00100011	230000h-23FFFFh
128	64	SA36	00100100	240000h-24FFFFh
128	64	SA37	00100101	250000h-25FFFFh
128	64	SA38	00100110	260000h-26FFFFh
128	64	SA39	00100111	270000h-27FFFh



Sect	or Size		Sector Address	(x16)
Kbytes	Kwords	Sector	A23-A16	Address Range
128	64	SA40	00101000	280000h-28FFFFh
128	64	SA41	00101001	290000h-29FFFFh
128	64	SA42	00101010	2A0000h-2AFFFFh
128	64	SA43	00101011	2B0000h-2BFFFFh
128	64	SA44	00101100	2C0000h-2CFFFFh
128	64	SA45	00101101	2D0000h-2DFFFFh
128	64	SA46	00101110	2E0000h-2EFFFFh
128	64	SA47	00101111	2F0000h-2FFFFFh
128	64	SA48	00110000	300000h-30FFFFh
128	64	SA49	00110001	310000h-31FFFFh
128	64	SA50	00110010	320000h-32FFFFh
128	64	SA51	00110011	330000h-33FFFFh
128	64	SA52	00110100	340000h-34FFFFh
128	64	SA53	00110101	350000h-35FFFFh
128	64	SA54	00110110	360000h-36FFFFh
128	64	SA55	00110111	370000h-37FFFFh
128	64	SA56	00111000	380000h-38FFFFh
128	64	SA57	00111001	390000h-39FFFFh
128	64	SA58	00111010	3A0000h-3AFFFFh
128	64	SA59	00111011	3B0000h-3BFFFFh
128	64	SA60	00111100	3C0000h-3CFFFFh
128	64	SA61	00111101	3D0000h-3DFFFFh
128	64	SA62	00111110	3E0000h-3EFFFFh
128	64	SA63	00111111	3F0000h-3FFFFFh
128	64	SA64	01000000	400000h-40FFFFh
128	64	SA65	01000001	410000h-41FFFFh
128	64	SA66	01000010	420000h-42FFFFh
128	64	SA67	01000011	430000h-43FFFFh
128	64	SA68	01000100	440000h-44FFFFh
128	64	SA69	01000101	450000h-45FFFFh
128	64	SA70	01000110	460000h-46FFFFh
128	64	SA71	01000111	470000h-47FFFFh
128	64	SA72	01001000	480000h-48FFFFh
128	64	SA73	01001001	490000h-49FFFFh
128	64	SA74	01001010	4A0000h-4AFFFFh
128	64	SA75 01001011		4B0000h-4BFFFFh
128	64	SA76	SA76 01001100 4	
128	64	SA77		
128	64	SA78	01001110	4E0000h-4EFFFFh
128	64	SA79	01001111	4F0000h-4FFFFFh
128	64	SA80	01010000	500000h-50FFFFh
128	64	SA81	01010001	510000h-51FFFFh



Secto	r Size		Sector Address	(x16)
Kbytes	Kwords	Sector	A23-A16	Address Range
128	64	SA82	01010010	520000h-52FFFFh
128	64	SA83	01010011	530000h-53FFFFh
128	64	SA84	01010100	540000h-54FFFFh
128	64	SA85	01010101	550000h-55FFFFh
128	64	SA86	01010110	560000h-56FFFFh
128	64	SA87	01010111	570000h-57FFFFh
128	64	SA88	01011000	580000h-58FFFFh
128	64	SA89	01011001	590000h-59FFFFh
128	64	SA90	01011010	5A0000h-5AFFFFh
128	64	SA91	01011011	5B0000h-5BFFFFh
128	64	SA92	01011100	5C0000h-5CFFFFh
128	64	SA93	01011101	5D0000h-5DFFFFh
128	64	SA94	01011110	5E0000h-5EFFFFh
128	64	SA95	01011111	5F0000h-5FFFFh
128	64	SA96	01100000	600000h-60FFFFh
128	64	SA97	01100001	610000h-61FFFFh
128	64	SA98	01100010	620000h-62FFFFh
128	64	SA99	01100011	630000h-63FFFFh
128	64	SA100	01100100	640000h-64FFFFh
128	64	SA101	01100101	650000h-65FFFFh
128	64	SA102	01100110	660000h-66FFFFh
128	64	SA103	01100111	670000h-67FFFh
128	64	SA104	01101000	680000h-68FFFFh
128	64	SA105	01101001	690000h-69FFFFh
128	64	SA106	01101010	6A0000h-6AFFFh
128	64	SA107	01101011	6B0000h-6BFFFFh
128	64	SA108	01101100	6C0000h-6CFFFh
128	64	SA109	01101101	6D0000h-6DFFFFh
128	64	SA110	01101110	6E0000h-6EFFFh
128	64	SA111	01101111	6F0000h-6FFFFh
128	64	SA112	01110000	700000h-70FFFFh
128	64	SA113	01110001	710000h-71FFFFh
128	64	SA114	01110010	720000h-72FFFFh
128	64	SA115	01110011	730000h-73FFFFh
128	64	SA116		
128	64	SA117	SA117 01110101	
128	64	SA118	SA118 01110110	
128	64	SA119		
128	64	SA120	01111000	780000h-78FFFFh
128	64	SA121	01111001	790000h-79FFFFh
128	64	SA122	01111010	7A0000h-7AFFFFh
128	64	SA123	01111011	7B0000h-7BFFFFh



Secto	or Size		Sector Address	(x16)
Kbytes	Kwords	Sector	A23-A16	Address Range
128	64	SA124	01111100	7C0000h-7CFFFh
128	64	SA125	01111101	7D0000h-7DFFFFh
128	64	SA126 01111110		7E0000h-7EFFFFh
128	64	SA127	01111111	7F0000h-7FFFFh
128	64	SA128	10000000	800000h-80FFFFh
128	64	SA129	10000001	810000h-81FFFFh
128	64	SA130	10000010	820000h-82FFFFh
128	64	SA131	10000011	830000h-83FFFFh
128	64	SA132	10000100	840000h-84FFFFh
128	64	SA133	10000101	850000h-85FFFFh
128	64	SA134	10000110	860000h-86FFFFh
128	64	SA135	10000111	870000h-87FFFFh
128	64	SA136	10001000	880000h-88FFFFh
128	64	SA137	10001001	890000h-89FFFFh
128	64	SA138	10001010	8A0000h-8AFFFFh
128	64	SA139	10001011	8B0000h-8BFFFFh
128	64	SA140	10001100	8C0000h-8CFFFh
128	64	SA141	10001101	8D0000h-8DFFFFh
128	64	SA142	10001110	8E0000h-8EFFFFh
128	64	SA143	10001111	8F0000h-8FFFFFh
128	64	SA144	10010000	900000h-90FFFFh
128	64	SA145	10010001	910000h-91FFFFh
128	64	SA146	10010010	920000h-92FFFFh
128	64	SA147	10010011	930000h-93FFFFh
128	64	SA148	10010100	940000h-94FFFFh
128	64	SA149	10010101	950000h-95FFFFh
128	64	SA150	10010110	960000h-96FFFFh
128	64	SA151	10010111	970000h-97FFFh
128	64	SA152	10011000	980000h-98FFFFh
128	64	SA153	10011001	990000h-99FFFFh
128	64	SA154	10011010	9A0000h-9AFFFh
128	64	SA155	10011011	9B0000h-9BFFFFh
128	64	SA156	10011100	9C0000h-9CFFFh
128	64	SA157	10011101	9D0000h-9DFFFFh
128	64	SA158		
128	64	SA159		
128	64	SA160	SA160 10100000	
128	64	SA161		
128	64	SA162	10100010	A20000h-A2FFFFh
128	64	SA163	10100011	A30000h-A3FFFFh
128	64	SA164	10100100	A40000h-A4FFFFh
128	64	SA165	10100101	A50000h-A5FFFFh



Sect	or Size		Sector Address	(x16)	
Kbytes	Kwords	Sector	A23-A16	Address Range	
128	64	SA166	10100110	A60000h-A6FFFFh	
128	64	SA167	10100111	A70000h-A7FFFFh	
128	64	SA168	10101000	A80000h-A8FFFFh	
128	64	SA169	10101001	A90000h-A9FFFFh	
128	64	SA170	10101010	AA0000h-AAFFFFh	
128	64	SA171	10101011	AB0000h-ABFFFFh	
128	64	SA172	10101100	AC0000h-ACFFFh	
128	64	SA173	10101101	AD0000h-ADFFFFh	
128	64	SA174	10101110	AE0000h-AEFFFFh	
128	64	SA175	10101111	AF0000h-AFFFFFh	
128	64	SA176	10110000	B00000h-B0FFFFh	
128	64	SA177	10110001	B10000h-B1FFFFh	
128	64	SA178	10110010	B20000h-B2FFFFh	
128	64	SA179	10110011	B30000h-B3FFFFh	
128	64	SA180	10110100	B40000h-B4FFFFh	
128	64	SA181	10110101	B50000h-B5FFFFh	
128	64	SA182	10110110	B60000h-B6FFFFh	
128	64	SA183	10110111	B70000h-B7FFFFh	
128	64	SA184	10111000	B80000h-B8FFFFh	
128	64	SA185	10111001	B90000h-B9FFFFh	
128	64	SA186	10111010	BA0000h-BAFFFFh	
128	64	SA187	10111011	BB0000h-BBFFFFh	
128	64	SA188	10111100	BC0000h-BCFFFh	
128	64	SA189	10111101	BD0000h-BDFFFFh	
128	64	SA190	10111110	BE0000h-BEFFFFh	
128	64	SA191	10111111	BF0000h-BFFFFFh	
128	64	SA192	11000000	C00000h-C0FFFFh	
128	64	SA193	11000001	C10000h-C1FFFFh	
128	64	SA194	11000010	C20000h-C2FFFFh	
128	64	SA195	11000011	C30000h-C3FFFFh	
128	64	SA196	11000100	C40000h-C4FFFFh	
128	64	SA197	11000101	C50000h-C5FFFFh	
128	64	SA198	11000110	C60000h-C6FFFFh	
128	64	SA199	11000111	C70000h-C7FFFFh	
128	64	SA200	11001000	C80000h-C8FFFFh	
128	64	SA201	SA201 11001001		
128	64	SA202	SA202 11001010		
128	64	SA203	SA203 11001011 (		
128	64	SA204	11001100	CC0000h-CCFFFFh	
128	64	SA205	11001101	CD0000h-CDFFFFh	
128	64	SA206	11001110	CE0000h-CEFFFFh	
128	64	SA207	11001111	CF0000h-CFFFFh	



Sect	tor Size	0	Sector Address	(x16)
Kbytes	Kwords	Sector	A23-A16	Address Range
128	64	SA208	11010000	D00000h-D0FFFFh
128	64	SA209	11010001	D10000h-D1FFFFh
128	64	SA210	11010010	D20000h-D2FFFFh
128	64	SA211	11010011	D30000h-D3FFFFh
128	64	SA212	11010100	D40000h-D4FFFFh
128	64	SA213	11010101	D50000h-D5FFFFh
128	64	SA214	11010110	D60000h-D6FFFFh
128	64	SA215	11010111	D70000h-D7FFFFh
128	64	SA216	11011000	D80000h-D8FFFFh
128	64	SA217	11011001	D90000h-D9FFFFh
128	64	SA218	11011010	DA0000h-DAFFFFh
128	64	SA219	11011011	DB0000h-DBFFFFh
128	64	SA220	11011100	DC0000h-DCFFFFh
128	64	SA221	11011101	DD0000h-DDFFFFh
128	64	SA222	11011110	DE0000h-DEFFFFh
128	64	SA223	11011111	DF0000h-DFFFFh
128	64	SA224	11100000	E00000h-E0FFFh
128	64	SA225	11100001	E10000h-E1FFFFh
128	64	SA226	11100010	E20000h-E2FFFFh
128	64	SA227	11100011	E30000h-E3FFFFh
128	64	SA228	11100100	E40000h-E4FFFFh
128	64	SA229	11100101	E50000h-E5FFFh
128	64	SA230	11100110	E60000h-E6FFFFh
128	64	SA231	11100111	E70000h-E7FFFh
128	64	SA232	11101000	E80000h-E8FFFFh
128	64	SA233	11101001	E90000h-E9FFFh
128	64	SA234	11101010	EA0000h-EAFFFFh
128	64	SA235	11101011	EB0000h-EBFFFFh
128	64	SA236	11101100	EC0000h-ECFFFFh
128	64	SA237	11101101	ED0000h-EDFFFFh
128	64	SA238	11101110	EE0000h-EEFFFFh
128	64	SA239	11101111	EF0000h-EFFFFh
128	64	SA240	11110000	F00000h-F0FFFh
128	64	SA241	11110001	F10000h-F1FFFFh
128	64	SA242	SA242 11110010	
128	64	SA243	SA243 11110011	
128	64	SA244	SA244 11110100	
128	64	SA245	SA245 11110101	
128	64	SA246	11110110	F60000h-F6FFFh
128	64	SA247	11110111	F70000h-F7FFFh
128	64	SA248	11111000	F80000h-F8FFFFh
128	64	SA249	11111001	F90000h-F9FFFh



Sect	Sector Size		Sector Address	(x16)
Kbytes	Kwords	Sector	A23-A16	Address Range
128	64	SA250	11111010	FA0000h-FAFFFFh
128	64	SA251	11111011	FB0000h-FBFFFFh
128	64	SA252	11111100	FC0000h-FCFFFh
128	64	SA253	11111101	FD0000h-FDFFFFh
128	64	SA254	11111110	FE0000h-FEFFFh
128	64	SA255	11111111	FF0000h-FFFFFFh



### **BUS OPERATION**

# **Table 2-1. BUS OPERATION**

						Doto	Ву	te#		
Mode Select	RE-	CE#	WE#	OE#	Address	Data I/O	Vil	Vih	WP#/	
Wode Select	SET#	CE#	VVE#	OE#	(Note4)	Q7~Q0	Data (I/O) Q15~Q8		ACC	
Device Reset	L	X	Х	Х	X	HighZ	HighZ	HighZ	L/H	
Standby Mode	Vcc ± 0.3V	Vcc± 0.3V	Х	Х	Х	HighZ	HighZ	HighZ	Н	
Output Disable	Н	L	Н	Н	X	HighZ	HighZ	HighZ	L/H	
Read Mode	Н	L	Н	L	AIN	DOUT	Q8-Q14=	DOUT	L/H	
Write	Н	L	L	Н	AIN	DIN	HighZ,	DIN	Note1,2	
Accelerate Program	Н	L	L	Н	AIN	DIN	Q15=A-1	DIN	Vhv	

#### Notes:

- 1. The first or last sector was protected if WP#/ACC=Vil.
- 2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
- 3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
- 4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address. In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.



# **Table 2-2. BUS OPERATION**

	Con	trol Ir	nput	AM	A11		A8		A5	<b>A3</b>				
Item	CE#	WE#	OE#	to A12	to A10	A9	to A7	A6	to A4	to A2	<b>A</b> 1	A0	Q7 ~ Q0	Q15 ~ Q8
Sector Lock Status Verification	L	Н	L	SA	X	V <sub>hv</sub>	X	L	Х	L	Н	L	01h or 00h (Note 1)	Х
Read Silicon ID Manufacturer Code	L	Н	L	Х	Х	$V_{hv}$	Х	L	Х	L	L	L	C2H	Х
Read Silicon ID N	/IX290	3L256	E											
Cycle 1	L	Н	L	Х	Х	V <sub>hv</sub>	Χ	L	Х	L	L	Н	7EH	22H(Word), XXH(Byte)
Cycle 2	L	Н	L	Х	Х	V <sub>hv</sub>	Х	L	Х	Н	Н	L	22H	22H(Word), XXH(Byte)
Cycle 3	L	Н	L	Х	Х	V <sub>hv</sub>	X	L	Х	Н	Н	Н	01H	22H(Word), XXH(Byte)

### Notes:

1. Sector unprotected code:00h. Sector protected code:01h.

2. Factory locked code: WP# protects high address sector: 99h.

WP# protects low address sector: 89h

Factory unlocked code: WP# protects high address sector: 19h.

WP# protects low address sector: 09h

3. AM: MSB of address.



#### **FUNCTIONAL OPERATION DESCRIPTION**

#### **READ OPERATION**

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

#### **PAGE READ**

This device is able to conduct MXIC MaskROM compatible high performance page read. Page size is 16 bytes or 8 words. The higher address Amax ~ A3 select the certain page, while A2~A0 for word mode, A2~A-1 for byte mode select the particular word or byte in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

### WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in *Figure 1*. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

### **DEVICE RESET**

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

### STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.



## **FUNCTIONAL OPERATION DESCRIPTION (cont'd)**

### **OUTPUT DISABLE**

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Byte or Word Data (I/O) pins will drive data.

### **BYTE/WORD SELECTION**

The BYTE# input pin is used to select the organization of the array data and how the data is input/output on the Data (I/O) pins. If the BYTE# pin is held HIGH, Word mode will be selected and all 16 data lines (Q0 to Q15) will be active.

If BYTE# is forced LOW, Byte mode will be active and only data lines Q0 to Q7 will be active. Data lines Q8 to Q14 will remain in a high impedance state and Q15 becomes the A-1 address input pin.

#### HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

### ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

#### WRITE BUFFER PROGRAMMING OPERATION

Programs 64bytes/32words in a programming operation. To trigger the Write Buffer Programming, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined programming Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax-A5.

"Write-Buffer-Page" address has to be the same for all address/ data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it'll return to normal READ mode.



# **FUNCTIONAL OPERATION DESCRIPTION (cont'd)**

## WRITE BUFFER PROGRAMMING OPERATION (cont'd)

ABORT will be executed for the Write Buffer Programming Sequence if following condition occurs:

- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle. A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

#### SECTOR PROTECT OPERATION

The device provides user programmable protection operations for selected sectors. Please refer to *Table 1* which show all Sector assignments.

During the protection operation, the sector address of any sector may be used to specify the Sector being protected.

## **AUTOMATIC SELECT BUS OPERATIONS**

The following five bus operations require A9 to be raised to Vhv. Please see AUTOMATIC SELECT COMMAND SEQUENCE in the COMMAND OPERATIONS section for details of equivalent command operations that do not require the use of Vhv.

### SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins A23 to A12, address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.



# **FUNCTIONAL OPERATION DESCRIPTION (cont'd)**

#### READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q7 to Q0.

## READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 99h(H)/89h(L) will be present on data bits Q7 to Q0. Otherwise, the factory unlocked code of 19h(H)/09h(L) will be present.

### INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

#### **COMMAND COMPLETION**

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

# **LOW VCC WRITE INHIBIT**

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

## WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

#### **LOGICAL INHIBIT**

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.



# **FUNCTIONAL OPERATION DESCRIPTION (cont'd)**

### **POWER-UP SEQUENCE**

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

### **POWER-UP WRITE INHIBIT**

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

# **POWER SUPPLY DECOUPLING**

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.



### **COMMAND OPERATIONS**

#### READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to *READ OPERATION* in the *BUS OPERATIONS* section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding 20us) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector (s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

- 1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.
- 2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

### **AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY**

The device provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct *cycle* defined in the *Table 3* (including 2 unlock cycles and the A0H program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.



## **COMMAND OPERATIONS (cont'd)**

# AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY (cont'd)

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

Status	Q7 <sup>*1</sup>	Q6 <sup>*1</sup>	Q5	Q1	RY/BY# (Note)
In progress	Q7#	Toggling	0	0	0
Exceed time limit	Q7#	Toggling	1	N/A	0

Note: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

## **ERASING THE MEMORY ARRAY**

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in **Section** *Advanced Sector Protection/Un-protection*.

### **SECTOR ERASE**

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. Note that the 50us timer-out counter is restarted after every erase command sequence. If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.



## **COMMAND OPERATIONS (cont'd)**

## **SECTOR ERASE (cont'd)**

The system can determine the status of the embedded sector erase operation by the following methods:

Status	Q7	Q6	Q5	Q3*1	Q2	RY/BY# <sup>*2</sup>
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Exceeded time limit	0	Toggling	1	1	Toggling	0

#### Notes:

- 1. The Q3 status bit is the 50us time-out indicator. When Q3=0, the 50us time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the 50us time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.
- 2. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
- 3. When an attempt is made to erase only protected sector (s), the erase operation will abort thus preventing any data changes in the protected sector (s). Q7 will output "0" and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector (s) will remain unchanged.
- 4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

### CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY# <sup>*1</sup>
In progress	0	Toggling	0	Toggling	0
Exceed time limit	0	Toggling	1	Toggling	0

<sup>\*1:</sup> RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.



# **COMMAND OPERATIONS (cont'd)**

### **ERASE SUSPEND/RESUME**

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until 20us time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector (s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle	N/A	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

#### SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 400us interval between Ease Resume and the next Erase Suspend command.



## **COMMAND OPERATIONS (cont'd)**

#### PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend is the only valid command that may be issued. The system can determine if the device has entered the Program-Suspended Read mode through Q6 and RY/BY#.

After the device has entered Program-Suspended mode, the system can read any sector (s) except those being programmed by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Program suspend read in program suspended sector			Inv	alid			1
Program suspend read in non-program suspended sector	Data	Data	Data	Data	Data	Data	1

When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security silicon.

### **PROGRAM RESUME**

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a 5us interval between Program Resume and the next Program Suspend command.

### **BUFFER WRITE ABORT**

Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read status register shown as following table:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Buffer Write Busy	Q7#	Toggle	0	N/A	N/A	0	0
Buffer Write Abort	Q7#	Toggle	0	N/A	N/A	1	0
Buffer Write Exceeded Time Limit	Q7#	Toggle	1	N/A	N/A	0	0



# **COMMAND OPERATIONS (cont'd)**

#### **AUTOMATIC SELECT OPERATIONS**

When the device is in Read mode, Program Suspended mode, Erase-Suspended Read mode, or CFI mode, the user can issue the *Automatic Select* command shown in *Table 3* (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active) or Program Suspended Read mode if Program Suspend was active.

Another way to enter Automatic Select mode is to use one of the bus operations shown in *Table 2-2. BUS OP-ERATION*. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

### **AUTOMATIC SELECT COMMAND SEQUENCE**

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

			Address	Data (Hex)	Representation
Manufacturer II		Word	X00	C2	
ivianuiaciurei ii	J	Byte	X00	C2	
Device ID	MY20CL 25CE	Word	X01/0E/0F	227E/2222/2201	
Device ID	MX29GL256E	Byte	X02/1C/1E	7E/22/01	
		Word	X03	99/19 (H)	Factory looked/uplooked
Secured Silicor		vvoru	703	89/09 (L)	Factory locked/unlocked
Secured Silicon	ı	Duto	X06	99/19 (H)	Factory locked/unlocked
		Byte	A00	89/09 (L)	Pactory locked/unlocked
Sector Protect Verify		Word	(Sector address) X 02	00/01	Unprotected/protected
Secioi Pioleci	verily	Byte	(Sector address) X 04	00/01	Unprotected/protected

After entering automatic select mode, no other commands are allowed except the reset command.



## **COMMAND OPERATIONS (cont'd)**

### **READ MANUFACTURER ID OR DEVICE ID**

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JE-DEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

After entering Automatic Select mode, performing a read operation with A1 & A0 held LOW will cause the device to output the Manufacturer ID on the Data I/O (Q7 to Q0) pins.

### **RESET**

In the following situations, executing reset command will reset device back to Read mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- · Auto-select mode
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in Auto-Select mode or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

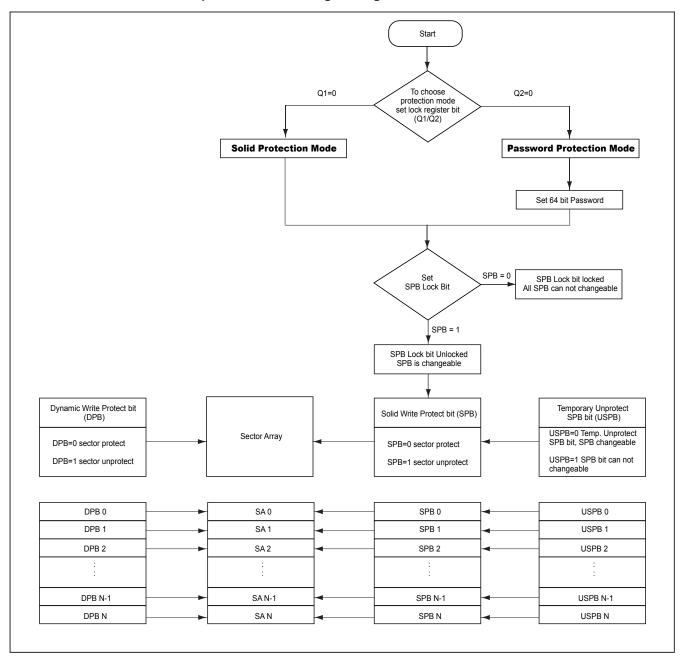


# Advanced Sector Protection/Un-protection

There are two ways to implement software Advanced Sector Protection on this device: Password method or Solid methods. Through these two protection method, user can disable or enable the programming or erasing operation to any individual sector or whole chip. The figure below helps describe an overview of these methods.

The device is default to the Solid mode and all sectors are unprotected when shipped from factory. Shows the detail algorithm of advance sector protecting.

### Advance Sector Protection/Unprotection SPB Program Algorithm:



### 1. Lock Register

User can choose favorite sector protecting method via setting Lock Register bits Q1 and Q2. Lock Register is a 16-bit one-time programmable register. Once programming either Q1 or Q2, they will be locked in that mode and the others will be disabled permanently. Q1 and Q2 can not be programmed at the same time, otherwise the device will abort the operation.

If user selects Password Protection mode, the password setting is required. User can set password by issuing password program command.

After the Lock Register Bits Command Set Entry command sequence is issued, the read and write operations for normal sectors are disabled until this mode exits.

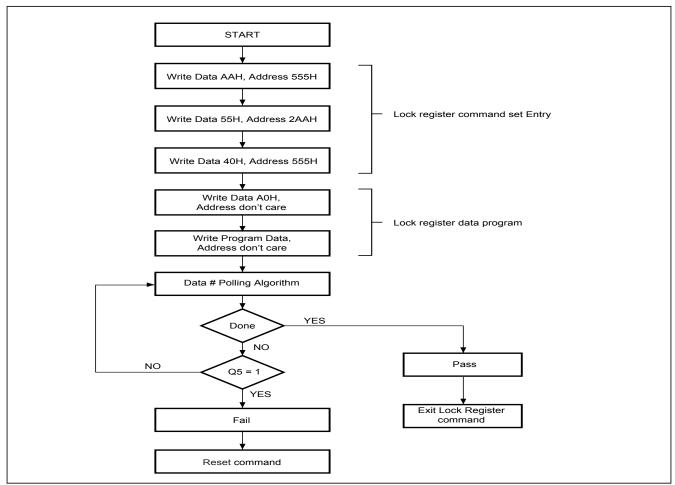
A Lock Register allows the memory sectors and extended memory sector protection to be configured.

### **Lock Register bits**

Q15-Q3	Q2	Q1	Q0
Don't care	Password Protection Mode	Solid Protection Mode	Secured Silicon Sector
Dont care	Lock Bit	Lock Bit	Protection Bit

Please refer to the command for Lock Register command set to read and program the Lock register.

## **Lock Register Program Algorithm:**





## 2. Solid write (non-volatile) protection Mode

## 2.1 Solid write Protection Bits (SPB)

The Solid write Protection bit (SPB) is a nonvolatile bit with the same endurances as the Flash memory. It is assigned to each sector individually. The SPB is Preprogramming, and its verification prior to erasure are managed by the device, so system monitoring is not necessary.

When a SPB is set to "0", the associated sector is protected, preventing any program or erase operation on this sector. The SPB bits are set individually by SPB program command. However, it cannot be cleared individually. Issuing the All SPB Erase command will erase all SPB in the same time. During SPB programming period, the read and write operations are disabled for normal sector until this mode exits.

If one of the protected sector need to be unprotected (corresponding SPB set to "1"), a few more steps are required. First, the SPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The SPBs can then be changed to reflect the desired settings. Setting the SPB Lock Bit once again locks the SPBs, and the device operates normally again.

To verify the programming state of the SPB for a given sector, issuing a SPB Status Read Command to the device is required. Refer to the flow chart below for details of SPB Program Algorithm.

### **Notes**

- 1. The Read actions within that sector will bring the SPB status back for that sector. All Read actions must be executed by read mode. The specific sector address is written as the program command at the same time.
- 2.Once SPB Lock Bit is set, its Program or erase command will not be executed and times-out without programming or erasing the SPB.
- 3. Always issue exit command after the execution of resetting the device to read mode and re-enables read and write actions for normal array.
- 4. To achieve the best effect of protection, it is recommended to execute the SPB Lock Bit Set command early in the boot code and protect the boot code by holding WP#/ACC = VIL. Note that the SPB and DPB bits have the same function when WP#/ACC = VHH, and it is same when ACC = VIH.

## 2.2 Dynamic Protection Bits (DPBS)

The Dynamic Protection allows the software application to easily protect sectors against inadvertent change. However, the protection can be easily disabled when changes are necessary.

All Dynamic Protection bit (DPB) are volatile and assigned to each sector. It can be modify individual. DPBs provide the protection scheme only for unprotected sectors that have their SPBs cleared (erase can be individually modified d to "1"). To modify the DPB status by issuing the DPB Set (programmed to "0") or DPB Clear (erased to "1") commands, then placing each sector in the protected or unprotected state seperately. After the DPB Clear command is issued(erased to "1"), the sector may be modified depending on the SPB state of that sector

When the parts are first shipped, the SPBs are cleared (erased to "1") and upon power up or reset, the DPBs can be set or cleared depending upon the ordering option chosen.





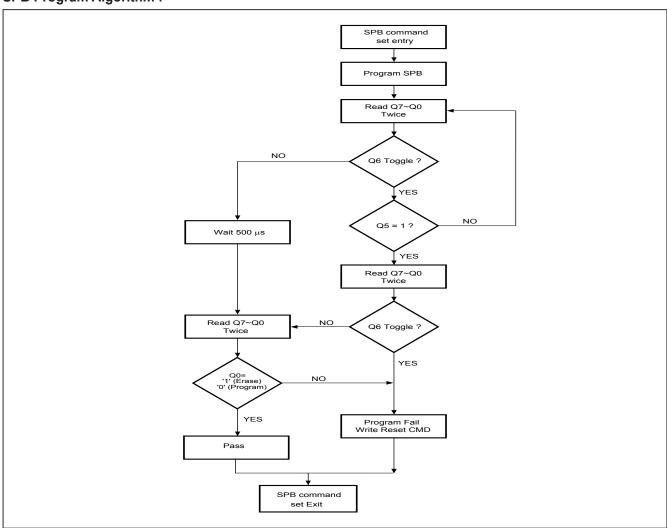
## 2.3 Temporary Un-protect Solid write protect bit (USPB)

Temporary Un-protect Solid write Protect Bits are volatile and unique for each sector and can be individually modified. By issuing the USPB Set or Clear command sequences, the USPBs are set (programmed to "0") or cleared (erased to "1"), thus mask each sector's solid write protect bit property. This feature allows software to temp unprotect write protect sectors despite of SPB's property when DPBs are cleared.

#### Notes:

- 1. The USPBs can be set (programmed to "0") or cleared (erased to "1") as often as needed. The USPBs are cleared (all 1s) upon power up. Hardware reset won"t change USPBs/DPBs status. The sectors SPBs would be in effective state after power up is chosen.
- 2. However, if there is a need to write a solid protect bit protect sector status, user don't have to clear all SPB bits. They just use software to set corresponding USPB to 0, which guarantees that corresponding DPB status is clear, and original solid protect bit protected sectors can be temporary written.
- 3. SPBLK should be cleared to modify USPB status.

## **SPB Program Algorithm:**



**Note:** SPB program/ erase status polling flowchart: check Q6 toggle, when Q6 stop toggle, the read status is 00H /01H (00H for program/ 01H for erase), otherwise the status is "fail" and "exit".



#### 3. Solid Protection Bit Lock Bit

The Solid Protection Bit Lock Bit (SPB) is assign to control all SPB status. It is a unique and volatile. When SPB=0 (set), all SPBs are locked and can not be changed. When SPB=1 (cleared), all SPBs are unlock and allows to be changed.

There is no software command sequence requested to unlocks this bit, unless the device is in the password protection mode. To clear the SPB lock bit, just take the device through a hardware reset or a power-up cycle. In order to prevent moified, the SPB Lock Bit must be set (SPB=0) after all SPBs are setting the desired status.

#### 4. Password Protection Method

The security level of Password Protection Method is higher then the Solid protection mode. The 64 bit password is requested before modify SPB lock bit status. When device is under password protection mode, the SPB lock bit is set "0", after a power-up cycle or Reset Command.

A correct password is required for password Unlock command, to unlock the SPB lock bit. Await 2us is necessary to unlocked the device after valid password is given. After that, the SPB bits are allows to be changed. The Password Unlock command are issued slower then 2  $\mu$ s every time, to prevent hacker from trying all the 64-bit password combinations.

To place the device in password protection mode, a few more steps are required. First, prior to entering the password protection mode, it is necessary to set a 64-bit password to verify it. Password verification is only allowed during the password programming operation. Second, the password protection mode is then activated by programming the password the Password Protection Mode Lock Bit to"0". This operation is not reversible. Once the bit is programmed, it cannot be erased, and the device remains permanently in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored are disabled.

The password is all "1"s when shipped from the factory, it is only capable to programming "0"s under password program command. All 64-bit password combinations are valid as a password. No special address is required for programming the password. In order to prevent access, the Password Mode Locking Bit must be set after the Password is programmed and verified. Once the Password Mode Lock Bit is set, prevents reading 64-bits password on the data bus and any future modification. There is no means to verify what the password is after it is set.

Entry command sequence will cause the read and write operation to be disabled for normal sector until this mode exits. Once sector under protected status, device will ignores the program/erase command, enable status polling and returns to read mode without contents change. The DPB, SPB,USPB and SPB lock bit status of each sector can be verified by issue status read commands.



# **Sector Protection Status Table**

F	Protection	Bit Statu	S	Sector Status
DPB	SPBLK	SPB	USPB	Sector Status
clear	clear	clear	clear	unprotect, DPB/SPB/USPB are changeable
clear	clear	clear	set	unprotect, DPB/SPB/USPB are changeable
clear	clear	set	clear	protect, DPB/SPB/USPB are changeable
clear	clear	set	set	unprotect, DPB/SPB/USPB are changeable
clear	set	clear	clear	unprotect, DPB/USPB are changeable
clear	set	clear	set	unprotect, DPB/USPB are changeable
clear	set	set	clear	protect, DPB/USPB are changeable
clear	set	set	set	unprotect, DPB/USPB are changeable
set	clear	clear	clear	protect, DPB/SPB/USPB are changeable
set	clear	clear	set	protect, DPB/SPB/USPB are changeable
set	clear	set	clear	protect, DPB/SPB/USPB are changeable
set	clear	set	set	protect, DPB/SPB/USPB are changeable
set	set	clear	clear	protect, DPB/USPB are changeable
set	set	clear	set	protect, DPB/USPB are changeable
set	set	set	clear	protect, DPB/USPB are changeable
set	set	set	set	protect, DPB/USPB are changeable



#### SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra OTP memory space of 128 words in length. The security sector can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

### Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the Security Sector is permanently locked before shipping from the factory. The device will have a 16-byte (8-word) ESN in the security region. The ESN occupies addresses 000000h to 00000Fh in byte mode or 000000h to 000007h in word mode.

Secured Silicon Sector Address Range	Standard Factory Locked	Express Flash Factory Locked	Customer Lockable
000000h-000007h	ESN	ESN or Determined by Customer	Determined by Customer
000008h-00007Fh	Unavailable	Determined by Customer	_

## **Customer Lockable: Security Sector NOT Programmed or Protected at the Factory**

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.



# **TABLE 3. COMMAND DEFINITIONS**

							Αι	itomatic Se	lect			Secu	ırity	Exit Security	
Comm- and		Read Mode	Reset Mode	I Silicon II) I Device II) I		Factory P		Sector Pro	Sector Protect Verify			Sector			
				Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
Cycle	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus	Addr			2AA	555	2AA	555	2AA	555	2AA	555	2AA	555	2AA	555
Cycle	Data			55	55	55	55	55	55	55	55	55	55	55	55
3rd Bus	Addr			555	AAA	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
Cycle	Data			90	90	90	90	90	90	90	90	88	88	90	90
4th Bus	Addr			X00	X00	X01	X02	X03	X06	(Sector) X02	(Sector) X04			XXX	XXX
Cycle	Data			C2h	C2h	ID1	ID1	99/19(H) 89/09(L)		00/01	00/01			00	00
5th Bus	Addr					X0E	X1C								
Cycle	Data					ID2	ID2								
6th Bus	Addr					X0F	X1E								
Cycle	Data					ID3	ID3								

Comm- and		Prog	ıram	Writ But Prog	ffer	Writ But Prog Abort	ffer Iram	Writ But Prog con	fer ram	Chip E	Erase	Sec Era		CFI F	Read	Prog Era Susp	ise	Prog Era Res	ase
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus	Addr	555	AAA	555	AAA	555	AAA	SA	SA	555	AAA	555	AAA	55	AA	XXX	XXX	XXX	XXX
Cycle	Data	AA	AA	AA	AA	AA	AA	29	29	AA	AA	AA	AA	98	98	B0	В0	30	30
2nd Bus	Addr	2AA	555	2AA	555	2AA	555			2AA	555	2AA	555						
Cycle	Data	55	55	55	55	55	55			55	55	55	55						
3rd Bus	Addr	555	AAA	SA	SA	555	AAA			555	AAA	555	AAA						
Cycle	Data	A0	A0	25	25	F0	F0			80	80	80	80						
4th Bus	Addr	Addr	Addr	SA	SA					555	AAA	555	AAA						
Cycle	Data	Data	Data	N-1	N-1					AA	AA	AA	AA						
5th Bus	Addr			WA	WA					2AA	555	2AA	555						
Cycle	Data			WD	WD					55	55	55	55						
6th Bus	Addr			WBL	WBL					555	AAA	Sec- tor	Sec- tor						
Cycle	Data			WD	WD					10	10	30	30						

WA= Write Address

WD= Write Data

SA= Sector Address

N-1= Word Count

WBL= Write Buffer Location

PWD= Password

PWDn=Password word 0, word 1, word n ID1/ID2/ID3: Refer to *Table 2-2* for detail ID.



		D	eep Po	wer Dow	/n				Pa	ssword	Protecti	ion			
Comma	and	En	Enter Exit		Comma	Password Command Set Entry		Password Program		word		word ock		word and Set kit	
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus	Addr	555	AAA	XXX	XXX	555	AAA	XXX	XXX	X00	X00	00	00	XXX	XXX
Cycle	Data	AA	AA	AB	AB	AA	AA	A0	A0	PWD0	PWD0	25	25	90	90
2nd Bus	Addr	2AA	555			2AA	555	PWA	PWA	X01	X01	00	00	XXX	XXX
Cycle	Data	55	55			55	55	PWD	PWD	PWD1	PWD1	03	03	00	00
3rd Bus	Addr	XXX	XXX			555	AAA			X02	X02	X00	X00		
Cycle	Data	B9	B9			60	60			PWD2	PWD2	PWD0	PWD0		
4th Bus	Addr									X03	X03	X01	X01		
Cycle	Data									PWD3	PWD3	PWD1	PWD1		
5th Bus	Addr										X04	X02	X02		
Cycle	Data					İ					PWD4	PWD2	PWD2		
6th Bus	Addr					Ì					X05	X03	X03		
Cycle	Data										PWD5	PWD3	PWD3		
7th Bus	Addr										X06	00	X04		
Cycle	Data										PWD6	29	PWD4		
8th Bus	Addr										X07		X05		
Cycle	Data										PWD7		PWD5		
9th Bus	Addr												X06		
Cycle	Data												PWD6		
10th Bus	Addr												X07		
Cycle	Data												PWD7		
11th Bus	Addr												00		
Cycle	Data												29		



			Lock Register							Global Non-Volatile							
Comm	and	Lock register Command Set Entry		Prog	ıram	Read		Lock re Comi Set		SF Comr Set E	mand	SPB Program		All SPB Erase		SPB Status Read	
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus	Addr	555	AAA	XXX	XXX	XXX	XXX	XXX	XXX	555	AAA	XXX	XXX	XXX	XXX	SA	SA
Cycle	Data	AA	AA	A0	A0	DATA	DATA	90	90	AA	AA	A0	A0	80	80	00/01	00/01
2nd Bus	Addr	2AA	555	XXX	XXX			XXX	XXX	2AA	555	SA	SA	00	00		
Cycle	Data	55	55	Data	Data			00	00	55	55	00	00	30	30		
3rd Bus	Addr	555	AAA							555	AAA						
Cycle	Data	40	40							C0	C0						
4th Bus	Addr																
Cycle	Data																
5th Bus	Addr																
Cycle	Data																

		Globa Vola			Global Volatile Freeze							Volatile					
Comma	and	SPB Command Set Exit		SPB Comr Set B		SPB Lock Set		SPB Status		SPB Comr Set	mand	and Command DPB Set		DPB Clear			
1et Rue		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus	Addr	XXX	XXX	555	AAA	XXX	XXX	XXX	XXX	XXX	XXX	555	AAA	XXX	XXX	XXX	XXX
Cycle	Data	90	90	AA	AA	A0	A0	00/01	00/01	90	90	AA	AA	A0	A0	A0	A0
2nd Bus	Addr	XXX	XXX	2AA	555	XXX	XXX			XXX	XXX	2AA	555	SA	SA	SA	SA
Cycle	Data	00	00	55	55	00	00			00	00	55	55	00	00	01	01
3rd Bus	Addr			555	AAA							555	AAA				
Cycle	Data			50	50							E0	E0				
4th Bus	Addr																
Cycle	Data																
5th Bus	Addr																
Cycle	Data																

		Volatile						
Comma	and	DPB \$	Status	DPB Command				
		Re	ad	Set I	Exit			
		Word	Byte	Word	Byte			
1st Bus	Addr	SA	SA	XXX	XXX			
Cycle	Data	00/01	00/01	90	90			
2nd Bus	Addr			XXX	XXX			
Cycle	Data			00	00			
3rd Bus	Addr							
Cycle	Data							
4th Bus	Addr							
Cycle	Data							
5th Bus	Addr							
Cycle	Data							

<sup>\*</sup> It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.

<sup>\*</sup> For the SPB Lock and DPB Status Read "00" means lock (protect), "01" means unlock (unprotect).

### COMMON FLASH MEMORY INTERFACE (CFI) MODE

#### QUERY COMMAND AND COMMAND FLASH MEMORY INTERFACE (CFI) MODE

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in *Table 4*.

Once user enters CFI query mode, user can issue reset command to exit CFI mode and return to read array mode. The unused CFI area is reserved by Macronix.

Table 4-1. CFI mode: Identification Data Values

(All values in these tables are in hexadecimal)

Description	Address (h)	Address (h)	Data (b)
Description	(Word Mode)	(Byte Mode)	Data (II)
	10	20	0051
Query-unique ASCII string "QRY"	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
Filmary veridor command set and control interface iD code	14	28	0000
Address for primary algorithm extended query table	(Word Mode)         (Byte Mode)         Data (           10         20         005           11         22         0052           12         24         0059           13         26         0002           14         28         0000           15         2A         0040           16         2C         0000           20de         17         2E         0000           18         30         0000           19         32         0000	0040	
Address for primary algorithm extended query table	16	2C	0000
Alternate vendor command set and control interface ID code	17	2E	0000
Alternate vendor command set and control interface in code	18	30	0000
Address for alternate algorithm extended guery table	19	32	0000
Address for alternate algorithm extended query table	1A	34	0000

Table 4-2. CFI mode: System Interface Data Values

Description	Address (h)	Address (h)	Doto (b)
Description	(Word Mode)	(Byte Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	36	0027
Vcc supply maximum program/erase voltage	1C	38	0036
VPP supply minimum program/erase voltage	1D	3A	0000
VPP supply maximum program/erase voltage	1E	3C	0000
Typical timeout per single word/byte write, 2 <sup>n</sup> us	1F	3E	0003
Typical timeout for maximum-size buffer write, 2 <sup>n</sup> us (00h, not	20	40	0006
support)	20	40	0000
Typical timeout per individual block erase, 2 <sup>n</sup> ms	21	42	0009
Typical timeout for full chip erase, 2 <sup>n</sup> ms (00h, not support)	22	44	0013
Maximum timeout for word/byte write, 2 <sup>n</sup> times typical	23	46	0003
Maximum timeout for buffer write, 2 <sup>n</sup> times typical	24	48	0005
Maximum timeout per individual block erase, 2 <sup>n</sup> times typical	25	4A	0003
Maximum timeout for chip erase, 2 <sup>n</sup> times typical (00h, not	26	40	0002
support)	26	4C	0002



Table 4-3. CFI mode: Device Geometry Data Values

Description	Address (h)	Address (h)	Data (h)
Description	(Word Mode)	(Byte Mode)	Data (h)
Device size = 2 <sup>n</sup> in number of bytes	27	4E	0019
Flash device interface description (02=asynchronous x8/x16)  Maximum number of bytes in buffer write = 2 <sup>n</sup> (00h, not suppor	28	50	0002
riash device interface description (02=asynchronous x8/x16)	29	52	0000
Maximum number of bytes in buffer write = 2° (00b, not support)	2A	54	0006
IMAXIII III II III III II II II II II II II	(Word Mode)         (Byte Mode)           27         4E           28         50           29         52           2Δ         54	0000	
Number of erase regions within device (01h:uniform, 02h:boot)	2C	58	0001
	2D	5A	00FF
	2E	5C	0000
	(Word Mode)  27  28  29  Oh, not support)  2B  form, 02h:boot)  2C  2D  2E  2F  30  31  32  33  34  35  36  37  38  39  3A  3B	5E	0000
[00, 21] - Sector Size in multiples of 2001 bytes	30	60	0002
	31 62 0000	0000	
Index for Free Ponk Area 2	32	64	0000
Index for Erase Bank Area 2	33	66	0000
	34	68	0000
	35	6A	0000
Index for Free Ponk Area 2	36	6C	0000
Index for Erase Bank Area 3	37	6E	0000
	38	70	0000
	39	72	0000
Index for Erose Donk Area 4	3A	74	0000
Index for Erase Bank Area 4	3B	76	0000
	3C	78	0000



Table 4-4. CFI mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h)	Address (h)	Data (h)
Description	(Word Mode)	(Byte Mode)	Data (II)
	40	80	0050
Query - Primary extended table, unique ASCII string, PRI	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0033
Unlock recognizes address (0= recognize, 1= don't recognize)	45	8A	0014
Erase suspend (2= to both read and program)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0001
Temporary sector unprotect (1=supported)	48	90	0000
Sector protect/Chip unprotect scheme	49	92	8000
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode (0=not supported)	4B	96	0000
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	4C	98	0002
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	9A	0095
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	9C	00A5
WP# Protection 04=Uniform sectors bottom WP# protect 05=Uniform sectors top WP# protect	4F	9E	0004/ 0005
Program Suspend (0=not supported, 1=supported)	50	A0	0001

#### **ELECTRICAL CHARACTERISTICS**

#### **ABSOLUTE MAXIMUM STRESS RATINGS**

Surrounding Temperature with B	ias	-65°C to +125°C
Storage Temperature		-65°C to +150°C
Mallana Danas	VCC	-0.5V to +4.0 V
	VI/O	-0.5V to +4.0 V
Voltage Range	A9 , WP#/ACC	-0.5V to +10.5 V
	The other pins.	-0.5V to Vcc +0.5V
Output Short Circuit Current (les	Output Short Circuit Current (less than one second)	

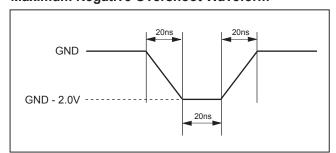
#### **OPERATING TEMPERATURE AND VOLTAGE**

Industrial (I) Grade	Surrounding Temperature (TA)	-40°C to +85°C
	Full VCC range	+2.7 V to 3.6 V
VCC Supply Voltages	Regulated VCC range	+3.0 V to 3.6 V
	VI/O range	1.65V to VCC

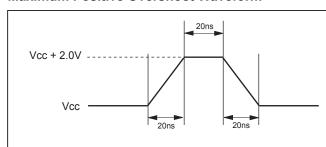
#### NOTICE:

- 1. Stresses greater than those listed under *ABSOLUTE MAXIMUM RATINGS* may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
- 2. Specifications contained within the following tables are subject to change.
- 3. During voltage transitions, all pins may overshoot GND to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figures below.

#### **Maximum Negative Overshoot Waveform**



#### **Maximum Positive Overshoot Waveform**





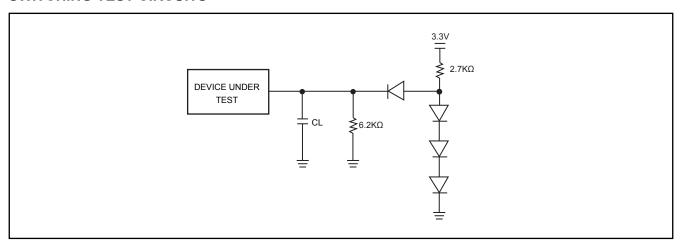
#### **DC CHARACTERISTICS**

Symbol	Description	Min	Тур	Max	Remark
lilk	Input Leak			±2.0uA	
lilk9	A9 Leak			35uA	A9=10.5V
lolk	Output Leak			±1.0uA	
			6mA	20mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=1MHz, Byte Mode
lcr1	Read Current		30mA	50mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=5MHz, Byte Mode
			60mA	100mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=10MHz
lcr2	VCC Page Read Current		2mA	10mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=10MHz
ICIZ	VCC Fage Read Current		5mA	20mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=33MHz
lio	V <sub>IO</sub> non-active current		0.2mA	10mA	
Icw	Write Current		26mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		30uA	100uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		30uA	100uA	Vcc=Vccmax, RESET# enable, other pin disable
Isbs	Sleep Mode Current		30uA	100uA	
ldpd	Vcc deep power down current		10uA		
Icp1	Accelerated Pgm Current, WP#/Acc pin(Word/Byte)		5mA	10mA	CE#=Vil, OE#=Vih
lcp2	Accelerated Pgm Current, Vcc pin, (Word/Byte)		20mA	30mA	CE#=Vil, OE#=Vih
Vil	Input Low Voltage	-0.1V		0.3xVI/O	
Vih	Input High Voltage	0.7xVI/O		VI/O+0.3V	
Vhv	Very High Voltage for Auto Select/ Accelerated Program	9.5V		10.5V	
Vol	Output Low Voltage			0.45V	lol=100uA
Voh	Ouput High Voltage	0.85xVI/O			loh=-100uA
Vlko	Low Vcc Lock-out voltage	2.3V		2.5V	

**Note:** Sleep mode enables the lower power when address remain stable for taa+30ns.



#### **SWITCHING TEST CIRCUITS**



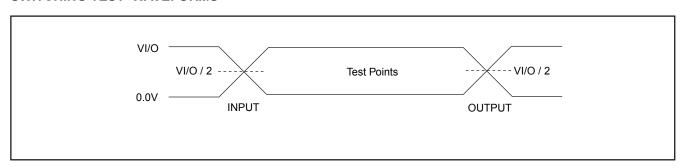
**Test Condition** 

Output Load Capacitance, CL: 1TTL gate, 30pF

Rise/Fall Times: 5ns

Input Pulse levels :0.0 ~ VI/O In/Out reference levels :0.5VI/O

#### **SWITCHING TEST WAVEFORMS**





### **AC CHARACTERISTICS**

Symbol	Description			9GL250 =2.7V			9GL250 =3.0V~		Unit
<b>Cy</b>			Min.	Тур.	Max.	Min.	Тур.	Max.	
Taa	Valid data output after address	VI/O=VCC			100			90	ns
Ida	Valid data output after address	VI/O=1.65 toVCC			110			110	ns
Tna	Page access time	VI/O=VCC			25			25	ns
Тра	rage access time	VI/O=1.65 toVCC			30			30	ns
Tce	Valid data output after CE# low	VI/O=VCC			100			90	ns
ice	Valid data output after CE# low	VI/O=1.65 toVCC			110			110	ns
Toe	Valid data output after OE# low	VI/O=VCC			25			25	ns
	valid data output after OL# low	VI/O=1.65 toVCC			30			30	ns
Tdf	Data output floating after OE# hi	<u> </u>			20			20	ns
Tsrw	Latency between read and write		35			35			ns
Toh	Output hold time from the earl address, CE#, OE#	liest rising edge of	0			0			ns
Trc	Read period time		100			90			ns
Twc	Write period time		100			90			ns
Tcwc	Command write period time					90			ns
Tas	Address setup time		0			0			ns
Taso	Address setup time to OE# low during toggle bit polling					15			ns
Tah	Address hold time					45			ns
Taht	Address hold time from CE# or OE# high during toggle bit polling		0			0			ns
Tds	Data setup time		30			30			ns
Tdh	Data hold time		0			0			ns
Tvcs	Vcc setup time		500			500			us
Tcs	Chip enable Setup time		0			0			ns
Tch	Chip enable hold time		0			0			ns
Toes	Output enable setup time		0			0			ns
		Read	0			0			ns
Toeh	Output enable hold time	Toggle & Data# Polling	10			10			ns
Tws	WE# setup time		0			0			ns
Twh	WE# hold time		0			0			ns
Tcepw	CE# pulse width	,	35			35			ns
Tcepwh	· ·	,	30			30			ns
Twp	WE# pulse width		35			35			ns
Twph	WE# pulse width high	,	30			30			ns
Tbusy	Program/Erase active time by RY/BY#	VI/O=VCC			100			90	ns
Tailered		VI/O=1.65 toVCC			110			110	ns
Tghwl	Read recover time before write		0	-		0			ns
Tghel	Read recover time before write		0			0			ns



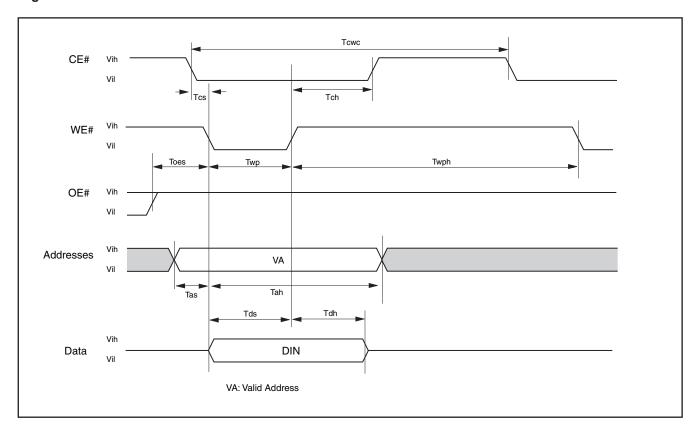
Symbol	Description			29GL256E (VCC=2.7V~3.6V)			9GL256 =3.0V~		Unit
	•		Min.	Тур.	Max.	Min.	Тур.	Max.	
Twhwh1	Program operation	Byte		11			11		us
Twhwh1	Program operation	Word		11			11		us
Twhwh1	Acc program operation (Word/By	te)		11			11		us
Twhwh2	Sector erase operation			0.6	5		0.6	5	sec
Tbal	Sector add hold time				50			50	us
Trdp	Release from deep power down	mode			200			200	us

Note: Not 100% tested.





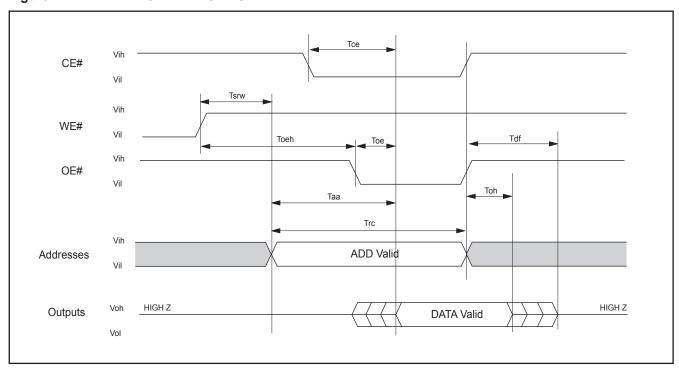
Figure 1. COMMAND WRITE OPERATION





#### **READ/RESET OPERATION**

Figure 2. READ TIMING WAVEFORMS

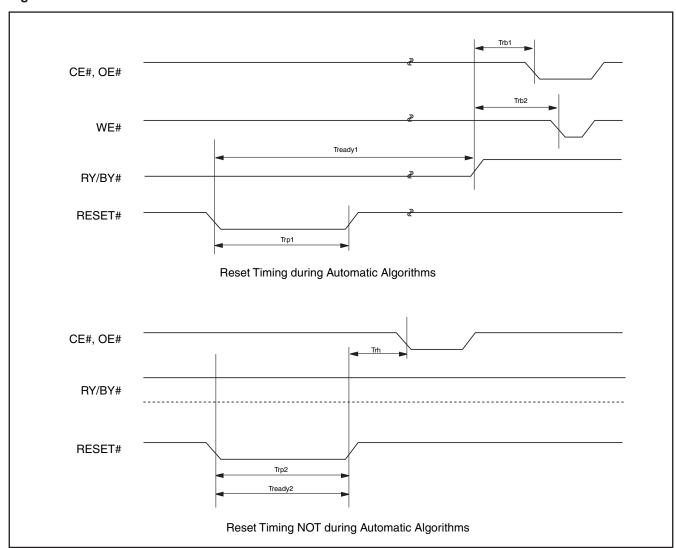




#### **AC CHARACTERISTICS**

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	200	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM







#### **ERASE/PROGRAM OPERATION**

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

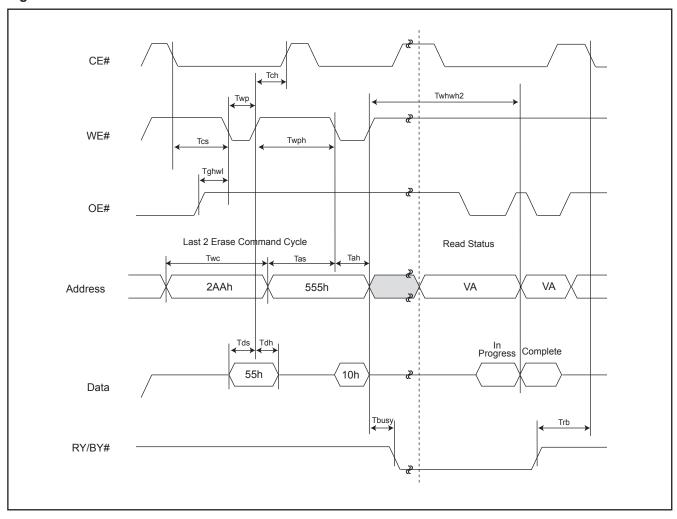




Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

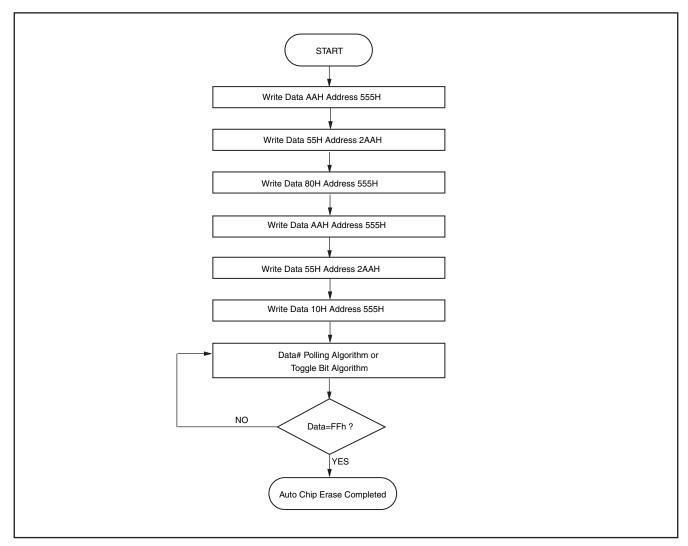




Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

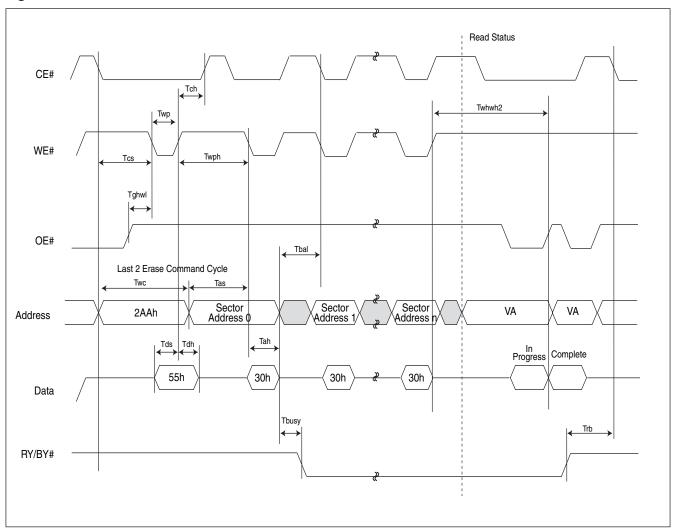




Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

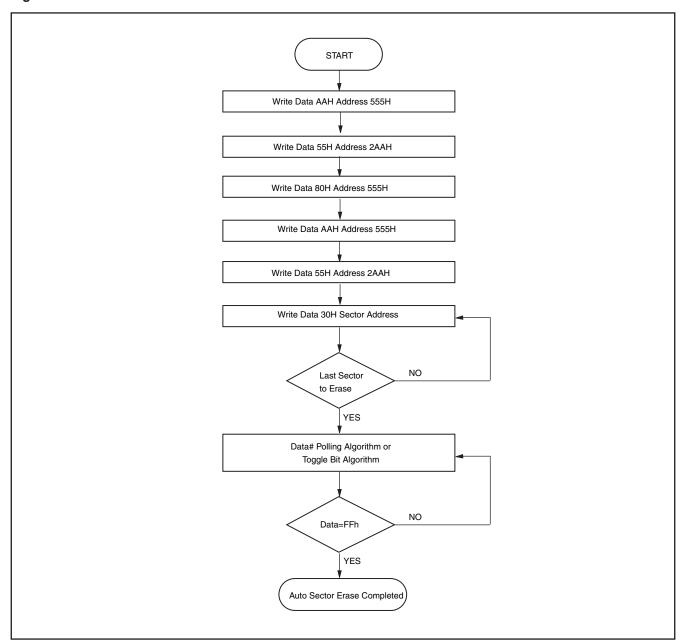






Figure 8. ERASE SUSPEND/RESUME FLOWCHART

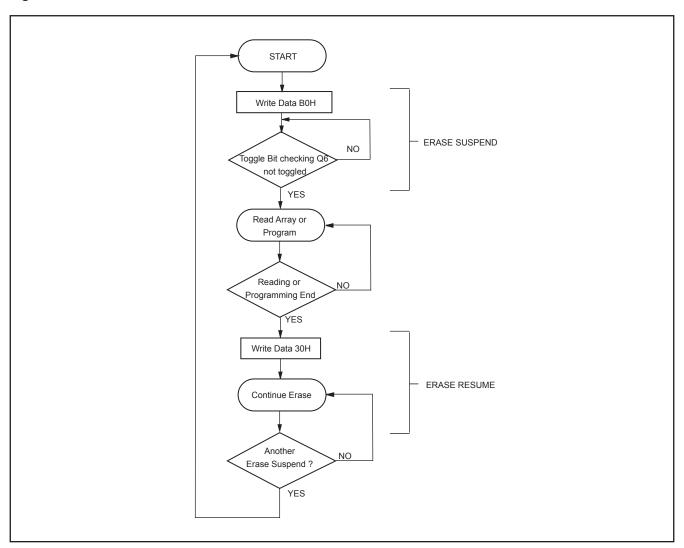




Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

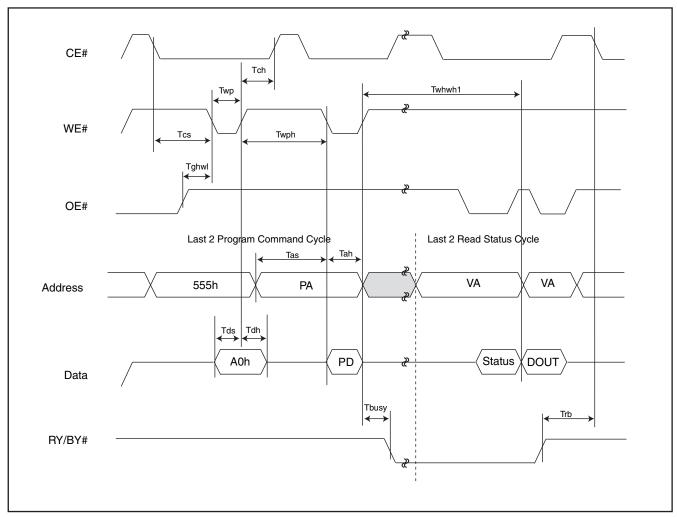


Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM

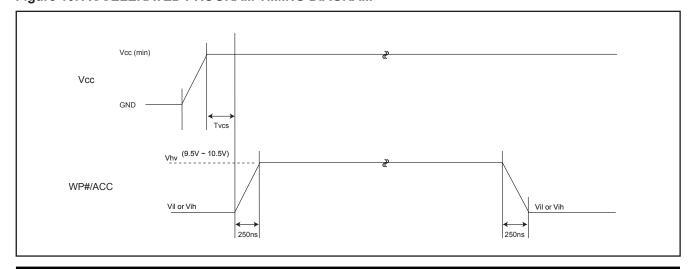
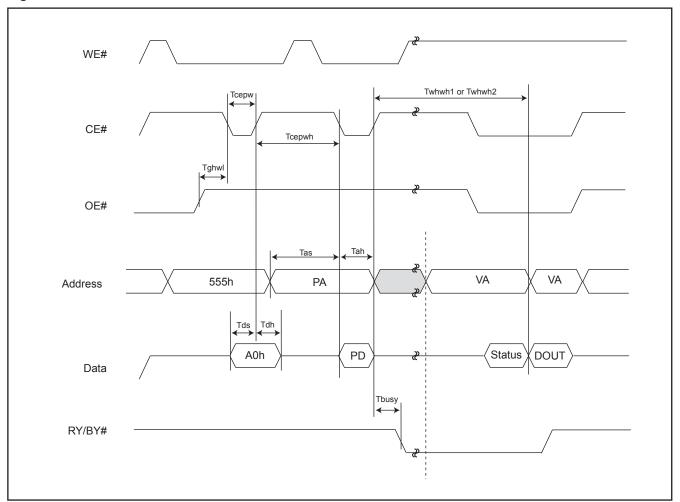






Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM



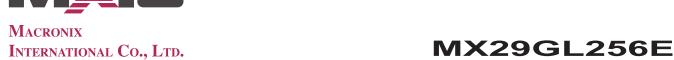


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

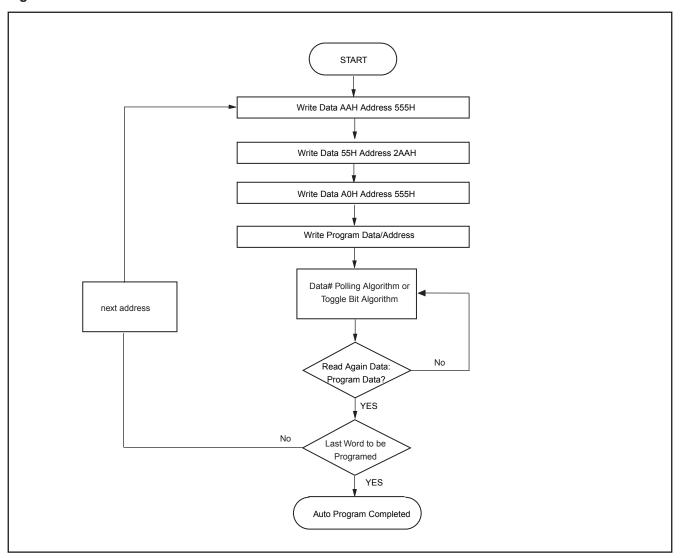
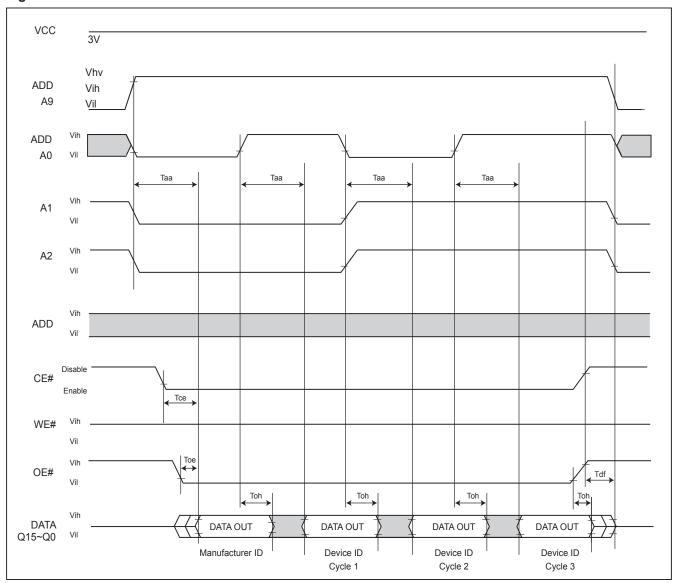




Figure 13. SILICON ID READ TIMING WAVEFORM

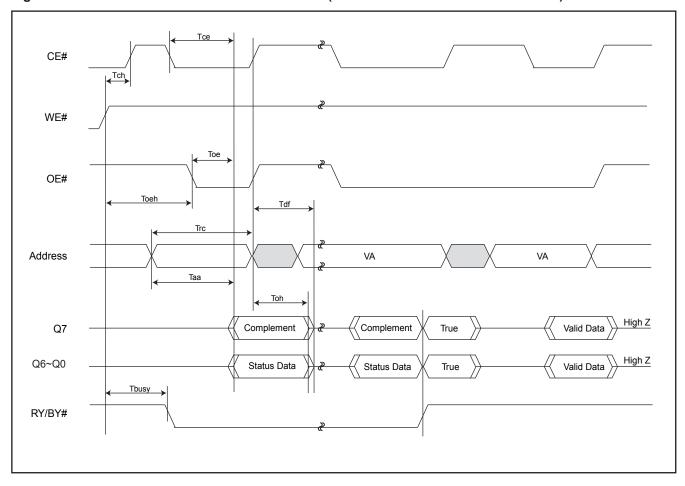






#### **WRITE OPERATION STATUS**

Figure 14. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

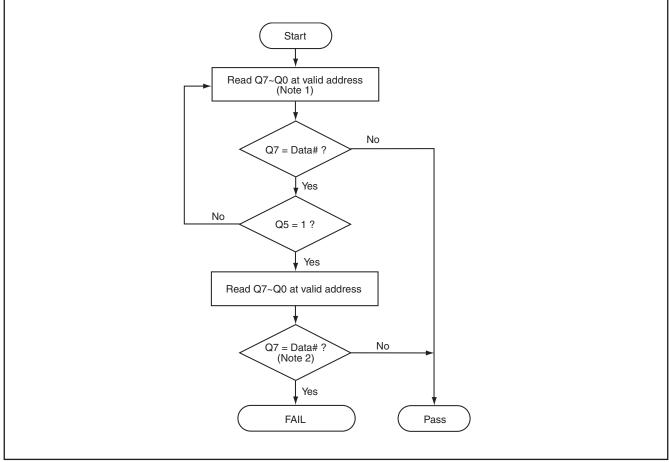




**M**ACRONIX **MX29GL256E** INTERNATIONAL Co., LTD.

Start

Figure 15. STATUS POLLING FOR WORD PROGRAM/ERASE



- 1. For programming, valid address means program address. For erasing, valid address means erase sectors address.
- 2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.



Start Read Q7~Q0 at last write address (Note 1) No Q7 = Data# ? Yes Q1=1 ? Only for write buffer program Yes No No Q5=1? Read Q7~Q0 at last write address (Note 1) Yes Read Q7~Q0 at last write address (Note 1) No Q7 = Data#? (Note 2) Q7 = Data# ? (Note 2) No Yes Write Buffer Abort Yes Pass **FAIL** 

Figure 16. STATUS POLLING FOR WRITE BUFFER PROGRAM

- 1. For programming, valid address means program address. For erasing, valid address means erase sectors address.
- 2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.





Figure 17. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

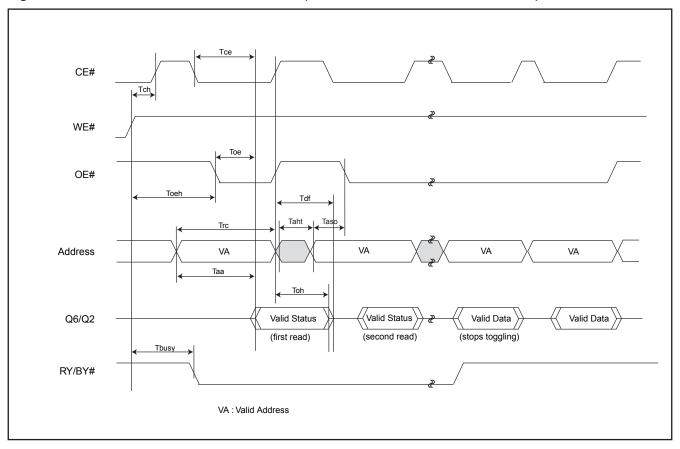
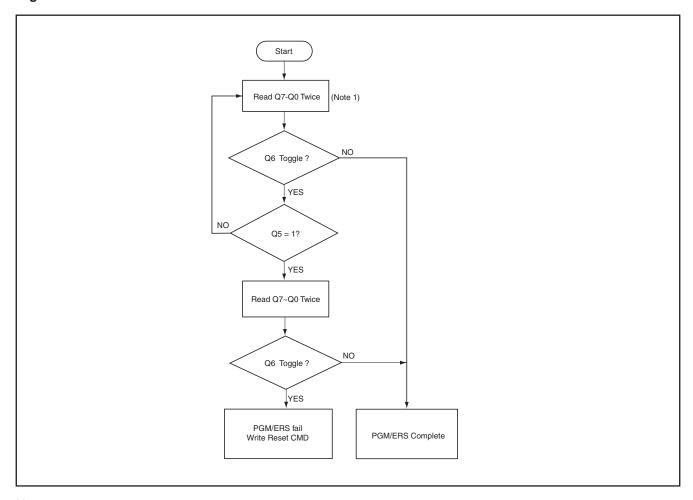




Figure 18. TOGGLE BIT ALGORITHM



- 1. Read toggle bit twice to determine whether or not it is toggling.
- 2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".



#### **AC CHARACTERISTICS**

#### WORD/BYTE CONFIGURATION (BYTE#)

Parameter	Description	Test Setup	All Speed Options	Unit
Telfl/Telfh	CE# to BYTE# from L/H	Max.	5	ns
Tflqz	BYTE# from L to Output Hiz	Max.	30	ns
Tfhqv	BYTE# from H to Output Active	Min.	90	ns

Figure 19. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)

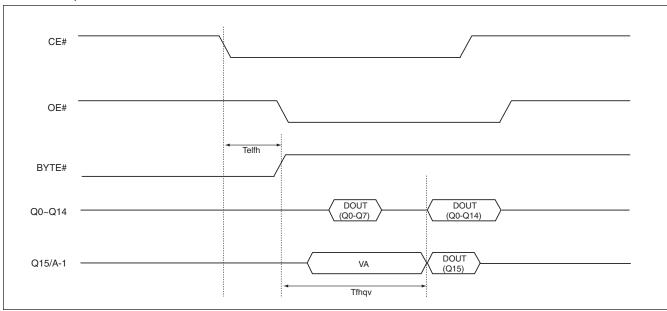
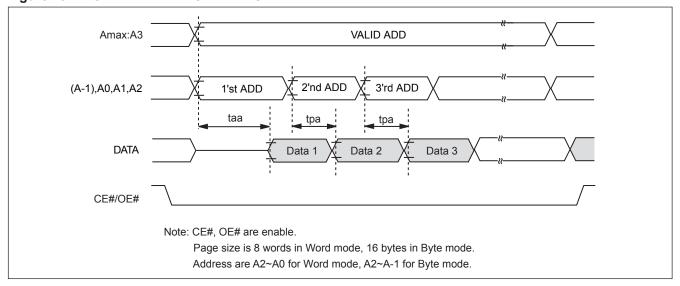


Figure 20. PAGE READ TIMING WAVEFORM





#### **AC CHARACTERISTICS**

ITEM		TYP	MAX
WEB high to release from deep power down mode	tRDP	100us	200us
WEB high to deep power down mode	tDP	10us	20us

Figure 21. DEEP POWER DOWN MODE WAVEFORM

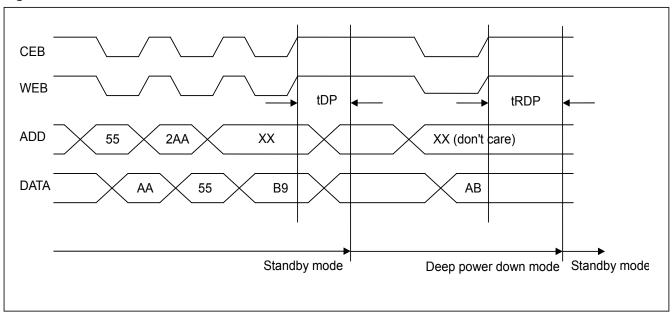
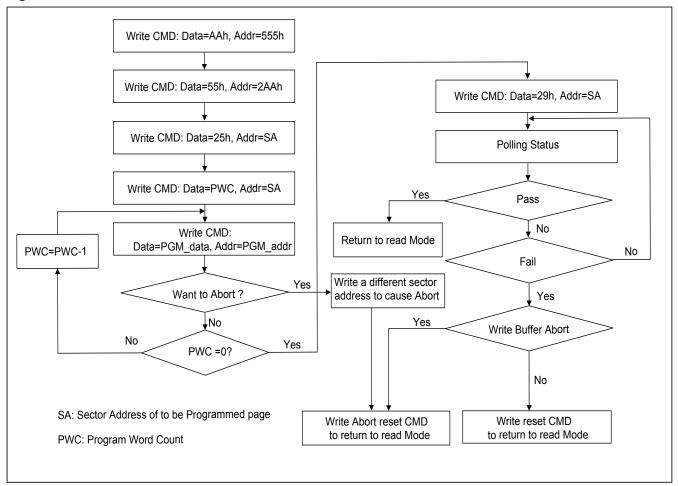




Figure 22. WRITE BUFFER PROGRAM FLOWCHART





#### **RECOMMENDED OPERATING CONDITIONS**

#### At Device Power-Up

AC timing illustrated in *Figure A* is recommended for the supply voltages and the control signals at device power-up (e.g. Vcc and CE# ramp up simultaneously). If the timing in the figure is ignored, the device may not operate correctly.

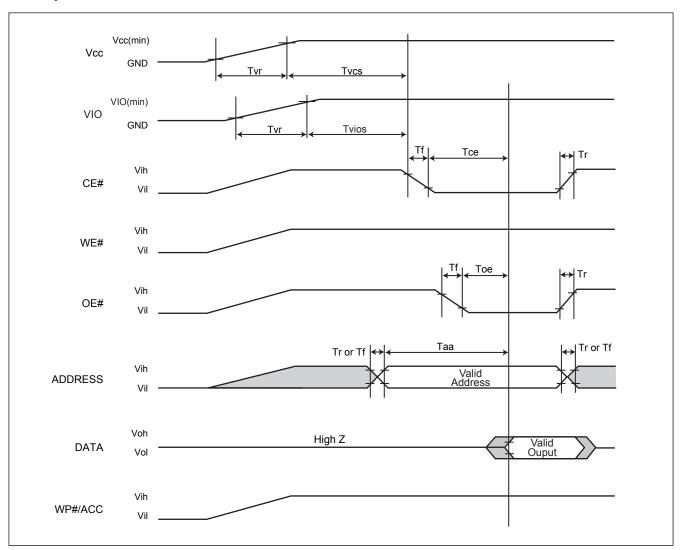


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V
Tvcs	Vcc Setup Time	500		us
Tvios	VIO Setup Time	500		us

- 1. Not test 100%.
- 2. VIO<VCC+200mV.



#### **ERASE AND PROGRAMMING PERFORMANCE**

PARAMETER		LIMITS		UNITS	
PARAIVIETER	MIN.	TYP. (1)	MAX. (2)	UNITS	
Chip Erase Time		128	300	sec	
Sector Erase Time		0.6	5	sec	
Chip Programming Time		100	350	sec	
Word Program Time		11	360	us	
Total Write Buffer Time		200		us	
ACC Total Write Buffer Time		100		us	
Erase/Program Cycles		100,000		Cycles	

#### Notes:

- 1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
- 2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
- 3. Erase/Program cycles comply with JEDEC JESD-47 & 22-A117 standard.
- 4. Exclude 00h program before erase operation.

#### **DATA RETENTION**

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55°C	20		years

#### **LATCH-UP CHARACTERISTICS**

	MIN.	MAX.
Input Voltage voltage difference with GND on WP#/ACC and A9 pins	-1.0V	10.5V
Input Voltage voltage difference with GND on all normal pins input	-1.0V	1.5Vcc
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing	•	

#### **PIN CAPACITANCE**

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	17	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF



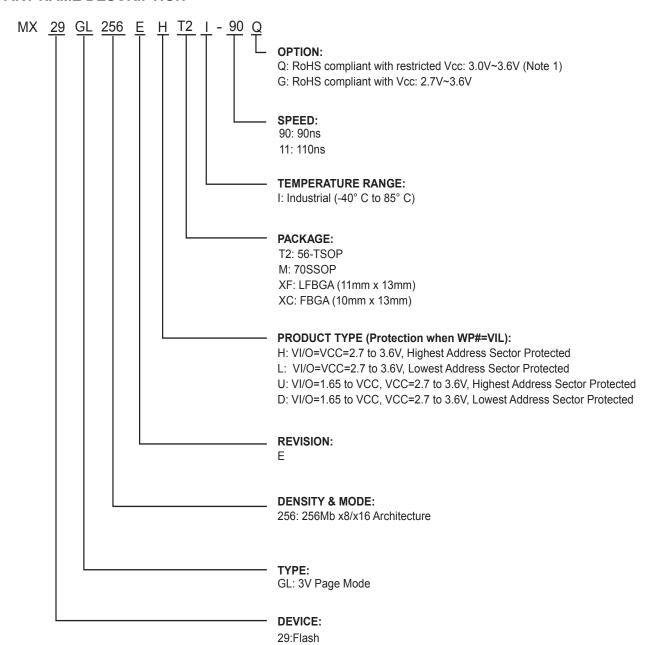
#### **ORDERING INFORMATION**

PART NO.	ACCESS TIME (ns)	PACKAGE	Remark
MX29GL256EHMC-90Q *	90	70 Pin SSOP	VI/O=VCC
MX29GL256EHXFI-90Q	90	64 LFBGA	VI/O=VCC
MX29GL256ELXFI-90Q	90	64 LFBGA	VI/O=VCC
MX29GL256EHXCI-90Q	90	64 FBGA	VI/O=VCC
MX29GL256ELXCI-90Q	90	64 FBGA	VI/O=VCC
MX29GL256EHT2I-90Q	90	56 Pin TSOP	VI/O=VCC
MX29GL256ELT2I-90Q	90	56 Pin TSOP	VI/O=VCC
MX29GL256EUXFI-11G	110	64 LFBGA	VI/O=1.65 to VCC
MX29GL256EDXFI-11G	110	64 LFBGA	VI/O=1.65 to VCC
MX29GL256EUT2I-11G	110	56 Pin TSOP	VI/O=1.65 to VCC
MX29GL256EDT2I-11G	110	56 Pin TSOP	VI/O=1.65 to VCC

<sup>\* 70-</sup>pin SSOP only for Pachinko Socket.



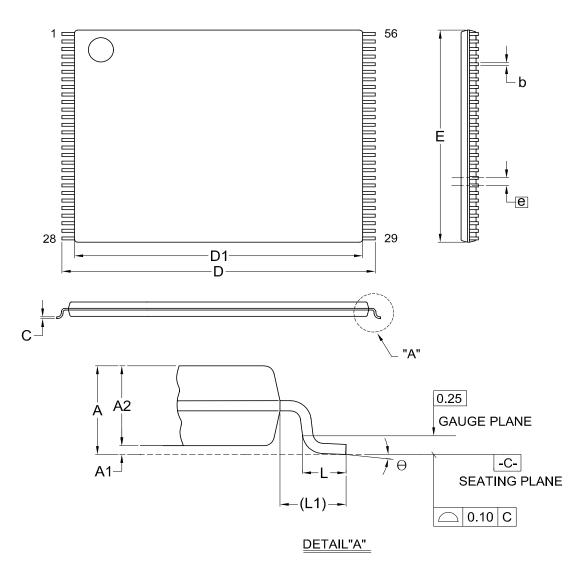
#### PART NAME DESCRIPTION



Note 1: 90Q covers 2.7V~3.6V for 100ns and 3.0V~3.6V for 90ns

#### **PACKAGE INFORMATION**

Doc. Title: Package Outline for TSOP(I) 56L (14X20mm)

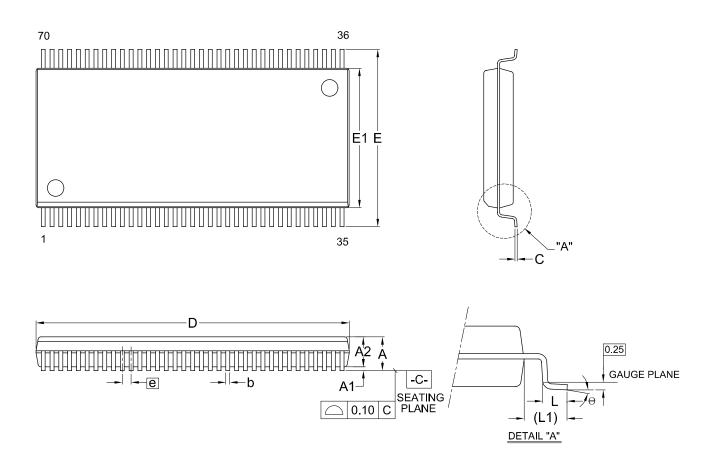


Dimensions (inch dimensions are derived from the original mm dimensions)

SY UNIT	MBOL	Α	A1	A2	b	С	D	D1	E	е	L	L1	Θ
	Min.		0.05	0.95	0.17	0.10	19.80	18.30	13.90		0.50	0.70	0
mm	Nom.		0.10	1.00	0.20	0.13	20.00	18.40	14.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	14.10		0.70	0.90	8
	Min.		0.002	0.037	0.007	0.004	0.780	0.720	0.547		0.020	0.028	0
Inch	Nom.		0.004	0.039	0.008	0.005	0.787	0.724	0.551	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.555		0.028	0.035	8

Dwg. No.	Revision		Refe	erence	
	Revision	JEDEC	EIAJ		
6110-1608	5	MO-142			

Doc. Title: Package Outline for SSOP 70L (500MIL)



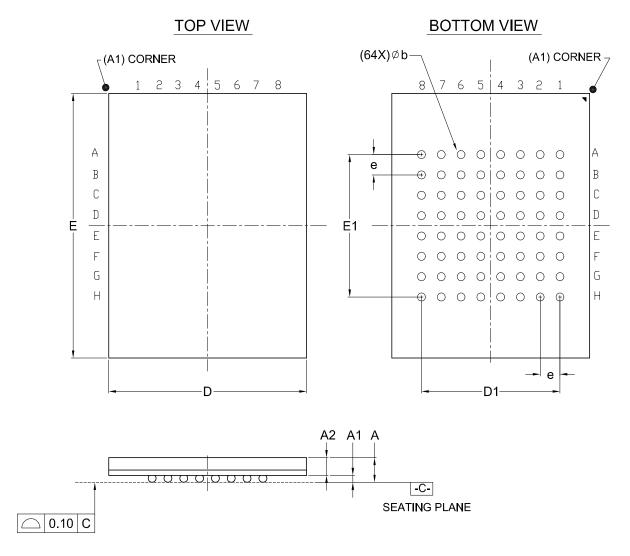
Dimensions (inch dimensions are derived from the original mm dimensions)

SY	MBOL	Α	<b>A</b> 1	<b>A</b> 2	þ	С	D	Е	E1	е	L	L1	Θ
	Min.	-	0.10	2.56	0.30	0.17	28.37	15.73	12.47	-	0.61	1.51	0
mm	Nom.		0.15	2.69	0.35	0.20	28.50	16.03	12.60	0.80	0.81	1.71	5
	Max.	3.05	0.23	2.82	0.43	0.25	28.63	16.33	12.73	l	1.01	1.91	10
	Min.		0.004	0.101	0.012	0.007	1.117	0.619	0.491	_	0.024	0.060	0
Inch	Nom.		0.006	0.106	0.014	0.008	1.122	0.631	0.496	0.031	0.032	0.068	5
	Max.	0.120	0.009	0.111	0.017	0.010	1.127	0.643	0.501	1	0.040	0.075	10

Descr. Ma	Revision	Reference					
Dwg. No.		JEDEC	EIAJ				
6110-1503	7	MO-174					



Doc. Title: Package Outline for CSP 64BALL(10X13X1.2MM,BALL PITCH 1.00MM,BALL DIAMETER 0.4MM)



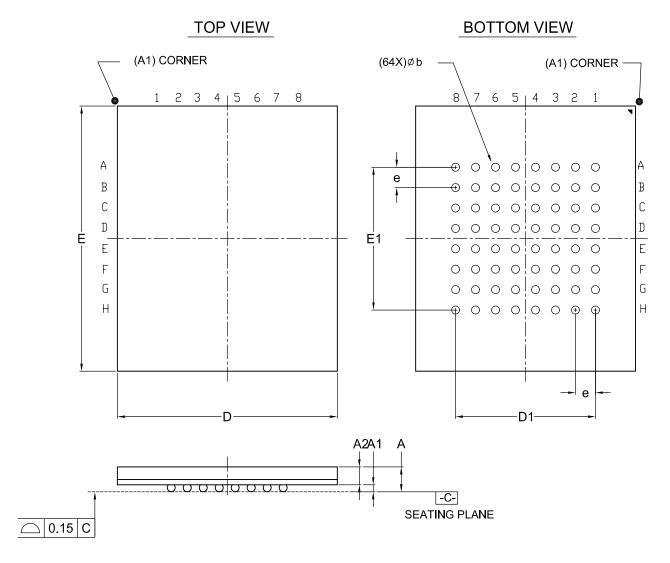
Dimensions (inch dimensions are derived from the original mm dimensions)

SY	MBOL	Α	<b>A</b> 1	A2	b	D	D1	E	E1	е
	Min.		0.25	0.65	0.35	9.90		12.90		
mm	Nom.		0.30		0.40	10.00	7.00	13.00	7.00	1.00
	Max.	1.20	0.35		0.45	10.10		13.10		
	Min.		0.010	0.026	0.014	0.390		0.508		
Inch	Nom.		0.012		0.016	0.394	0.276	0.512	0.276	0.039
	Max.	0.047	0.014		0.018	0.398		0.516		

Dwg. No.	Revision	Reference					
		JEDEC	EIAJ				
6110-4220	4	MO-216					



#### Title: Package Outline for CSP 64BALL(11X13X1.4MM,BALL PITCH 1.00MM,BALL DIAMETER 0.6MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SY	MBOL	Α	<b>A</b> 1	A2	b	D	D1	E	E1	е
	Min.		0.40	0.65	0.50	10.90		12.90		
mm	Nom.		0.50		0.60	11.0	7.00	13.00	7.00	1.00
	Max.	1.40	0.60		0.70	11.10		13.10		
	Min.		0.016	0.026	0.020	0.429		0.508		
Inch	Nom.		0.020		0.024	0.433	0.276	0.512	0.276	0.039
	Max.	0.055	0.024	ļ	0.028	0.437		0.516		

DWG.NO.	REVISION		ISSUE DATE		
		JEDEC	EIAJ		1990E DATE
6110-4247	0	MO <b>-</b> 192			07-27-'05



#### **REVISION HISTORY**

Revision No.	Description	Page	Date
1.0	1. Revised 70-SSOP ground pin configurations	P4	APR/28/2009
	2. Added overshoot & undershoot specifications	P41	
	3. Removed "Preliminary"	P2	
	4. Changed data retention from 10 years to 20 years	P2,65	
	5. Modified <i>Tdf</i> (max.) = 20ns	P44	
1.1	1. Added 1.8V VI/O information	P2,41,44	JUN/29/2009
		P68,69	
	2. Modified <i>Tsrw</i> (min.) = 35ns	P44	
	3. Added Icr2 parameter and "status Polling for write buffer program"	P42,60	
	flowchart; revised Voh remark		
	4. Added notes	P45,68	
	5. Content correction	P18,43	
	6. Modifed the title of <i>Figure 16</i> as write buffer and added notes	P60	
1.2	1. Added unused CFI area reservation notice.	P38	NOV/22/2010
	2. Added wording "e.g. Vcc and CE# ramp up simultaneously"	P66	
	3. Modified Figure A. AC Timing at Device Power-Up	P66	
	4. Modified Timing waveform at Figure 10 and Figure 14	P54, 58	
	5. Modified "PIN CAPACITANCE" table	P67	
	6. Modified environmental hazzardous substance wording	P2,69	
	7. Modified Figure 2. READ TIMING WAVEFORMS	P47	
1.3	1. Modified Figure 16. Status Polling For Write Buffer Program	P60	JUN/03/2011
	2. Announced "Not recommended for new designs"	P1,2	
	3. Modified the description of Write Buffer Programming Operation	P18	
1.4	1. Added Tdf spec for CE# high	P44	JUL/26/2011
	2. Added the parameter for VIO setup up time	P66	



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