19-4102; Rev 0; 5/08

Highly Efficient, All-Internal MOSFET, 6-Channel PMIC for 2AA Digital Camera Systems

MAX8858

General Description

The MAX8858 PMIC provides a complete power-supply solution for digital still cameras (DSCs) and digital video cameras (DVCs). The MAX8858 improves performance, component count, and board space utilization compared to currently available solutions for two AA cell and dual-battery designs. On-chip power MOSFETs provide up to 95% efficiency for critical power supplies. The CCD inverter can operate directly from two AA/NiMH batteries without the use of any additional external components.

- Step-up synchronous-rectified DC-DC converter (SU). The MAX8858 is bootstrapped from V_{VSU}.
- MAIN synchronous-rectified step-up DC-DC converter (M) with active discharge for DSP I/O supply voltage.
- SDZ synchronous-rectified step-down DC-DC converter (SDZ) with active discharge for DSP DDR supply voltage.
- Low-voltage (down to 1V) synchronous-rectified step-down DC-DC converter (SD) with active discharge for DSP core supply voltage.
- High-voltage step-up DC-DC converter (CCDBST) for CCD imagers or positive LCD bias supplies.
- Transformerless inverting DC-DC converter (CCDINV) with active discharge for CCD imagers or negative LCD bias supplies. **This converter can connect directly to two AA batteries.**

Individual ON_ inputs provide independent on/off control for the SU, CCDBST, and CCDINV converters, while dual-function inputs allow independent on/off control or power-up sequencing of the MAIN, SDZ, and SD converters.

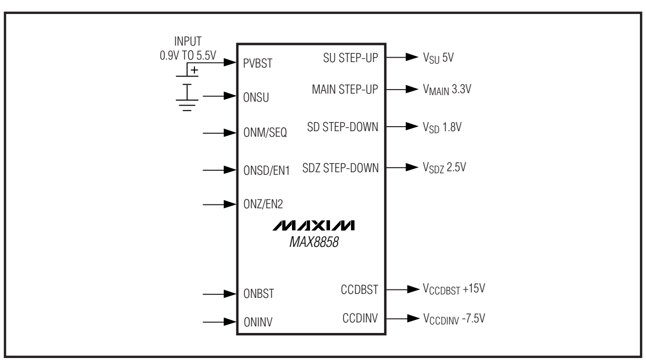
The MAX8858 is available in a 5mm x 5mm x 0.8mm, 32-pin thin QFN package and operates over the -40°C to +85°C extended temperature range.

Applications

DSCs and DVCs

PDAs and Portable Media Players

Typical Operating Circuit



Features

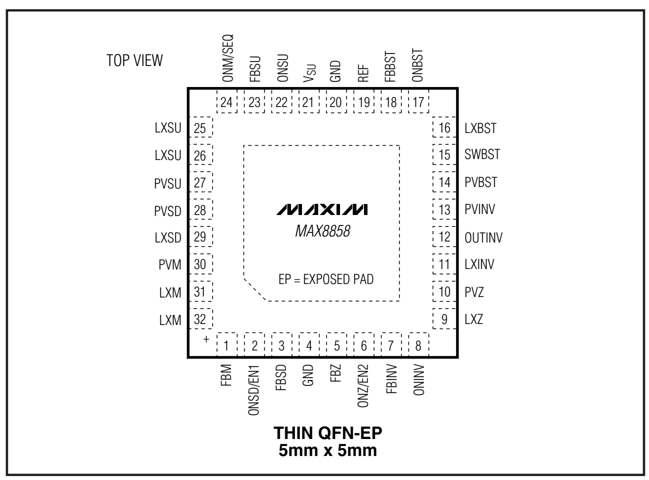
- ♦ 95% Efficient Synchronous-Rectified DC-DC Converters
- ♦ Up to 90% Efficient Boost-Buck Operation
- ♦ Up to 85% Efficient, High-Voltage DC-DC Converters
- ♦ Transformerless Inverting Converter with Active Discharge for CCD
- ♦ Preset Power-Up Sequencing for MAIN, SDZ, and SD Converters
- ♦ Inverter Operates Directly from Two AA Batteries
- ♦ Internal Compensation on All Channels
- ♦ True Shutdown™ on All Step-Up Converters
- ♦ Overload Protection
- ♦ Startup into Short Protection
- ♦ Soft-Start for Controlled Inrush Current
- ♦ 100% Duty Cycle on Step-Down Converters
- ♦ 2MHz ±5% Switching Frequency
- ♦ 0.1µA Shutdown Supply Current
- ♦ All Internal Power MOSFETs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8858ETJ+	-40°C to +85°C	32 Thin QFN-EP*

+Denotes a lead-free package.
**EP = Exposed pad.*

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

ON__, FB__, PV__, SU, REF to GND ....-0.3V to +6V
SWBST to GND......................................-0.3V to (V_{PVBST} + 0.3V)
LXSD, LXZ Current (Note 1)...632.5mA
LXSU, LXM Current (Note 1)..2.85A
LXINV to GND..........................(V_{PVINV} - 22V) to (V_{PVINV} + 0.3V)
OUTINV to GND ....-14V to (V_{PVINV} + 0.3V)
LXBST to GND...-0.3V to +28V
EP (PG_) to GND...-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN, Single-Layer Board
(derate 21.3mW/°C above +70°C)............................1702mW
32-Pin TQFN, Multilayer Board
(derate 34.5mW/°C above +70°C)...........................2759mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LXSU and LXM have internal clamp diodes to PG_ (EP) and VPWR, where VPWR is the internal power node that is connected to the higher voltage of PVBST and PVSU or PVM, respectively. LXSD and LXZ have internal clamp diodes to PVSD and PVZ, respectively, and PG_ (EP). LXINV has internal clamp diodes to PVINV and PG_(EP). Applications that forward bias these diodes must be careful not to exceed the power dissipation limits of the device.

ELECTRICAL CHARACTERISTICS

(V_{PVBST} = V_{PVINV} = V_{PVSD} = V_{PVZ} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{VSU} = 5V, V_{EP} = V_{GND} = 0V, C_{REF} = 0.22µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	(Note 3)		0.9		5.5	V
Minimum SU Startup Voltage				1.2	1.5	V
SU Step-Up Startup Frequency				2		MHz
Shutdown Supply Current	V_{ONSU} = 0V	T_A = +25°C		0.1	10	µA
	V_{PVBST} = 5.5V	T_A = +85°C		0.1		
Supply Current with SU Step-Up Enabled	V_{ONSU} = 2.4V, I_{PVBST} + I_{VSU} (does not include switching losses)			40	70	µA
Supply Current with SU Step-Up and SD Step-Down Enabled	V_{ONSU} = $V_{ONSD/EN1}$ = 2.4V, I_{PVBST} + I_{VSU} + I_{PVSD} (does not include switching losses)			330	500	µA
Supply Current with SU Step-Up and MAIN Step-Up Enabled	V_{ONSU} = $V_{ONM/SEQ}$ = 2.4V, I_{PVBST} + I_{VSU} + I_{PVM} (does not include switching losses)			330	500	µA
Supply Current with SU Step-Up and SDZ Step-Down Enabled	V_{ONSU} = $V_{ONZ/EN2}$ = 2.4V, I_{PVBST} + I_{VSU} + I_{PVZ} (does not include switching losses)			330	500	µA
Supply Current with SU Step-Up and CCDBST Step-Up Enabled	V_{ONSU} = V_{ONBST} = 2.4V, I_{VSU} + I_{PVBST} (does not include switching losses)			600	900	µA
Supply Current with SU Step-Up and CCDINV Inverter Enabled	V_{ONSU} = V_{ONINV} = 2.4V, I_{PVBST} + I_{VSU} + I_{PVINV} (does not include switching losses)			550	850	µA
REFERENCE (REF)						
Reference Output Voltage	I_{REF} = 20µA		1.24	1.25	1.26	V
Reference Load Regulation	10µA < I_{REF} < 100µA			3	10	mV
Reference Line Regulation	3.3V < (V_{PVSU} = V_{VSU}) < 5.5V			0	5	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = V_{PVZ} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{VSU} = 5V, V_{EP} = V_{GND} = 0V, C_{REF} = 0.22µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR (OSC)					
SU, MAIN, SDZ, SD Switching Frequency		1.9	2	2.1	MHz
SU, MAIN Step-Up Maximum Duty Cycle			85		%
SDZ, SD Step-Down Maximum Duty Cycle	(Note 4)			100	%
CCDBST, CCDINV Switching Frequency		0.634	0.667	0.700	MHz
CCDBST, CCDINV Maximum Duty Cycle			90		%
SU STEP-UP DC-DC CONVERTER					
Step-Up Voltage Adjust Range		3.3		5.0	V
FBSU Regulation Voltage	No load	0.995	1.015	1.025	V
FBSU Load Regulation			-7.5		mV/A
FBSU Line Regulation			-10		mV/D
FBSU Input Leakage Current	V_{FBSU} = 1.01V	-50	-5	+50	nA
Idle Mode™ Trip Level	(Note 5)		50		mA
LXSU Leakage Current	V_{LXSU} = 0V, 5V, V_{PVBST} = 5V	-5	0.1	+5	µA
n-Channel On-Resistance	I_{LXSU} = 190mA		0.1		Ω
p-Channel On-Resistance	I_{LXSU} = -190mA		0.14		Ω
n-Channel Current Limit		2.0	2.3	2.6	A
p-Channel Turn-Off Current			10		mA
Soft-Start Interval	Full load		7.5		ms
Overload Protection Fault Delay			100		ms
Startup into a Short Circuit	Fault timing		30		ms
MAIN STEP-UP DC-DC CONVERTER					
Step-Up Voltage Adjust Range		3.3		V_{VSU}	V
FBM Regulation Voltage	No load	0.995	1.015	1.025	V
FBM Load Regulation			-7.5		mV/A
FBM Line Regulation			-10		mV/D
FBM Input Leakage Current	V_{FBM} = 1.01V	-50	-5	+50	nA
Idle-Mode Trip Level	(Note 5)		50		mA
LXM Leakage Current	V_{LXM} = 0V, 5V, V_{PVBST} = 5V	-5	0.1	+5	µA
n-Channel On-Resistance	I_{LXM} = 190mA		0.1		Ω
p-Channel On-Resistance	I_{LXM} = -190mA		0.14		Ω
PVM Pulldown Resistance		30	60	90	Ω
n-Channel Current Limit		2.0	2.3	2.6	A

Idle Mode is a trademark of Maxim Integrated Products, Inc.

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ELECTRICAL CHARACTERISTICS (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = V_{PVZ} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{VSU} = 5V, V_{EP} = V_{GND} = 0V, C_{REF} = 0.22µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
p-Channel Turn-Off Current			10		mA
Soft-Start Interval	Full load		15		ms
Overload Protection Fault Delay			100		ms
Startup into a Short Circuit	Fault timing		30		ms
SDZ STEP-DOWN DC-DC CONVERTER					
Step-Down Output Voltage Adjust Range		1		V_{VSU}	V
FBZ Regulation Voltage	No load	0.995	1.015	1.025	V
FBZ Load Regulation			-50		mV/A
FBZ Line Regulation			-10		mV/D
FBZ Input Leakage Current	V_{FBZ} = 1.01V	-50	-5	+50	nA
Idle-Mode Trip Level	(Note 5)		50		mA
LXZ Leakage Current	V_{LXZ} = 0V, 5V, V_{PVBST} = 5V	-5	0.1	+5	µA
n-Channel On-Resistance	I_{LXZ} = 190mA		0.21		Ω
p-Channel On-Resistance	I_{LXZ} = -190mA		0.24		Ω
LXZ Pulldown Resistance		30	60	90	Ω
p-Channel Current Limit		0.425	0.5	0.575	A
n-Channel Turn-Off Current			10		mA
Soft-Start Interval			1.25		ms
Overload Protection Fault Delay			100		ms
SD STEP-DOWN DC-DC CONVERTER					
SD Step-Down Output Voltage Adjust Range		1		V_{VSU}	V
FBSD Regulation Voltage	No load	0.995	1.015	1.025	V
FBSD Load Regulation			-60		mV/A
FBSD Line Regulation			-7		mV/D
FBSD Input Leakage Current	V_{FBSD} = 1.01V	-50	-5	+50	nA
Idle-Mode Trip Level	(Note 5)		50		mA
LXSD Leakage Current	V_{LXSD} = 0V, 5V, V_{PVBST} = 5V	-5	0.1	+5	µA
n-Channel On-Resistance	I_{LXSD} = 190mA		0.21		Ω
p-Channel On-Resistance	I_{LXSD} = -190mA		0.24		Ω
LXSD Pulldown Resistance		30	60	90	Ω
p-Channel Current Limit		0.425	0.5	0.575	A
n-Channel Turn-Off Current			10		mA
Soft-Start Interval			2.5		ms
Overload Protection Fault Delay			100		ms
CCDBST DC-DC CONVERTER					
CCDBST Ouput Voltage Adjust Range		V_{PVBST}		18	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = V_{PVZ} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{VSU} = 5V, V_{EP} = V_{GND} = 0V, C_{REF} = 0.22µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FBBST Regulation Voltage	No load	1.005	1.02	1.035	V
FBBST Load Regulation			-15		mV/A
FBBST Line Regulation			-20		mV/D
FBBST Input Leakage Current	V_{FBBST} = 1.01V	-50	-5	+50	nA
SWBST Leakage Current	V_{SWBST} = 0V	-5	0.1	+5	µA
LXBST Leakage Current	V_{LXBST} = 28V	-5	0.1	+5	µA
Load Switch On-Resistance	I_{SWBST} = 190mA		0.09		Ω
DMOS On-Resistance	I_{LXBST} = -190mA		0.4		Ω
SWBST Current Limit		0.8	1.0	1.2	A
SWBST Short-Circuit Current Limit		1.1	1.3	1.6	A
Soft-Start Interval			7.5		ms
Overload Protection Fault Delay			100		ms
CCDINV DC-DC CONVERTER					
CCDINV Output Voltage Adjust Range		V_{PVINV} - 16		0	V
FBINV Regulation Voltage	No load	-10	0	+10	mV
FBINV Load Regulation			23		mV/A
FBINV Line Regulation			20		mV/ (D-0.5)
FBINV Input Leakage Current	V_{FBINV} = 0V	-50	-5	+50	nA
LXINV Leakage Current	V_{LXINV} = -14.5V, V_{PVINV} = 5V	-5	0.1	+5	µA
HVPMOS On-Resistance	I_{LXINV} = -190mA		0.575		Ω
HVPMOS Current Limit		0.8	1.0	1.2	A
OUTINV Discharge Current	V_{LXINV} = V_{OUTINV} = -7.5V, ONINV = GND, V_{ONSU} = 2.4V		50		mA
OUTINV Input Leakge Current	V_{OUTINV} = -12V	-5	0.1	+5	µA
Soft-Start Interval			7.5		ms
Overload Protection Fault Delay			100		ms
LOGIC INPUTS/OUTPUTS					
ONSU Input-Low Level	1.5V ≤ V_{PVSU} = V_{VSU} = V_{PVBST} < 5.5V (Note 6)			0.5	V
ONSU Input-High Level	1.5V ≤ V_{PVSU} = V_{VSU} = V_{PVBST} < 5.5V, V_H is the higher of V_{PVSU} and V_{PVBST} (Note 6)	V_H - 0.2V (1.3V max)			V
ONSD/EN1, ONZ/EN2, ONM/SEQ, ONBST, ONINV Input-Low Level	3.3V ≤ V_{PVSU} = V_{VSU} = V_{PVBST} (Note 7)			0.5	V
ONSD/EN1, ONZ/EN2, ONM/SEQ, ONBST, ONINV Input-High Level	3.3V ≤ V_{PVSU} = V_{VSU} = V_{PVBST} (Note 7)	1.4			V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = V_{PVZ} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{VSU} = 5V, V_{EP} = V_{GND} = 0V, C_{REF} = 0.22µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

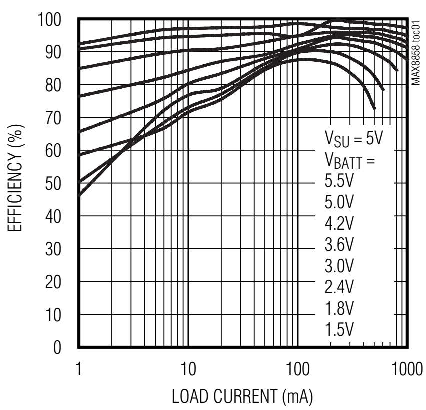
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ON_ Pulldown Resistance			1		MΩ
THERMAL-LIMIT PROTECTION					
Thermal Shutdown			+165		°C

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.
Note 3: Once the SU converter has reached regulation, the battery voltage can decay to 0.9V without loss of regulation.
Note 4: Guaranteed by design and characterization, not production tested.
Note 5: The idle-mode current threshold is the transition point between fixed-frequency PWM operation and idle-mode operation. The specification is given in terms of output load current for inductor values shown in Figure 1. For the step-up converter, the idle-mode transition varies with input-to-output voltage ratio.
Note 6: Production tested at 1.5V. Guaranteed by design up to 5.5V.
Note 7: Production tested at 3.3V.

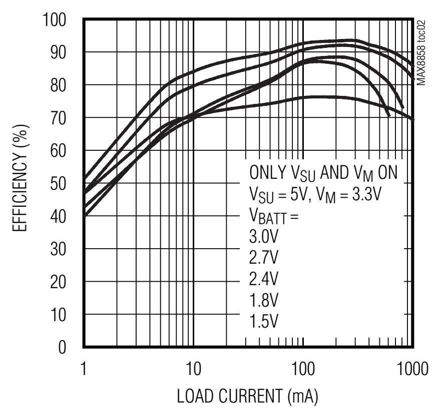
Typical Operating Characteristics

(V_{PVBST} = V_{PVINV} = V_{PVSD} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{PVZ} = 5V, C_{REF} = 0.22µF, T_A = +25°C (circuit of Figure 1, unless otherwise noted.)

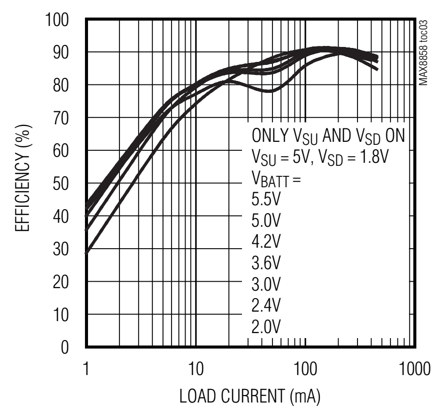
V_{SU} STEP-UP EFFICIENCY vs. LOAD CURRENT



V_M STEP-UP EFFICIENCY vs. LOAD CURRENT



V_{SD} STEP-DOWN EFFICIENCY vs. LOAD CURRENT



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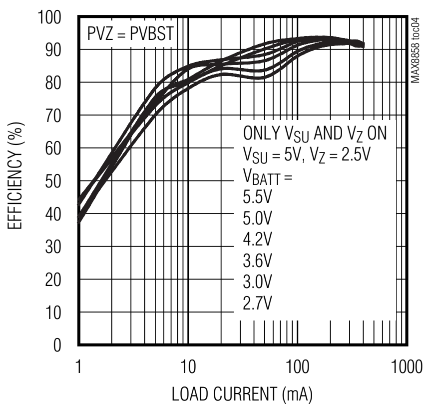
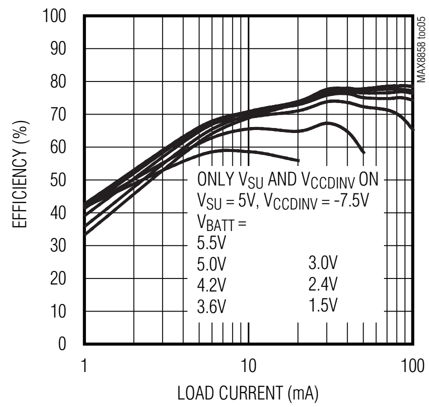
Typical Operating Characteristics (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{PVZ} = 5V, C_{REF} = 0.22µF, T_A = +25°C (circuit of Figure 1, unless otherwise noted.)

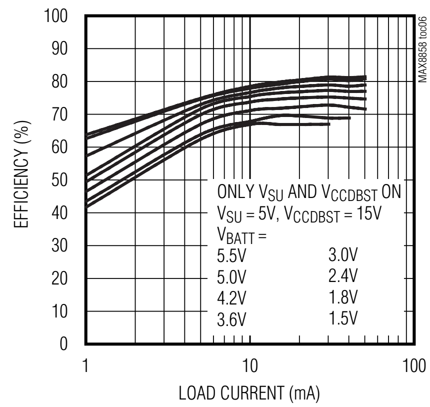
V_{SDZ} STEP-DOWN EFFICIENCY vs. LOAD CURRENT



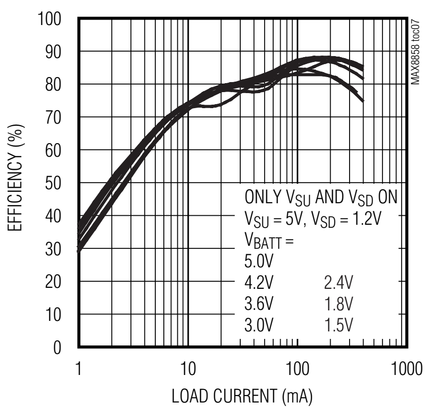
V_{CCDINV} INVERTER EFFICIENCY vs. LOAD CURRENT



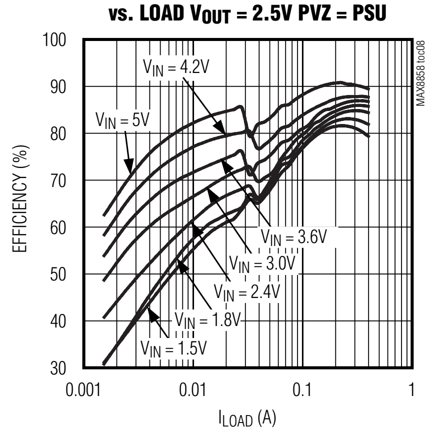
V_{CCDBST} STEP-UP EFFICIENCY vs. LOAD CURRENT



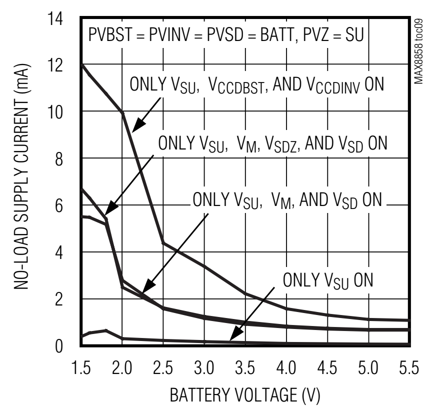
V_{SD} STEP-DOWN EFFICIENCY vs. LOAD CURRENT



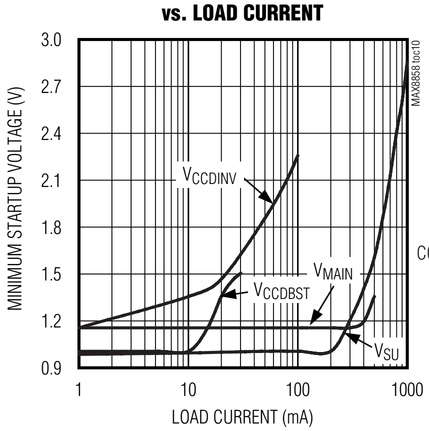
V_{SDZ} BOOST-BUCK EFFICIENCY vs. LOAD V_{OUT} = 2.5V PVZ = PSU



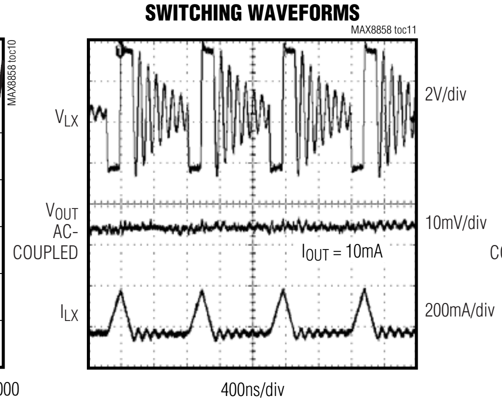
NO-LOAD SUPPLY CURRENT vs. BATTERY VOLTAGE



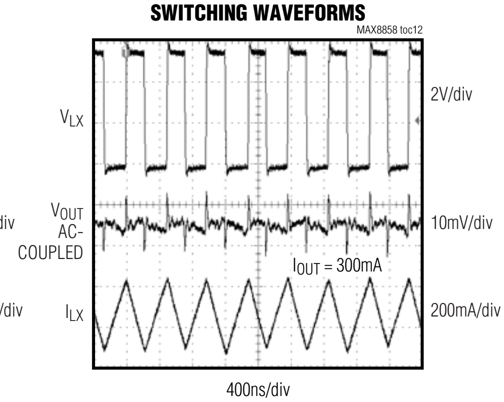
MINIMUM STARTUP VOLTAGE vs. LOAD CURRENT



V_{SU} STEP-UP IDLE-MODE SWITCHING WAVEFORMS



V_{SU} STEP-UP HEAVY LOAD SWITCHING WAVEFORMS

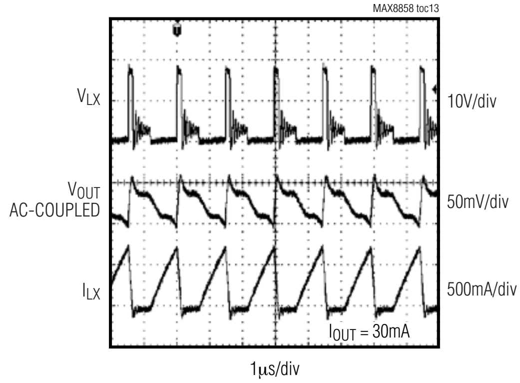


Typical Operating Characteristics (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{PVZ} = 5V, C_{REF} = 0.22µF, T_A = +25°C (circuit of Figure 1, unless otherwise noted.)

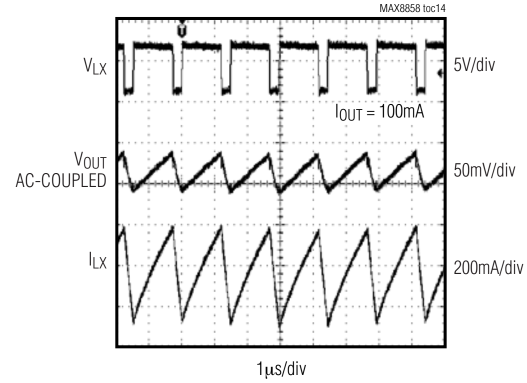
V_{CCDBST} STEP-UP SWITCHING WAVEFORMS

MAX8858 toc13



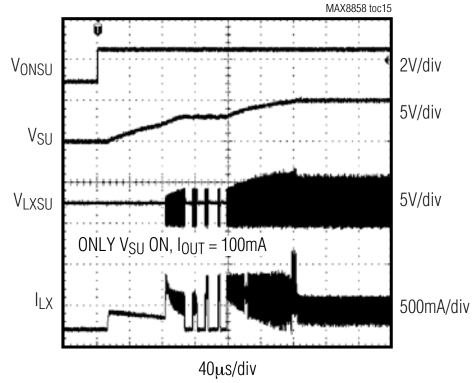
V_{CCDINV} INVERTER SWITCHING WAVEFORMS

MAX8858 toc14



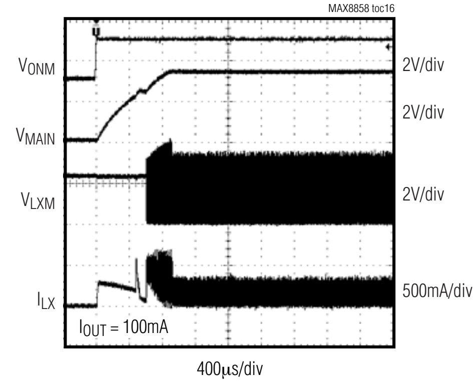
V_{SU} STEP-UP STARTUP WAVEFORMS

MAX8858 toc15



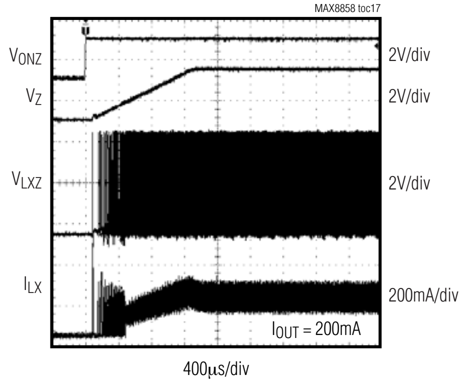
V_{MAIN} STEP-UP STARTUP WAVEFORMS

MAX8858 toc16



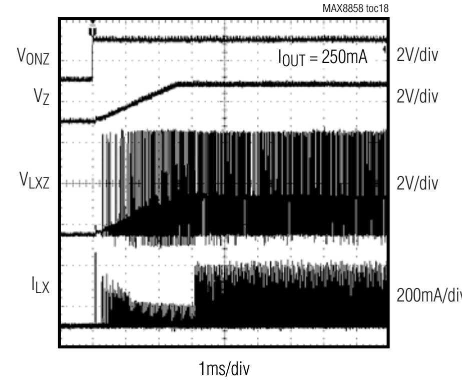
V_{SDZ} STEP-DOWN STARTUP WAVEFORMS

MAX8858 toc17



V_{SD} STEP-DOWN STARTUP WAVEFORMS

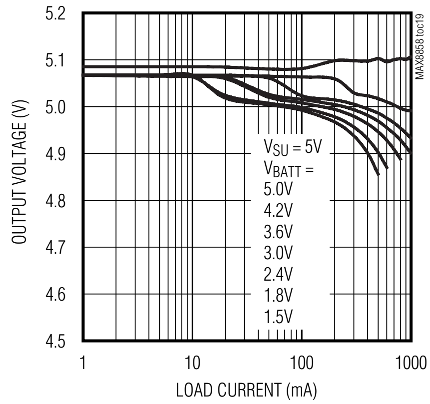
MAX8858 toc18



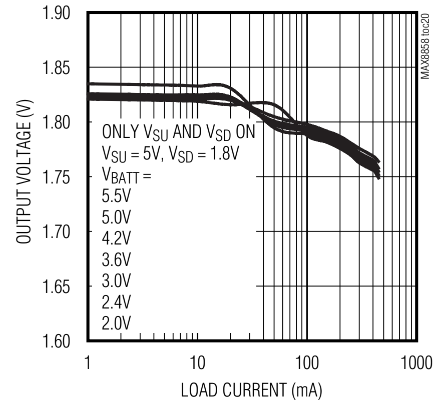
Typical Operating Characteristics (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{PVZ} = 5V, C_{REF} = 0.22µF, T_A = +25°C (circuit of Figure 1, unless otherwise noted.)

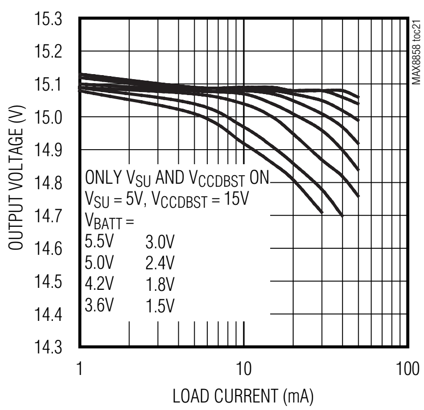
V_{SU} OUTPUT VOLTAGE vs. LOAD CURRENT



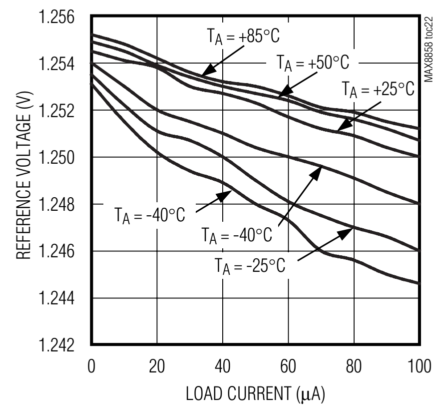
V_{SD} OUTPUT VOLTAGE vs. LOAD CURRENT



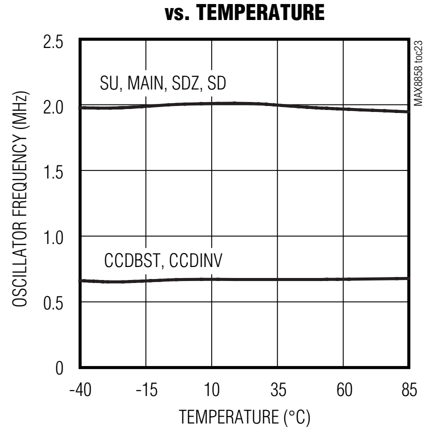
V_{CCDBST} OUTPUT VOLTAGE vs. LOAD CURRENT



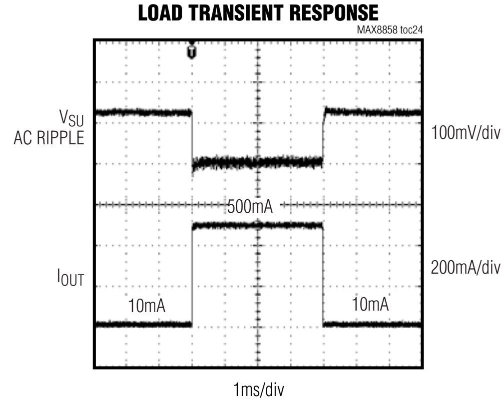
REFERENCE VOLTAGE vs. LOAD CURRENT OVER TEMPERATURE



OSCILLATOR FREQUENCY vs. TEMPERATURE



V_{SU} STEP-UP LOAD TRANSIENT RESPONSE

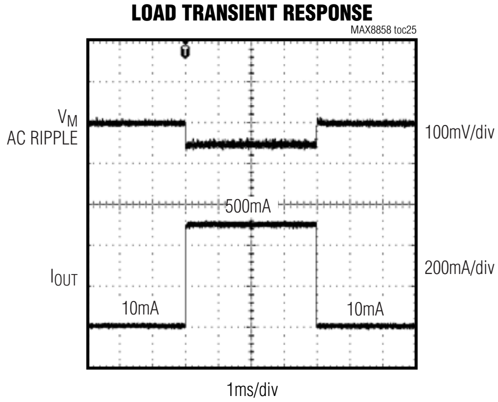


Highly Efficient, All-Internal MOSFET, 6-Channel PMIC for 2AA Digital Camera Systems

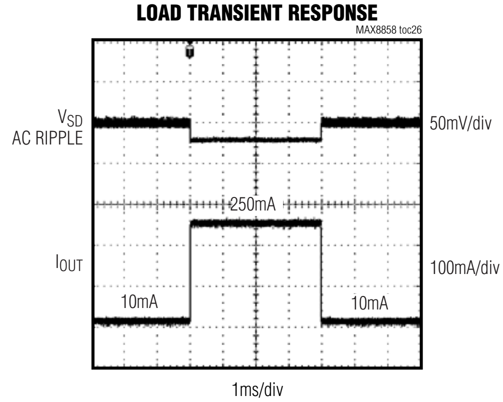
Typical Operating Characteristics (continued)

(V_{PVBST} = V_{PVINV} = V_{PVSD} = 2.4V, V_{PVM} = 3.3V, V_{PVSU} = V_{PVZ} = 5V, C_{REF} = 0.22µF, T_A = +25°C (circuit of Figure 1, unless otherwise noted.)

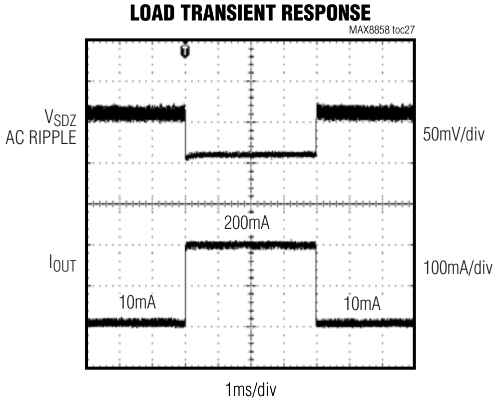
V_M STEP-UP LOAD TRANSIENT RESPONSE



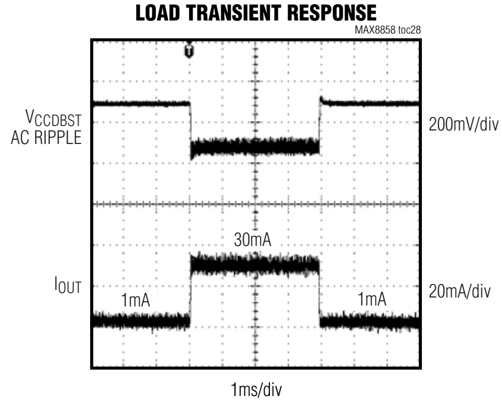
V_{SD} STEP-DOWN LOAD TRANSIENT RESPONSE



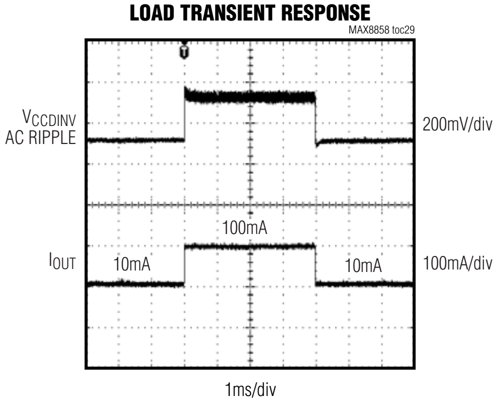
V_{SDZ} STEP-DOWN LOAD TRANSIENT RESPONSE



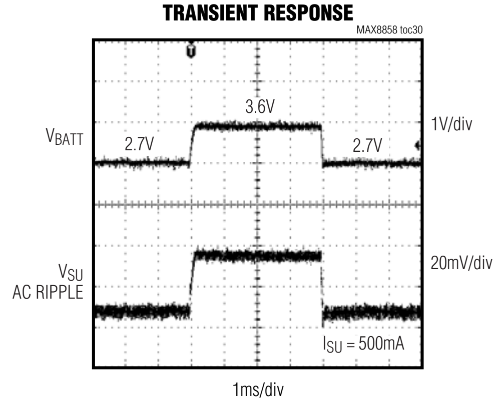
V_{CCDBST} STEP-UP LOAD TRANSIENT RESPONSE



V_{CCDINV} INVERTER LOAD TRANSIENT RESPONSE



V_{SU} STEP-UP LINE TRANSIENT RESPONSE



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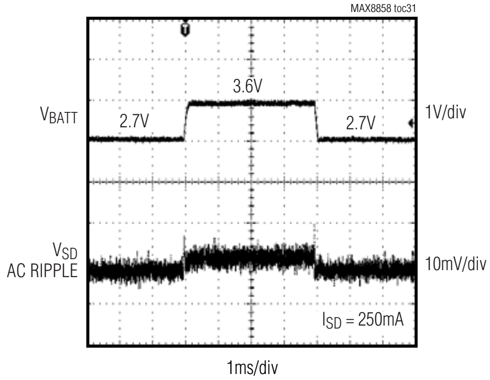
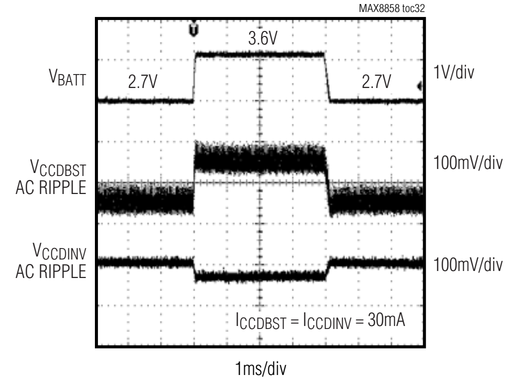
Typical Operating Characteristics (continued)

($V_{PVBST} = V_{PVINV} = V_{PVSD}$ = 2.4V, V_{PVM} = 3.3V, $V_{PVSU} = V_{PVZ}$ = 5V, C_{REF} = 0.22µF, T_A = +25°C (circuit of Figure 1, unless otherwise noted.)

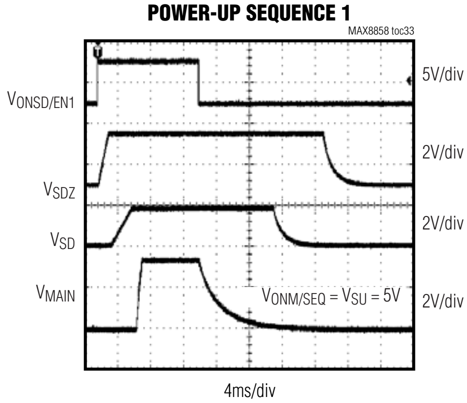
V_{SD} STEP-DOWN LINE TRANSIENT RESPONSE



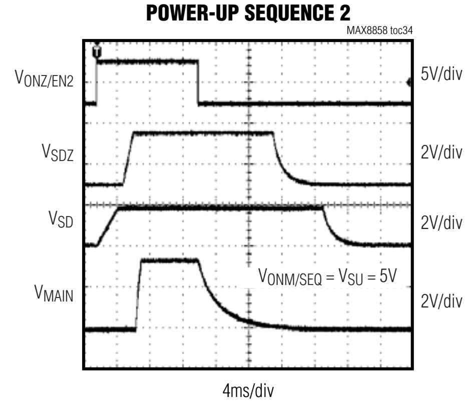
CCD LINE TRANSIENT RESPONSE



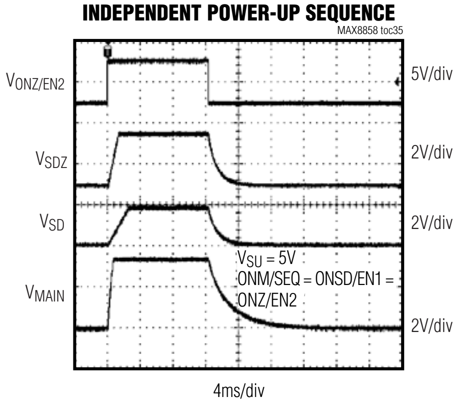
POWER-UP SEQUENCE 1



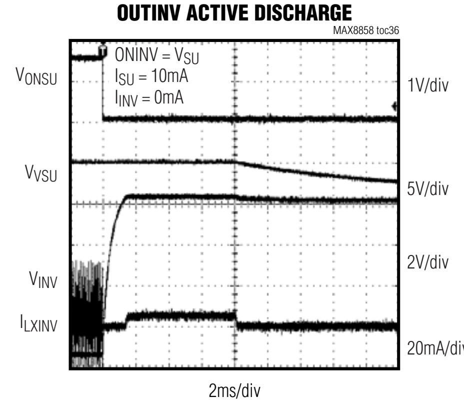
POWER-UP SEQUENCE 2



INDEPENDENT POWER-UP SEQUENCE



OUTINV ACTIVE DISCHARGE



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Pin Description

PIN	NAME	FUNCTION
1	FBM	MAIN Step-Up Converter Feedback Input. The feedback threshold is 1.015V. FBM is high impedance in shutdown.
2	ONSD/EN1	SD Dual-Function Enable Input. When ONM/SEQ = V_{SU} before V_{VSU} reaches regulation, then ONSD/EN1 selects power-up sequence 1. If ONM/SEQ = GND when V_{VSU} reaches regulation, ONSD/EN1 turns V_{SD} on and off. See the *Power-Up Sequencing and On/Off Control (MAIN, SDZ, SD Converters)* section. ONSD/EN1 has an internal 1MΩ resistor to GND.
3	FBSD	SD Step-Down Converter Feedback Input. The feedback threshold is 1.015V. FBSD is high impedance in shutdown.
4, 20	GND	Analog Ground. Connect GND to EP as close as possible to the IC using a star connection for best performance.
5	FBZ	SDZ Step-Down Converter Feedback Input. The feedback threshold is 1.015V. FBZ is high impedance in shutdown.
6	ONZ/EN2	SDZ Dual-Function Enable Input. When ONM/SEQ = V_{SU} before V_{VSU} reaches regulation, then ONZ/EN2 selects power-up sequence 2. If ONM/SEQ = GND when V_{VSU} reaches regulation, ONZ/EN2 turns V_{SDZ} on and off. See the *Power-Up Sequencing and On/Off Control (MAIN, SDZ, SD Converters)* section.
7	FBINV	CCD Inverting Converter Feedback Input. The feedback threshold is 0V. FBINV is internally pulled to GND in shutdown.
8	ONINV	CCD Inverting Converter On/Off Control Input. Connect ONINV to SU to turn the CCDINV converter on. CCDINV does not turn on until the SU step-up converter has reached regulation.
9	LXZ	SDZ Step-Down Converter Switching Node. LXZ is high impedance in shutdown.
10	PVZ	SDZ Step-Down Converter Power Input. Bypass PVZ to GND with a 1µF ceramic capacitor installed as close as possible to the IC.
11	LXINV	CCD Inverting Converter Switching Node. LXINV is high impedance in shutdown.
12	OUTINV	CCD Inverting Converter Discharge Node. Install a 100Ω resistor between OUTINV and the INV output capacitor. OUTINV discharges the CCDINV output capacitor for 8ms when ONINV is driven low. OUTINV is high impedance when ONINV is high and when the IC is in shutdown.
13	PVINV	CCD Inverting Converter Power Input. Bypass PVINV to GND with a 1µF ceramic capacitor installed as close as possible to the IC.
14	PVBST	CCDBST Converter and IC Power Input. Bypass PVBST to GND with a 1µF ceramic capacitor installed as close as possible to the IC.
15	SWBST	CCDBST True Shutdown Switch Input. Connect the inductor for the CCDBST converter between LXBST and SWBST. SWBST is high impedance in shutdown.
16	LXBST	CCDBST Open-Drain Switching Node. Connect the inductor for the CCDBST converter between LXBST and SWBST. LXBST is high impedance in shutdown.
17	ONBST	CCD Boost Converter On/Off Control Input. Connect ONBST to SU to turn on the CCDBST output. CCDBST does not turn on until the SU step-up converter has reached regulation. ONBST has an internal 1MΩ pulldown resistor to GND.
18	FBBST	CCDBST Converter Feedback Input. The feedback threshold is 1.02V. FBBST is high impedance in shutdown.

Pin Description (continued)

PIN	NAME	FUNCTION
19	REF	1.25V Reference Output. Bypass REF to GND with a 0.22µF ceramic capacitor installed as close as possible to the IC. REF is internally pulled to GND in shutdown.
21	V_{SU}	Power Input Bootstrapped from PVSU. Connect V_{SU} to PVSU through an optional RC filter.
22	ONSU	SU Step-Up Converter On/Off Control Input. Connect ONSU to PVBST to turn on the SU output. No other outputs turn on until the SU step-up converter has reached regulation. ONSU has an internal 1MΩ pulldown resistor to GND.
23	FBSU	SU Step-Up Converter Feedback Input. The feedback threshold is 1.015V. FBSU is high impedance in shutdown.
24	ONM/SEQ	MAIN/SDZ/SD Dual-Function Enable Input. ONM/SEQ selects either a preset power-up sequence for the MAIN, SDZ, and SD converters, or allows independent control of the on/off behavior of these converters. Connect ONM/SEQ to V_{SU} before V_{VSU} has reached regulation to select a preset power-up sequence. ONSD/EN1 and ONZ/EN2 select the particular power-up sequence. Alternatively, connect ONM/SEQ to GND before V_{VSU} reaches regulation to select independent control of the MAIN, SDZ, and SD converters. ONM/SEQ controls the on/off behavior of the V_{MAIN} converter when independent control is selected. See the *Power-Up Sequencing and On/Off Control (MAIN, SDZ, SD Converters)* section.
25, 26	LXSU	SU Step-Up Converter Switching Node. LXSU is high impedance in shutdown.
27	PVSU	SU Step-Up Converter Power Output. Bypass PVSU to GND with 2x 22µF, 6.3V X5R ceramic capacitors installed as close as possible to the IC.
28	PVSD	SD Step-Down Converter Power Input. Bypass PVSD to GND with a 10µF ceramic capacitor installed as close as possible to the IC.
29	LXSD	SD Step-Down Converter Switching Node. LXSD is high impedance in shutdown.
30	PVM	Step-Up Converter Power Output. Bypass PVM to GND with 2x 22µF, 6.3V X5R ceramic capacitors installed as close as possible to the IC.
31, 32	LXM	MAIN Step-Up Converter Switching Node. LXM is high impedance in shutdown.
—	EP	Exposed Pad. EP is internally connected to all converters' power ground. There are internal bond wires physically connecting the exposed pad to the internal power grounds (PGs) of all the converters. Connect EP to the power ground plane and GND as close as possible to the device for best performance.

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Detailed Description

The MAX8858 can accept inputs from a variety of sources including 1-cell Li+ batteries, 2-cell alkaline or NiMH batteries, and systems designed to accept either battery type. It includes six DC-DC converter channels to build a multiple-output DSC power-supply system:

- Step-up DC-DC synchronous-rectified converter (SU) with on-chip power FETs, internal compensation, and True Shutdown.
- MAIN step-up DC-DC synchronous-rectified converter (M) with on-chip power FETs, internal compensation, True Shutdown, and active discharge.
- SDZ step-down DC-DC synchronous rectified converter (SDZ) with on-chip power FETs, internal compensation and active discharge (typically step-down from SU).
- Core step-down DC-DC synchronous rectified converter (SD) with on-chip power FETs, internal compensation, and active discharge.
- CCD step-up DC-DC converter (CCDBST) with on-chip power FETs, internal compensation, and an internal switch for True Shutdown.
- CCD inverting DC-DC converter (CCDINV) with on-chip power FET, internal compensation, and active discharge. CCDINV operates directly from two AA batteries without the need for additional external components.

The four synchronous-rectified DC-DC converters operate at a 2MHz switching frequency, while the high-voltage boost and inverting converters switch at 667kHz, and are synchronized to the other converters. Other features include soft-start and overload protection. The IC is protected against short circuits at startup; if the SU output does not reach regulation within 30ms, the device latches off, protecting the MAX8858. The IC latches off all outputs when the die temperature reaches +165°C.

A typical application circuit for the MAX8858 using two AA batteries or dual-battery operation is shown in Figure 1.

All converters operate in a low-noise PWM mode with constant switching frequency under moderate to heavy loading. In the synchronous rectified converters (SU, MAIN, SD, and SDZ), efficiency is enhanced at light loads by switching to an idle mode where the converter switches only as needed to service the load.

Individual ON_ inputs provide independent on/off control for the SU, CCDBST, and CCDINV converters, while dual-function inputs allow independent on/off control or power-up sequencing of the MAIN, SDZ, and SD converters. The MAX8858 guarantees startup with an input voltage as low as 1.5V and remains operational with input voltages down to 0.9V. The MAX8858 also includes overload protection and soft-start circuitry. See Figure 2 for the functional diagram.

All DC-DC converters use peak current-mode control and are internally compensated. All converters utilize load line architecture to allow the output capacitor to be the dominant pole by lowering the loop gain. As a result, the MAX8858 matches the load-and-line regulation to the voltage droop seen during transients. This is sometimes called voltage positioning. This architecture minimizes the voltage overshoot when the load is removed, and voltage droop during transition from a light load to full load (see the Load Transient graphs in *Typical Operating Characteristics* section). Thus, the voltage delivered to the load remains within specification more effectively than with regulators that might have tighter initial DC accuracy, but greater transient overshoot and undershoot. This type of response is of great importance in digital cameras where the load can vary significantly in small time periods.

SU Step-Up DC-DC Converter

The SU step-up DC-DC switching converter typically generates a 5V output voltage from a 1.5V to 4.2V battery input voltage, but any output voltage from 3.3V to 5V is possible. The SU output voltage must be greater than or equal to the voltage output of the MAIN and SDZ converters. An internal switch and internal synchronous rectifier allow conversion efficiencies as high as 95%. Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered.

The SU converter is a current-mode converter. The difference between the feedback voltage and a 1V reference signal generates an error signal that programs the peak inductor current to regulate the output voltage. The peak inductor current limit is typically 2.3A. Inductor current is sensed across the internal switch and summed with an internal slope compensation signal.

At light loads (less than 50mA when boosting to 5V from a 1.8V input), efficiency is enhanced by an idle mode in which switching occurs only as needed to service the load. This idle-mode threshold is determined by comparing the current-sense signal to an internal reference (Figure 2). In idle mode, the synchronous rectifier shuts off once its current falls to 10mA, preventing negative inductor current.

The step-up output, PVSU, can start up into a load (see the *Typical Operating Characteristics* section). The soft-start duration is proportional to the size of the output capacitor and load, but is limited to a maximum of 7.5ms. Under normal operation, PVSU provides power to the device. After PVSU reaches regulation, the input voltage can drop as low as 0.9V without affecting circuit operation (although available output power from the boost converter is reduced at very low input voltages). All other outputs are locked out until SU reaches its regulation voltage.

The SU step-up converter features True Shutdown, eliminating the body diode path from input to output and allows the boost output to fall to GND in shutdown. This helps control the inrush current during startup, which results in longer battery life. SU is internally compensated, reducing external component requirements.

MAIN Step-Up DC-DC Converter

The MAIN step-up DC-DC switching converter typically operates with battery voltages from 1.5V to 4.2V. The converter's output voltage is adjustable from 3.3V to V_{VSU} (V_{VSU} is typically set to 5.0V). Internal switches provide conversion efficiency as high as 95%.

At light loads (less than 50mA when boosting to 5V from a 1.8V input), efficiency is enhanced by an idle mode in which switching occurs only as needed to service the load. The idle-mode current threshold is determined by comparing the current-sense signal to an internal reference (Figure 2). In idle mode, the synchronous rectifier shuts off once its current falls to 10mA, preventing negative inductor current.

The MAIN converter is enabled through a preset power-up sequence, or through independent on/off control, depending on the state of the ONSD/EN1, ONZ/EN2, and ONM/SEQ digital inputs. See the *Power-Up Sequencing and On/Off Control (MAIN, SDZ, SD Converters)* section for more details. MAIN features True Shutdown, eliminating the DC conduction path from input to output and allowing the step-up output to fall to GND in shutdown. During shutdown, PVM is pulled to GND through an internal 60Ω resistor. See the *Shutdown* section for more information.

SD/SDZ Step-Down DC-DC Converter

The SD step-down DC-DC converter is optimized to generate low-output voltages (down to 1V) at high efficiency, typically to power a DSP core. The SDZ converter is configured as a step-down for DSP DDR supply voltage. The SD and SDZ step-down converters are powered from PVSD and PVZ, respectively. PVSD and PVZ can be connected directly to the battery if there is sufficient headroom; otherwise, they are powered from the output of another converter. The SD and SDZ step-down converters can also operate from the SU step-up converter output for boost-buck operation.

Under moderate to heavy loading, the SD and SDZ converters operate in a low-noise PWM mode with constant frequency. Efficiency is enhanced under light (50mA typ) loading by operating in idle mode where the step-down converter switches only as needed to service the load. The SD and SDZ step-down converters are inactive until the SU step-up converter is in regulation.

The SD/SDZ converters are enabled through a preset power-up sequence, or through independent on/off control, depending on the state of the ONSD/EN1, ONZ/EN2, and ONM/SEQ inputs. See the *Power-Up Sequencing and On/Off Control (MAIN, SDZ, SD Converters)* section.

2.5V Boost-Buck Operation

When generating 2.5V or a similar voltage from two AA batteries, boost-buck operation is needed so that a regulated output is maintained for input voltages above and below 2.5V. In this case, the input of the SDZ step-down converter (PVZ) is connected to the output of the SU step-up converter. The compound efficiency with this connection is typically up to 90%.

CCDBST and CCDINV Converters

The MAX8858 includes high-voltage boost and inverting DC-DC converters to supply both positive and negative CCD (and/or LCD) bias. Both converters use a fixed-frequency, PWM, current-mode control scheme. The heart of the current-mode PWM controller is a comparator that compares the feedback error signal against the sum of the amplified current-sense signal and a slope compensation ramp. At the beginning of each clock cycle, the internal power switch turns on until the PWM comparator trips. During this time, the current in the inductor ramps up, storing energy in the inductor's magnetic field. When the power switch turns off, the inductor releases the stored energy while the current ramps down, providing current to the output. These converters operate at 667kHz switching frequency.

CCD Boost Converter (CCDBST)

The CCDBST high-voltage boost converter generates a positive output voltage up to 18V. An internal power switch, internal True Shutdown switch (between PVBST

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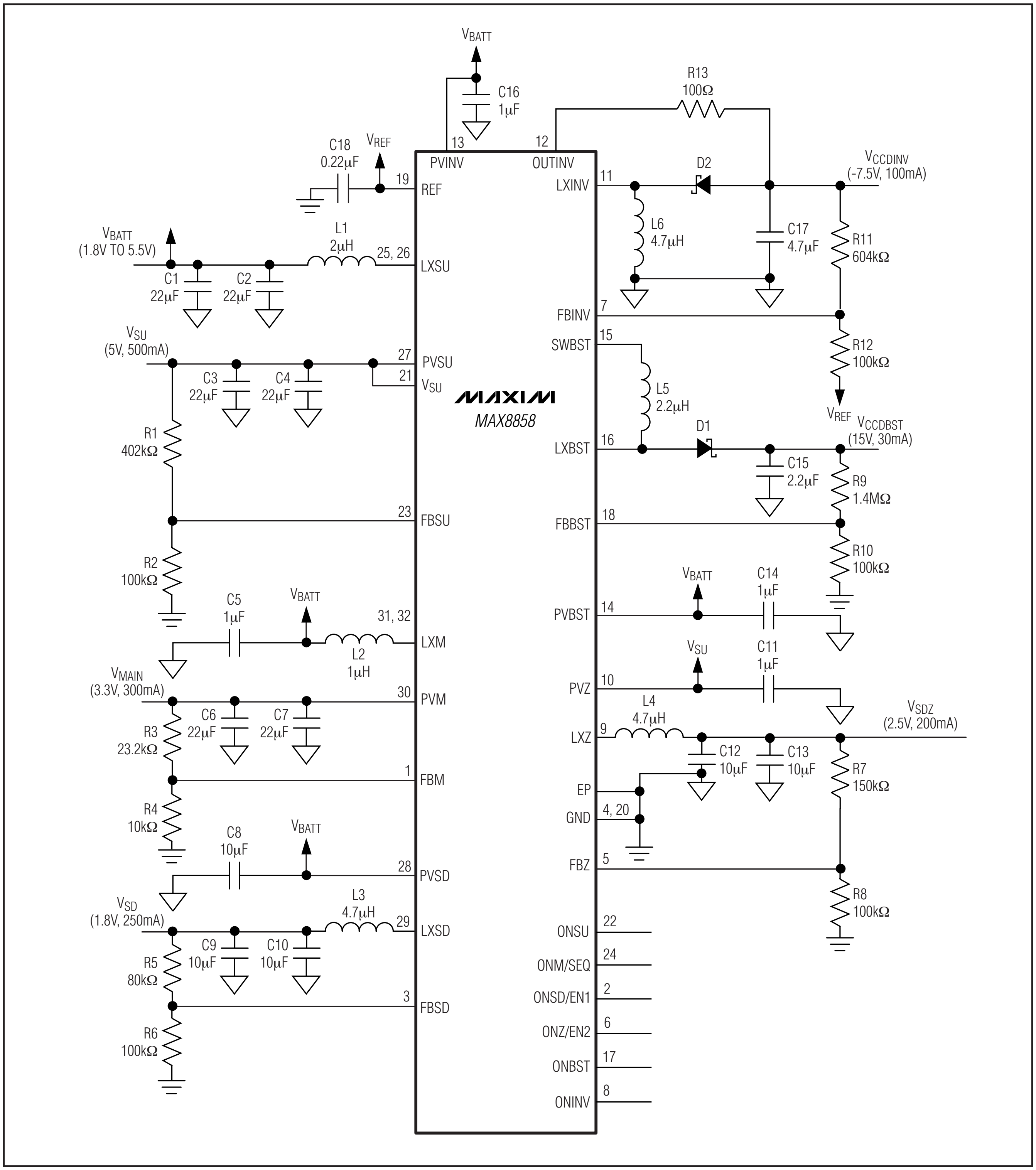

Figure 1. MAX8858 Typical Application Circuit

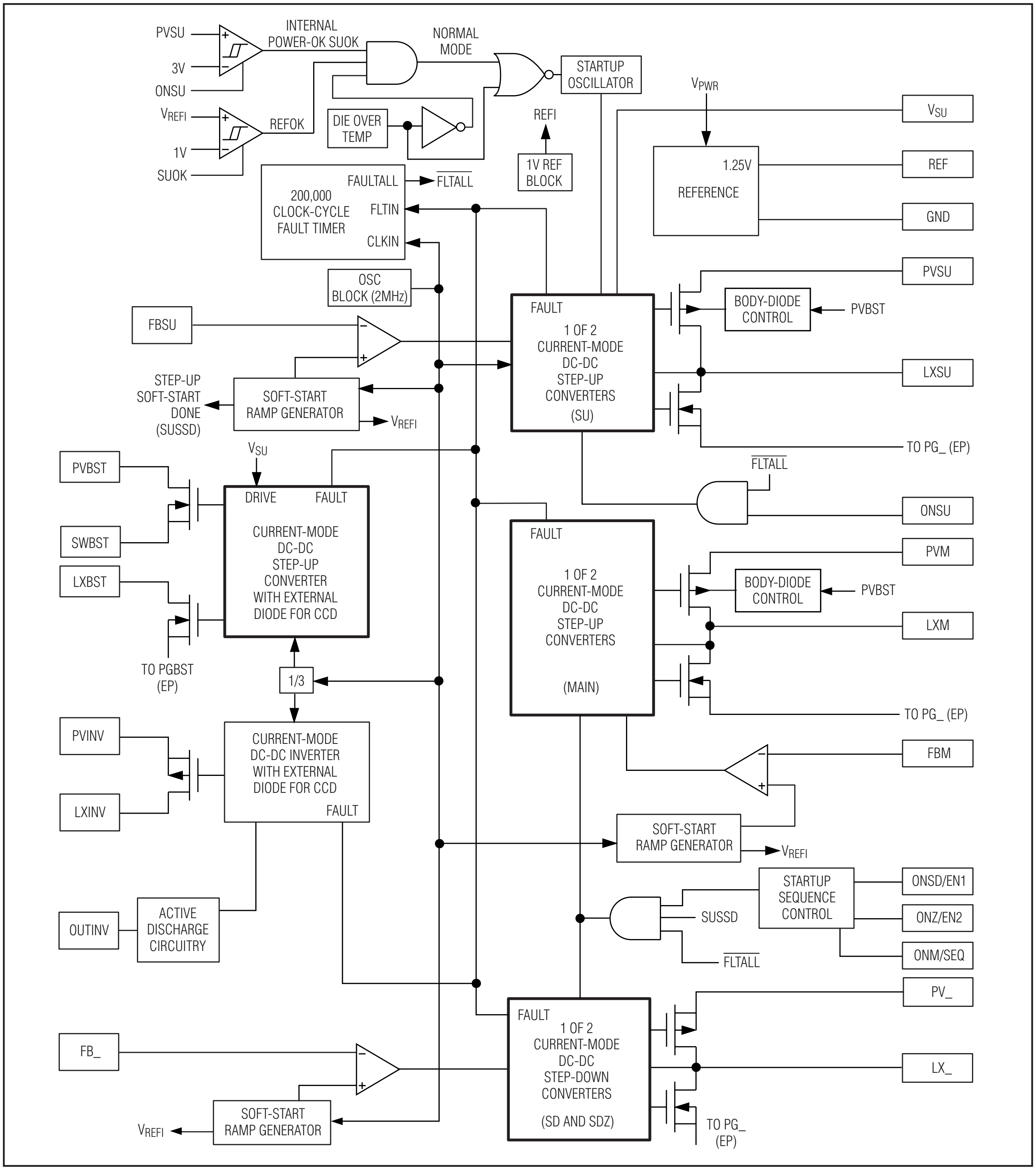

Figure 2. MAX8858 Functional Diagram

and SWBST), and external catch diode allow conversion efficiencies as high as 85%.

The internal True Shutdown switch disconnects the battery from the load by opening the battery connection to the inductor. The True Shutdown switch stays on at all times during normal operation. The CCDBST converter also features soft-start to limit inrush current and minimize battery loading at startup. This is accomplished by ramping the reference voltage at the input of the error amplifier. The boost reference is ramped from 0 to 1.02V (where 1.02V is the feedback voltage). During startup, the boost converter load switch turns on before the boost converter reference voltage is ramped up. This effectively limits startup inrush current to below 500mA and provides short-circuit protection.

CCD Inverter (CCDINV)

The CCDINV inverter generates output voltages down to V_{PVINV} - 16V. An internal power switch and external catch diode allow conversion efficiencies as high as 80%. The inverter soft-starts by ramping the reference input of the error amplifier from 1.25V to 0V (where 0V is the feedback voltage).

CCDINV Active Discharge

The CCDINV active-discharge circuitry pulls the CCDINV converter output to GND when ONINV is driven low. This active-discharge circuitry requires that the SU converter be on for 8ms, so that CCDINV has sufficient time to discharge to GND (see Figure 3). When a fault condition causes the SU converter to shut down, the active-discharge circuitry does not function, and CCDINV decays to GND through its feedback resistance. Install a 100Ω resistor between OUTINV and the INV output capacitor.

Power-Up Sequencing and On/Off Control (MAIN, SDZ, SD Converters)

The MAX8858 provides both preset power-up sequencing and independent on/off control of the MAIN, SDZ, and SD converters. The state of ONM/SEQ is sampled when V_{VSU} reaches regulation to determine whether a preset power-up sequence or independent on/off control is selected. Connect ONM/SEQ to V_{SU} before V_{VSU} reaches regulation to select a preset power-up sequence. Alternatively, connect ONM/SEQ to GND before V_{VSU} reaches regulation to select independent on/off control of the MAIN, SDZ, and SD converters.

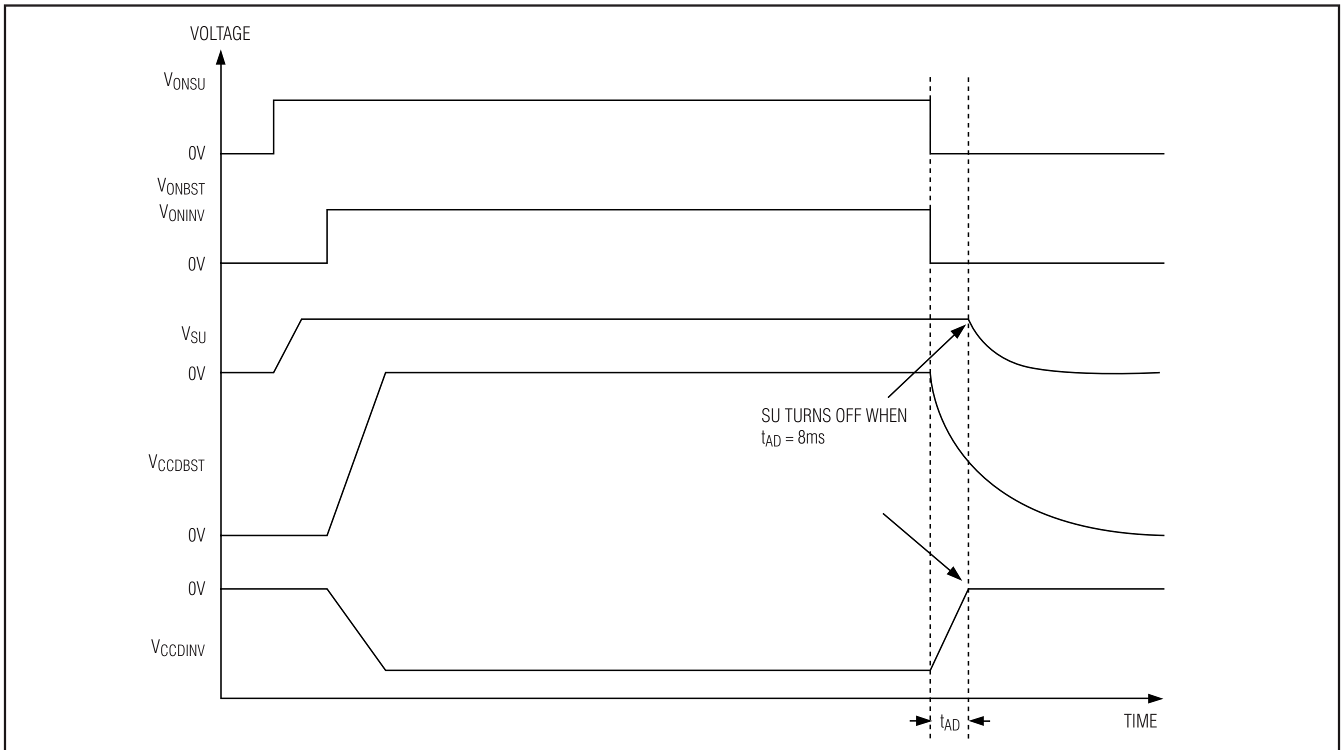

Figure 3. CCDINV Active Discharge

If ONM/SEQ = V_{SU} when V_{VSU} reaches regulation, a preset power-up sequence is selected. ONSD/EN1 and ONZ/EN2 determine which power-up sequence is selected. If ONSD/EN1 is driven high, power-up sequence 1 is selected, where the SDZ converter powers up first, followed by the SD converter, and finally, the MAIN converter (see Table 1 and Figure 4). If ONZ/EN2 is driven high, power-up sequence 2 is selected, where the SD converter powers up first, followed by the SDZ converter, and finally, the MAIN converter (see Table 1 and Figure 5). In both cases, the power-down sequence is the opposite of the power-up sequence, and each converter output is actively discharged.

If ONM/SEQ = GND when V_{VSU} reaches regulation, independent control of the MAIN, SDZ, and SD converters is enabled. After V_{VSU} reaches regulation, ONM/SEQ, ONSD/EN1, and ONZ/EN2 control the on/off behavior of the MAIN, SD, and SDZ converters, respectively (see Table 1 and Figure 6). Each converter provides active-discharge circuitry, so that each output pulls to GND when its respective ON_ input is driven low.

Soft-Start

All DC-DC converter channels feature soft-start to limit inrush current and prevent excessive battery loading at startup by ramping each channel to the regulation voltage. This is accomplished by ramping the internal reference inputs to each channel error amplifier when a channel is enabled.

The soft-start ramps for most channels take approximately 7.5ms. The exceptions are the SD/SDZ step-down converters. For the SDZ converter, the soft-start ramp takes 1.25ms, while for the SD converter, the soft-start ramp takes 2.5ms. The soft-start time for SD is shorter relative to other channels because SD typically has a lower output voltage. The soft-start time for SDZ is even shorter to ensure that when ONZ and ONSD are tied together, SDZ comes into regulation first followed by the SD converter. Since MAIN and SU are step-up converters, their soft-start time is load dependent, but does not exceed 7.5ms. Note, however, that no converters start until the SU step-up converter reaches regulation.

Table 1. Power-Up Sequencing and On/Off Control

ONM/SEQ STATE AT V_{SU} POWER-UP*	INPUT STATES AFTER V_{SU} POWER-UP			MAX8858 STARTUP BEHAVIOR
	ONSD/EN1	ONZ/EN2	ONM/SEQ	
0	0	0	0	Independent control. All converters are off.
0	0	0	1	Independent control. Only the MAIN converter turns on.
0	0	1	0	Independent control. Only the SDZ converter turns on.
0	0	1	1	Independent control. The SDZ and MAIN converters turn on.
0	1	0	0	Independent control. Only the SD converter turns on.
0	1	0	1	Independent control. The SD and MAIN converters turn on.
0	1	1	0	Independent control. The SD and SDZ converters turn on.
0	1	1	1	Independent control. All converters turn on.
1	0	0	Don't care	Preset power-up sequence. No sequence selected, all converters off.
1	0	1	Don't care	Preset power-up sequence. Power-up sequence 2 selected (see Figure 5).
1	1	0	Don't care	Preset power-up sequence. Power-up sequence 1 selected (see Figure 4).
1	1	1	Don't care	Preset power-up sequence. No sequence selected, all converters off.

**The logic state of ONM/SEQ at the time that the SU converter reaches regulation determines whether a preset power-up sequence or independent on/off control is selected.*

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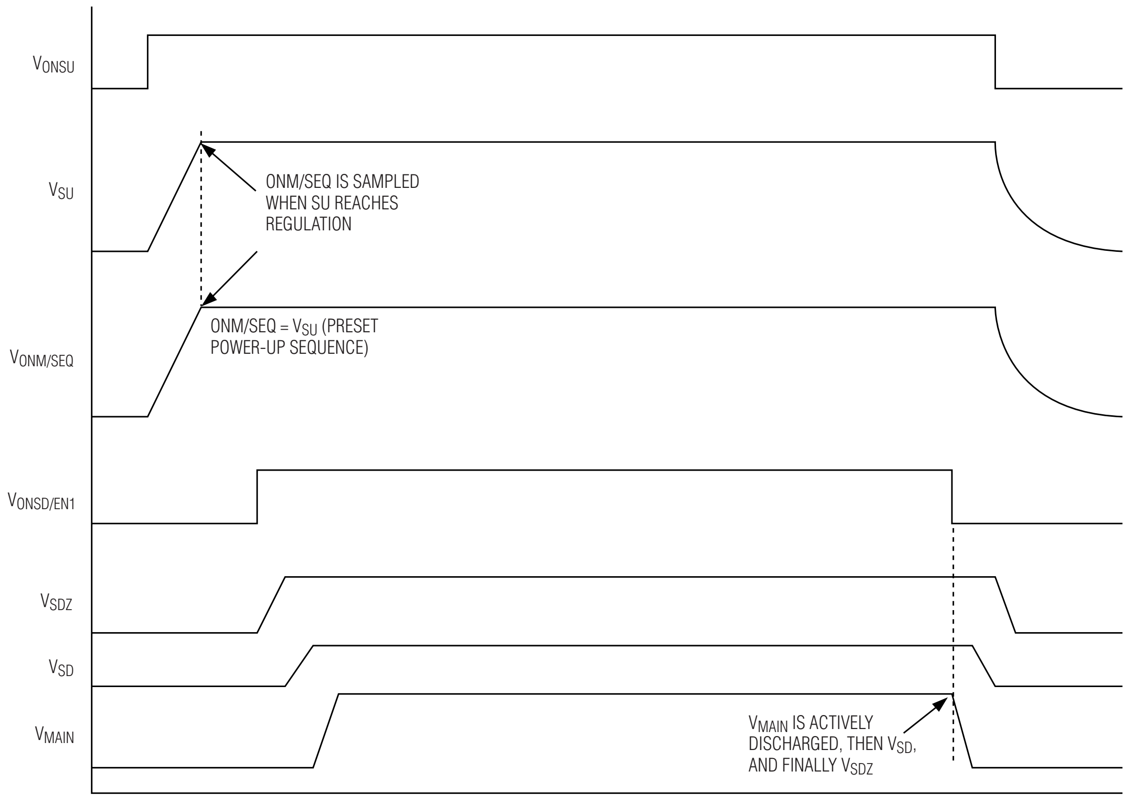

Figure 4. Power-Up Sequence 1

Reference

The MAX8858 has a precise 1.250V voltage reference at REF. Bypass REF to GND with a 0.22µF ceramic capacitor. REF can source up to 100µA for external loads. REF is internally pulled to GND during shutdown.

Oscillator

The operating frequency is internally set to 2MHz. Note that although all converter channels are synchronized, they do not operate at the same frequency. The SU, MAIN, SD, and SDZ converters all operate at 2MHz, while the CCDBST and CCDINV converters operate at 667kHz to optimize efficiency.

Fault Protection

The MAX8858 has robust fault and overload protection. After power-up, the device monitors for an out-of-regulation state such as an overload or short-circuit condition. If any DC-DC converter remains faulted for 100ms, all outputs latch off until the SU step-up DC-DC converter is reinitialized by toggling ONSU or recycling power to the IC. If the SU output falls 10% below its regulation voltage or is shorted, the device enters a fault state immediately. The device then shuts down all outputs. All outputs stay latched off until the SU DC-DC converter is reinitialized by toggling ONSU or by cycling power to the IC.

If the short circuit at SU exists before IC power-up, the SU step-up converter goes through soft-start once (30ms) and then latches off, since V_{VSU} never reaches regulation. The part draws about 1A of input current during the soft-start period. The MAX8858 limits the time under this condition to prevent thermal runaway. Cycling ONSU or power to the IC reinitiates the soft-start sequence for the SU step-up converter.

An overload/short-circuit condition in the CCDBST converter stops switching in the CCDBST converter immediately. The True Shutdown switch limits the inductor current for 100ms. If the overload/short-circuit condition persists beyond this time, the device enters a fault condition. All channels are shut down and stay latched off

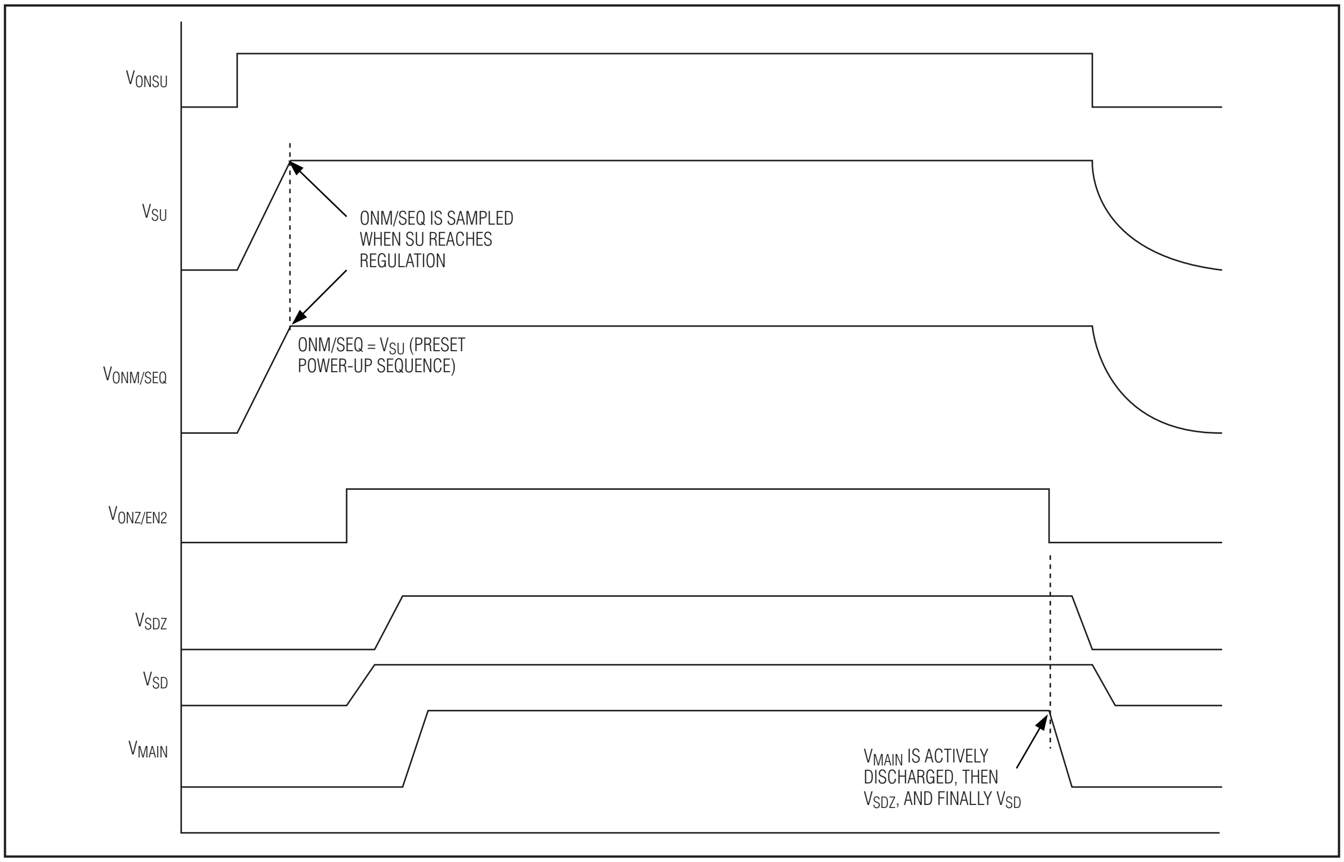

Figure 5. Power-Up Sequence 2

until the SU step-up DC-DC converter is reinitialized by toggling ONSU or recycling power to the IC. If the overload/short-circuit condition is removed within 100ms, soft-start is reinitiated.

For all other outputs, if an overload/short-circuit condition exists for over 100ms on the output, a fault condition occurs. Once in fault, all outputs are shut down and stay latched off until the SU step-up DC-DC converter is reinitialized by toggling ONSU or recycling power to the IC.

Shutdown

The SU step-up converter is activated with a logic-high input signal at ONSU. All other converters are individually activated with logic-high levels on their respective ON_ inputs. For automatic startup of any channel, connect the corresponding ON_ to PVSU or a logic level greater than 1.4V. To select a preprogrammed power-up sequence, see the *Power-Up Sequencing and ON/OFF Control (MAIN, SDZ, SD Converters)* section for details. Driving all ON_ inputs (or ONSU) logic-low places the MAX8858 in shutdown mode and reduces supply current to 0.1µA.

In shutdown, the control circuitry, internal switching MOSFETs, and synchronous rectifiers turn off and LX_ becomes high impedance.

In conventional boost circuits, the body diode of the synchronous rectifier or external Schottky diode is forward biased in shutdown and allows current flow from the input to the output. Some form of external switch and circuit needs to be used to avoid this current path during the shutdown of the converter. The MAX8858 eliminates the need of external circuitry on all six converter channels, providing True Shutdown.

Design Procedure

Setting Output Voltages

All MAX8858 output voltages are set with resistive voltage-dividers. Connect a resistive voltage-divider from the converter's output to the corresponding FB_ input and then to GND (except for FBINV) to set the output voltage. The FB_ threshold is 1.015V for all channels except for FBBST (1.02V) and FBINV (0V). The FB_ input

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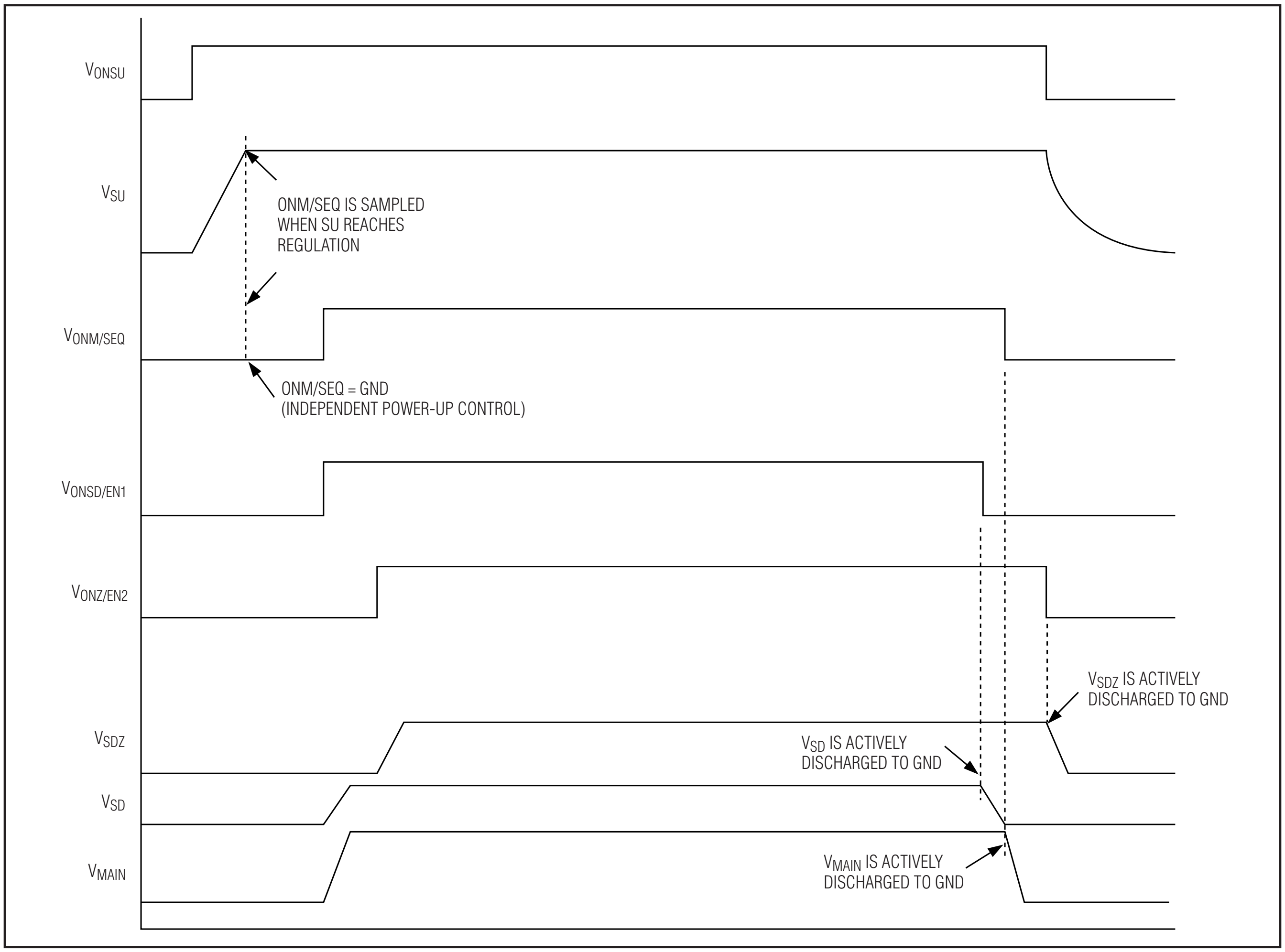

Figure 6. Independent Power-Up Sequence

bias current is less than 50nA, so choose the bottom-side (R_{BOTTOM} from FB_-to-GND) resistor to be 100kΩ or less. Then calculate the top-side (R_{TOP} from output-to-FB_) resistor:

$$R_{TOP} = R_{BOTTOM}[(V_{OUT}/V_{FB\_}) - 1]$$

where $V_{FB\_}$ is the feedback regulation voltage of the particular DC-DC converter channel.

Setting Inverter Output Voltage

The MAX8858 features a CCD inverter. The CCD inverter feedback input (FBINV) has a threshold of 0V. Connect a resistive voltage-divider from the negative output (V_{CCDINV}) to the FBINV input, and then to REF to set the negative output voltage. The FBINV input bias current is less than 50nA, so choose the FBINV-to-REF resistor, R_{REF} (R12 in Figure 1) to be 100kΩ or less. Then calculate the output-to-FBINV resistor, R_{INV} (R11 in Figure 1), as follows:

$$R_{INV} = R_{REF} (|V_{CCDINV}|/1.25V)$$

Filter Capacitor Selection

The input capacitor in a DC-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source.

The DC-DC converter output filter capacitors keep output ripple small and ensure control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and low-ESR

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tantalum capacitors are suitable, with ceramic capacitors exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$$V_{RIPPLE} = I_{L(PEAK)} \times [1/(2\pi f_{OSC} C_{OUT})]$$

The ESR of the output capacitor is significant and can affect control-loop stability. It is recommended to use capacitors with an ESR less than 50mΩ.

Step-Up Component Selection

This section describes component selection for the SU and MAIN step-up converters. The external components required for the step-up converters are an inductor and input and output filter capacitors. The inductor is typically selected to operate with continuous current for best efficiency. An exception might be if the step-up ratio, (V_{OUT}/V_{IN}), is greater than $1/(1 - D_{MAX})$, where D_{MAX} is the maximum PWM duty factor stated in the *Electrical Characteristics* table.

In most step-up designs, a reasonable inductor value (L_{IDEAL}) can be derived from the following equation that sets continuous peak-to-peak inductor current at 1/3 the DC inductor current:

$$L_{IDEAL} = [3.5 \times V_{IN(MIN)} \times D \times (1 - D)]/(I_{OUT} \times f_{OSC})$$

where D is the duty factor given by:

$$D = 1 - (V_{IN}/V_{OUT})$$

Given L_{IDEAL}, the continuous mode peak-to-peak inductor current is $I_{OUT}/[3(1 - D)]$. The peak inductor current, $I_{L(PEAK)} = 1.25 \times I_{OUT}/(1 - D)$. Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises and a larger output capacitance might be required to suppress output ripple.

In the current-mode step-up converter, the output capacitor affects the control-loop stability. A 2µH inductor with 2x 22µF output capacitors is recommended for optimum performance in the SU step-up converter in the MAX8858. Use a 1µH inductor for the MAIN step-up converter.

Step-Down Component Selection

This section describes component selection for the SDZ and SD step-down converters. The external components required for a step-down converter are an inductor and input and output filter capacitors. The step-down converters provide best efficiency with continuous inductor current. A reasonable inductor value (L_{IDEAL}) can be derived from the following equation:

$$L_{IDEAL} = [3 \times V_{IN} \times D_{SD} \times (1 - D_{SD})]/(I_{OUT} \times f_{OSC})$$

This sets the peak-to-peak inductor current at 1/3 the DC inductor current. D_{SD} is the step-down switch duty cycle:

$$D_{SD} = V_{OUT}/V_{IN}$$

Given L_{IDEAL}, the peak-to-peak inductor current is $I_{OUT}/3$. The absolute-peak inductor current is $1.17 \times I_{OUT}$. Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises and a larger output capacitance might required to suppress output ripple. Larger values than L_{IDEAL} can be used to obtain higher output current, but typically with a physically larger inductor.

CCD Component Selection

CCD Inductor Selection

The high-switching frequency of CCDBST and CCDINV converters allows for the use of small inductors. The L5 and L6 inductors in Figure 1 are recommended for most applications. Use inductors with a ferrite core or equivalent. Powdered-iron cores are not recommended for use with high-switching frequencies. The inductor's saturation rating must meet or exceed the LXBST and LXINV current limits. For highest efficiency, use inductors with a low DC resistance. Table 2 lists recommended inductors for the CCD outputs.

CCD Diode Selection

High switching frequencies demand a high-speed rectifier. Schottky diodes, such as the CMHSH5-4 or MBR0530L, are recommended for best performance. Ensure that the diode's peak current rating exceeds the specified current limit, and that its breakdown voltage exceeds the output voltage. Schottky diodes are preferred due to their low-forward voltage. However, ultra-high-speed silicon rectifiers are also acceptable.

CCDBST and CCDINV Output Filter Capacitors

For most applications, 2.2µF and 10µF ceramic output filter capacitors are suitable for the CCDBST and CCDINV outputs, respectively. Lower values might be acceptable to save space at low output currents or if higher ripple can be tolerated. The minimum capacitor values required for stability are calculated as follows:

For CCDBST output stability, the filter capacitor, C_{BST}, should satisfy:

$$C_{BST} > (10 \times L \times I_{BST})/(R_{CS} \times (1 - D_{BST}) \times V_{BST}^2)$$

where I_{BST} is the output current, V_{BST} is the output voltage, $R_{CS} = 0.015\Omega$, and D_{BST} is the boost switch duty cycle:

$$D_{BST} = 1 - (V_{PVBST}/V_{BST})$$

Table 2. CCD Inductor Selection Guide

OUTPUT VOLTAGE AND LOAD CURRENT	INDUCTOR	L (µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (mm)
15V, 50mA -7.5V, 100mA	TOKO DE2818C 1072AS-100M	10	150	0.95	3.0 x 3.2 x 1.8
	TOKO DP418C S1024AS-100M	10	100	0.92	4.2 x 4.2 x 1.8
	TOKO DE2818C 1072AS-4R7M	4.7	70	1.3	3.0 x 3.2 x 1.8
15V, 20mA -7.5V, 40mA	TOKO DE2818C 1072AS-2R2M	2.2	40	1.5	3.0 x 3.2 x 1.8
	TDK MLP2520S2R2M	2.2	80	1.3	2.5 x 2.0 x 1.0
	TDK MLP2520S4R7L	4.7	110	1.1	2.5 x 2.0 x 1.0

For CCDINV stability, the filter capacitor, C_{INV}, should satisfy the following:

$$C_{INV} > (3 \times L \times V_{REF} \times I_{INV})/(R_{CS} \times (1 - D_{INV}) \times (V_{REF} - V_{INV}) \times V_{INV})$$

where I_{INV} is the output current, V_{INV} is the output voltage, R_{CS} = 0.015Ω, and D_{INV} is the inverter switch duty cycle:

$$D_{INV} = |V_{INV}|/(|V_{INV}| + V_{PVINV})$$

Applications Information

Figure 1. Two-AA/NiMH-Battery Operation

Figure 1 is optimized for 2-cell alkaline or NiMH inputs (1.5V to 3.6V). The SU step-up converter generates 5V. The 1.8V supply for the DSP core is stepped down from the battery input. The -7.5V for CCDINV and +15V for the CCDBST are derived directly from the battery.

Designing a PCB

Good PCB layout is critical to achieve optimal performance from the MAX8858. Poor board design can cause excessive conducted and/or radiated noise. Conductors carrying discontinuous currents and any high-current path should be made as short and wide as possible. LX_ nodes should be made as small as possible to reduce radiated noise.

Input capacitors for step-down converters (PVSD and PVZ) and output capacitors for step-up converters (PVSU and PVM) should be connected from their respective PV_ terminals to the exposed pad (PG_) with minimal trace length to minimize loop area. Each converter should have its own power ground plane, where the input and output bypass capacitors and inductors (INV) are grounded together to minimize crosstalk between converters. Connect all converters' power ground planes together at the exposed pad.

Create a separate low-noise analog ground plane for the reference bypass capacitor ground terminal and the feedback resistor grounds. Connect the low-noise analog ground plane to the power-ground plane at a single point (exposed pad) to minimize the effects of power-ground currents.

Place the reference bypass capacitor as close as possible to the REF and AGND pins for best performance. Feedback resistors should be placed as close as possible to the device with FB_ nodes routed away from LX_ traces to maximize noise immunity.

Refer to the MAX8858 Evaluation Kit for a PCB layout example.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 Thin QFN-EP	T3255+5	21-0140