19-3000; Rev 1; 2/04

MAX5865 Evaluation Kit

Evaluates: MAX5863/MAX5864/MAX5865

General Description

The MAX5865 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX5865 40Msps analog front end. The MAX5865 integrates a dual-channel analog-to-digital converter (ADC), a dual-channel digital-to-analog converter (DAC), and a 1.024V internal voltage reference. The EV kit board accepts AC- or DC-coupled, differential or single-ended analog inputs for the receive ADC and includes circuitry that converts the transmit DAC differential output signals to single-ended analog outputs. The EV kit includes circuitry that generates a clock signal from an AC sine wave input signal. The EV kit operates from a +3.0V analog power supply, +3.0V digital power supply, and ±5V bipolar power supply.

The EV kit comes with Windows® 98/2000/XP-compatible software that provides an interface to exercise the features of the MAX5865. The program is menu driven and offers a graphical user interface (GUI) with control buttons and status displays. The GUI is used to control the MAX5865 SPI-compatible serial interface.

The MAX5865 EV kit evaluates the 22Msps MAX5864 or the 7.5Msps MAX5863 analog front end (IC replacement is required).

Windows is a registered trademark of Microsoft Corp.

Features

- **Quick Dynamic Performance Evaluation**
- **50Ω Matched Clock Input and Analog Signal Lines**
- **Single-Ended to Fully Differential Analog Input Signal Configuration**
- **Differential to Single-Ended Output Signal-Conversion Circuitry**
- **AC- or DC-Coupled Input Signals Configuration**
- **SMA Coaxial Connectors for Clock Input, Analog Inputs, and Analog Output**
- **On-Board Clock-Shaping Circuit**
- **High-Speed PC Board Design**
- **Fully Assembled and Tested**
- **Windows-Compatible Software**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX5865EVKIT	0°C to +70°C	48 Thin QFN-EP*

**EP = Exposed pad.*

Part Selection Table

PART	MAXIMUM SAMPLING SPEED (Msps)
MAX5863ETM	7.5
MAX5864ETM	22
MAX5865ETM	40

MAX5865 EV Kit Software Files

PROGRAM	DESCRIPTION
INSTALL.EXE	Installs the EV kit software
MAX5865.EXE	Application program
HELPFILE.HTM	MAX5865 EV kit Help file
PORT95NT.EXE	SST's freeware DLPortIO driver
IMAGE 1.GIF	Interface figure
UNINST.INI	Uninstalls the EV kit software

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
Kemet	864-963-6300	864-963-6322	www.kemet.com
Murata	770-436-1300	770-436-3030	www.murata.com
Pericom	800-435-2336	408-435-1100	www.pericom.com
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Texas Instruments	972-644-5580	214-480-7800	www.ti.com

Note: *Please indicate that you are using the MAX5865 when contacting these component suppliers.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C8	8	0.1µF ±10%, 10V X5R ceramic capacitors (0402) Taiyo Yuden LMK105BJ104KV or TDK C1005X5R1A104K
C9–C15, C27, C68–C71	12	2.2µF ±10%, 10V X5R ceramic capacitors (0603) Taiyo Yuden JMK107BJ225KA or TDK C1608X5R0J225K
C16–C19	4	22pF ±5%, 50V C0H ceramic capacitors (0402) Murata GRP1555C1H220J or Taiyo Yuden UMK105CH220JW
C20, C21, C22, C26	4	1000pF ±10%, 50V X7R ceramic capacitors (0402) Taiyo Yuden UMK105BJ102KW or TDK C1005X7R1H102KT
C23, C24, C25	3	0.33µF ±10%, 10V X5R ceramic capacitors (0603) Taiyo Yuden LMK107BJ334KA
C28–C34, C36–C39, C41–C55, C66, C67	28	0.1µF ±10%, 25V X7R ceramic capacitors (0603) Murata GRM188R71E104K or TDK C1608X7R1E104K
C56–C59	0	Not installed, ceramic capacitors (0402)
C60–C65	6	10µF ±10%, 10V tantalum capacitors (A) AVX TAJA106K010R or Kemet T494A106K010AS
IA, IAP, IAN, QA, QAP, QAN, CLOCK, ID, QD	9	SMA PC-mount vertical connectors
J1, J2, J3	3	2 x 10 pin headers
J4	1	DB25 right-angle male plug
JU1–JU8	8	3-pin headers
JU9, JU10, JU11	3	2-pin headers
L1	1	Ferrite bead (1206) Panasonic EXC-CL3216U1

DESIGNATION	QTY	DESCRIPTION
R1–R4	4	24.9Ω ±1% resistors (0402)
R5–R9	5	2kΩ ±1% resistors (0603)
R10, R11	2	4.02kΩ ±1% resistors (0603)
R12	1	6.04kΩ ±1% resistor (0603)
R13	1	5kΩ ±10% 1/4in potentiometer, 12 turn
R14–R21	8	10kΩ ±1% resistors (0603)
R22–R25	0	Not installed resistors (0402)
R26, R27, R28, R36, R71–R80	0	Not installed resistors (0603)
R29–R35	7	49.9Ω ±1% resistors (0603)
R37–R44	8	100Ω ±5% resistors (0603)
R45–R66, R70	23	51Ω ±5% resistors (0603)
R67, R68, R69	3	10kΩ ±5% resistors (0603)
T1, T2	2	Transformers (1:1) Coilcraft TTWB3010-1
U1	1	MAX5865ETM (48-pin thin QFN-EP)
U2	1	Dual-CMOS differential line receiver (8-pin SO) Maxim MAX9113ESA
U3, U4	2	Low-jitter operational amplifiers (8-pin SO) Maxim MAX4108ESA
U5	1	Buffer/driver tri-state output (48-pin TSSOP) Texas Instruments SN74ALVCH16244DGGR or Pericom PI74ALVCH16244A
U6	1	Hex buffer/driver (14-pin TSSOP) Texas Instruments SN74LV07APWR
None	1	MAX5865 PC board
None	1	Software CD-ROM disk MAX5865 EV kit
None	11	Shunts (JU1–JU11)

Quick Start

Recommended Equipment

- Two +3.0VDC power supplies
- Two +2.0VDC power supplies
- One ±5.0V bipolar DC power supply
- One function generator with low phase noise and low jitter for clock input (e.g., HP 8662A)
- Two function generators for single-ended analog inputs (e.g., HP 8662A)
- One 10-bit digital pattern generator for data inputs (e.g., Tektronix DG2020A)
- Two spectrum analyzers (e.g., HP 8560E)
- One logic analyzer or data-acquisition system (e.g., HP 1663EP, HP 16500C)
- Voltmeter
- Oscilloscope
- MAX5865 evaluation software
- Windows 98/2000/XP computer with a spare printer port
- 25-pin female-to-male I/O extension cable
- Analog input filters (select appropriate ADC input filters per application specific)

Procedure

The MAX5865 EV kit is a fully assembled and tested surface-mount board. Follow the steps below for proper board operation. **Do not turn on power supplies or enable signal generators until all connections are completed:**

1) Verify that shunts are installed across pins 1 and 2 of jumpers JU1, JU2, JU3, and JU4 (single-ended analog signals IA and QA converted to differential input signals with transformers T1 and T2).
2) Verify that shunts are installed across pins 2 and 3 of jumpers JU5, JU6, JU7, and JU8 (differential analog output signals converted to single-ended signals ID and QD with operational-amplifier circuits U3 and U4).
3) Verify that no shunts are installed across jumpers JU9 and JU10.
4) Verify that a shunt is installed across jumper JU11 (internal reference).
5) Connect the 25-pin I/O extension cable from the computer's parallel port to the MAX5865 EV kit board DB25 right-angle male plug J4. The EV kit software uses a loopback connection to confirm that the correct port has been selected.
6) Install the evaluation software on your computer by running the INSTALL.EXE program on the CD-ROM. The program files are copied and icons are created for them in the Start menu.
7) Connect the clock-function signal generator (HP 8662A) to the CLOCK SMA connectors on the EV kit.
8) Connect the two function generators to SMA connectors IA and QA.
9) Synchronize the two function generators to the clock function generator.
10) Connect the logic analyzer to the 2 x 10 square pin header J1. The CLOCK signal is available on pin J1-2 and bits DA0–DA7 are available on the even pins J1-4 to J1-18. All other header J1 pins are connected to ground. The clock pin and data pins are labeled CLK and DA0–DA7 on the EV board.
11) Verify that the logic analyzer is programmed for an 8-bit input at CMOS voltage levels.
12) Verify that the 10-bit digital pattern generator is programmed for valid CMOS output voltage levels.
13) Connect the digital pattern generator DG2020A output to the J3 input header connector on the EV kit board. The input header pins are labeled for proper connection with the digital pattern generator (i.e., connect bit 0 to the J3-19 header pin labeled DD0, connect bit 1 to the J3-17 header pin labeled DD1, etc. Input data pins are the odd pins of header J3. All other pins are connected to ground).
14) Synchronize the digital pattern generator with the clock function generator.
15) Connect a +3.0V power supply to the VDD pad. Connect the ground terminal of this supply to the GND pad.
16) Connect a +3.0V power supply to the VCLK pad. Connect the ground terminal of this supply to the GND pad.
17) Connect a +2.0V power supply to the OVDD pad. Connect the ground terminal of this supply to the OGND pad.
18) Connect a +2.0V power supply to the VDDRV pad. Connect the ground terminal of this supply to the OGND pad.
19) Connect the +5.0V terminal of the bipolar power supply to the VCC pad. Connect the ground terminal of this supply to the GND pad.

20) Connect the -5.0V terminal of the bipolar power supply to the VEE pad.

21) Turn on the five power supplies.

22) Probe resistor pad R28 with an oscilloscope and adjust potentiometer R13 to set the clock duty cycle to 50%.

23) Start the MAX5865 program by opening its icon in the Start menu.

24) Click on the **Xcvr control command** to set the MAX5865 in receive/transmit (transceiver) operational mode.

25) Enable the clock function generator (HP 8662A). Set the clock function generator output power to $2.4V_{P-P}$ (11.6dBm) and the frequency (f_{CLK}) to greater than 22MHz but less than or equal to 40MHz.

26) Enable the function generators.

27) Set the IA function-generator output signal to $1.024V_{P-P}$ and the frequency to ≤ $f_{CLK}/2$.

28) Set the QA function-generator output signal to $1.024V_{P-P}$ and and the frequency to ≤ $f_{CLK}/2$.

29) Use the logic analyzer to analyze the 8-bit ADC digital output. The IA channel digital data is available on the falling edge of the clock. The QA digital data is available on the rising edge of the clock. Ensure that the ADC input is not overdriven by observing the output digital codes and adjusting the input signal level for code of -0.5dB full scale.

30) Enable the digital pattern generator. Program the digital pattern generator to transmit the digital data for the DAC I channel on the falling edge of the clock and transmit the digital data for the Q channel on the rising edge of the clock.

31) Connect the spectrum analyzers to the ID and QD SMA connectors to analyze the analog outputs.

32) Use the spectrum analyzer to analyze the analog output spectrum or view the analog output waveforms using an oscilloscope.

Detailed Description of Software

The evaluation software's main window (shown in Figure 1) can be used to program the MAX5865 to one of the six operational modes: shutdown, idle, receive (Rx), transmit (Tx), transceiver (Xcvr), and standby.

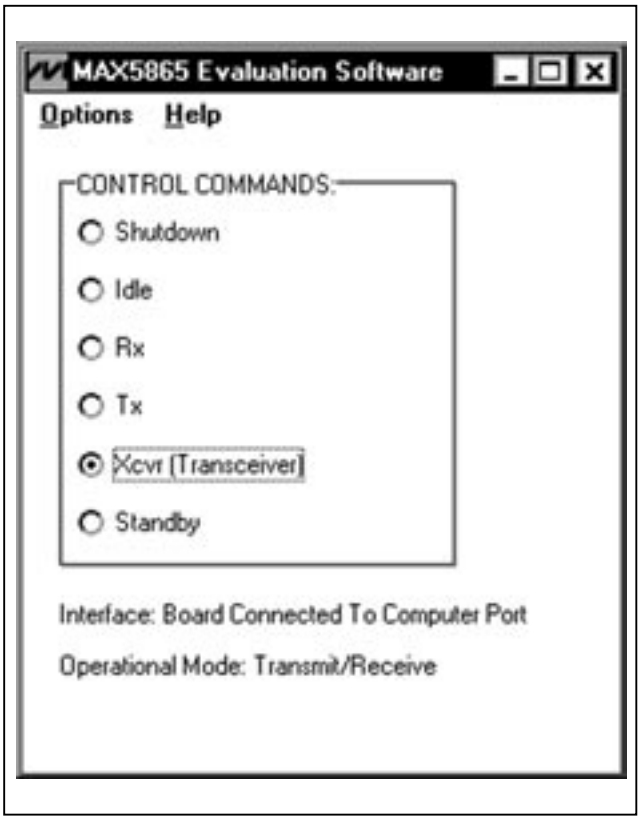

Figure 1. MAX5865 EV Kit Software Main Window

Click one of the buttons to program the MAX5865 to the desired operational mode after power has been applied to the EV kit. Use the keyboard arrow keys to cycle through the control commands. See Table 1 for the description of each operational mode.

The MAX5865 evaluation software uses a 3-wire bit-banging interface that is compatible with SPI™/ QSPI™/ MICROWIRE™/DSP interfaces to program the MAX5865 through the parallel port on the computer. Table 1 lists the byte command for each operational mode.

Detailed Description of Hardware

The MAX5865 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX5865, MAX5864, or

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MICROWIRE is a trademark of National Semiconductor Corp.

Table 1. Operational Modes

MODE	EV KIT FUNCTION	COMMAND BYTE SENT TO MAX5865
Shutdown	Device shutdown. REF is off, ADCs are off, the ADC bus is tri-stated, and DACs are off. The DAC input bus must be set to zero or OV_{DD} to achieve the lowest shutdown-mode power consumption.	xxxx x000
Idle	REF is on, ADCs are off, the ADC bus is tri-stated, and DACs are off. The DAC input bus must be set to zero or OV_{DD} to achieve the lowest Idle Mode™ power consumption.	xxxx x001
Receive (Rx)	REF is on, ADCs are on, and DACs are off. The DAC input bus must be set to zero or OV_{DD} to achieve the lowest Rx-mode power consumption.	xxxx x010
Transmit (Tx)	REF is on, ADCs are off, the ADC bus is tri-stated, and DACs are on.	xxxx x011
Transceive (Xcvr)	REF is on, ADCs and DACs are on.	xxxx x100
Standby	REF is on, ADCs are off, the ADC bus is tri-stated, and DACs are off. The DAC input bus must be set to zero or OV_{DD} to achieve the lowest standby-mode power consumption.	xxxx x101

x = Don't care

MAX5863 analog front end. The MAX5863/MAX5864/MAX5865 integrate a 1.024V temperature-stable voltage reference, a dual-input 8-bit parallel-output receive ADC, and a 10-bit parallel-input dual-output transmit DAC. The MAX5863/MAX5864/MAX5865 accept AC-coupled or DC-coupled, differential, or single-ended analog inputs at the receive ADC. The digital output produced by the ADC can be easily captured with a high-speed logic analyzer or data-acquisition system. The MAX5863/MAX5864/MAX5865 digital inputs at the transmit DAC are designed for CMOS-compatible voltage levels. The DAC produces differential analog outputs with 1.4VDC common mode.

The EV kit comes with the MAX5865 installed, which operates at speeds of up to 40Msps. The EV kit operates from a +3.0V analog power supply, +3.0V digital power supply, and ±5V bipolar operational amplifier power supply. For best dynamic performance, set the digital power supply to +2V. The EV kit includes circuitry that generates a clock signal from an AC sine wave provided by the user. Other features include: circuitry to convert single-ended inputs to differential input analog signals and circuitry to convert the differential outputs of the DAC to single-ended analog signals. The MAX5865 EV kit can be used to evaluate the 22Msps MAX5864 or the 7.5Msps MAX5863 after replacing the MAX5865.

Idle Mode is a trademark of Maxim Integrated Products, Inc.

Power Supplies

The MAX5865 EV kit can operate from a single +3.0V power supply connected to the VDD, OVDD, VCLK, and VDDRV input power pads and their respective ground pads for simple board operation. An additional ±5V bipolar power supply is needed at VCC and VEE when the operational-amplifier differential to single-ended output circuitry (U3 and U4) is used. See the *Transmit Dual DAC Outputs* section for further details. However, two +3.0V (VDD and VCLK) and two +2V (OVDD and VDDRV) power supplies are recommended for best dynamic performance. The EV kit PC board ground layer is divided into two sections: digital (OGND) and analog (GND). The EV kit PC board power plane is divided into four sections: VDD (MAX5865 analog circuit), OVDD (MAX5865 output driver circuit), VCLK (clock-shaping circuit U2), and VDDRV (digital components U5 and U6). VDD, VCLK, VCC, and VEE inputs are referenced to analog ground GND. OVDD and VDDRV inputs are referenced to the OGND ground. Using separate power supplies for each input section reduces crosstalk noise and improves the integrity of the output signals. Another advantage of using separate power supplies is that the input power sources do not have to be at the same voltage level for the EV kit circuit to operate normally. VDD has a +2.7V to +3.3V input range, OVDD has a +1.8V to VDD input range, VCLK has a +2.7V to +3.3V input range , and VDDRV has a +2.0V to +3.3V input range.

Clock Signal

An on-board clock-shaping circuit generates a clock signal from an AC sine wave signal applied to the CLOCK SMA connector. The input clock signal should not exceed a magnitude of 2.6V_{P-P}. The frequency of the signal determines the sampling frequency (f_{CLK}) of the MAX5865 EV kit circuit and should not exceed 40MHz. The differential line receiver (U2) processes the input signal to generate the CMOS clock signal. The clock signal's duty cycle can be adjusted with potentiometer R13. A 50% duty cycle is recommended. The clock signal is available at the J1-2 header pin (CLK) and can be used as the external clock for the logic analyzer.

Transmit Dual 10-Bit DAC Input

The MAX5865 integrates a dual 10-bit DAC capable of operating with clock speeds up to 40Msps. The digital data for the I and Q channels are alternately clocked onto the DAC's bus DD0–DD9. Data for the I channel is latched on the falling edge of the clock signal and data for the Q channel is latched on the rising edge of the clock signal. The MAX5865 EV kit provides a 0.1in 2 x 10 header (J3) to interface a 10-bit CMOS pattern generator to the EV kit. The header data pins are labeled on the board with the appropriate data bits designation. Use the labels on the EV kit to match the data bits from the pattern generator to the corresponding data pins on header J3. Header pins J3-1 through J3-19 (odd pins) are data pins DD0–DD9. All other header pins are connected to digital ground OGND.

Transmit Dual DAC Outputs

The MAX5865 transmit DAC outputs are ±400mV_{P-P} full-scale differential analog signals and are biased to 1.4VDC common mode. The full-scale output and DC common-mode level are set by the internal voltage reference. A variation in the reference voltage results in proportional changes to the DAC full-scale output and the DC common-mode level. The ID and QD outputs are simultaneously updated on the rising edge of the clock signal. The differential ID and QD output signals can be sampled at the IDP, IDN, QDP, and QDN PC pads or converted to single-ended signals using on-board operational-amplifier circuits. Configure jumpers JU5, JU6, JU7, and JU8 to select the output signal format. See Tables 2 and 3 to configure jumpers JU5–JU8. When jumpers JU5–JU8 are configured for operational-amplifier conversion, the differential signals are converted into a 50Ω single-ended signal with operational amplifiers U3 and U4. The single-ended output signals can be sampled at the ID SMA connector for the ID channel and QD SMA connector for the QD channel. When jumpers JU5–JU8 are configured for DC-coupled differential outputs, the DC-coupled differential signals can be sampled at the IDP and IDN PC pads for the ID channel. The QD channel can be probed at the QDP and QDN PC pads.

Table 2. DAC ID Channel Analog Output Selection

JU5 POSITION	JU6 POSITION	EV KIT FUNCTION
1-2	1-2	ID channel DC-coupled differential output available at the IDP (DAC voltage output) and IDN (complementary DAC voltage output) PC pads
2-3	2-3	ID channel differential output converted to single-ended signal using operational-amplifier configuration; available at ID SMA connector

Table 3. DAC QD Channel Analog Output Selection

JU7 POSITION	JU8 POSITION	EV KIT FUNCTION
1-2	1-2	QD channel DC-coupled differential output available at the QDP (DAC voltage output) and QDN (complementary DAC voltage output) PC pads
2-3	2-3	QD channel differential output converted to single-ended signal using operational-amplifier configuration; available at QD SMA connector

Receive Dual ADC Analog Inputs

The MAX5865 integrates a dual 8-bit ADC that accepts differential or single-ended analog input signals. The inputs are simultaneously sampled on the rising edge of the clock. The EV kit is designed to accept differential or single-ended, AC- or DC-coupled input signals with full-scale amplitude of less than $1.024V_{P-P}$ (+4dBm). Ensure that the ADC input is not overdriven by observing the output digital codes and adjusting the input signal level for code of -0.5dB full scale. See Table 4 for instructions to configure jumpers JU1, JU2, JU3, JU4, JU9, and JU10 for the desired analog input. During single-ended operation the signal is applied directly to the ADC input. While in differential mode, an on-board transformer uses the single-ended analog input to generate a differential analog signal that is applied at the ADC's differential input pins.

The EV kit does not include analog input filters for the ADC channels. Note that function generators exhibit high harmonic distortions that could degrade the true performance of the ADC. Select appropriate filters per specific applications, test tones, and improve the signal integrity of the function generators.

Note: When a differential signal is applied to the ADC, the positive and negative input pins of the ADC each receive half of the input signal supplied at SMA connectors IA and QA with an offset voltage of VDD/2.

Receive Dual 8-Bit ADC Output

The 8-bit digital output data for the IA and QA channels are multiplexed at output data bus DA0–DA7. The IA channel data is available on the falling edge of the clock. The QA channel data is available on the rising edge of the clock. The MAX5865 EV kit provides a 0.1in 2 x 10 header (J1) to interface with a logic-analyzer or data-acquisition system. The header data pins are labeled on the board with the appropriate data bit designations. Use the labels on the EV kit to match the output data bits to the data-acquisition system. Header pins J1-4 through J1-18 (even pins) are data pins DA0–DA7. Header pin J1-2 is a clock signal pin. All other header pins are connected to digital ground OGND.

Reference Voltage Options

The MAX5865 provides two reference modes of operation that can be selected by applying a voltage input to the REFIN pin. The reference voltage sets the full-scale input voltage of the ADC and the full-scale output voltage of the DAC. The MAX5865 EV kit provides jumper JU11 and the REFIN PC board pad that allows access to the input pin and selects one of the two reference modes: internal reference mode or buffered external reference mode. See Table 5 for instructions to select the voltage reference mode. Using an external reference enhances accuracy and drift performance or can be used for gain control.

Table 4. Single-Ended/Differential/AC-Coupled/DC-Coupled Jumper Configuration

JUMPER	SHUNT POSITION	PIN CONNECTION	EV KIT OPERATION
JU1	2 and 3	IA+ pin AC-coupled to SMA connector IAP through R1 and C28.	**Single-ended input, AC-coupled.** Analog input signal is applied to the IAP SMA connector, **channel IA**: • R26 opened (default).
JU2	2 and 3	IA- pin connected to COM pin through R2.	
JU9	Installed	IA+ pin assumes the DC offset at REFP and REFN.	
JU1	2 and 3	IA+ pin DC-coupled to SMA connector IAP through R1 and R26.	**Single-ended input, DC-coupled.** Analog input signal is applied to the IAP SMA connector, **channel IA**: • R26 shorted (0Ω) • C28 opened (removed) • R29 opened (removed)
JU2	2 and 3	IA- pin connected to COM pin through R2.	
JU9	Not installed	IA+ pin assumes the DC offset from the analog input source.	
JU1	1 and 2	IA+ pin connected to pin 6 of transformer T1 through R1.	**Differential input, AC-coupled.** Single-ended analog input signal is applied to IA SMA connector, **channel IA.**
JU2	1 and 2	IA- pin connected to pin 4 of transformer T1 through R2.	

Table 4. Single-Ended/Differential/AC-Coupled/DC-Coupled Jumper Configuration (continued)

JUMPER	SHUNT POSITION	PIN CONNECTION	EV KIT OPERATION
JU1	2 and 3	IA+ pin DC-coupled to SMA connector IAP through R1 and R26.	**Differential input, DC-coupled.** Analog input signals are applied to IAP and IAN SMA connectors, **channel IA**: • R26 shorted (0Ω) • C28 opened (removed) • R29 opened (removed)
JU2	Not installed	IA- pin DC-coupled to SMA connector IAN through R2.	
JU9	Not installed	IA+ and IA- pins assume the DC offset from the analog input source.	
JU3	2 and 3	QA+ pin AC-coupled to SMA connector QAP through R4 and C30.	**Single-ended input, AC-coupled.** Analog input signal is applied to the QAP SMA connector, **channel QA**: • R27 opened (default)
JU4	2 and 3	QA- pin connected to COM pin through R3.	
JU10	Installed	QA+ pin assumes the DC offset at the REFP and REFN.	
JU3	2 and 3	QA+ pin DC-coupled to SMA connector QAP through R4 and R27.	**Single-ended input, DC-coupled.** Analog input signal is applied to the QAP SMA connector , **channel QA**: • R27 shorted (0Ω) • C30 opened (removed) • R31 opened (removed)
JU4	2 and 3	QA- pin connected to COM pin through R3.	
JU10	Not installed	QA+ pin assumes the DC offset from the analog input source.	
JU3	1 and 2	QA+ pin connected to pin 3 of transformer T2 through R4.	**Differential input, AC-coupled.** Single-ended analog input signal is applied to QA SMA connector, **channel QA**.
JU4	1 and 2	QA- pin connected to pin 1 of transformer T2 through R3.	
JU3	2 and 3	QA+ pin DC-coupled to SMA connector QAP through R4 and R27.	**Differential input, DC-coupled.** Analog input signals are applied to QAP and QAN SMA connectors, **channel QA**: • R27 shorted (0Ω) • C30 opened (removed) • R31 opened (removed)
JU4	Not installed	QA- pin DC-coupled to SMA connector QAN through R3	
JU10	Not installed	QA+ and QA- pins assume the DC offset from the analog input source.	

Table 5. Voltage Reference Modes

REFIN VOLTAGE	REFERENCE MODE
VDD (shunt across jumper JU11)	Internal reference mode. Internal reference voltage equal to 0.512V. Sets the full-scale ADC input to 1.024V_{P-P} and DAC output voltage to 400mV_{P-P}.
External 1.024V (remove shunt from jumper JU11)	Buffered external reference mode. ADC full-scale input voltage set to REFIN. DAC full-scale output voltage proportional to REFIN.

Loopback Test

The MAX5865 EV kit circuit provides header J2 that, when configured, connects the ADC digital output bus to the DAC digital input. This allows a preliminary evaluation of the MAX5865 using analog input signals only.

Note: Configuring header J2 supplies an 8-bit output pattern to the 10-bit input, resulting in a loss of the DAC performance. Install shunts across the J2 pin headers to connect the DA7 output bit to the DD9 input bit, DA6 output bit to the DD8 input bit, etc. The maximum frequency for the ADC output loopback to DAC input is 25MHz. The maximum frequency for the ADC output loopback DAC input can be increased to 30MHz by changing resistors R37 through R44 to 25Ω.

TDD Mode

A time-division duplex (TDD) operating mode can also be implemented by connecting the ADC digital output to the DAC digital input bus. Use the MAX5865 EV kit software to switch between receive and transmit mode to implement TDD mode. Operating in this configuration, the ADC digital buffer (U5) is bypassed. Avoid excessive digital ground currents by keeping the digital bus capacitance to a minimum in this mode. Refer to the *FDD and TDD Modes* section in the MAX5865 data sheet for further details.

Evaluating the MAX5864 or MAX5863

The MAX5865 EV kit can be used to evaluate the MAX5864 or MAX5863, which are pin and function compatible with the MAX5865. The MAX5863 operates at clock frequencies of >2MHz, but ≤7.5MHz. The MAX5864 operates at clock frequencies >7.5MHz, but ≤22MHz. Replace the MAX5865 (U1) with the MAX5864 or the MAX5863 and refer to the respective data sheet for detailed technical information.

Board Layout

The MAX5865 EV kit is a four-layer board design optimized for high-speed signals. All high-speed signal lines are routed through 50Ω impedance-matched transmission lines. The length of these 50Ω transmission lines is matched to within 40 mils (1mm) to minimize layout-dependent data skew. The board layout separates the digital and analog ground plane of the circuit for optimum performance.

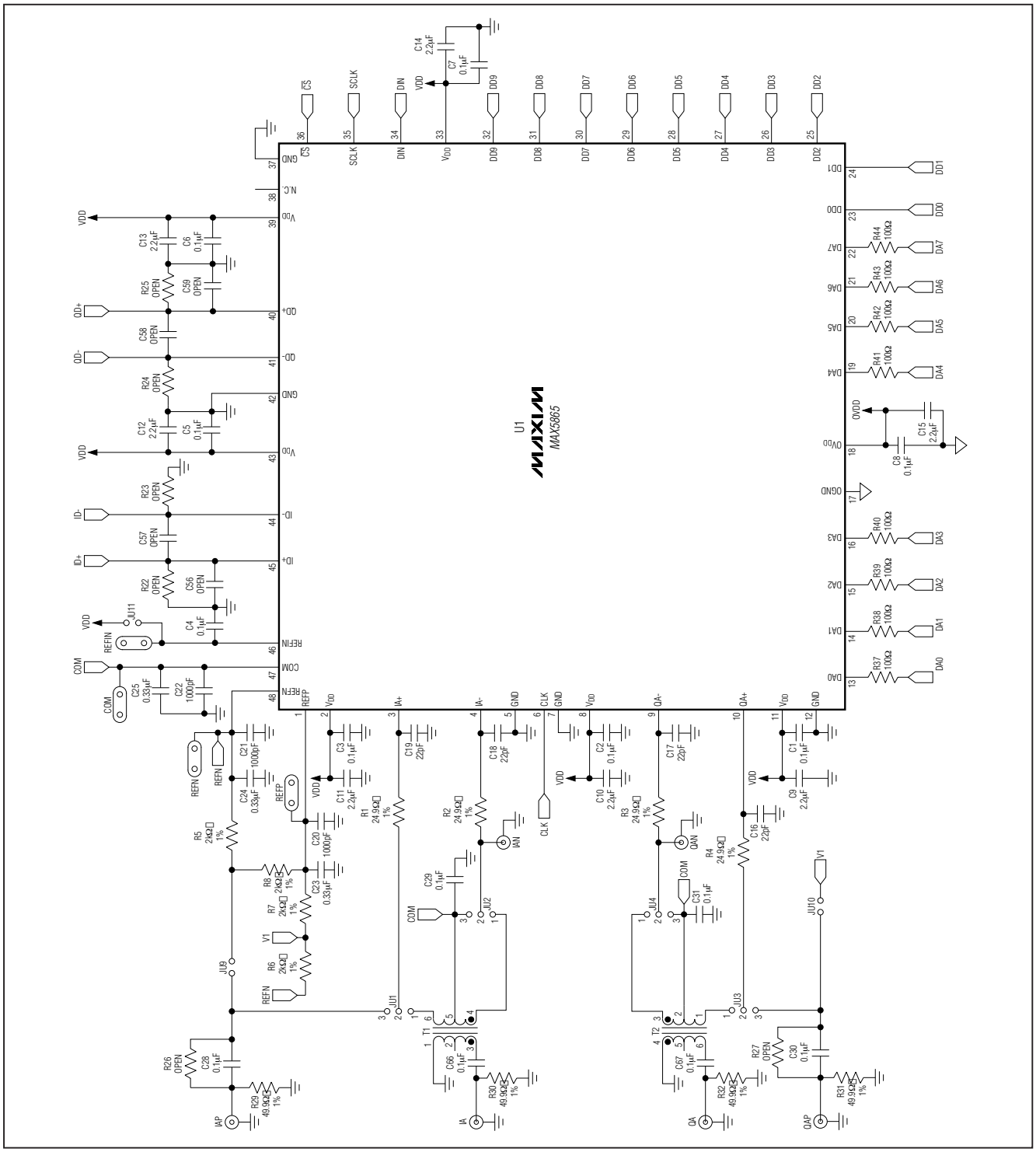

Figure 2. MAX5865 EV Kit Schematic (Sheet 1 of 3)

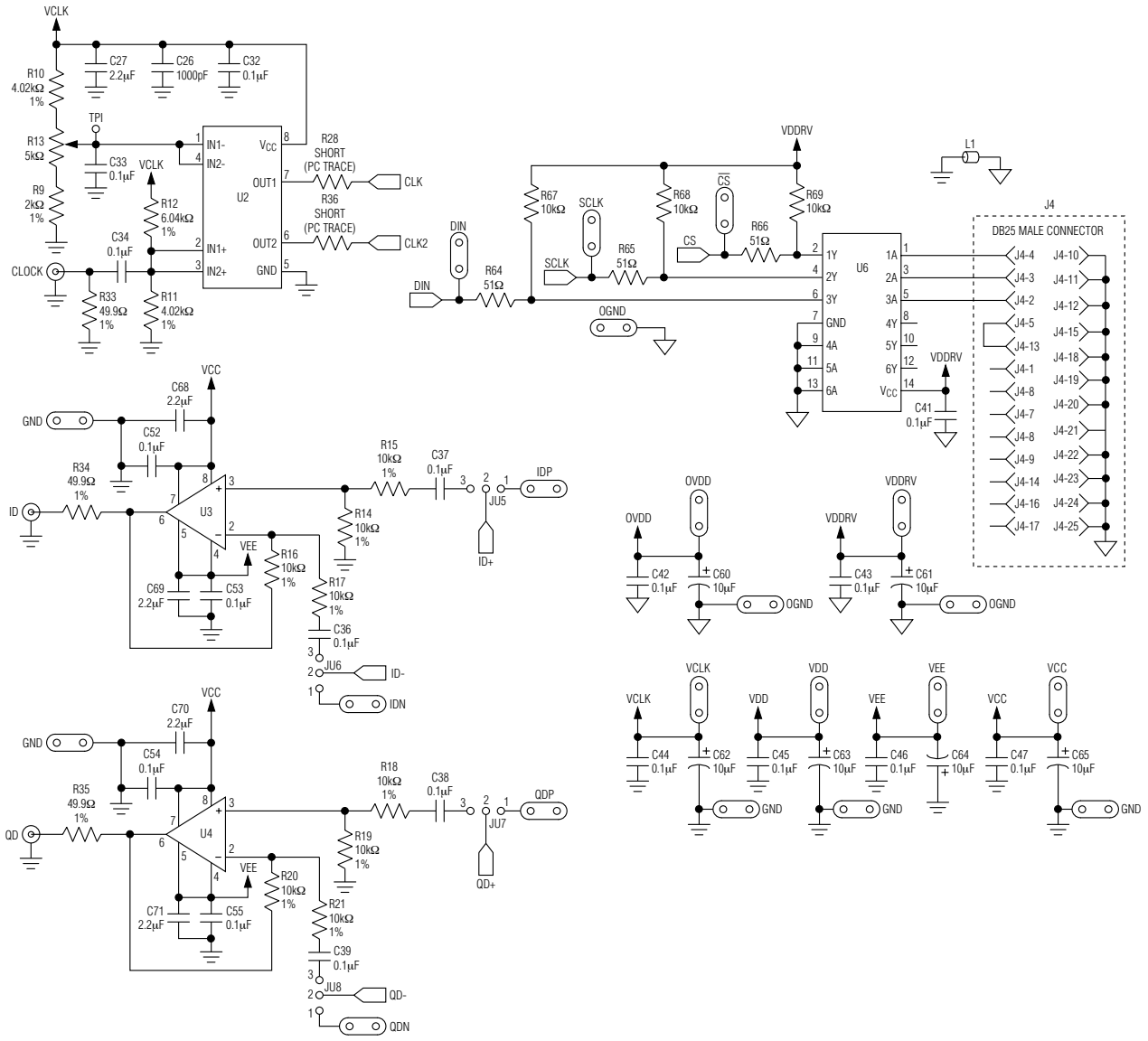

Figure 3. MAX5865 EV Kit Schematic (Sheet 2 of 3)

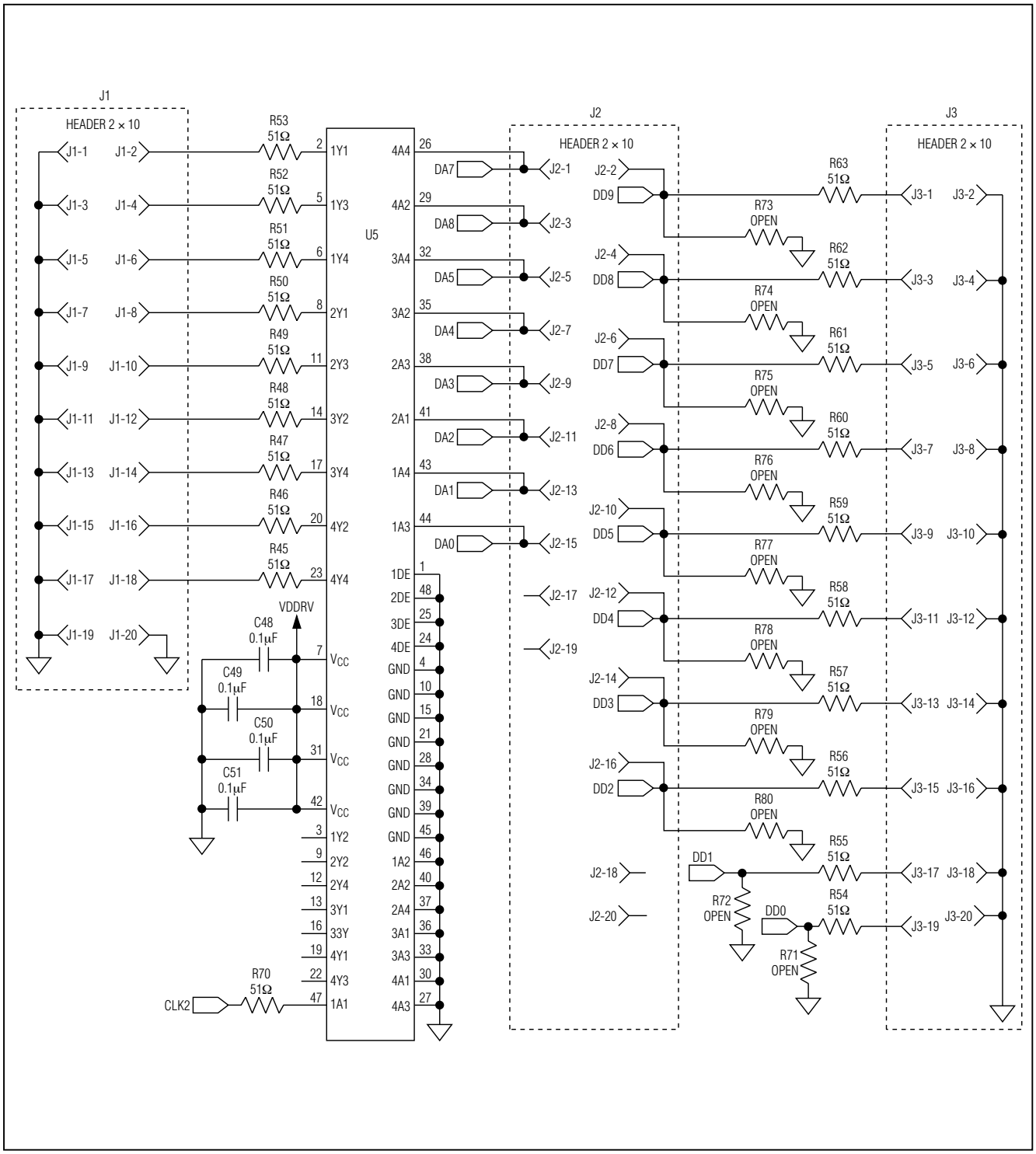

Figure 4. MAX5865 EV Kit Schematic (Sheet 3 of 3)

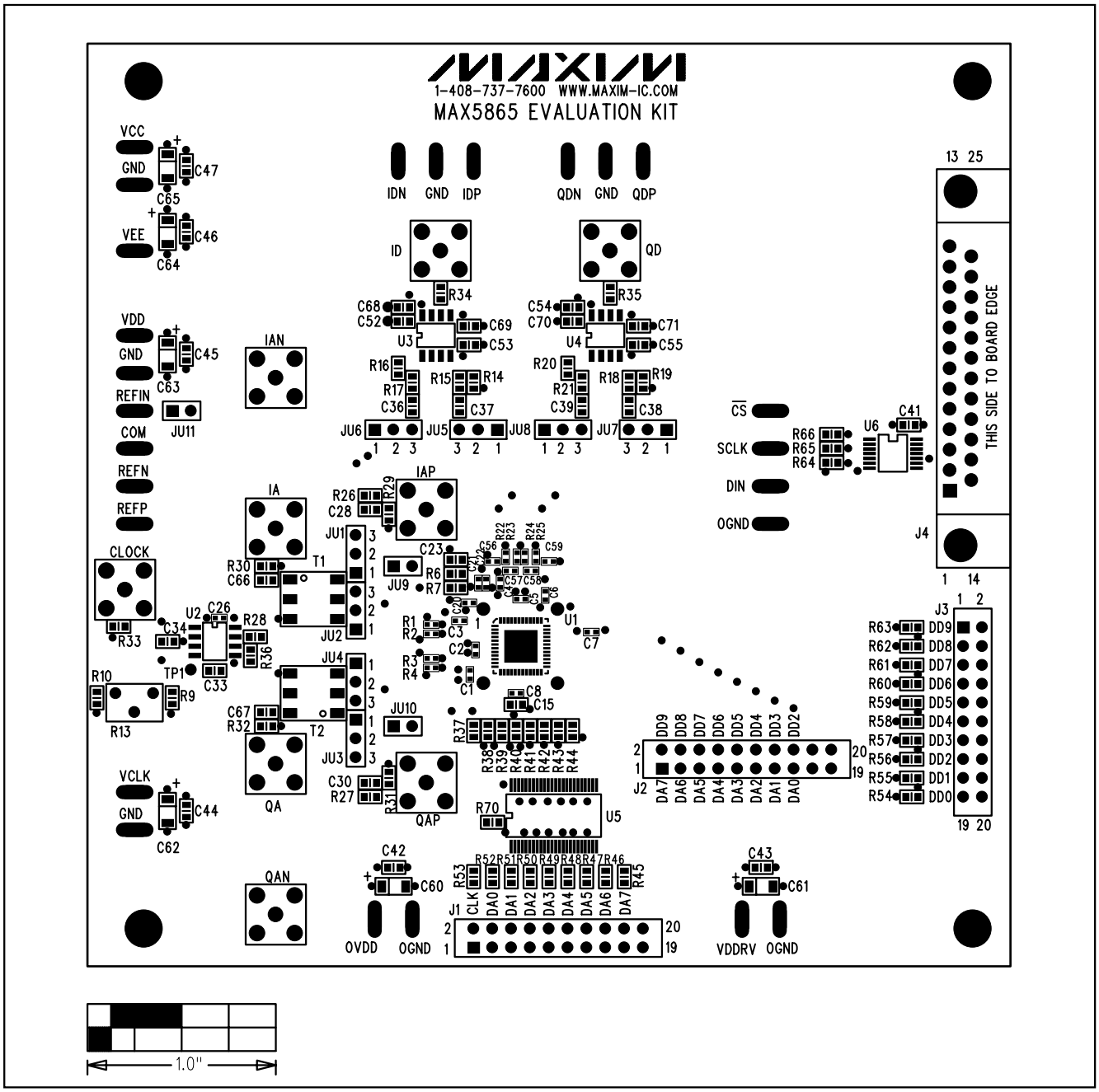

Figure 5. MAX5865 EV Kit Component Placement Guide—Component Side

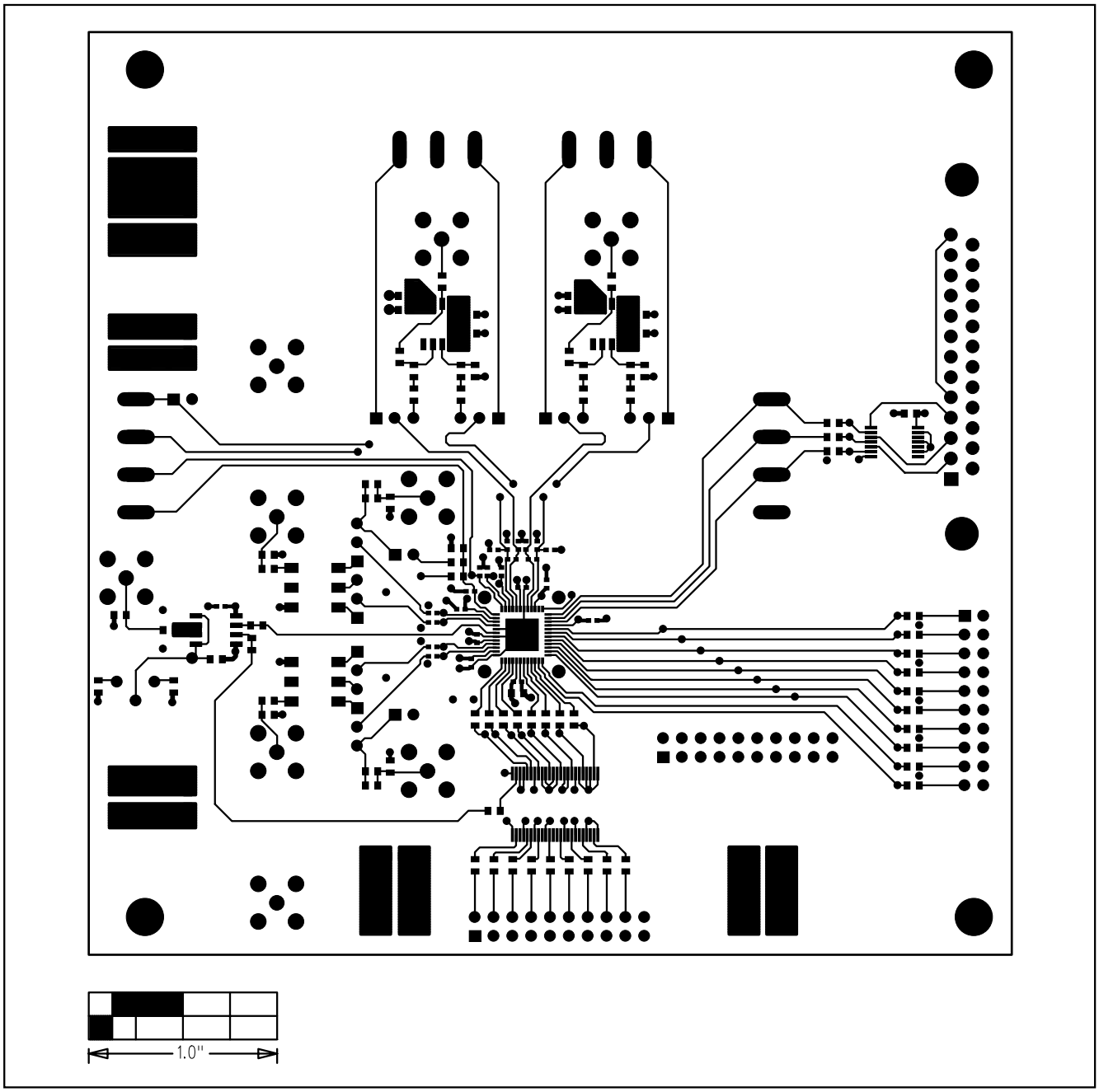

Figure 6. MAX5865 EV Kit PC Board Layout—Component Side

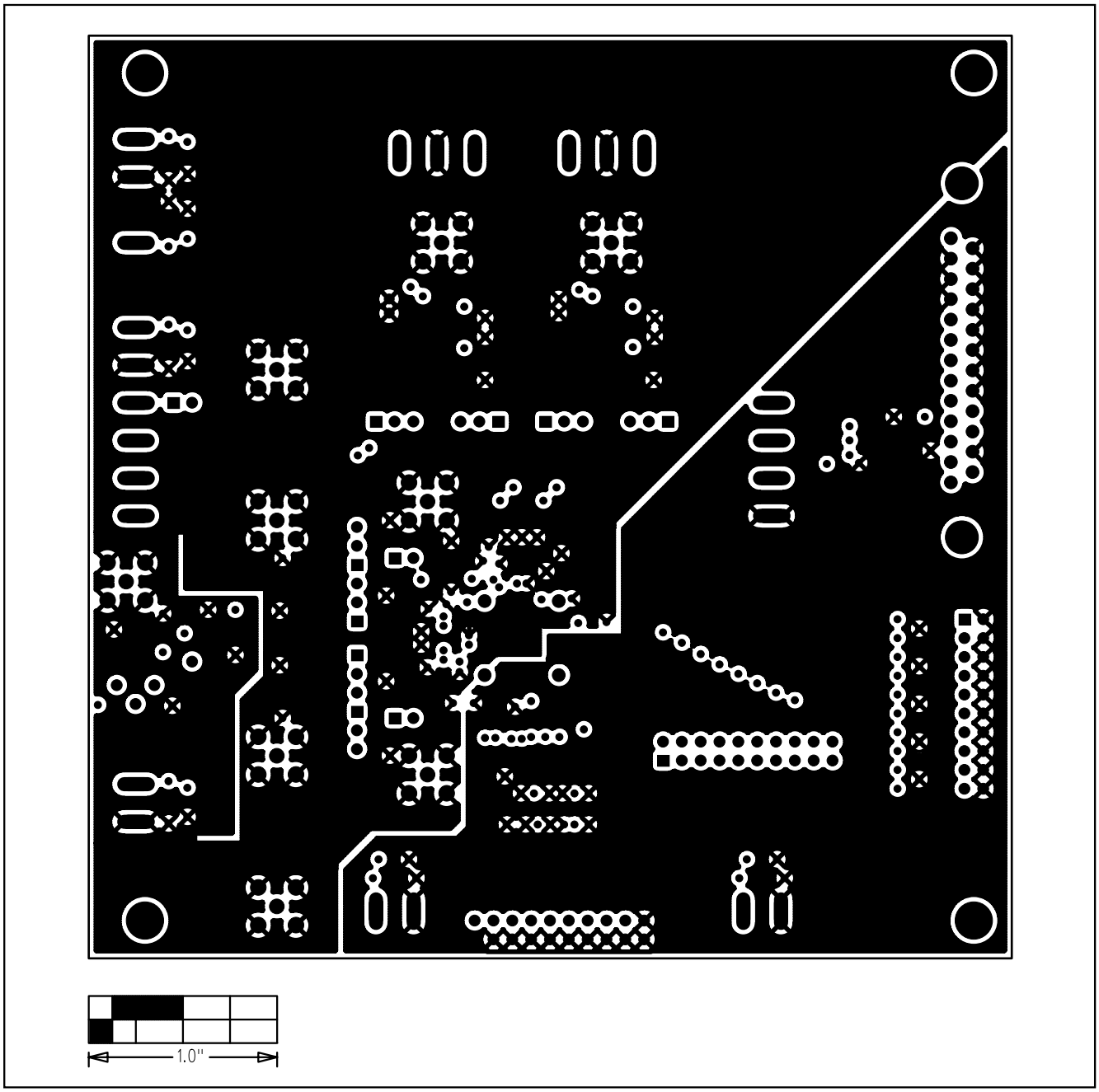

Figure 7. MAX5865 EV Kit PC Board Layout—Ground Planes

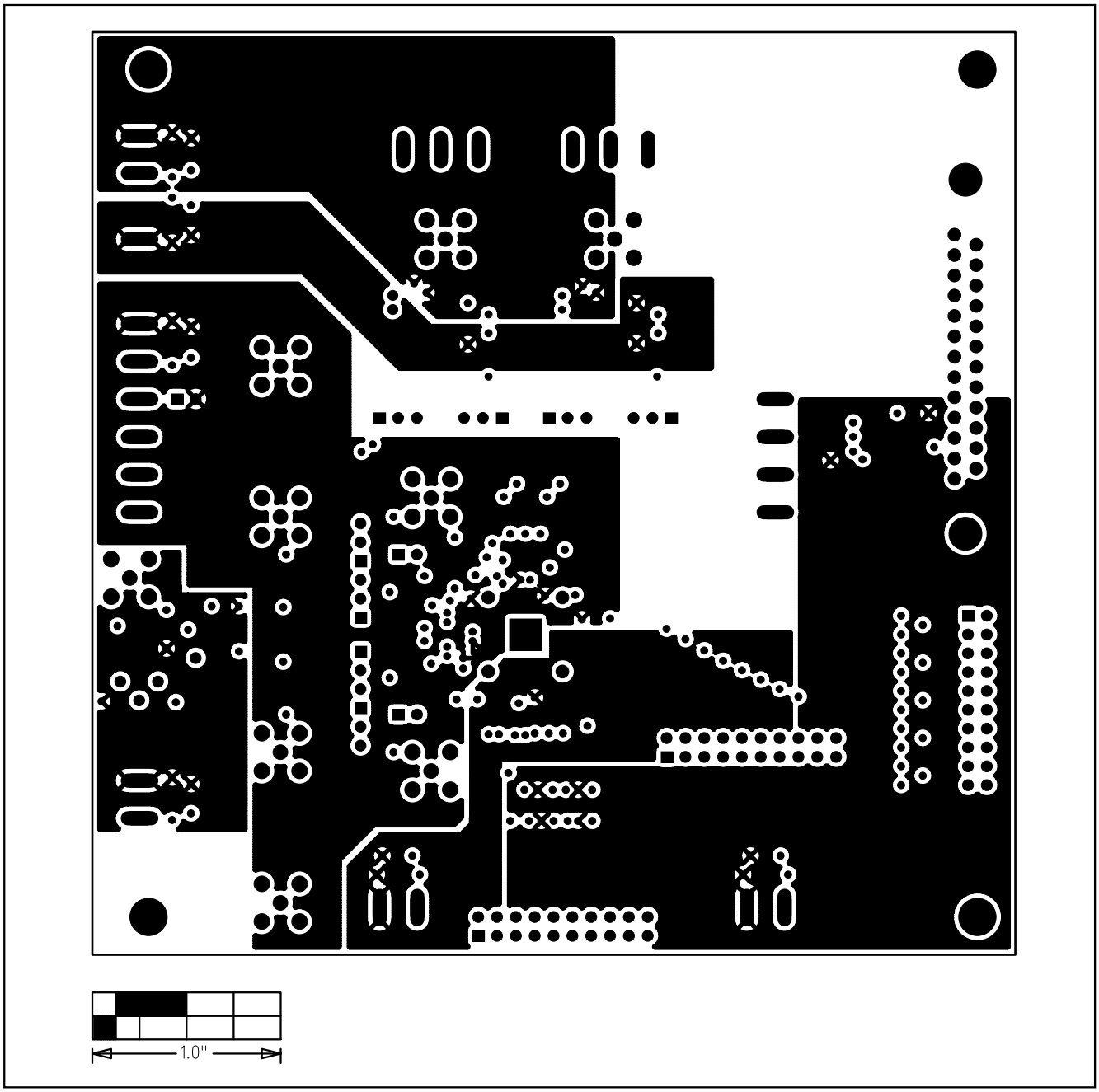

Figure 8. MAX5865 EV Kit PC Board Layout—Power Planes

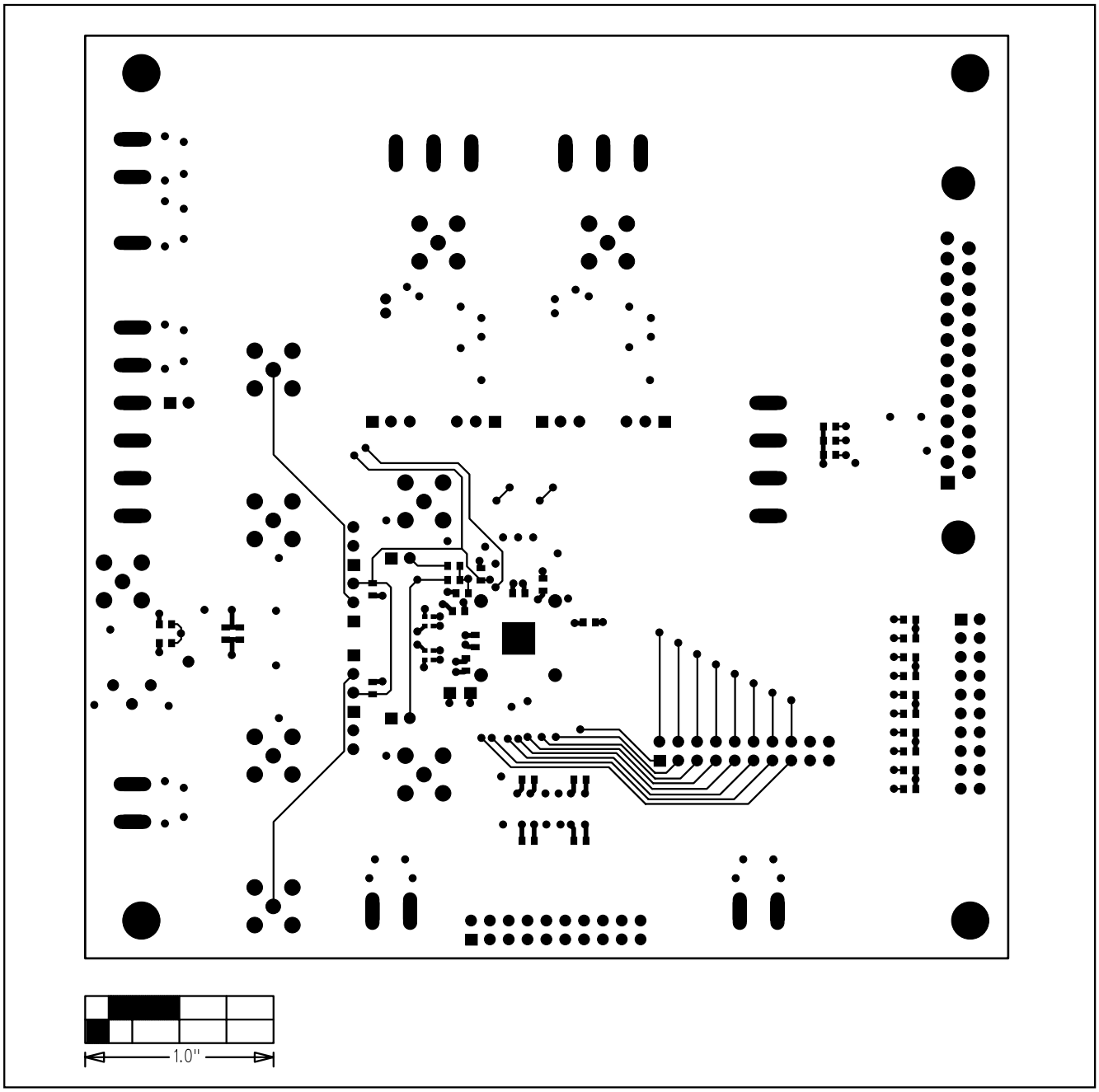

Figure 9. MAX5865 EV Kit PC Board Layout—Solder Side

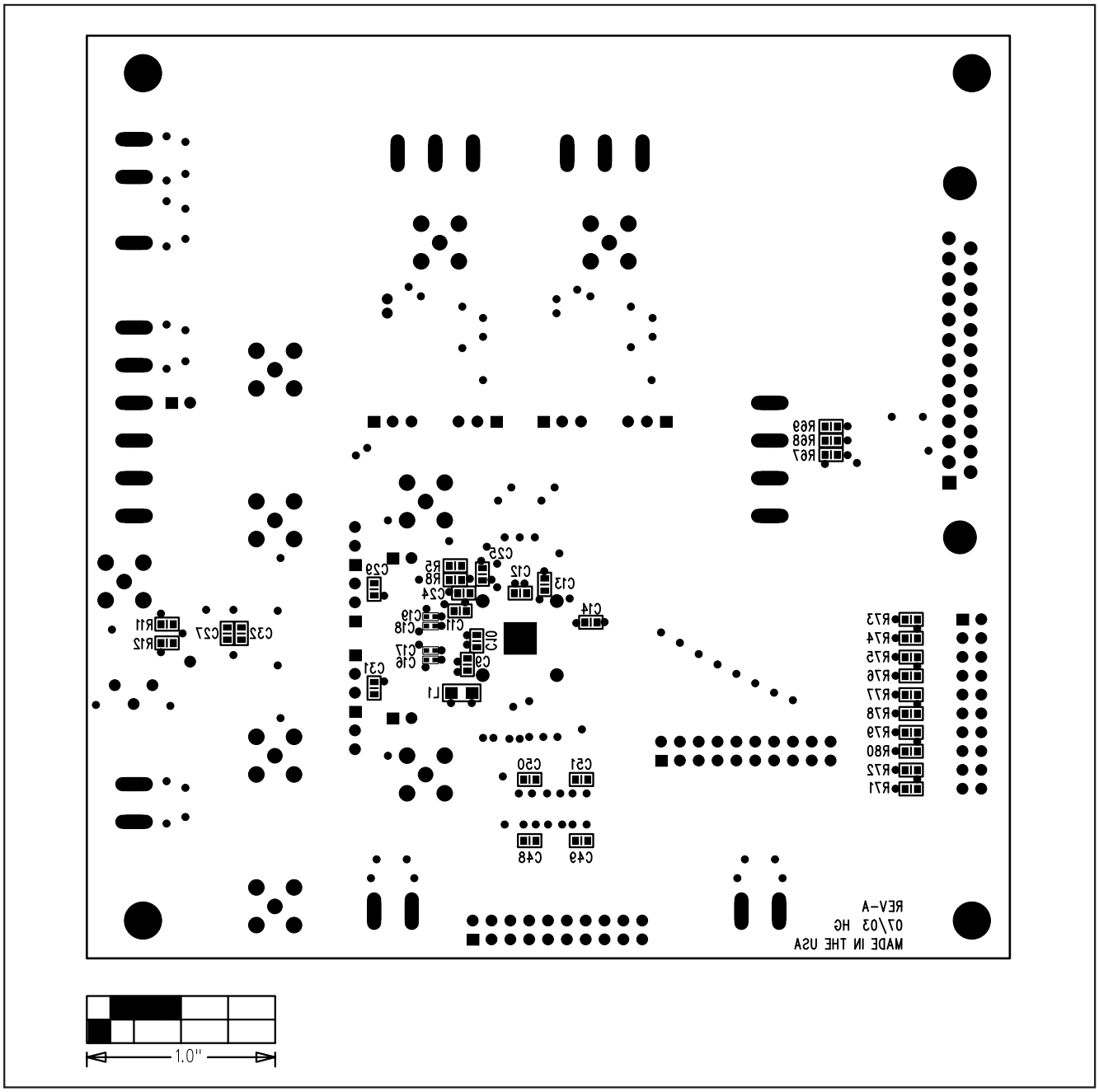

Figure 10. MAX5865 EV Kit Component Placement Guide—Solder Side