ATA6570

High-Speed CAN Transceiver with Partial Networking

Features

- High-Speed CAN Transceiver Fully Compliant to ISO 11898-2, ISO 11898-5, ISO 11898-6, ISO 11898-2: 2016 and SAEJ 2962-2
- Autonomous Bus Biasing According to ISO 11898-2: 2016
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Standard CAN Data Rate up to 1Mbit/s and CAN FD Data Rate up to 5Mbit/s (CAN FD)
- 4 Mbit/s SPI Interface
- Differential Bus Receiver with Wide Common Mode Range
- Very Low Current Consumption in Sleep and Standby with Full Wake-Up Capability
- Power-Down of the Complete Node via the INH-Output (Switching Off External Voltage Regulator(s))
- Six Operation Modes:
  - Power-Off mode
  - Microcontroller Reset mode
  - Sleep mode
  - Standby mode
  - Normal mode
  - Overtemp mode
- Four Wake-Up Sources
  - Local wake-up via pin WAKE
  - Remote wake-up pattern according to ISO 11898-2: 2016
  - Remote wake-up frame according to ISO 11898-2: 2016 (selective wake-up)
  - Host wake-up via SPI
- Wake-Up Source Recognition
- Transceiver Disengages from the Bus In Overtemperature and Low Power Supply Mode
- RXD Recessive Clamping Detection
- Transmit Data (TXD) Dominant Timeout Function
- Undervoltage Detection on VS, VCC and VIO Pins
- Overtemperature Protection
- 3.3V to 5V Microcontrollers Can Be Interfaced Directly Via the VIO Pin
- Battery Supply and CAN Bus Pins Protected Against Transients According to ISO 7637
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Short-Circuit Protected to GND and VCC
- VS Operating Voltage up to 28V, VS DC Supply Voltage up to 42V
- Watchdog with Independent Clock Source
- Watchdog Can Be Operated in Window and Time-Out Mode

  - Optional cyclic wake-up in watchdog Time-Out mode
  - Watchdog automatically re-enabled when wake-up event captured
  - Watchdog period selectable
  - Watchdog reset period selectable
- Qualified According to AEC-Q100
- Two Ambient Temperature Grades Available:
  - ATA6570-GNQW1 up to T_{amb} = +125°C
  - ATA6570-GNQW0 up to T_{amb} = +150°C
- Fulfills the OEM Hardware Requirements for CAN Interfaces in Automotive Applications, Rev. 1.3
- Fulfills the OEM Requirements for Partial Networking Rev. 2.2
- SOIC14 Package

Description

The ATA6570 is a stand-alone high-speed CAN transceiver that interfaces a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus designed for high-speed CAN applications in the automotive environment.

The ATA6570 provides local and enhanced remote wake-up capabilities and is available in a SOIC14 package. It has a very low power consumption in Standby and Sleep mode. Besides local wake-up via WAKE and remote wake-up pattern according to ISO 11898-2: 2016, ATA6570 additionally supports ISO 11898-2: 2016 compliant CAN partial networking. A CAN frame decoder evaluates the bus traffic and checks for a matching frame that has been configured into registers via the SPI. The device is able to keep the complete ECU in a low power mode even when bus traffic is present until a valid wake-up frame is received. It also features a watchdog (per default off) and a Serial Peripheral Interface (SPI).

The ATA6570 is a CAN-FD device. However, selective wake-up is only possible using classical CAN frames. In Sleep mode, the device can be configured to either ignore CAN-FD frames, or to treat CAN-FD frames as frames with errors and increment the internal error counter.

The VIO pin allows the automatic adjustment of the I/O levels to the I/O level of the connected microcontroller.

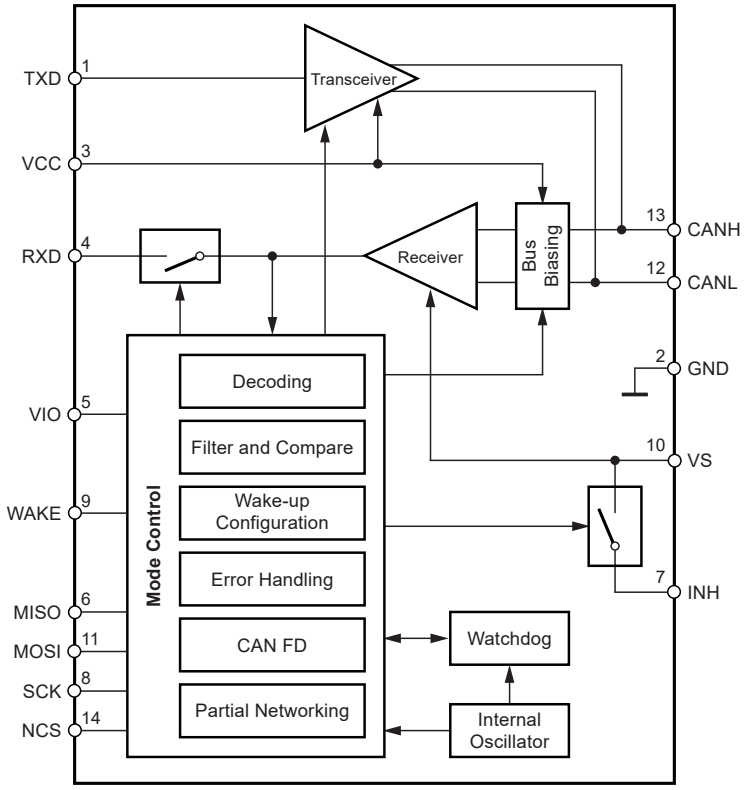
The SPI interface controls the device and provides status and diagnosis information to the Host MCU.

All these features make the ATA6570 an excellent choice for high speed CAN networks, especially in applications where nodes are always connected to the battery but are only activated when they are really needed in the application.

Table 1. ATA6570 Family Members

Device	Grade 0	Grade 1	SOIC14
ATA6570-GNQW1		x	x
ATA6570-GNQW0	x		x

Figure 1. Simplified Block Diagram



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1. Pin Configuration

Figure 1-1. Pin Configuration

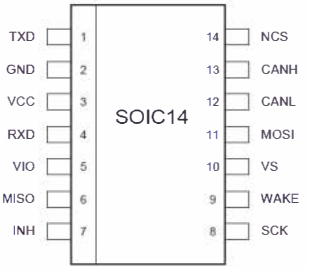


Table 1-1. Pin Description

Pin	Symbol	Function
1	TXD	Transmit data input
2	GND	Ground
3	VCC	5V CAN transceiver supply voltage
4	RXD	Receive data output, reads out data from the CAN bus
5	VIO	Supply voltage for I/O level adapter
6	MISO	MISO: SPI data output
7	INH	High side output for switching external voltage regulators
8	SCK	SPI clock
9	WAKE	High voltage input for local wake-up
10	VS	Battery supply voltage
11	MOSI	MOSI: SPI data input
12	CANL	Low level CAN bus line
13	CANH	High level CAN bus line
14	NCS	NCS: SPI chip select input

1.1 Supply Pin (VS)

The VS supply pin is the power supply pin for the ATA6570 device. In an application, this pin usually is connected to the battery via a serial diode for reverse battery protection. This pin sustains standard automotive conditions, such as 40V during load dump.

An undervoltage detection circuit is implemented to avoid a malfunction or false bus messages. After switching on VS, the IC starts in Standby mode and the INH output is switched on.

1.2 Ground Pin (GND)

The IC does not affect the CAN bus in the event of GND disconnection.

1.3 Supply Pin (VCC)

This is the supply pin for the CANH and CANL bus drivers, the bus differential receiver and the bus biasing voltage circuitry. VCC is monitored for undervoltage conditions.

1.4 Supply Pin (VIO)

This is the supply pin for the digital input/outputs pins. VIO is monitored for undervoltage conditions. See Fail-safe Mechanisms.

1.5 Bus Pins (CANH AND CANL)

These are the CAN bus terminals.

CANL is a low-side driver to GND, and CANH is a high-side driver to VCC. In Normal mode and with TXD high, the CANH and CANL drivers are off, and the voltage at CANH and CANL is approximately 2.5V, provided by the internal bus biasing circuitry. This state is called recessive.

When TXD is low, CANL is pulled to GND and CANH to VCC, creating a differential voltage on the CAN bus. This is called the dominant state.

In Standby mode, the CANH and CANL drivers are off. If the device is in unpowered mode or sleep mode, CANH and CANL are highly resistive with extremely low leakage current to GND, making the device ideally passive.

Pins CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage, and are also protected against overtemperature conditions.

1.6 Input Pin (TXD)

This is the device input pin to control the CAN bus level. In the application, this pin is connected to the microcontroller transmit terminal. Pin TXD has an internal pull up toward VIO to ensure a safe defined recessive driver state in case this pin is left floating.

In Normal mode, when TXD is high or floating, the CAN bus is driven to the recessive state.

TXD must be pulled to GND in order to activate the CANH and CANL drivers and set the bus to the dominant state. A TXD dominant timeout timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)}$ TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high.

The transmitter is also disabled if pin TXD is held low (e.g., by a short- circuit to GND), during which the device is switched into Normal mode and the bus lines are in the recessive state. The transceiver remains in this state until pin TXD goes high.

1.7 Output Pin (RXD)

In Normal and Silent modes this pin reports the state of the CAN bus to the microcontroller. In the application, this pin is connected to the microcontroller receive terminal. RXD is high when the bus is recessive. When the bus is dominant, RXD is low.

The output is a push-pull structure. The high side is connected to VIO and the low side to GND.

In Standby mode the RXD output is switched to VIO. When a wake-up event is detected, RXD will be forced to low.

An RXD recessive clamping function (see section 2.4.8 RXD Recessive Clamping) is implemented. This fail-safe feature prevents the controller from sending data on the bus if the RXD line is clamped to high (e.g., recessive).

1.8 Inhibit Output Pin (INH)

The inhibit output pin provides an internal switch towards VS and is used to control external voltage regulators. If the device is in normal or standby mode, the inhibit high-side switch is turned on. When the device is in sleep mode, the inhibit switch is turned off, thus disabling the connected external voltage regulators or other connected external devices.

A wake-up event on the CAN bus or at the WAKE pin switches the INH pin to the VS level. After a system power-up (VS rises from zero), the INH pin switches to the VS level automatically.

The INH output pin has an additional function when the watchdog is enabled. At every watchdog reset the INH pin will be switched off for a predefined time. This will trigger a power-on reset of the microcontroller if the supply of the microcontroller is controlled by the INH pin.

1.9 Wake Input Pin (WAKE)

In the ATA6570, this pin is a high-voltage input used for waking up the device from sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If the WAKE pin is not needed in the application, the local wake-up should be disabled and the WAKE pin should be connected to GND to ensure optimal EMI performance.

The WAKE pin has a special design structure and is triggered by a LOW-to-HIGH and/or a HIGH-to-LOW transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit.

An internal filter is implemented to avoid a false wake-up event due to parasitic pulses. A serial resistor should be inserted in order to limit the input current mainly during transient pulses and ESD. The recommended resistor value is 10kΩ. An external 10nF capacitor is advised for better EMC and ESD performances.

1.10 SPI Input Pin (MOSI)

Master-Out-Slave-In serial data port input connected to an output of the microcontroller.

1.11 SPI Output Pin (MISO)

Master-In-Slave-Out serial data port output connected to an input of the microcontroller; this pin is in tri-state if NCS is high.

1.12 SPI Clock Pin (SCK)

Serial data clock; default level is low due to internal pull-down.

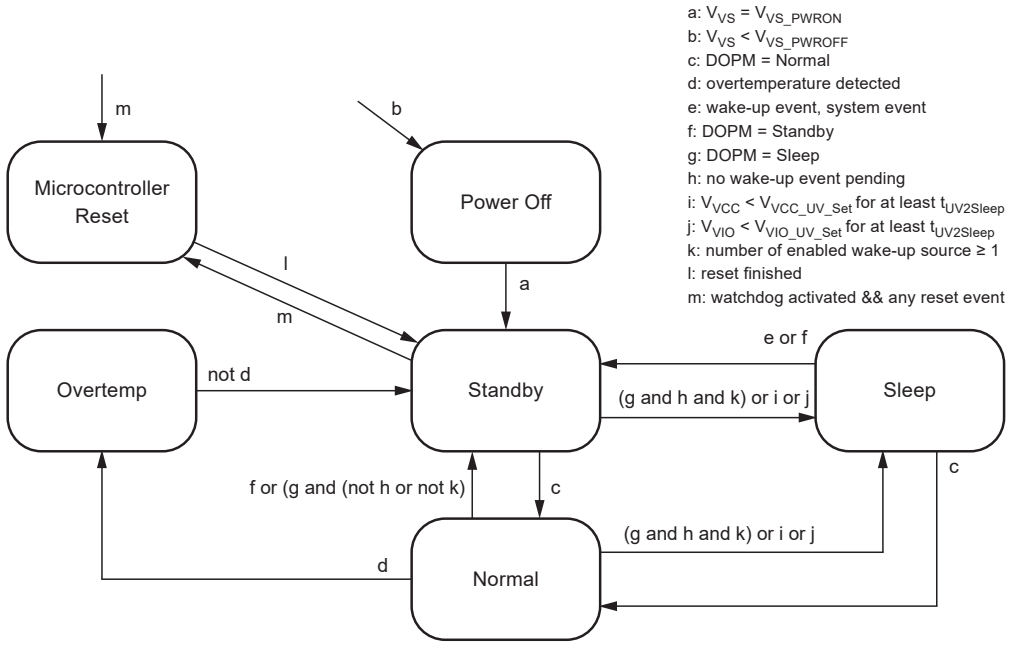
1.13 SPI Chip Select Pin (NCS)

Chip select pin; active low. If chip select is not active, no data are loaded from MOSI on SCK edges or provided at MISO.

2. Functional Description

2.1 Device Operation Modes

Figure 2-1. Overview to the Device Operation Modes



The mode control unit in the ATA6570 implements six different states as depicted in Figure 2-1. All of the states are briefly described in this section.

Table 2-1. Operating Modes and Functions

Block	Device Operating Mode				
	Power off	Standby	Normal	Sleep	Overtemp
SPI	disabled	active	active	active if VIO supplied	disabled
INH	high-ohmic	VS level	VS level	high-ohmic	VS level
CAN	TRX Off	TRX Standby / TRX Biased Standby	TRX Normal / TRX Standby / TRX Biased Standby / TRX Silent (determined by bits COPM)	TRX Standby / TRX Biased Standby	TRX Off
RXD	VIO level	VIO level / low if wake-up / interrupt event detected	CAN bit stream if COPM = 01/10/11, otherwise same as Standby/Sleep	VIO level / low if wake-up/ interrupt event detected	VIO level / low if wake-up / interrupt event pending

2.1.1 Power-Off Mode

The device is in Power-Off mode when the supply voltage of the device V_{VS} is lower than the defined device power-off detection voltage threshold (V_{VS_PWROFF}). This is the default mode when the battery is first connected. In this mode the integrated CAN transceiver is in the TRX off mode (see section 2.2.1 TRX Off Mode). The watchdog is also in off mode. The pins CANH and CANL are high ohmic and the INH output is switched off. The device is not able to provide any functionality. As soon as V_{VS} rises above the power-on detection threshold (V_{VS_PWRON}), the device boots up. The whole device is reset and initialized. After $t_{startup}$ the device is in the Standby mode.

2.1.2 Standby Mode

The Standby mode is the default mode after a Power-on Reset. In Standby mode, the integrated CAN transceiver is unable to transmit or receive data. The INH pin is at the VS level and the external voltage regulator controlled by the pin is switched on.

The ATA6570 supports the autonomous bus biasing according to ISO 11898-2: 2016 in Standby and Sleep modes (provided $V_{VS} > V_{VS\_UV\_CAN\_Clear}$). The bus pins are biased to GND (via R_{CANH}, R_{CANL}) when the bus is inactive, and at approximately 2.5V when there is a remote CAN bus wake-up request Wake-Up Pattern (WUP) detected (according to ISO 11898-2: 2016).

In Standby mode, the ATA6570 supports both CAN bus remote wake-up via a standard WUP and via a selective wake-up frame (WUF). The CAN bus remote wake-up is only activated when the register bit CWUE is set to ‘1’ (see section 2.3.5.23 TRXECR – Transceiver Event Capture Enable Register (address 0x23)). The low power wake-up comparator in the receiver then monitors the corresponding bus activities and wakes up the whole device after detecting a valid wake-up event (V_{VS} must be above the VS CAN undervoltage release threshold, otherwise the integrated transceiver is in TRX off mode and no bus wake-up can be detected).

In the case that CPNE = PNCFOK = ‘1’, the selective wake-up is enabled. After a successful detection of a wake-up pattern, the bus pin is first biased to 2.5V and the device is ready for decoding further coming WUFs. Only after detecting a valid WUF, a wake-up event is registered and the wake-up process is finished. Decoding of CAN data and remote frames is supported during all mode transitions of the device. If the data frame is a valid WUF, the device will indicate a wake-up event.

If the selective wake-up is disabled and CAN remote wake-up is enabled, the standard wake-up via WUP is activated. The device biases its bus pin to 2.5V after a successful detection of a wake-up pattern, registers the wake-up event, and the wake-up process is finished.

The device also supports detecting system events (see section 2.4.11 Wake-Up and Interrupt Event Diagnosis via Pin RXD) and a local wake-up event via the WAKE pin in Standby mode. The internal wake-up flags CWUS, LWURS and LWUFS (see sections 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63) and 2.3.5.20 WKESR – WAKE Event Status Register (address 0x64)) and system event status registers are set to ‘1’ by the device if the corresponding event is detected.

The device will not leave the Standby mode after detecting a valid wake-up event. It will only set the corresponding internal status register bits. A transition to the Normal mode will only happen when the register bits DOPM are set to ‘111’ via SPI.

In Standby mode, the detection of a wake-up event or an interrupt event (see section 2.4.11 Wake-Up and Interrupt Event Diagnosis via Pin RXD) is denoted via pin RXD, provided that the corresponding event interrupt is enabled (see section 2.3.5.22 SECR – System Event Capture Enable Register (address 0x04) to section 2.3.5.25 WKECR – WAKE Event Capture Enable Register (address 0x4C)). The RXD pin is usually at V_{VIO} level and will be forced to low if an enabled event is detected. At the same time, a set of status registers (see section 2.3.5.17 GESR – Global Event Status Register (address 0x60)

to section 2.3.5.20 WKESR – WAKE Event Status Register (address 0x64)) is provided, which allows the microcontroller to get further detailed information about the device via SPI.

As shown in Figure 2-1, the device will enter the Standby mode in the following cases:

1. From Power-off mode after Power-on Reset after V_{VS} rises above the power-on detection voltage threshold V_{VS_PWRON}
2. From Overtemp mode after the chip temperature falls by more than the thermal shutdown hysteresis T_{Jsd_hys}
3. From Sleep mode after detecting enabled wake-up event or interrupt event
4. From Sleep mode, Normal mode via SPI (DOPM=0x4) if a valid interface voltage V_{VIO} is applied
5. If trying a switch to Sleep mode (DOPM=0x1 is written) via SPI when there is a wake-up event pending or all wake-up sources are disabled

The watchdog can be activated (Window or Time-out mode) in Standby mode. To avoid unwanted configuration of the watchdog, configuration can only be done in Standby mode.

2.1.3 Sleep Mode

Sleep mode is the most power-saving mode of the device. In this mode the INH output is switched off. Therefore, the external voltage regulator(s) controlled by this pin is also switched off. This is the only difference between Sleep mode and Standby mode. If a valid interface supply voltage (V_{VIO}) is applied, registers of the device can still be accessed via its SPI interface.

As in Standby mode, the device can react on a variety of wake-up events (see section 2.3 Wake-Up). Customers are allowed to configure the device to let it be woken up in different ways. If a valid interface voltage V_{VIO} is applied, it is even possible to wake-up the device from Sleep mode via an SPI command (DOPM = Standby/Normal).

In Sleep mode, the INH output switches on when either a CAN bus wake-up event, a host wake-up event (via SPI), a local wake-up, or an interrupt event (see section 2.4.12 Interrupt Event/Wake-Up Event Delay) is detected or a watchdog reset (Time-out mode is enabled) occurs and the device switches to microcontroller reset mode.

As shown in Figure 2-1, the device enters the Sleep mode in following cases:

1. From the Normal mode or Standby mode via an SPI command, if no wake-up event is pending and at least one wake-up source (see section 2.3 Wake-Up) is enabled; or,
2. From the Normal mode or Standby mode in the case of detecting VCC or VIO undervoltage ($V_{VIO} < V_{VIO\_UV\_Set}$ or $V_{VCC} < V_{VCC\_UV\_Set}$ for $t > t_{UV2Sleep}$). In this case, all pending wake-up events will be cleared. CAN bus wake-up (CWUE = 1; see section 2.3.5.23 TRXECR – Transceiver Event Capture Enable Register (address 0x23)) and local wake-up via the WAKE pin (LWUFE = 1 && LWURE = 1) are enabled. Selective wake-up is disabled (please refer to section 2.11 VCC/VIO Undervoltage Protection for details about VCC/VIO undervoltage protection).

The ATA6570 provides a bit SMTS (see 2.1.7.2 DMSR – Device Mode Status Register (address 0x03)) to denote, whether or not the recent transition to the Sleep mode is triggered by a VCC/VIO undervoltage event. The bit can be read by the microcontroller in the Sleep mode (if a valid interface supply voltage is provided), or after waking up from the Sleep mode.

2.1.4 Normal Mode

The ATA6570 provides its full functionality in the Normal mode.

Wake-up flag CWUS and interrupt event status registers will still be set to ‘1’ by the device if the corresponding event is detected.

As shown in Figure 2-1 the device will enter the Normal mode from the Standby mode or Sleep mode via an SPI command.

2.1.5 Overtemp Mode

The Overtemp mode is the operation mode which protects the device from an overtemperature damage. The overtemperature protection is only active in Normal mode.

The device provides two levels of overtemperature protection. If the chip temperature rises above the overtemperature protection prewarning threshold ($T > T_{OT\_Prew}$), the device first set the status bit to OTPWS = 1. If the overtemperature prewarning interrupt is enabled (OTPWE = 1), an overtemperature prewarning interrupt will be generated (OTPW = 1, RXD signalization if COPM = 00 and DOPM = 111 (Normal mode)).

The device will enter the Overtemp mode when the chip temperature rises above the overtemperature protection shutdown threshold (T_{Jsd}). In the Overtemp mode the integrated CAN transceiver is switched to the TRX Off mode. The CAN bus pins are high ohmic. No further wake-up event will be detected, but the pending wake-up/interrupt event will still be signaled by a low level on pin RXD.
As shown in Figure 2-1, the device will enter the Overtemp mode from Normal mode when the chip temperature rises up the overtemperature protection shutdown threshold.

The device will exit the Overtemp mode and enter the Standby mode when the chip temperature falls by more than the thermal shutdown hysteresis (T_{Jsd_hys}) or when the device is powered off.

2.1.6 Microcontroller Reset Mode

Reset mode only exists when the watchdog is activated. In this mode, the INH output is switched off and the transceiver is disabled. The device leaves the Reset mode when the reset pulse width is reached.

2.1.7 Related Registers

2.1.7.1 DMCR – Device Mode Control Register (address 0x01)

The device operation mode is selected via bits DOPM in the device mode control register. The register is accessed via SPI at address 0x01.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	DOPM[2:0]			DMCR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	1	0	0	

Bit 7...3: Reserved for future use

Bit 2..0: DOPM[2:0] – Select device operation mode

DOPM[2:0]	Device Operation Mode
3’b001	Sleep mode
3’b100	Standby mode
3’b111	Normal mode

2.1.7.2 DMSR – Device Mode Status Register (address 0x03)

The register provides device operation mode transition related information to the external microcontroller.

Bit	7	6	5	4	3	2	1	0	
	SMTS	**OTPWS**	**NMTS**			**-**			**DMSR**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	1	0	0	0	0	0	

Bit 7: SMTS, Sleep mode transition status

The device sets the bit to ‘0’ if the recent transition to Sleep mode is triggered by an SPI command and sets the bit to ‘1’ if the recent transition to Sleep mode is forced by an VCC/VIO undervoltage.

Bit 6: OTPWS, overtemperature prewarning status

The device sets the bit to ‘1’ if IC temperature is over overtemperature prewarning threshold and to ‘0’ vice versa.

Bit 5: NMTS, Normal mode transition status

The device sets the bit to ‘0’ when IC has entered Normal mode after power-up and set the bit to ‘1’ when the IC has powered up but has not yet switched to Normal mode.

Bit 4...0: Reserved for future use

2.2 Integrated CAN Transceiver Operation Modes

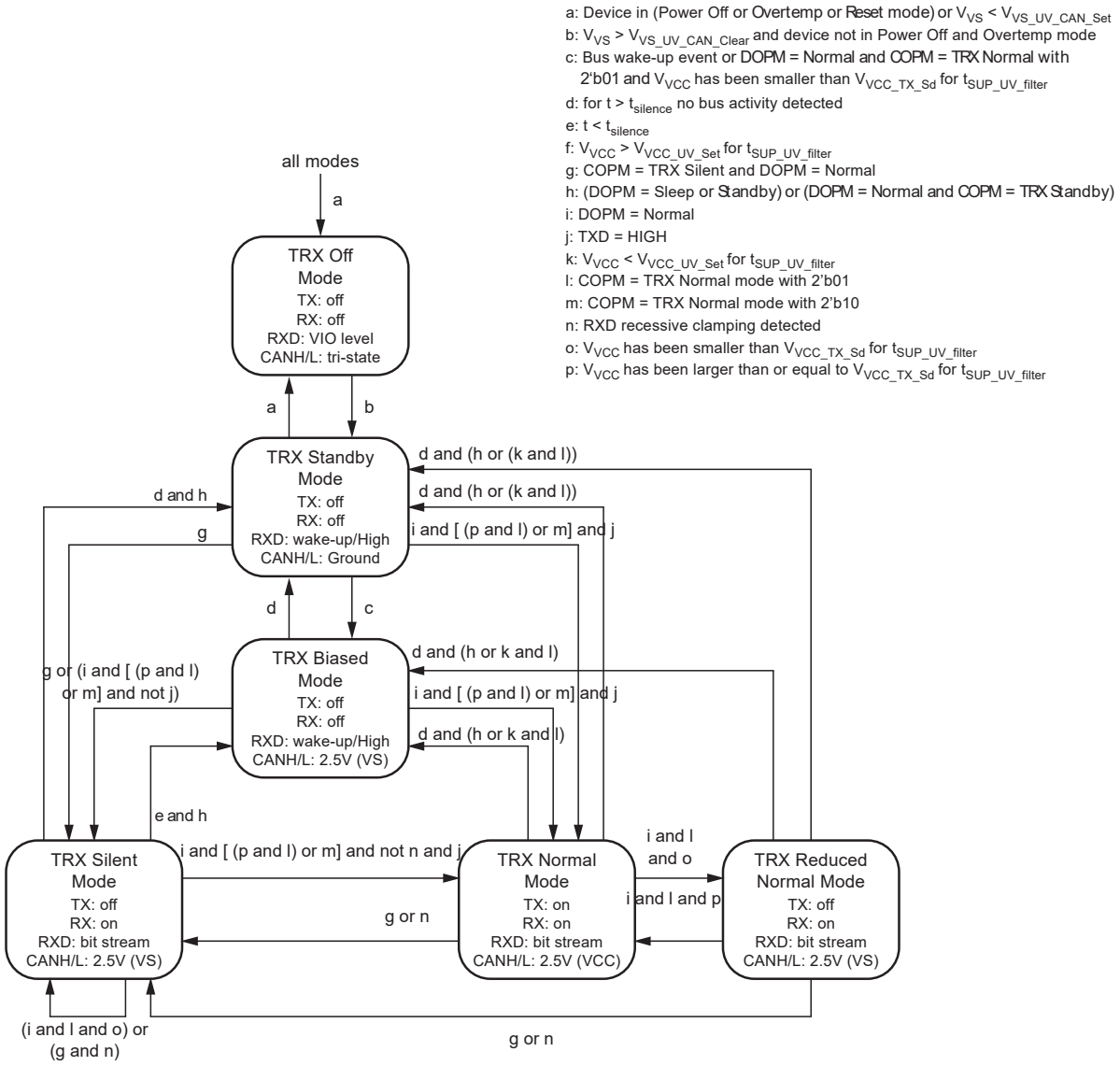
The integrated high-speed CAN transceiver in the ATA6570 is designed for standard bit rates up to 1Mbit/s and CAN Flexible Data Rate (CAN-FD) bit rates up to 5Mbit/s. It provides differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2, ISO 11898-5, ISO 11898-6 and ISO/DIS 11898-2: 2016 compliant.

The integrated CAN transceiver supports four operating modes: TRX Normal, TRX Silent, TRX Standby and TRX Biased Standby (see Figure 2-2). The CAN transceiver operation mode depends on the device operation mode and on the setting of bits COPM in the CAN mode control register (see section 2.2.7.1 TRXCR – CAN Transceiver Control Register (address 0x20)). When the device is in Normal mode, all four operation modes can be selected. The TRX biased Standby mode cannot be selected via the COPM bits directly. Refer to section2.2.3 TRX Biased Standby Mode. The operating modes of the integrated transceiver can be selected via bits COPM in the CAN mode control register (see section 2.2.7.1 TRXCR – CAN Transceiver Control Register (address 0x20)). When the device is in Standby or Sleep mode, the transceiver is either in TRX Standby mode or in TRX Biased Standby mode.

The CAN transceiver supports autonomous bus biasing according to ISO 11898-2: 2016. It is active in CAN TRX Standby mode. The bus is biased to 2.5V if there is activity on the bus (TRX Biased Standby mode). In TRX Biased Standby mode, the CAN bias voltage is derived directly from V_{VS}. If there is no activity on the bus for $t > t_{Silence}$, the bus is biased to GND (TRX Standby mode).

In other transceiver active operation modes, namely TRX Normal or TRX Silent mode, the bus pins CANH and CANL are biased to 2.5V (see section 2.2.7.1 TRXCR – CAN Transceiver Control Register (address 0x20)). The CAN bias voltage is derived from V_{VCC} in TRX Normal mode and derived from V_{VS} in TRX Silent mode. In TRX off mode, the bus pins are highly resistive and the transceiver is disengaged from the bus.

Figure 2-2. Overview to the Integrated CAN TRX Operation Modes



2.2.1 TRX Off Mode

The CAN transceiver is completely switched off in the TRX Off mode. The CAN bus pins CANH and CANL are highly resistive and RXD pin is at the VIO level.

As shown in Figure 2-2 the integrated CAN transceiver will enter the TRX Off mode in following cases:

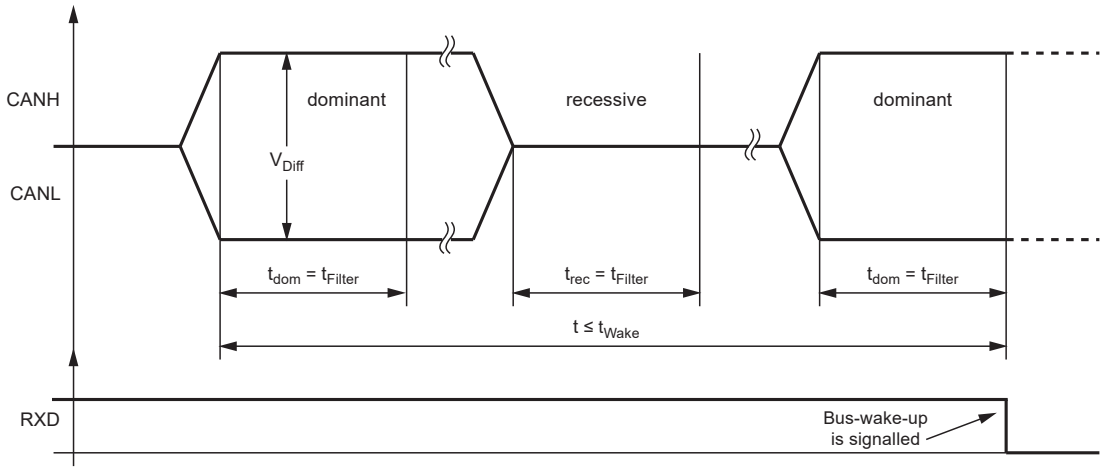
1. The device switches to Power-Off mode,
2. The device switches to Overtemp mode; or,
3. V_{VS} falls below the CAN undervoltage detection threshold $V_{VS\_UV\_CAN\_Set}$

It will be switched on again and enters CAN TRX Standby mode when V_{VS} rises above the CAN undervoltage release threshold, and the device is no longer in Power-off/ Overtemp mode.

2.2.2 TRX Standby Mode

In TRX Standby mode, the transmitter and the receiver are switched off to reduce current consumption. The wake-up comparator monitors the bus lines for a valid remote bus wake-up pattern (WUP), provided CAN bus wake-up detection is enabled (CWUE=1). Two periods of dominant bus levels, separated by a period of recessive bus level each of at least t_{Filter} switches the RXD pin to low to signal a wake-up request to the microcontroller. Figure 2-3 describes the process and timing of the WUP detection. In the TRX Standby mode the bus lines are biased to ground to reduce current consumption to a minimum.

Figure 2-3. Timing of CAN Standard Wake-Up via Wake-Up Pattern (WUP)



As shown in Figure 2-2, the CAN transceiver will enter the TRX Standby mode in the following cases:

1. When the device leaves Power off mode or Overtemp mode and sufficient V_{VS} is applied; or,
2. Any of the conditions for CAN TRX Biased Standby mode are valid for longer than $t_{Silence}$ (see section 2.2.3 TRX Biased Standby Mode).

2.2.3 TRX Biased Standby Mode

The CAN transceiver behavior in the TRX Biased Standby mode is basically the same as in the TRX Standby mode. The only difference is that in the TRX Biased Standby mode the bus pins are biased to 2.5V. The integrated CAN transceiver will enter this mode when activity is detected on the CAN bus while the transceiver is in TRX Standby mode. The transceiver will return to TRX Standby mode if the CAN bus is silent for longer than $t_{Silence}$ (see section 2.5 WUP Detection and Bias Control).

As shown in Figure 2-2 the CAN transceiver will enter the TRX Biased Standby mode in following cases:

1. From TRX Silent/Normal/Reduced normal mode, when $t_{Silence}$ time-out is not detected and the device is in Standby (DOPM = 100) or Sleep mode (DOPM = 001),
2. From TRX Silent/Normal/Reduced normal mode, when $t_{Silence}$ time-out is not detected and the device is in Normal mode (DOPM = 111) and the COPM is set to TRX Standby mode (COPM = 00),
3. From TRX Normal/Reduced normal mode (COPM = 01), when VCC < $V_{VCC\_UV\_Set}$ is detected and $t_{Silence}$ time out is not detected,
4. From TRX Standby mode when the device is in Normal mode (DOPM = 111), COPM is set to TRX Normal mode (COPM = 01) and VCC < $V_{VCC\_TX\_Sd}$ has been detected; or,
5. From TRX Standby mode when a wake-up event is detected on the CAN bus.

2.2.4 TRX Silent Mode

The TRX Silent mode is a receive-only mode of the CAN transceiver. For instance, it can be used to test the connection of the bus medium or for the software-driven selective wake-up. In the TRX Silent mode

the device can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state. All other IC functions continue to operate as they do in the TRX Normal mode. CAN biasing remains active. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.
As shown in Figure 2-2 the CAN transceiver will enter the TRX Silent mode in following cases:

1. The device is in Normal mode (DOPM = Normal) and CAN transceiver is in TRX Silent mode (COPM = TRX Silent)
2. The device is in Normal mode and CAN transceiver is in TRX Normal mode and a RXD recessive clamping failure is detected

It will remain in TRX Silent mode if VCC undervoltage or an RXD recessive clamping failure is detected, even if CAN TRX Normal mode is selected in device Normal mode.

2.2.5 TRX Normal Mode

In the TRX Normal mode the integrated transceiver is able to transmit and receive data via the CANH and CANL bus lines. The output driver stage is active and drives data from the TXD input to the CAN bus. The receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of V_{VCC} is active.

The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible electromagnetic emission (EME).

As shown in Figure 2-2 the CAN transceiver will enter the TRX Normal mode in following cases:

1. The device is in Normal mode (DOPM = Normal) **AND** the CAN transceiver has been enabled by setting bits COPM to ‘01’ or ‘10’ **AND** no VCC undervoltage is detected **AND** no RXD recessive clamping is detected;
2. The transceiver is in the TRX Reduced Normal mode and $V_{VCC} > V_{VCC\_TX\_Sd}$ for $t > t_{SUP\_UV\_filter}$

If pin TXD is held low (e.g., by a short-circuit to GND) when CAN TRX Normal mode is selected via bits COPM, the transceiver will not enter CAN TRX Normal mode but will switch to or remain in TRX Silent mode. It will remain in TRX Silent mode until pin TXD goes high in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

The application can determine whether the CAN transceiver is ready to transmit data or is disabled by reading the CAN Transmitter Status bit (TXS) in the Transceiver Status Register (see section 2.2.7.2 TRXSR – CAN Transceiver Status Register (address 0x22)).

2.2.6 TRX Reduced Normal Mode

In the TRX Reduced Normal mode, the transmitter is switched off as VCC is lower than the $V_{VCC\_TX\_Sd}$ threshold. All other features available in the TRX Normal mode are also provided in the TRX Reduced Normal mode.

As shown in Figure 2-2 the CAN transceiver will enter the TRX Reduced Normal mode when the transceiver is in TRX Normal mode and $V_{VCC} < V_{VCC\_TX\_Sd}$ for $t > t_{SUP\_UV\_filter}$.

2.2.7 Related Registers

2.2.7.1 TRXCR – CAN Transceiver Control Register (address 0x20)

Bit	7	6	5	4	3	2	1	0	
	-	**CFDPE**	**PNCFOK**	**CPNE**	**-**	**-**	**COPM[1:0]**		**TRXCR**

Read /Write	R	R/W	R/W	R/W	R	R	R/W	R/W
Initial Value	0	1	0	0	0	0	0	1

Bit 7: Reserved for future use

Bit 6: CFDPE The external microcontroller should set the bit to ‘1’, if CAN FD frames should be ignored in Sleep mode with selective wake-up activated. When this bit is set to "0", CAN FD frames are interpreted by the ATA6570 as frames with errors, and the error counter will be incremented when a CAN FD frame is received when the device is in Sleep mode and the selective wake-up is activated. By default, the bit is set to 1 after power-on reset. The bit shall be set to 1 for continuous sending "dom-rec" bits with a bitrate higher than 1Mbit/s.

Bit 5: PNCFOK The external microcontroller should set the bit to ‘1’ after successfully configuring the partial networking registers, and to ‘0’ vice versa. In addition, the device will reset the bit to 0 automatically after any write access to the partial networking configuration related registers.

Bit 4: CPNE The external microcontroller should set the bit to ‘1’ to enable selective wake-up and to ‘0’ vice-versa.

Bit 3..2: Reserved for future use

Bit 1..0: COPM The TRXCR register is a control register. Therefore, the state of the transceiver will not be mirrored to this register. COPM bit only defines the expected state of the transceiver when the device is switched to Normal mode. The finite state machine in Figure 2-2 will not change the COPM bits. [1:0] – Select CAN Transceiver operation mode:

COPM[1:0]	CAN TRX Operation Mode
2’b00	TRX Standby mode
2’b01	TRX Normal mode (when DOPM = Normal), VCC undervoltage detection active for the transceiver finite state machine. The transceiver switches to the TRX biased Standby mode immediately after detecting the VCC undervoltage.
2’b10	TRX Normal mode (when DOPM = Normal), VCC undervoltage detection inactive for the transceiver finite state machine. The transceiver switches from TRX Normal/Reduced Normal mode to TRX biased Standby mode when the device is forced to Sleep mode by a VCC undervoltage event.
2’b11	TRX Silent mode

2.2.7.2 TRXSR – CAN Transceiver Status Register (address 0x22)

Bit	7	6	5	4	3	2	1	0	
	TXS	**PNERRS**	**PNCFS**	**PNOSCS**	**CBSS**	**-**	**VCCS**	**TXDOUT**	**TRXSR**
Read/Write	R	R	R	R	R	R	R	R	

Initial Value	0	1	0	0	1	0	0	0	

Bit 7: TXS Transmitter status, the device sets the bit to ‘1’ if the transmitter is ready to transmit data and to ‘0’ if CAN transmitter is disabled.

Bit 6: PNERRS Partial networking error detection status, the device sets the bit to ‘0’ if no CAN partial networking error detected (PNEFD = 0 & PNCFOK = 1 & no oscillator hardware failure detected (default)), to ‘1’ vice-versa (PNEFD = 1 || PNCFOK = 0).

Bit 5: PNCFS Partial networking configuration status, the device sets the bit to ‘0’ if partial networking configuration error is detected (PNCFOK = 0), to ‘1’ vice-versa.

Bit 4: PNOSCS Partial networking oscillator ok, the device sets the bit to ‘1’ if CAN partial networking oscillator is running at target frequency, to ‘0’ vice-versa.

Bit 3: CBSS Bus status, the device sets the bit to ‘1’ if CAN bus is inactive (for longer than $t_{Silence}$), to ‘0’ vice-versa.

Bit 2: Reserved for future use

Bit 1: VCCS V_{VCC} status, the device sets the bit to ‘1’ if V_{VCC} is below the undervoltage detection threshold, to ‘0’ vice-versa.

Bit 0: TXDOUT TXD time out status, the device sets the bit to ‘1’ if CAN transmitter is disabled due to a TXD dominant timeout event, to ‘0’ if no TXD dominant timeout event was detected.

2.2.7.3 BFIR - Bus Failure Indication Register (address 0x33)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**-**	**-**	**-**	**BOUT**	**BSC**	**BFIR**
Read /Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: Reserved for future use

Bit 1: BOUT, bus dominant timeout event indicator, the BOUT bit shows the current status of the bus dominant timeout detection. If the bit reads ‘1’ the bus is currently in dominant timeout state; otherwise the bit reads ‘0’.

Bit 0: BSC, bus short-circuit event capture indicator, the BSC bit shows the current status of the bus short-circuit event detection. If the bit reads ‘1’ the bus is currently in short-circuit state; otherwise the bit reads ‘0’.

2.2.7.4 TRXESR2 – Transceiver Event Status Register 2 (address 0x35)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**-**	**-**	**-**	**-**	**RXDRCS**	**TRXESR2**
Read /Write	R	R	R	R	R	R	R	R	

Initial Value	0	0	0	0	0	0	0	0

Bit 7..1: Reserved for future use

Bit 0: RXDRCS RXD recessive clamping status, the device sets the bit to '1' if the event is enabled in the TRXECR2 register and a RXD recessive clamping event is detected. The bit is reset to '0' by the device either when the device enters Sleep, Standby or Unpowered mode, or the RXD pin shows dominant again.

2.3 Wake-Up

2.3.1 Local Wake-Up via Pin WAKE

The device provides the high-voltage WAKE input pin that can be used to wake-up the device. It is an edge-sensitive pin (low-to-high or high-to-low transition). Thus, even if the WAKE pin is at high or low voltage, it is possible to switch the IC into Sleep mode. It is usually connected to the ignition for generating a local wake-up in the application if the ignition is switched on.

A glitch-suppression circuit is integrated to avoid unexpected wake-up on the WAKE pin. The voltage on the pin is detected as stable only when the level remains stable for t_{local_wu}. Therefore, a local wake-up request is detected when the logic level on the pin WAKE has been already stable for at least t_{local_wu} and the new level remains stable for at least t_{local_wu}.

Local wake-up via pin WAKE can be enabled/disabled via the register bits LWUFE and LWURE (see section 2.3.5.25 WKECR – WAKE Event Capture Enable Register (address 0x4C)) and the logic level at pin WAKE can be read via the register PWKS (see section 2.3.5.16 PWKS – Pin WAKE Status Register (address 0x4B)) if a valid interface voltage V_{VIO} is provided.

To reduce the battery current during low-power mode, the WAKE pin has internal pull-up/pull-down currents that are activated when a stable level at the wake pin has been detected:

- High level on pin is followed by an internal pull up towards VS.
- Low level is followed by an internal pull down toward GND.

Local wake-up can only be activated in Standby and Sleep mode. In Normal mode, the status of the voltage on pin WAKE can always be read via bit PWKVS. Otherwise, PWKVS is only valid if local wake-up is enabled.
In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin should be connected to GND to ensure optimal EMI performance.

2.3.2 Remote Wake-Up Pattern According to ISO 11898-2: 2016 (Partial Networking Disabled)

If the CAN transceiver is in TRX Standby mode and CAN bus wake-up is enabled (CWUE = 1), but CAN selective wake-up is disabled (CPNE = 0 or PNCFOK = 0), the device will monitor the bus for a standard wake-up pattern as specified in ISO11898-2: 2016.

This filtering helps avoid spurious wake-up events, which could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise, spikes on the bus, transients or EMI.

The wake-up pattern consists of multiple consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bits in between the above-mentioned phases that are shorter than t_{Filter} are ignored.

The complete dominant-recessive-dominant pattern, as shown in Figure 2-3, must be received within t_{Wake} to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event.

When a valid CAN WUP is detected on the bus, the wake-up bit CWUS in the transceiver event status register is set (see section 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63)) and pin RXD is driven low. If the device was in Sleep mode when the wake-up event was detected, it will switch pin INH to VS to activate external voltage regulators (e.g., for supplying VCC and VIO) and enter Standby mode.

CAN wake-up via WUP can only be disabled via bit CWUE. If CWUE is set to '0', no remote wake-up via the CAN bus is possible. If CWUE is set to '1' and selective wake-up is disabled, the device will switch to Standby mode after detecting the wake-up pattern (WUP), coming from Sleep mode. If CWUE is set to '1' and the selective wake-up is enabled, the device will first switch on the bus biasing after detecting the WUP and will only switch afterward to the Standby mode, when it detects a valid WUF (please refer to the next section for WUF).

2.3.3 Remote Wake-up Frame According to ISO 11898-2: 2016

2.3.3.1 CAN Selective Wake-Up

Partial networking makes it possible for a CAN node or a CAN sub-network to be woken up individually by means of dedicated and predefined frames, the so called wake-up frames (WUF). When a particular node's tasks are not required, it is in selective Sleep mode.

The transceiver monitors the bus for dedicated CAN wake-up frames, when both CAN wake-up (CWUE = '1') and CAN selective wake-up (CPNE = '1') are enabled, and the partial networking registers are configured correctly (PNCFOK = '1'). An accurate oscillator and a low-power, high-speed comparator are running: in this case, to support the correct detection of the wake-up frame.

According to ISO11898-1 a wake-up frame is a CAN frame consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up CAN frame (ID and data) is fully configurable via SPI communication. A standard (11-bit) or extended (29-bit) identifier, for the wake-up frame format, can be selected via bit IDE in the Frame control register CFCR (see section 2.3.5.10 CFCR - CAN Frame Configuration Register (address 0x2F)).

In the ID registers (see section 2.3.5.2 CIDR0 - CAN ID Register 0 (address 0x27) to section 2.3.5.5 CIDR3 - CAN ID Register 3 (address 0x2A)) a valid WUP can be defined and stored. To allow a group of identifiers to be recognized as valid by an individual node. An ID mask (see section 2.3.5.6 CIDMR0 - CAN ID Mask Register 0 (address 0x2B) to section 2.3.5.9 CIDMR3 - CAN ID Mask Register 3 (address 0x2E)) can be defined in the mask registers, where a 1 means 'don't care'.

A single wake-up frame can wake-up multiple groups of nodes by comparing the incoming data field with the data mask, as the data field indicates which nodes are to be woken up. Groups of nodes can be predefined and associated with bits in a data mask.

The number of data bytes expected in the data field of a CAN wake-up frame are set with the data length code (bits DLC in the frame control register in section 2.3.5.10 CFCR - CAN Frame Configuration Register (address 0x2F)). If DLC ≠ 0000 (one or more data bytes expected), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (register for data mask to be defined) must also be set to 1 for a successful wake-up. Each matching pair of logic 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

If DLC = 0000, a node will wake-up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are 1 per default). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes will be woken up. The data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0 (see section 2.3.5.10 CFCR - CAN Frame Configuration Register (address 0x2F)), only the identifier field is evaluated to determine if the frame contains a valid wake-up frame. If PNDM = 1 (the default value), the data field is included as part of the wake-up filtering.

When PNDM = 0, a valid wake-up frame is detected and a wake-up event is captured (and CWUS is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error.

When PNDM = 1, a valid wake-up frame is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND
- the data length code in the received frame matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

The internal error counter will be incremented when an erroneous CAN frame (e.g., a "stuffing" error) is received prior to the ACK field. If a CAN frame is received without any errors appearing in front of the ACK field, the counter will be decremented. Any data received after the CRC delimiter and before the next SOF will be ignored by the partial networking module. If the counter overflows (FEC > ERRCNT, see section 2.3.5.11 EFCR - Error Frame Counter Threshold Register (address 0x3A)), a frame detect error is captured (PNEFD = 1, see section 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63)) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

If partial networking is assumed to be configured correctly, the PNCFOK has to be set to 1 by the application software. The PNCFOK will be cleared after a write access to any of the CAN partial networking configuration registers (see section 2.3.5.1 DRCR - Data Rate Configuration Register (address 0x26) to 2.3.5.14 CDMR0..7 - CAN Data Mask Registers 0...7 (address 0x68…0x6F)).

Any valid wake-up pattern (according to ISO 11898-2: 2016) will trigger a wake-up event, if selective wake-up is disabled (CPNE = 0) or partial networking is not configured correctly (PNCFOK = 0), and the CAN transceiver is in TXD Standby mode with wake-up enabled (CWUE = 1).

All wake-up patterns will be ignored, if the CAN transceiver is in TRX Normal/Silent mode or CAN wake-up is disabled (CWUE = 0).

2.3.3.2 CAN Selective Wake-Up and CAN FD

CAN Flexible Data Rate (CAN FD) is an improved CAN protocol in regards of bandwidth and payload. As specified in ISO 11898-1: 2015, CAN FD is based on the CAN protocol and still uses the CAN bus arbitration method. However, after the arbitration phase of a classical CAN frame, the data rate is

increased and the data bits are transferred with a higher bit rate than in the arbitration phase and returns to the longer bit time at the CRC Delimiter, before the controllers transmit their acknowledge bits. Besides the increased bit speed, the new CAN FD allows data frames up to 64 bytes compared with the maximum of 8 bytes with classical CAN.

The ATA6570 can be configured to recognize CAN FD frames as valid frames. When CFDPE = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The device remains in Sleep mode with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the device ignores further bus signals until idle is again detected.

When CFDPE is set to 0, CAN FD frames are interpreted as frames with errors by the partial networking module. So the error counter is incremented when a CAN FD frame is received. Bit PNEFD is set to 1 and the device wakes up if the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow.

2.3.4 Wake-Up via SPI

In case of an SPI command while the system is in a low-power mode, but with enabled SPI interface, the device will be woken up and enter the operation mode issued together with the SPI command. An SPI command failure, for instance invalid length of SPI command, write access to read-only register and so forth, and will also trigger an interrupt event of the device (see Wake-Up Events).

2.3.5 Related Registers for Configuring the CAN Partial Networking

2.3.5.1 DRCR - Data Rate Configuration Register (address 0x26)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	DR[2:0]			DRCR
Read /Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	1	0	1	

Bit 7..4: Reserved for future use

Bit 2..0: DR[2:0] – Select CAN data rate

DR[2:0]	CAN Data Rate (Kbit/s)
3’b000	50
3’b001	100
3’b010	125
3’b011	250
3’b100	Reserved (intended for future use; currently selects 500Kbit/s)
3’b101	500
3’b110	Reserved (intended for future use; currently selects 500Kbit/s)
3’b111	1000

2.3.5.2 CIDR0 - CAN ID Register 0 (address 0x27)

Bit	7	6	5	4	3	2	1	0	
	ID0[7:0]								CIDR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: ID0 bits ID07 to ID00 of the extended frame format

2.3.5.3 CIDR1 - CAN ID Register 1 (address 0x28)

Bit	7	6	5	4	3	2	1	0	
	ID1[7:0]								CIDR1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: ID1 bits ID15 to ID08 of the extended frame format

2.3.5.4 CIDR 2 - CAN ID Register 2 (address 0x29)

Bit	7	6	5	4	3	2	1	0	
	ID2[7:0]								CIDR2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: ID2 bits ID23 to ID18 of the extended frame format; bits ID05 to ID00 of the standard frame format

Bit 1..0: ID2 bits ID17 to ID16 of the extended frame format

2.3.5.5 CIDR3 - CAN ID Register 3 (address 0x2A)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	ID3[4:0]					CIDR3
Read /Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..5: Reserved for future use

Bit 4..0: ID3 bits ID28 to ID24 of the extended frame format, bits ID10 to ID06 of the standard frame format

2.3.5.6 CIDMR0 - CAN ID Mask Register 0 (address 0x2B)

Bit	7	6	5	4	3	2	1	0	
	IDM0[7:0]								CIDMR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: IDM0 Mask bits ID07 to ID00 of the extended frame format. 1 means ‘don't care’.

2.3.5.7 CIDMR1 - CAN ID Mask Register 1 (address 0x2C)

Bit	7	6	5	4	3	2	1	0	
	IDM1[7:0]								**CIDMR1**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: IDM1 Mask bits ID15 to ID08 of the extended frame format. 1 means ‘don't care’.

2.3.5.8 CIDMR2 - CAN ID Mask Register 2 (address 0x2D)

Bit	7	6	5	4	3	2	1	0	
	IDM2[7:0]								**CIDMR2**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: IDM2 Mask bits ID23 to ID18 of the extended frame format; bits ID05 to ID00 of the standard frame format

Bit 1..0: IDM2 Mask bits ID17 to ID16 of the extended frame format. 1 means ‘don't care’.

2.3.5.9 CIDMR3 - CAN ID Mask Register 3 (address 0x2E)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**IDM3[4:0]**					**CIDMR3**
Read /Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..5: Reserved for future use

Bit 4..0: IDM3 Mask bits ID28 to ID24 of the extended frame format, bits ID10 to ID06 of the standard frame format. 1 means ‘don't care’.

2.3.5.10 CFCR - CAN Frame Configuration Register (address 0x2F)

Bit	7	6	5	4	3	2	1	0	
	IDE	**PNDM**	**-**	**-**	**DLC[3:0]**				**CFCR**
Read /Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	1	0	0	0	0	0	0	

Bit 7: IDE Identifier format, the external microcontroller should set the bit to ‘1’ if identifier is in extended frame format (29-bit), set to ‘0’ if identifier is in standard frame format (11-bit)

Bit 6: PNDM Partial networking data mask, the external microcontroller should set the bit ‘1’ if data length code and data field are evaluated at wake-up, set to ‘0’ if data length code and data field are ‘don’t care’ for wake-up

Bit 5..4: Reserved for future use

Bit 3..0: DLC[3:0] Data length configuration, select number of data bytes expected in a CAN frame

DLC[3:0]	Number of Data Bytes
4’b0000	0
4’b0001	1
4’b0010	2
4’b0011	3
4’b0100	4
4’b0101	5
4’b0110	6
4’b0111	7
4’b1000	8
4’b1001 to 4’b1111	Tolerated, 8 bytes expected; DM0 (data mask 0) ignored

2.3.5.11 EFCR - Error Frame Counter Threshold Register (address 0x3A)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	EERCNT					EFCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	1	1	1	1	1	

Bit 7..5: Reserved for future use

Bit 4:0: Set the error frame counter overflow threshold. If the counter overflows (counter > ERRCNT), a frame detect error is captured (PNEFD = 1) and the device wakes up.

2.3.5.12 FECR – Failure Error Counter Register (address 0x3B)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	FEC					FECR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..5: Reserved for future use

Bit 4:0: If the device receives a CAN frame containing errors (e.g., a ‘stuffing’ error) that are received in advance of the ACK field, an internal error counter is incremented. If a CAN frame is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC

delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (FEC > ERRCNT, see section 2.3.5.12 FECR – Failure Error Counter Register (address 0x3B)), a frame detect error is captured (PNEFD = 1, see section 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63)) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

2.3.5.13 GLFT – Glitch Filter Threshold Register (address 0x67)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	GLF[2:0]			GLFT
Read /Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	1	0	

Bit 7..3: Reserved for future use

Bit 2..0: Set the glitch filter threshold from 5% to 55% of the arbitration bit rate.

GLF[2:0]	#samples(≤500Kbit/s)	#samples(1Mbit/s)
3'b000	1 [<2.42%/<5.17%]	1 [<4.83%/<10.35%]]
3'b001	2 [<4.83%/<7.76%]	2 [<9.66%/<15.52%]
3'b010	3 [<7.25%/<10.35%]	3 [<14.49%/<20.7%]]
3'b011	4 [<9.66%/<12.94%]	4 [<19.32%/<20.87%]
3'b100	5 [<12.08%/<15.52%]	5 [<24.15%/<31.05%]
3'b101	6 [<14.49%/<18.11%]	6 [<28.99%/<36.22%]
3'b110	7 [<16.91%/<20.7%]	7 [<33.82%/<41.40%]
3'b111	24 [<57.97%/<64.69%]	13 [<62.8%/<72.45%]

Assumption: clock tolerance ±3%; transmitter ±0.5% tolerance

2.3.5.14 CDMR0..7 - CAN Data Mask Registers 0...7 (address 0x68…0x6F)

Bit	7	6	5	4	3	2	1	0	
	DM0…7[7:0]								CDMR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

Bit 7..0: DM0…7[7:0] data mask 0…7 configuration

Table 2-2. Data Mask and the CAN Data Filed

CAN frame	...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC	...
Data mask	DLC > 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame	...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC	...
Data mask	DLC = 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame	...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC	...
Data mask	DLC = 7			DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame		...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	CRC	...
Data mask	DLC = 6				DM2	DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame			...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	CRC	...
Data mask	DLC = 5					DM3	DM4	DM5	DM6	DM7	CRC	...
CAN frame				...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	CRC	...
Data mask	DLC = 4						DM4	DM5	DM6	DM7	CRC	...
CAN frame					...	DLC	Byte 0	Byte 1	Byte 2	Byte 3	CRC	...
Data mask	DLC = 3							DM5	DM6	DM7	CRC	...
CAN frame						...	DLC	Byte 0	Byte 1	Byte 2	CRC	...
Data mask	DLC = 2								DM6	DM7	CRC	...
CAN frame							...	DLC	Byte 0	Byte 1	CRC	...
Data mask	DLC = 1									DM7	CRC	...
CAN frame								...	DLC	Byte 0	CRC	...
DM x												
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0					
Byte x												
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0					

2.3.5.15 BFECR - Bus Failure Event Capture Enable Register (address 0x32)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**-**	**-**	**-**	**BOUTE**	**BSCE**	**BFECR**
Read /Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: Reserved for future use

Bit 1: BOUTE, bus dominant timeout event capture enable, the BOUTE bit must be set to ‘1’ to enable the bus dominant timeout detection. Setting the bit to `0` disables the bus dominant timeout detection.

Bit 0: BSCE, bus short-circuit event capture enable, the BSCE bit must be set to ‘1’ to enable the bus short-circuit event detection. Setting the bit to `0` disables the bus short-circuit event detection.

2.3.5.16 PWKS – Pin WAKE Status Register (address 0x4B)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	-	PWKVS	-	PWKS
Read /Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: Reserved for future use

Bit 1: PWKVS Pin WAKE voltage status, the device sets the bit to ‘1’ if WAKE is high, to ‘0’ if WAKE is low. PWKVS is always “0” in power-down mode if local wake-up is disabled.

Bit 0: Reserved for future use

2.3.5.17 GESR – Global Event Status Register (address 0x60)

Bit	7	6	5	4	3	2	1	0	
	OSCS	-	BFES	-	WKES	TRXES	-	SYSES	GESR
Read /Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	1	

Bit 7: System oscillator status, the device sets the bit to ‘1’ if a hardware failure of the system oscillator is detected and sets the bit to ‘0’ when the system oscillator is disabled for power saving purpose or the hardware failure disappeared after the oscillator is enabled (for instance, in device Normal mode).

Bit 6: Reserved for future use

Bit 5: Bus failure event status, the device sets the bit to ‘1’ if there is bus failure event pending (any bit in the BFESR register is ‘1’). The bit reads ‘0’ if all status bits in the BFESR register are cleared.

Bit 4: Reserved for future use

Bit 3: WKES WAKE event status, the device sets the bit to ‘1’ if there is a wake pin event pending (any bit in the WKESR register is ‘1’). The bit reads ‘0’ if all status bits in the WKESR register are cleared.

Bit 2: TRXES Transceiver event status, the device sets the bit to ‘1’ if there is a transceiver event pending (any bit in the TRXESR register is ‘1’). The bit reads ‘0’ if all status bits in the TRXESR register are cleared.

Bit 1: Reserved for future use

Bit 0: SYSES System event status, the device sets the bit to ‘1’ if there is a system event pending (any bit in the SESR register is ‘1’). The bit reads ‘0’ if all status bits in the SESR register are cleared.

2.3.5.18 SESR – System Event Status Register (address 0x61)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	PWRONS	-	OTPW	SPIFS	-	SESR
Read /Write	R	R	R	R/W	R	R/W	R/W	R	

Initial Value	0	0	0	1	0	0	0	0

Bit 7..5: Reserved for future use

Bit 4: PWRONS Power-on status, the device sets the bit to ‘1’ if the device has left Power-off mode after power-on. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. PWRONS is also cleared when the device is forced to Sleep mode due to an undervoltage event. The information stored in PWRONS could be lost in this case. Bit NMTS in the Device Mode Status Register (DMSR), which is set to 0 when the device switches to Normal mode after power-on, compensates for this.

Bit 3: Reserved for future use

Bit 2: OTPW Overtemperature prewarning status, the device sets the bit to ‘1’ if the event is enabled in the SECR register and the chip temperature has exceeded the overtemperature prewarning threshold. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. OTPW is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 1: SPIFS SPI failure status, the device sets the bit to ‘1’ if the event is enabled in the SECR register and an SPI failure is detected. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. SPIFS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 0: Reserved for future use

2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**PNEFD**	**BS**	**-**	**-**	**TRXF**	**CWUS**	**TRXESR**
Read /Write	R	R	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7...6: Reserved for future use

Bit 5: PNEFD Partial networking frame detection status, the device sets the bit to ‘1’ if a partial networking frame detection error is detected (error counter overflow). The bit can be reset to ‘0’ by writing a ‘1’ to the bit. PNEFD is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 4: BS Bus status, the device sets the bit to ‘1’ if the event is enabled in the TRXECR register and no activity on CAN bus is detected for $t_{Silence}$. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. BS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 3..2: Reserved for future use

Bit 1: TRXF Transceiver failure status, the device sets the bit to ‘1’ if the event is enabled in the TRXECR register and a CAN failure event was detected. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. TRXF is also cleared when the device is forced to Sleep mode due to an undervoltage event.
TRXF is triggered if:

- TXD is clamped dominant and system is in TRX Normal mode
- a VCC undervoltage is detected, COPM = 01 and system is in TRX Normal or TRX Reduced Normal mode

- a RXD recessive clamping error is detected and system is in TRX Normal or TRX Silent mode.

The RXD recessive clamping error detection must additionally be enabled in the TRXECR2 register.

Bit 0: CWUS CAN wake-up status, the device sets the bit to ‘1’ if the event is enabled in the TRXECR register and a CAN wake-up event was detected. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. CWUS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

2.3.5.20 WKESR – WAKE Event Status Register (address 0x64)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	-	LWURS	LWUFS	WKESR
Read /Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: Reserved for future use

Bit 1: LWURS Local Wake-up Rising Edge Status, the device sets the bit to ‘1’ if the event detection is enabled in the WKECR register and a rising edge on the WAKE pin is detected. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. LWURS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

Bit 0: LWUFS Local Wake-up Falling Edge Status, the device sets the bit to ‘1’ if the event detection is enabled in the WKECR register and a falling edge on WAKE pin is detected. The bit can be reset to ‘0’ by writing a ‘1’ to the bit. LWUFS is also cleared when the device is forced to Sleep mode due to an undervoltage event.

2.3.5.21 BFESR - Bus Failure Event Indication Status Register (address 0x65)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	-	BOUTS	BSCS	BFESR
Read /Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: Reserved for future use

Bit 1: BOUTS bus dominant timeout event status bit, the device sets the bit to ‘1’ if a bus dominant timeout event is detected. The bit is set to ‘0’ by writing ‘1’ to the bit via SPI.

Bit 0: BSCS device bus short-circuit event status bit, the device sets the bit to ‘1’ if a bus short-circuit event is detected. The bit is set to ‘0’ by writing ‘1’ to the bit via SPI.

2.3.5.22 SECR – System Event Capture Enable Register (address 0x04)

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	-	OTPWE	SPIFE	-	SECR
Read /Write	R	R	R	R	R	R/W	R/W	R	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..3: Reserved for future use

Bit 2: OTPWE overtemperature prewarning event capture, the OTPWE bit must be set to ‘1’ to enable the overtemperature prewarning detection. Setting the bit to ‘0’ disables the overtemperature prewarning detection.

Bit 1: SPIFE SPI failure event capture, the SPIFE bit must be set to ‘1’ to enable the SPI failure detection. Setting the bit to ‘0’ disables the SPI failure detection.

Bit 0: Reserved for future use

2.3.5.23 TRXECR – Transceiver Event Capture Enable Register (address 0x23)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**BSE**	**-**	**-**	**TRXFE**	**CWUE**	**TRXECR**
Read/Write	R	R	R	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7...5: Reserved for future use

Bit 4: BSE Bus status capture enable, the BSE bit must be set to ‘1’ to enable the CAN bus silence detection. Setting the bit to ‘0’ disables the CAN bus silence detection.

Bit 3..2: Reserved for future use
Bit 1: TRXFE Transceiver failure status capture enable, the TRXFE bit must be set to ‘1’ to enable the CAN failure detection. Setting the bit to ‘0’ disables the CAN failure detection.

Bit 0: CWUE CAN bus wake-up detection enable, the CWUE bit must be set to ‘1’ to enable the CAN wake-up detection. Setting the bit to ‘0’ disables the CAN wake-up detection. At an undervoltage event the bit is set to ‘1’ automatically.

2.3.5.24 TRXECR2 – Transceiver Event Capture Enable Register 2 (address 0x34)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**-**	**-**	**-**	**-**	**RXDRCE**	**TRXECR2**
Read/Write	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..1: Reserved for future use

Bit 0: RXDRCE RXD recessive clamping capture enable, the RXDRCE bit must be set to ‘1’ to enable the RXD recessive clamping detection. Setting the bit to ‘0’ disables the RXD recessive clamping detection.

2.3.5.25 WKECR – WAKE Event Capture Enable Register (address 0x4C)

Bit	7	6	5	4	3	2	1	0	
	-	**-**	**-**	**-**	**-**	**-**	**LWURE**	**LWUFE**	**WKECR**
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..2: Reserved for future use

Bit 1: LWURE The bit must be set to “1” to enable the WAKE pin rising edge detection interrupt. Setting the bit to “0” disables the interrupt. The LWURE bit is set automatically before a sleep mode is activated due to an undervoltage event.

Bit 0: LWUFE The bit must be set to “1” to enable the WAKE pin falling edge detection interrupt. Setting the bit to “0” disables the interrupt. The LWUFE bit is set automatically before a sleep mode is activated due to an undervoltage event.

2.3.5.26 DIDR – Device ID Register (address 0x7E)

Bit	7	6	5	4	3	2	1	0	
	DID[7:0]								**DIDR**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	1	1	1	0	1	0	0	

Bit 7..0: The device ID is 0x74 for ATA6570.

2.3.5.27 RWPR – Register Write Protection Register (address 0x0A)

Bit	7	6	5	4	3	2	1	0	
	-	**WP6**	**WP5**	**WP4**	**WP3**	**WP2**	**WP1**	**WP0**	**RWPR**
Read /Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7: Reserved for future use

Bit 6: address area 0x67 to 0x6F – partial networking data byte registers, the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice-versa

Bit 5: address area 0x50 to 0x5F – the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice-versa

Bit 4: address area 0x40 to 0x4F– WAKE pin configuration, the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice- versa

Bit 3: address area 0x30 to 0x3F– the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice-versa

Bit 2: address area 0x20 to 0x2F– transceiver control and partial networking, the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice-versa

Bit 1: address area 0x10 to 0x1F – the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice-versa

Bit 0: address area 0x06 to 0x09 – the external microcontroller should set the bit to ‘1’ to enable register write protection, to ‘0’ vice-versa

2.4 Fail-Safe Features

2.4.1 TXD Dominant Timeout Function

A TXD dominant timeout timer is started when the TXD pin is set to low and the transceiver is in TRX Normal mode. If the low state on the TXD pin persists for longer than $t_{to(dom)}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant timeout timer is reset when the TXD pin is set to high. The TXD dominant timeout time also defines the minimum possible bit rate of 4Kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated (TRXF = 1; see section 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63)), if enabled (TRXFE = 1; see section 2.3.5.23 TRXECR – Transceiver Event Capture Enable Register (address 0x23)). In addition, the status of the TXD dominant timeout can be read via the TXDOUT bit in the transceiver status register (see section 2.2.7.2 TRXSR – CAN Transceiver Status Register (address 0x22)) and bit TXS is set to 0. TXDOUT is reset to 0 and TXS is set to 1 when the TXD pin is set to high again.

2.4.2 TXD-to-RXD Short-Circuit Detection

When a short-circuit appears between the RXD and TXD pins, the bus will be locked into a permanent dominant state, due to the typically stronger low-side driver of the RXD pin than the high-side driver of the connected microcontroller to TXD. To prevent such lock-ups, the implemented TXD-to-RXD short-circuit detection disables the transmitter. The TXD-dominant time-out-timer is used to detect this failure, refer to section 2.4.1 TXD Dominant Timeout Function for the behavior in this case. The TXD-dominant time-out-timer is activated when the transceiver is in the TRX normal mode and the TXD pin is low.

2.4.3 Bus Dominant Clamping Detection

A CAN bus short circuit (to VS, VCC or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the Normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The Bus dominant time-out-timer is activated when the transceiver is in the TRX normal mode, the TXD pin is high and the bus is dominant. The timer for detection the bus dominant clamping detection failure will be reset by any signal change at TXD pin or on the CAN bus.
When the bus dominant clamping is detected and the failure detection is enabled (BOUTE = 1; see section 2.3.5.15 BFECR - Bus Failure Event Capture Enable Register (address 0x32)), the bit BOUT and BOUTS is set to 1 by the device and a bus failure interrupt is generated (BFES = 1; see section 2.3.5.17 GESR – Global Event Status Register (address 0x60). The bit BOUT is reset to ‘0’ as soon as the bus state is changed to recessive again. In other words, the status of the bus dominant clamping can be read via the BOUT bit in the bus status register (see section 2.2.7.3 BFIR - Bus Failure Indication Register (address 0x33)).

2.4.4 Bus Recessive Clamping Detection

The bus failure flag (BSC = 1; see section 2.2.7.3 BFIR - Bus Failure Indication Register (address 0x33)) is set, if the failure detection is enabled (BSCE = 1; see section 2.3.5.15 BFECR - Bus Failure Event Capture Enable Register (address 0x32)), when the device detects a CAN bus recessive clamping for $t_{bus\_rec\_clamp}$. In case a bus recessive clamping is detected, the bit BSC and BSCS are set to 1 and a bus failure interrupt is generated (BFES = 1; see section 2.3.5.17 GESR – Global Event Status Register (address 0x60)). The status of the bus recessive clamping failure can be read via the BSC bit in the bus status register. The bit BSC is reset to ‘0’ as soon as the bus state is changed to dominant again.

2.4.5 Internal Pull-up Structure at the TXD Input Pin

The TXD pin has an internal pull-up structure to VIO. This ensures a safe, defined state in case the pin is left floating. The pull-up current flows into the pin in all states, meaning the pin should be in high state during TRX Standby mode to minimize the current consumption.

2.4.6 Undervoltage Detection on Pin VCC

An enabled CAN failure interrupt is generated (TRXF = 1) when the CAN transceiver supply voltage V_{VCC} falls below the undervoltage detection threshold ($V_{VCC\_UV\_Set}$), provided COPM = 01. In addition, status bit VCCS is set to 1 (see section 2.2.7.2 TRXSR – CAN Transceiver Status Register (address 0x22)).

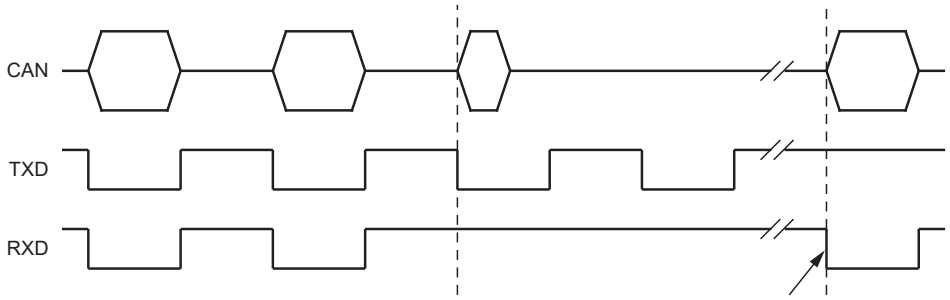
2.4.7 Short-Circuit Protection of the Bus Pins

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage (V_{VS}, V_{VCC}). A current limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

2.4.8 RXD Recessive Clamping

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped to high (e.g., recessive). That is, if the RXD pin cannot signalize a dominant bus condition because it is e.g., shorted to VCC, the transmitter is disabled to avoid possible data collisions on the bus. In TRX Normal mode and TRX Silent mode, the device permanently compares the state of the high-speed comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than $t_{RXD\_rec\_clmp}$ without the RXD pin doing the same, a recessive clamping situation is detected.

Figure 2-4. RXD Recessive Clamping Detection



A CAN transceiver failure interrupt (not denoted at RXD pin) is generated (TRXF = 1; see section 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63)), if enabled (TRXFE = 1 and RXDRCE = 1; see section 2.3.5.23 TRXECR – Transceiver Event Capture Enable Register (address 0x23) and section 2.3.5.24 TRXECR2 – Transceiver Event Capture Enable Register 2 (address 0x34)). In addition, the status of the RXD recessive clamping failure can be read via the RXDRCS bit in the status register (see section 2.2.7.4 TRXESR2 – Transceiver Event Status Register 2 (address 0x35)) and bit TXS is set to 0.
The RXD recessive clamping detection is reset by either entering sleep, or standby or unpowered mode or the RXD pin shows dominant again.

2.4.9 Overtemperature Detection

The device provides two levels of overtemperature protection. In the case that the chip temperature rises above the overtemperature protection prewarning threshold ($T > T_{OT\_Prew}$), the device will first set the status bit OTPWS=1. If the overtemperature prewarning event capture is enabled (OTPWE = 1), COPM is set to 00 (and DOPM is set to 111), an overtemperature prewarning interrupt will be generated

(OTPW = 1). If DOPM is set to 111 but COPM is not 00 and the overtemperature prewarning event capture is enabled (OTPWE = 1), only the overtemperature prewarning flag will be set (OTPW = 1) and no interrupt will be generated. The device will enter the Overtemp mode when the chip temperature rises above the overtemperature protection shutdown threshold (T_{Jsd}). In the Overtemp mode the CAN transceiver is switched to the TRX Off mode. The transmitter and the receiver are both disabled and the CAN pins are highly resistive. No wake-up event will be detected. A pending wake-up will still be signaled by a low level on pin RXD.

2.4.10 Loss of Power at Pin VS

A loss of power at pin VS has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

2.4.11 Wake-Up and Interrupt Event Diagnosis via Pin RXD

Wake-up and interrupt event diagnosis in the device is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (see section 2.3.5.18 SESR – System Event Status Register (address 0x61) to section 2.3.5.21 BFESR - Bus Failure Event Indication Status Register (address 0x65)) and is signaled on pin RXD, if enabled.

The device provides a mechanism which indicates to the microcontroller that a wake-up has occurred. This mechanism works continuously after power-on of the device.

The device sets the internal wake-up flags (CWUS, LWURS and LWUFS see section 2.3.5.19 TRXESR – Transceiver Event Status Register (address 0x63) and section 2.3.5.25 WKECR – WAKE Event Capture Enable Register (address 0x4C)) if a valid wake-up event occurs. The following mechanisms are implemented to signal a wake-up to the microcontroller:

1. RXD = low, if V_{VS} and V_{VIO} are present
2. INH pin = active, if only V_{VS} is present

A distinction is made between regular wake-up events (see Table 2-3) and interrupt events (see Table 2-4). At least one regular wake-up source must be enabled to allow the device to switch to Sleep mode in order to avoid a deadlock.

Table 2-3. Wake-up Events

Symbol	Event	Power-on	Description
CWUS	CAN bus wake-up	Disabled	A CAN wake-up event was detected
LWURS	Rising edge on WAKE pin	Disabled	A rising-edge wake-up was detected on pin WAKE
LWUFS	Falling edge on WAKE pin	Disabled	A falling-edge wake-up was detected on pin WAKE

Table 2-4. Interrupt Events

Symbol	Event	Power-on	Description
PWRONS	Device power-on	Always enabled	The device has exited Power-off mode (after battery power has been restored/ connected)

.....continued

Symbol	Event	Power-on	Description
OTPW	Overtemperature prewarning	Disabled	The device temperature has exceeded the overtemperature warning threshold (only in Normal mode)
SPIFS	SPI failure	Disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal DOPM code or attempted write access to locked register (not in Sleep mode)
PNEFD	Partial networking frame detection error	Always enabled	Partial networking frame detection error counter overflow
BS	CAN bus silence	Disabled	No activity on CAN bus for $t_{Silence}$
TRXF	CAN transceiver failure	Disabled	One of the following CAN failure events detected (not in Sleep mode): • TXD dominant clamping detected (TXD dominant timeout detected) • CAN transceiver deactivated due to a V_{VCC} undervoltage event (if COPM = 01, $V_{VCC} < V_{VCC\_UV\_Set}$) • CAN transceiver recessive clamping error detected (TRX Normal or Silent mode only)
BOUTS	Bus dominant time out failure	Disabled	Bus is detected as dominant for $t > t_{BUS\_dom}$ (not in sleep mode)
BSCS	Bus short-circuit (recessive time out) failure	Disabled	The device detects a CAN bus recessive clamping for four consecutive dominant-recessive cycles (not in sleep mode)

PWRONS and PNEFD system events are always captured. Other wake-up and interrupt event detection can be enabled/disabled for the remaining events individually via the event capture enable registers (see section 2.3.5.22 SECR – System Event Capture Enable Register (address 0x04) to section 2.3.5.25 WKECR – WAKE Event Capture Enable Register (address 0x4C)).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in TRX Standby mode, pin RXD (if VIO is applied) is forced low to indicate that a wake-up or interrupt event has been detected. If the device is in Sleep mode when the event occurs, pin INH is forced high and the device switches to Standby mode. If VIO is applied, pin RXD is forced to low. If the device is in Standby mode when the event occurs, pin RXD is forced low to flag an interrupt/wake-up event. The detection of any enabled wake-up or interrupt event will trigger a wake-up in Standby or Sleep mode. (Please refer to Table 2-3 for an overview on RXD pin in different operating modes.)

The microcontroller can monitor events via the event status registers. An extra status register, the event summery status register (see section 2.3.5.17 GESR – Global Event Status Register (address 0x60)), is

provided to help speed up software polling routines. By polling the global event status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant register, respectively.

After the event source has been identified, the status bit should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits. It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

2.4.12 Interrupt Event/Wake-Up Event Delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN TRX Standby mode, they can have a significant effect on the software processing time (because pin RXD is repeatedly driven low, requiring a response from the microcontroller each time a interrupt/wake-up is generated). The device incorporates an interrupt/wake-up delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (high) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after td(event), pin RXD goes low again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d\_evt\_cap}$, pin RXD remains high (since there are no pending events). The event capture registers can be read at any time.

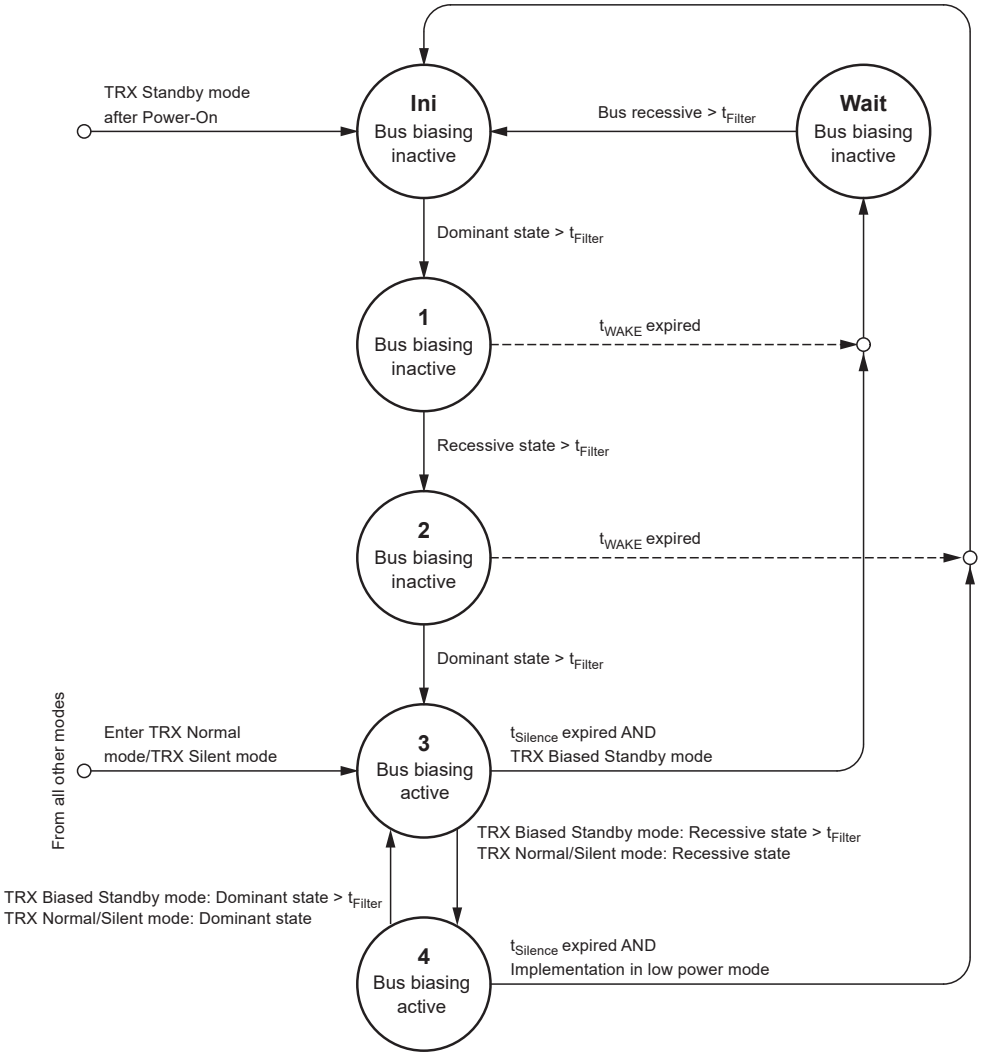
2.4.13 Sleep Mode Protection

It is very important that event detection is configured correctly when the device switches to Sleep mode to ensure it will respond to a wake-up event. For this reason, and to avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the device switches to Sleep mode. Otherwise the device will switch to Standby mode in response to a Go-to-Sleep command (DOPM = Sleep).

2.5 WUP Detection and Bias Control

In case a WUP shall trigger the system to move from Sleep to another state, this WUP must be configured in the way, that a “Normal” CAN frame will be able to wake the device and start the automatic bus biasing. The configuration depends on the CAN data rate and the user’s choice how robust the system shall be against unintended wake ups in case of disturbances.

Figure 2-5. WUP Detection and Bias Control



2.6 Device ID

A byte is reserved at address 0x7E for a device identification code.

2.7 Lock Control Register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the device updating status registers etc.

2.8 Window Watchdog

The watchdog is used to monitor the proper function of the microcontroller and to trigger a reset if the microcontroller stops serving the watchdog due to a lock up in the software or any malfunction. As in the ATA6570 there is no additional reset output pin available for the microcontroller reset, the microcontroller reset has to be triggered via the INH pin which is switched off for a defined duration in the microcontroller

reset mode. Therefore, the supply voltage of the microcontroller ramps down and a Power-on Reset is performed of the microcontroller. The INH is switched off in the microcontroller reset mode. The window watchdog (WWD) built in the ATA6570 is per default deactivated .

When the WWD is enabled it supports two operating modes: Window mode (see Figure 2-6, only available in device normal mode) and Timeout mode (see Figure 2-7). In Window mode, a watchdog trigger event within a closed watchdog window resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be reset at any time within the timeout time by a watchdog trigger. Watchdog timeout mode can also be used for cyclic wake-up of the microcontroller.

Figure 2-6. Window Watchdog in Window Mode

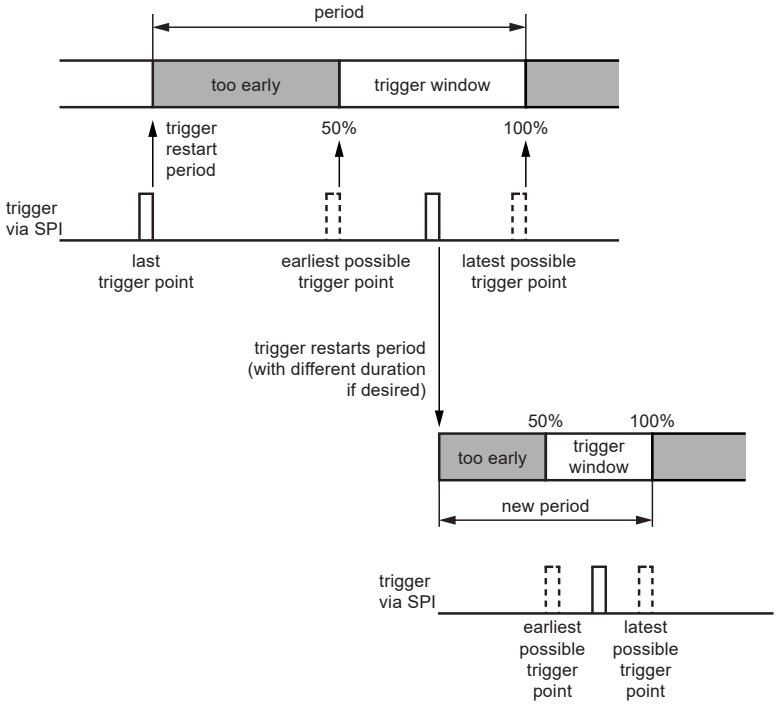
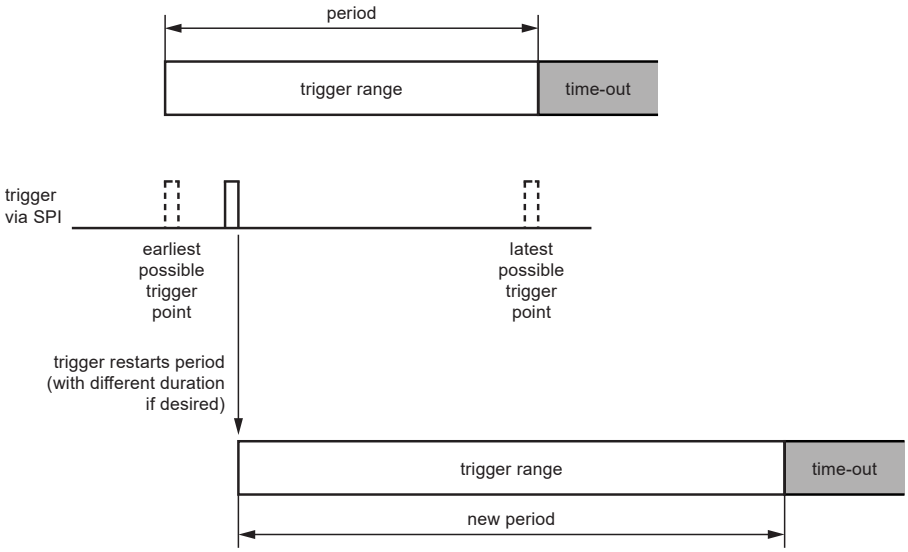


Figure 2-7. Window Watchdog in Time-out Mode



In order to avoid unwanted configuration of the window watchdog (WWD), the ATA6570 only allows users to configure the WWD (write access to WDCR1 register and WDCR2, see Table 2-5 and Table 2-6) when the device is in Standby mode. If the WWD is deactivated by default, the microcontroller shall configure the WWD correctly before the WWD is enabled (WDC=010/100). As soon as the WWD is activated, the watchdog takes the latest configuration and starts working. If the WWD is active by default, the microcontroller is allowed to configure the WWD any time when the device is in Standby mode. Every write access to the WDCR1 and WDCR2 registers via SPI will reset the watchdog timer and the settings are immediately valid. If Window mode is selected (WDC = 100), the watchdog will remain in (or switch to) Time-out mode until the device enters Normal mode (Window mode is only supported when the device is in Normal mode).

Any attempt to configure the watchdog (write access to WDCR1 register and WDCR2 register, see Table 2-5 and Table 2-6) while the device is not in Standby mode will deactivate the inhibit switch and the device will set the watchdog status register correspondingly (illegal watchdog configuration; see Table 2-7). After reset the device enters the Standby mode.

Table 2-5. Watchdog Configuration Register 1 (WDCR1, 0x36)

Bits	Symbol	Access	Value	Description
7:5	WDC	R/W		Watchdog mode control
			001	Off mode (default)
			100	Window mode
4:3	WDPRE	R/W		Watchdog Period control (extend watchdog period T ms by the factor defined below)
			00	Watchdog prescale factor 1 (default)
			01	Watchdog prescale factor 1.5
			10	Watchdog prescale factor 2.5
			11	Watchdog prescale factor 3.5

.....continued				
Bits	**Symbol**	**Access**	**Value**	**Description**
2	WDSLP	R/W		Set to 1 to let the window watchdog running in sleep mode, otherwise set to 0. Set to 0 by default.
1	WDLW	R/W		Set to 1 if a reset to window watchdog timer and a long open window exist after INH switch to high. Otherwise set to 0. Set to 1 by default.
0	ADCH	R/W		Enable (1) and disable (0) active discharger of external voltage regulator via VIO pin. By default set to 0.

Eight watchdog periods (8ms to 4096ms) are supported in the ATA6570. The watchdog period is programmable via the watchdog period bits (WWDP) in the watchdog control register 2 (WDCR2). The selected period is valid for both Window and Time-out modes. The default watchdog period is 128ms. A watchdog trigger event (an SPI write access to WDTRIG register with the pattern 01010101) resets the watchdog timer. The watchdog period and the reset pulse width can also be configured via the WRPL bits in the watchdog control register 2. A window watchdog active discharger is integrated in the ATA6570 to ensure a predictable reset of the external microcontroller. In the ATA6570 if the WWD active discharger is activated (ADCH=1), the discharger will draw a minimum of 2mA discharging current from VIO pin when a microcontroller reset is triggered by the window watchdog.

In order to let the WWD continue working when the device is in Sleep mode, the WDSLP bit of the WWD control register must be set to 1. When the device goes to Sleep mode with WDSLP='1', the counter gets reset and restarts counting immediately. Otherwise, the WWD counter is reset when the device switches to Sleep mode and waits the next INH Low-to-High event to restart itself (entering long window mode if the mode is enabled).

Table 2-6. Watchdog Control Register 2 (address 37h)

Bits	Symbol	Access	Value	Description
7:4	WWDP	R/W		Window watchdog period configuration (ms, prescale factor =1, ±10%)
			1000	8
			0001	16
			0010	32
			1011	64
			0100	128 (default)
			1101	256
			1110	1024
			0111	4096

.....continued

Bits	Symbol	Access	Value	Description
0:3	WRPL	R/W		Window watchdog reset pulse length (ms)
			1000	1 to 1.5
			0001	3.6 to 5
			0010	10 to 12.5
			1011	20 to 25
			0100	40 to 50
			1101	60 to 75
			1110	100 to 125
			0111	150 to 190 (default)

The watchdog is a valuable safety mechanism, so it is critical that it is configured correctly. Two features are provided to prevent watchdog parameters being changed by mistake:

- Redundant states of configuration bits WDC, WWDP and WRPL;
- Reconfiguration protection: only configurable in Standby mode.

Redundant states associated with control bits WDC, WWDP and WRPL ensure that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be changed to reconfigure WDC, WWDP or WRPL). If an attempt is made to write an invalid code to WDCR1 register or WDCR2 register, the SPI operation is abandoned and the CACC bit in watchdog status register is set.

Table 2-7. Watchdog Status Register (WDSR 0x38h)

Bits	Symbol	Access	Description
			Watchdog Status Register
7	OFF	R	Window watchdog is off
6	CACC	R/W	Corrupted write access to the window watchdog configuration registers
5	ILLCONF	R/W	An attempt is made to reconfigure the watchdog control register while the device is not in Standby mode
4	TRIGS	R	The device set the bit to 1 if window watchdog is in first half of window and set the bit to 0 if window watchdog is in second half of window. If the WWD is not in window mode, the bit is always be set to 0.
3	OF	R/W	Watchdog overflow (Timeout mode or Window mode in standby or normal mode)
2	OFSLP	R/W	Watchdog overflow in Sleep mode (Timeout mode)
1	ETRIG	R/W	Watchdog triggered too early (Window mode)
0	-	R	

Writing 1 to the corresponding bit of the watchdog status register will reset the bit.

A microcontroller reset is triggered immediately in response to an illegal watchdog configuration (configuration of WWD in normal or sleep mode), a watchdog failure in Window mode (watchdog overflow or triggered too early), and when the watchdog overflows in Timeout mode. If a reset is triggered by the window watchdog, the window watchdog reset event register will be set. The device will enter the reset mode and enter Standby mode after reset is finished.

If there is a corrupted write access to the window watchdog configuration registers, and/or an illegal configuration of watchdog control register when the watchdog is in off mode, the corresponding status register bit will be set. If the register bits are not reset to zero before enabling the window watchdog, a reset will be triggered to the microcontroller immediately after enabling the window watchdog.

2.8.1 WDTRIG - Watchdog Trigger Register (address 0x39)

Bit	7	6	5	4	3	2	1	0	
	WDTRIG								**WDTRIG**
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

A watchdog trigger event (an SPI write access to WDTRIG register with the pattern 01010101) resets the watchdog timer.

2.8.2 Watchdog Behavior in Window Mode

The watchdog runs continuously in Window mode. The watchdog will be in Window mode if WDC = 100 and the device enters the Normal mode. In Window mode, the watchdog can only be triggered during the second half of the watchdog period. If the watchdog overflows, or is triggered in the first half of the watchdog period (defined by WWDP in WDCR2 in Table 2-6), a reset is performed after the device enters the Reset mode. The INH output switches off for a defined length. After the reset, the reset source (either ‘watchdog triggered too early’ or ‘watchdog overflow’) can be read via the watchdog status bits in the watchdog status register (WDSR). If the watchdog is triggered in the second half of the watchdog period, the watchdog timer is restarted.

2.8.3 Watchdog Behavior in Time-Out Mode

The watchdog runs continuously in Time-Out mode. The watchdog will be in Time-Out mode if WDC = 010. In Time-Out mode, the watchdog timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event is captured in the watchdog status register (WDSR). In Time-Out mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the ATA6570 is in Sleep mode. When the device is in Sleep mode with watchdog Time-Out mode selected, a wake-up event is generated after the nominal watchdog period (WWDP). The device switches to the Reset mode.

2.8.4 Watchdog Behavior during Power-on and after Microcontroller Reset

After the watchdog has been activated, starts a long open window (600ms to 650ms started from INH is high). Within this long open window the watchdog must be triggered by the microcontroller, otherwise the watchdog will trigger a reset to the microcontroller via INH pin. After the first trigger within the long open window the WWD starts its normal operating modes.

If the WDLW bit from the window watchdog control register is set to 1 (default value), the watchdog timer will always be reset after INH is switched on and starts the long open window. Otherwise, the WWD will continue its normal operating modes.

2.8.5 Watchdog During VIO Undervoltage and Overtemperature

The window watchdog is stopped and reset if the device detects VIO undervoltage event. If the device is forced to Sleep mode due to VIO undervoltage, even if the watchdog is enabled in Sleep mode (WDSLP = 1), the window watchdog is stopped. The window watchdog is reset and restarts when the device leaves Sleep mode.
The window watchdog is stopped if the device enters Overtemperature mode. The watchdog is reset and restarts when the device enters Standby mode.

2.9 General-Purpose Memory (GPMn)

Device allocates 4 bytes of RAM as general-purpose registers for storing user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09.

2.9.1 General Purpose Memory 0 (address 0x06)

Bit	7	6	5	4	3	2	1	0	
	GPM0[7:0]								**GPM0**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: - GPM0[7:0] General purpose memory bits

2.9.2 General Purpose Memory 1 (address 0x07)

Bit	7	6	5	4	3	2	1	0	
	GPM1[7:0]								**GPM1**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: - GPM1[7:0] General purpose memory bits

2.9.3 General Purpose Memory 2 (address 0x08)

Bit	7	6	5	4	3	2	1	0	
	GPM2[7:0]								**GPM1**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: - GPM2[7:0] General purpose memory bits

2.9.4 General Purpose Memory 3 (address 0x09)

Bit	7	6	5	4	3	2	1	0

	GPM3[7:0]								GPM3
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit 7..0: - GPM3[7:0] General purpose memory bits

2.10 VIO Supply Pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels of the TXD, RXD and the SPI interface pins to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

2.11 VCC/VIO Undervoltage Protection

If an undervoltage is detected on pins VCC or VIO, and it remains valid for longer than the undervoltage detection delay time, $t_{VSUP\_UV\_filter}$, the device is forced to Sleep mode after $t_{UV2Sleep}$ (see Figure 2-1). A number of preventative measures are taken when the device is forced to Sleep mode to avoid deadlock and unpredictable states:

- All previously captured events (address range 0x61 to 0x65) are cleared before the device switches to Sleep Mode to avoid repeated attempts to wake up while an undervoltage is present.
- Both CAN remote wake-up (CWUE = 1) and local wake-up via the WAKE pin (LWUFE = LWURE = 1) are enabled in order to avoid a deadlock situation where the device cannot be woken up after entering Sleep mode.
- Partial Networking is disabled (CPNE = 0) to ensure immediate wake-up in response to bus traffic after the device has recovered from an undervoltage event.
- The Partial Networking Configuration bit is cleared (PNCFOK = 0) to indicate that partial networking might not have been configured correctly when the device switched to Sleep mode.

Status bit SMTS is set to 1 when a transition to Sleep mode is forced by an undervoltage event (see 2.1.7.2 DMSR – Device Mode Status Register (address 0x03)). This bit can be sampled after the device wakes up from Sleep mode to allow the settings of CWUE, LWUFE, LWURE and CPNE to be readjusted if an undervoltage event forced the transition to Sleep mode (SMTS = 1).

2.12 Serial Peripheral Interface (SPI)

2.12.1 General

The SPI-interface is used to communicate with a microcontroller. Commands, data and status information are transferred via SPI. In this way, the ATA6570 can be configured and operated.

The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 2-8.

Figure 2-8. SPI Timing Protocol

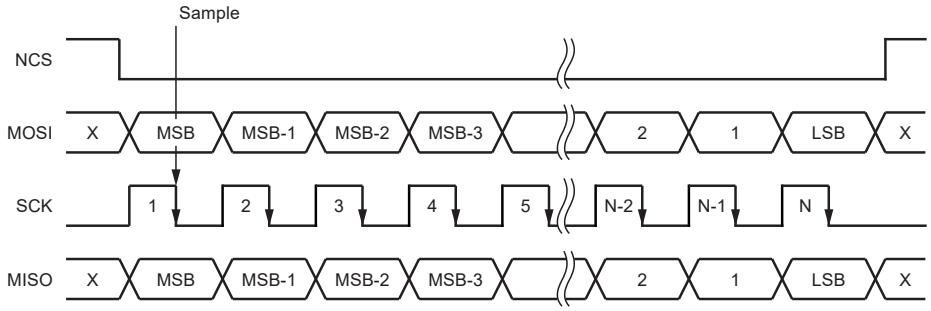
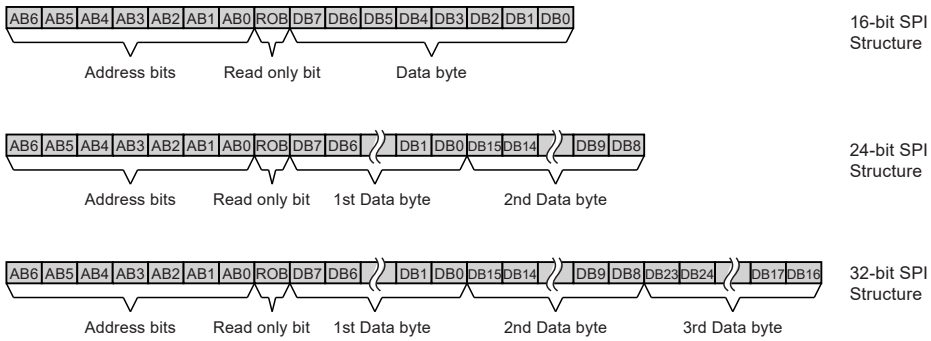


Figure 2-9. SPI Data Structure for Write Operation



The SPI data is stored in dedicated 8-bit registers and each register is assigned a unique 7-bit address. Then 16 bits must be transmitted to the device for a single register write operation. The first byte contains the 7-bit address along with a ‘read-only’ bit (the LSB). The read-only bit must be 0 to indicate a write operation. If this bit is 1, a read operation is performed and any data after this bit is ignored. The second byte contains the data to be written to the register. The contents of the addressed register(s) are returned via pin MISO, while a read or write operation is performed. For faster programming 24- and 32-bit read and write operations are also supported. In this case the register address is automatically incremented: once for a 24-bit operation and twice for a 32-bit operation.

Attempting to write to a non-existing registers is not prohibited, if the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event).

The number of the transmitted SPI bits is always monitored during SPI communication and in case of numbers not equal to 16, 24 or 32 the write operation is aborted.
An SPI failure event is captured (SPIF = 1) if the SPI failure detection is enabled (SPIFE = 1) and the following SPI failure is detected:

1. SPI clock count error (only 16-, 24- and 32-bit commands are valid), both read and write operation
2. Illegal DOPM code or
3. Attempted write access to locked register

If more than 32 bits are clocked in on pin MOSI during a read operation, the data stream on MOSI is reflected on MISO from bit 33 onwards.

2.12.2 Register Summary

The ATA6570 has 128 register with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in the table below.

Addr.	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page(s)
Device control reg.										
0x01	DMCR	-	-	-	-	-	DOPM[2:0]			
0x03	DMSR	SMTS	OTPWS	NMTS	-	-	-	-	-	
0x04	SECR	-	-	-	-	-	OTPWE	SPIFE	-	
0x06	GPM0	GPM0[7:0]								
0x07	GPM1	GPM1[7:0]								
0x08	GPM2	GPM2[7:0]								
0x09	GPM3	GPM3[7:0]								
0x0A	RWPR	-	WP6	WP5	WP4	WP3	WP2	WP1	WP0	
TRX control reg.										
0x20	TRXCR	-	CFDPE	PNCFOK	CPNE	-	-	COPM[1:0]		
0x22	TRXSR	TXS	PNERRS	PNCFS	PNOSCS	CBSS	-	VCCS	TXDOUT	
0x23	TRXECR	-	-	-	BSE	-	-	TRXFE	CWUE	
0x26	DRCR	-	-	-	-	DR[3:0]				
0x27	CIDR0	ID0[7:0]								
0x28	CIDR1	ID1[7:0]								
0x29	CIDR2	ID2[7:0]								
0x2A	CIDR3	-	-	-	ID3[4:0]					
0x2B	CIDMR0	IDM0[7:0]								
0x2C	CIDMR1	IDM1[7:0]								
0x2D	CIDMR2	IDM2[7:0]								
0x2E	CIDMR3	-	-	-	IDM3[4:0]					
0x2F	CFCR	IDE	PNDM	-	-	DLC[3:0]				
0x32	BFECR	-	-	-	-	-	-	BOUTE	BSCE	
0x33	BFIR	-	-	-	-	-	-	BOUT	BSC	
0x34	TRXECR2	-	-	-	-	-	-	-	RXDRCE	
0x35	TRXESR2	-	-	-	-	-	-	-	RXDRCS	
0x36	WDCR1	WDC[2:0]			WDPRE[1:0]		WDSLP	WDLW	ADCH	
0x37	WDCR2	WWDP[3:0]				WRPL[3:0]				
0x38	WDSR	OFF	CACC	ILLCONF	TRIGS	OF	OFSLP	ETRIG	-	
0x39	WDTRIG	WDTRIG[7:0]								
0x3A	EFCR				ERRCNT[4:0]					
0x3B	FECR				FEC[4:0]					
0x67	GLF						GLF[2:0]			
0x68	CDMR0	DM0[7:0]								

.....continued

Addr.	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page(s)
0x69	CDMR1	DM1[7:0]								
0x6A	CDMR2	DM2[7:0]								
0x6B	CDMR3	DM3[7:0]								
0x6C	CDMR4	DM4[7:0]								
0x6D	CDMR5	DM5[7:0]								
0x6E	CDMR6	DM6[7:0]								
0x6F	CDMR7	DM7[7:0]								
WAKE control and status registers										
0x4B	PWKS	-	-	-	-	-	-	PWKVS	-	
0x4C	WKECR	-	-	-	-	-	-	LWURE	LWUFE	
Event status registers										
0x60	GESR	OSCS	-	BFES	-	WKES	TRXES	-	SYSES	
0x61	SESR	-	-	-	PWRONS	-	OTPW	SPIFS	-	
0x63		-	-	PNEFD	BS	-	-	TRXF	CWUS	
0x64	WKESR	-	-	-	-	-	-	LWURS	LWUFS	
0x65		-	-	-	-	-	-	BOUTS	BSCS	
Device ID register										
0x7E	DIDR	DIDR[7:0]								

2.12.3 Operating Modes and Register Bit Settings

When switching from one operating mode to another, a number of register bits may change their state automatically. This will happen when the device switches to Power-Off mode or when the device is forced to Sleep mode because of an undervoltage event.

These changes are summarized in the table below. SPI operations are ignored during state changes (automatic state changes have priority).

Register Bit	Power Off	Standby	Normal	Sleep	Overtemp	Forced Sleep (UV)
BS	0	no change	no change	no change	no change	0
BSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
DR	101	no change	no change	no change	no change	no change
TRXF	0	no change	no change	no change	no change	0
CFDPE	1	no change	no change	no change	no change	no change
TRXFE	0	no change	no change	no change	no change	no change

.....continued

Register Bit	Power Off	Standby	Normal	Sleep	Overtemp	Forced Sleep (UV)
TXDOUT	0	actual state	actual state	actual state	actual state	actual state
COPM	01	no change	no change	no change	no change	no change
PNOSCS	0	actual state	actual state	actual state	actual state	actual state
CPNE	0	no change	no change	no change	no change	0
PNERRS	1	actual state	actual state	actual state	actual state	actual state
PNCFS	0	actual state	actual state	actual state	actual state	actual state
TXS	0	0	actual state	0	0	0
CWUS	0	no change	no change	no change	no change	0
CWUE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
SMTS	0	no change	no change	0	no change	1
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change
DIDR	01110000	01110000	01110000	01110000	01110000	01110000
WPn	0	no change	no change	no change	no change	no change
IDMn	00000000	no change	no change	no change	no change	no change
DOPM	100	100	111	001	don’t care	001
NMTS	1	no change	0	no change	no change	no change
OTPW	0	no change	no change	no change	no change	0
OTPWE	0	no change	no change	no change	no change	no change
OTPWS	0	actual state	actual state	actual state	actual state	actual state
PNCFOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNEFD	0	no change	no change	no change	no change	0
PWRONS	1	no change	no change	no change	no change	0
SPIFS	0	no change	no change	no change	no change	0
SPIFE	0	no change	no change	no change	no change	no change
SYSES	1	no change	no change	no change	no change	0

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Register Bit	Power Off	Standby	Normal	Sleep	Overtemp	Forced Sleep (UV)
TRXES	0	no change	no change	no change	no change	0
VCCS	0	actual state	actual state	actual state	actual state	actual state
OSCS	0	no change	no change	no change	no change	no change
BFES	0	no change	no change	no change	no change	0
WKES	0	no change	no change	no change	no change	0
LWUFS	0	no change	no change	no change	no change	0
LWUFE	0	no change	no change	no change	no change	1
LWURE	0	no change	no change	no change	no change	0
LWURE	0	no change	no change	no change	no change	1
PWKVS	0	no change	no change	no change	no change	no change
GLF	010	no change	no change	no change	no change	no change
RXDRCS	0	no change	no change	no change	no change	no change
RXDRCE	0	no change	no change	no change	no change	no change
BOUTE	0	no change	no change	no change	no change	no change
BSCE	0	no change	no change	no change	no change	no change
BOUTS	0	no change	no change	no change	no change	no change
BSCS	0	no change	no change	no change	no change	no change

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
CANH, CANL DC voltage Transient voltage, according to ISO 7637 part 2	V_{CANH}, V_{CANL}	−27 −150	+42 +100	V
Maximum differential bus voltage	V_{Diff}	−5	+18	V
DC voltage on pin TXD, RXD, MISO, MOSI, NCS, SCK, VCC, VIO	V_x	−0.3	+5.5	V
DC voltage on pin VS	V_{VS}	−0.3	+40	V
DC voltage on pin VS (for 2ms, 2500 pulses)	V_{VS}	−2		V
DC voltage on pin INH, WAKE	V_{INH}, V_{WAKE}	−0.3	+40	V
ESD according to IBEE CAN EMC test specification following IEC 62228, IEC 61000-4-2: - Pin VS, CANH, CANL, WAKE to GND		±8		kV
HBM JESD22-A114/AEC-Q100-002 - Pin CANH, CANL to GND - Pin VS, WAKE to GND		±8 ±4		kV
HBM JESD22-A114/AEC-Q100-002 - All pins		±2		kV
Charge Device Model ESD AEC-Q100-011		±500		V
Machine Model ESD AEC-Q100-003		±100		V
Storage temperature	T_{stg}	−55	+175	°C
Virtual junction temperature	T_{vJ}	−40	+175	°C

4. Thermal Characteristics

Table 4-1. Thermal Characteristics SOIC14

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal Package Resistance					
Thermal resistance virtual junction to ambient, where IC is soldered to PCB according to JEDEC	R_{thvJA}	—	110	—	K/W
Thermal Shutdown of the Bus Drivers Output					
ATA6570-GNQW1 (Grade 1)	T_{Jsd}	150	175	195	°C
ATA6570-GNQW0 (Grade 0)	T_{Jsd}	160	175	195	°C
Thermal shutdown hysteresis	T_{Jsd_hys}	—	30	—	°C

5. Electrical Characteristics

All parameters valid for 4.55V ≤ V_{VS} ≤ 28V, 4.7V ≤ V_{VCC} ≤ 5.5V, 2.8V ≤ V_{VIO} ≤ 5.5V, all voltages are defined with respect to ground, $R_{(CANH-CANL)}$ = 60Ω, Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C, typical values are given at V_{VS} = 13V, T_{amb} = 25°C, unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
VS									
0.10	Supply voltage threshold for power-on detection	V_{VS} rising	VS	V_{VS_PWRON}	4.1		4.55	V	A
0.20	Supply voltage threshold for power-off detection	V_{VS} falling	VS	V_{VS_PWROFF}	2.8		3.1	V	A
0.30	Supply voltage threshold for CAN TRX undervoltage detection release	V_{VS} rising	VS	$V_{VS\_UV\_CAN\_Clear}$	4.5		5	V	A
0.40	Supply voltage threshold for CAN TRX undervoltage detection	V_{VS} falling	VS	$V_{VS\_UV\_CAN\_Set}$	4.1		4.55	V	A
0.50	VS supply current	Sleep mode, DOPM = Sleep, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V	VS	I_{VS_Sleep}			30	µA	A
0.51		Standby mode, DOPM = Standby, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V)	VS	I_{VS_Stb}			40	µA	A
0.52		Additional current in Standby mode with bus biasing ON	VS	I_{VS_Bias}			140	µA	A
0.53		Additional current when partial networking enabled, bus active, CPNE = 1, PNCFOK = 1	VS	ΔI_{VS_Pn}			350	µA	A
0.55		Normal mode, TRX Normal mode, partial networking enabled, bus active, CPNE = 1, PNCFOK = 1	VS	I_{VS_Norm}		1	1.5	mA	A
VCC									
1.10	VCC undervoltage detection set threshold	V_{VCC} falling	VCC	$V_{VCC\_UV\_Set}$	3.7		4.25	V	A
1.20	VCC TX undervoltage shutdown threshold	V_{VCC} falling	VCC	$V_{VCC\_TX\_Sd}$	4.0		4.7	V	A
1.30	VCC supply current	CAN TRX Normal mode, CAN recessive, V_{TXD} = V_{VIO}	VCC	I_{VCC_Norm}			2	mA	A
1.31		Device Standby/ Normal mode and CAN TRX Standby mode	VCC	I_{VCC_Stb}			3	µA	A
1.32		Device Sleep mode and CAN TRX Standby mode	VCC	I_{VCC_Sleep}			3	µA	A
1.40	Supply current in normal mode	Dominant, V_{TXD} = 0V	VCC	I_{VCC_dom}	30	50	70	mA	A
1.41	Supply current in normal mode	Short between CANH and CANL	VCC	I_{VCC_short}			85	mA	B
VIO									
2.10	VIO undervoltage detection set threshold	V_{VIO} falling	VIO	$V_{VIO\_UV\_Set}$	2.4		2.8	V	A
2.20	VIO supply current	Standby/Normal, TXD = 1	VIO	I_{VIO_Stb}			5	µA	A
2.21	VIO supply current	Sleep, TXD = 1, Tamb ≤ 125°C	VIO	I_{VIO_Sleep}			5	µA	A
2.30	Active discharge current	VIO = 0.5V	VIO	I_{VIO_Disch}	2			mA	B
MOSI, SCK, NCS									

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.10	High-level input voltage		MOSI, SCK, NCS	V_{MOSI_H}, V_{SCK_H}, V_{NCS_H}	0.7× V_{VIO}		V_{VIO} + 0.3	V	A
3.20	Low-level input voltage		MOSI, SCK, NCS	V_{MOSI_L}, V_{SCK_L}, V_{NCS_L}	−0.3		0.3× V_{VIO}	V	A
3.30	Input current		MOSI	I_{I_MOSI}	−5		+5	µA	A
3.40	Pull-up resistance on pin NCS		NCS	R_{PU_NCS}	40	60	80	kΩ	A
3.50	Pull-down resistance on pin SCK		SCK	R_{PD_SCK}	40	60	80	kΩ	A
MISO, RXD									
4.10	High-level output voltage	I = −4mA	MISO, RXD	V_{MISO_H}, V_{RXD_H}	V_{VIO} − 0.4		V_{VIO}	V	A
4.20	Low-level output voltage	I = 4mA	MISO, RXD	V_{MISO_L}, V_{RXD_L}			0.4	V	A
4.40	Off-state leakage current		MISO	I_{leak_MISO}	−5		+5	µA	A
TXD									
5.10	High-level input voltage		TXD	V_{TXD_H}	0.7× V_{VIO}		V_{VIO} + 0.3	V	A
5.20	Low-level input voltage		TXD	V_{TXD_L}	−0.3		0.3× V_{VIO}	V	A
5.30	Pull- up resistor		TXD	R_{PU_TXD}	40	60	80	kΩ	A
WAKE									
6.10	High-level input current	V_{WAKE} = 4.2V, V_{VS} ≥ 5.2V	WAKE	I_{WAKE_H}	−10	−5	−1	µA	A
6.20	Low-level input current	V_{WAKE} = 2.3V	WAKE	I_{WAKE_L}	1	5	10	µA	A
6.30	Threshold voltage	WAKE rising	WAKE	V_{WAKE_TH}	2.8		4.1	V	A
6.31		WAKE falling	WAKE	V_{WAKE_TH}	2.4		3.75	V	A
6.40	Input hysteresis voltage		WAKE	V_{hys}	0.25		0.8	V	C
INH									
7.10	On mode high-level voltage	Normal mode or Standby mode, I_{INH} = −180µA	INH	V_{INH_On}	V_{VS} −0.8		V_{VS}	V	A
7.20	Off mode leakage current	Leakage of grounded INH pin in Off Mode	INH	I_{INH_Off}	−2		2	µA	A
CANH, CANL (see Figure 6-3 for the definition of R_L and the test circuit)									
8.10	Single-ended dominant output voltage	R_L = 50Ω to 65Ω	CANH	V_{CANH}	2.75	3.5	4.5	V	B
8.11			CANL	V_{CANL}	0.5	1.5	2.25	V	B
8.30	Transmitter voltage symmetry	V_{Sym} = (V_{CANH} + V_{CANL}) / V_{CC} R_L = 60Ω, C_1 = 4.7nF f_{TXD} = 1MHz		V_{Sym}	0.9	1.0	1.1		D

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.40	Bus differential output voltage	CAN TRX Normal mode, V_{TXD} = 0V, t < $t_{to(dom)TXD}$ R_L = 50Ω to 65Ω V_{VCC} = 4.7V to 5.5V		V_{Diff}	1.5		3	V	B
8.41		CAN TRX Normal mode, V_{TXD} = 0V, t < $t_{to(dom)TXD}$ R_L = 45Ω to 70Ω V_{VCC} = 4.7V to 5.5V		V_{Diff}	1.4		3.2	V	D
8.42		CAN TRX Normal mode, V_{TXD} = 0V, t < $t_{to(dom)TXD}$ R_L = 2240Ω V_{VCC} = 4.7V to 5.5V		V_{Diff}	1.5		5	V	D
8.50	Recessive output voltage	Single-ended output voltage on CANH/CANL, CAN TRX Normal mode, V_{VCC} > 4.3V, V_{TXD} = V_{VIO}, no load	CANH, CANL	V_{CANH}, V_{CANL}	2	0.5 × V_{VCC}	3	V	A
8.51		Single-ended output voltage on CANH/CANL, CAN TRX Standby mode, V_{TXD} = V_{VIO}, no load	CANH, CANL	V_{CANH}, V_{CANL}	−0.1		+0.1	V	A
8.52		Single-ended output voltage on CANH/CANL, CAN TRX Biased Standby/TRX Silent mode, V_{TXD} = V_{VIO}, no load	CANH, CANL	V_{CANH}, V_{CANL}	2	2.5	3	V	A
8.53		Differential output voltage (bus biasing active), no load		V_{Diff}	−50		+50	mV	A
8.54		Differential output voltage (bus biasing inactive), no load		V_{Diff}	−50		+50	mV	A
8.60	Differential receiver threshold voltage	CAN TRX Normal/TRX Silent modes, V_{CANL} = V_{CANH} = −12V to +12V		$V_{Diff\_rx\_th}$	0.5	0.7	0.9	V	A
8.61		CAN TRX Standby mode, V_{CANL} = V_{CANH} = −12V to +12V		$V_{Diff\_rx\_th}$	0.4	0.7	1.15	V	A
8.70	Differential receiver hysteresis voltage	CAN TRX Normal/TRX Silent mode, V_{CANL} = V_{CANH} = −12V to +12V		V_{Hys_rx}	50	120	200	mV	C
8.80	Leakage current	V_{VS} = V_{VCC} = V_{VIO} = 0V V_{CANH} = V_{CANL} = 5 V	CANH, CANL	I_{leak}	−5		+5	µA	A
		VS = VCC = VIO connected to GND with 47kΩ V_{CANH} = V_{CANL} = 5V	CANH, CANL	I_{leak}	−5		+5	µA	D
8.90	Maximum driver output current	CAN TRX Normal mode; CAN dominant, V_{TXD} = 0, t < $t_{to(dom)TXD}$, V_{VCC} = 5V V_{CANH} = −5V	CANH	I_{CANH_max}	−75		−35	mA	A
8.91	Maximum driver output current	CAN TRX Normal mode, CAN dominant; V_{TXD} = 0, t < $t_{to(dom)}$, V_{VCC} = 5V V_{CANL} = +27V	CANL	I_{CANL_max}	35		75	mA	A
8.100	Single-ended input resistance	V_{CANH} = V_{CANL} = 4V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	A
		−2V ≤ V_{CANH} ≤ 7V −2V ≤ V_{CANL} ≤ 7V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	D

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.110	Matching of internal resistance between CANH and CANL	$V_{CANH} = V_{CANL} = 4V$ $mR = 2 \times (R_{CANH} - R_{CANL}) / (R_{CANH} + R_{CANL})$		mR	−0.01		+0.01		A
		$-2V \le V_{CANH} \le 7V$ $-2V \le V_{CANL} \le 7V$ $mR = 2 \times (R_{CANH} - R_{CANL}) / (R_{CANH} + R_{CANL})$		mR	−0.01		+0.01		D
8.120	Differential internal resistance	$V_{CANH} = V_{CANL} = 4V$		R_{Diff}	18	30	56	kΩ	A
		$-2V \le V_{CANH} \le 7V$ $-2V \le V_{CANL} \le 7V$		R_{Diff}	18	30	56	kΩ	D
8.130	Common-mode input capacitance			$C_{i(cm)}$			20	pF	D
8.140	Differential input capacitance			C_{Diff}			10	pF	D
8.141	Differential bus voltage range for Recessive state detection	Bus biasing active Bus biasing inactive		VDiff_rec_a VDiff_rec_i	−3.0 −3.0		+0.5 +0.4	V V	D D
8.142	Differential bus voltage range for Dominant state detection	Bus biasing active Bus biasing inactive		VDIFF_dom_a VDIFF_dom_i	0.9 1.15		8.0 8.0	V V	D D
Transceiver Timing, Pins WAKE, INH, CANH, CANL, TXD and RXD. Please refer to Figure 5-1, Figure 5-2 and Figure 6-3 for the definition of the timing parameters and the test circuit.									
9.10	Delay time from TXD to bus dominant	R_L = 60Ω, C2 = 100pF	CANH, CANL, TXD	t_{TXDBUS_dom}		65		ns	C
9.20	Delay time from TXD to bus recessive	R_L = 60Ω, C2 = 100pF	CANH, CANL, TXD	t_{TXDBUS_rec}		90		ns	C
9.30	Delay time from bus dominant to RXD	R_L = 60Ω, C2 = 100pF	CANH, CANL, RXD	t_{BUSRXD_dom}		60		ns	C
9.40	Delay time from bus recessive to RXD	R_L = 60Ω, C2 = 100pF	CANH, CANL, RXD	t_{BUSRXD_rec}		65		ns	C
9.50	Propagation delay from TXD to RXD (The input signal on TXD shall have rise- and fall times (10%/90%) of less than 10ns.) (Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.)	R_L = 60Ω, C2 = 100pF, C_{RXD} = 15pF	TXD, RXD	t_{Loop}	100		220	ns	A
9.51		R_L = 150Ω, C2 = 100pF, C_{RXD} = 15pF	TXD, RXD	t_{Loop}			300	ns	C
9.60	Received recessive bit time on pin RXD	t_{B_TXD} = 500ns R_L = 60Ω, C2 = 100pF, C_{RXD} = 15pF	RXD	$t_{Bit(RXD)}$	400		550	ns	C
9.61		t_{B_TXD} = 200ns R_L = 60Ω, C2 = 100pF, C_{RXD} = 15pF	RXD	$t_{Bit(RXD)}$	120		220	ns	A
9.70	Receiver timing symmetry	$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ t_{B_TXD} = 500ns (Please refer to the 9.100 for $t_{Bit(Bus)}$)		Δt_{Rec}	−65		+40	ns	C
9.71		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ t_{B_TXD} = 200ns (Please refer to the 9.110 for $t_{Bit(Bus)}$)		Δt_{Rec}	−45		+15	ns	A
9.80	TXD dominant timeout time	V_{TXD} = 0V, Normal mode	TXD	$t_{to(dom)}$	2.7		3.3	ms	B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.90	Bus dominant timeout time	$V_{CANH-CANL}$ > 0.9 V		t_{BUS_dom}	2.7		3.3	ms	B
9.100	Transmitted recessive bit width on the bus	t_{B_TXD} = 500ns		$t_{Bit(Bus)}$	435		530	ns	C
9.110		t_{B_TXD} = 200ns		$t_{Bit(Bus)}$	155		210	ns	A
9.120	CAN activity filter time for standard remote wake-up pattern (WUP)	First pulse (after first recessive) and second pulse for wake-up on pins CANH and CANL, CAN TRX Standby	CANH, CANL	t_{Filter}	0.5		1.8	µs	A
9.130	Bus bias reaction time		CANH, CANL	t_{Bias}			200	µs	C
9.140	Time-out time for bus inactivity	Bus recessive time measurement started in all CAN TRX modes	CANH, CANL	$t_{Silence}$	0.95		1.17	s	B
9.150	CAN start-up time	When switching to CAN TRX Normal mode	CANH, CANL	$t_{TRX\_startup}$			220	µs	A
9.160	Event capture delay time	CAN TRX Standby mode	RXD	$t_{d\_evt\_cap}$	0.9		1.1	ms	B
9.180	Delay time from bus wake-up to INH high	Load on INH pin, R_{LOAD} = 10kΩ	INH	t_{WU_INH}			100	µs	A
9.190	Undervoltage detection filter time		VCC, VIO	$t_{VSUP\_UV\_filter}$	6		54	µs	A
9.200	Delay time from VIO/VCC undervoltage detection to enter Sleep mode		VCC, VIO	$t_{UV2Sleep}$	200		400	ms	B
9.210	Start-up time after power on	From V_{VS} rises above the power-on detection threshold V_{VS_PWRON} until pin INH high	VS	$t_{startup}$			1	ms	A
9.220	Standard remote wake-up timeout time	Between first and second dominant pulses, CAN TRX Standby mode		t_{Wake}	900		1200	µs	B
9.230	Debouncing time for recessive clamping state detection	$V_{(CAN\_H-CAN\_L)}$ > 900mV, RXD = high	RXD	$t_{RXD\_rec\_clmp}$	60	90	175	ns	D
9.240	Local wake-up time		WAKE	t_{local_wu}	5		50	µs	B
9.250	Transmitter resume time	From TXD goes high to TX operates after TXD dominant timeout event detected		$t_{TX\_resume\_TXD\ OUT}$			4	µs	D
9.260	Bus recessive clamping detection time	Bus recessive clamping time after TXD goes low		$t_{bus\_rec\_clamp}$	1			µs	D
SPI Timing									
10.10	Clock cycle time	Normal/Standby/Sleep mode	SPI	t_{clk}	250			ns	D
10.20	SPI enable lead time	Normal/Standby/Sleep mode	SPI	t_{EN_Lead}	50			ns	D
10.30	SPI enable lag time	Normal/Standby/Sleep mode	SPI	t_{EN_Lag}	50			ns	D
10.40	Clock HIGH time	Normal/Standby/Sleep mode	SPI	t_{Clk_H}	125			ns	D
10.50	Clock low time	Normal/Standby/Sleep mode	SPI	t_{Clk_L}	125			ns	D
10.60	Data input set-up time	Normal/Standby/Sleep mode	SPI	t_{Setup}	50			ns	D
10.70	Data input hold time	Normal/Standby/Sleep mode	SPI	t_{Hold}	50			ns	D
10.80	Data output valid time	Normal/Standby/Sleep mode	SPI	t_{Dout_v}			65	ns	D
10.90	Chip select pulse width high	Normal/Standby/Sleep mode, pin MISO, C_L = 20pF	SPI	t_{NCS_pw}	250			ns	D
Temperature Protection									
11.30	Overtemperature protection prewarning threshold			T_{OT_Prew}	120	134	147	°C	B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11.31	Overtemperature protection prewarning hysteresis			$T_{OT\_Prew\_hys}$		10		°C	C

* Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 5-1. CAN Transceiver Timing Diagram 1

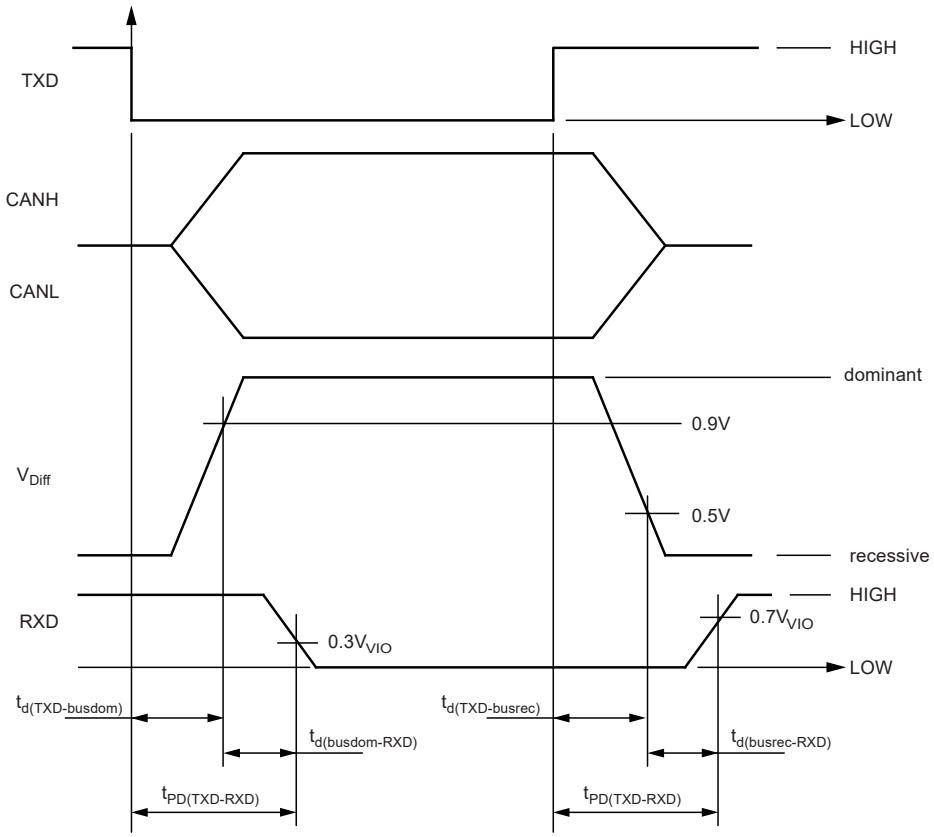
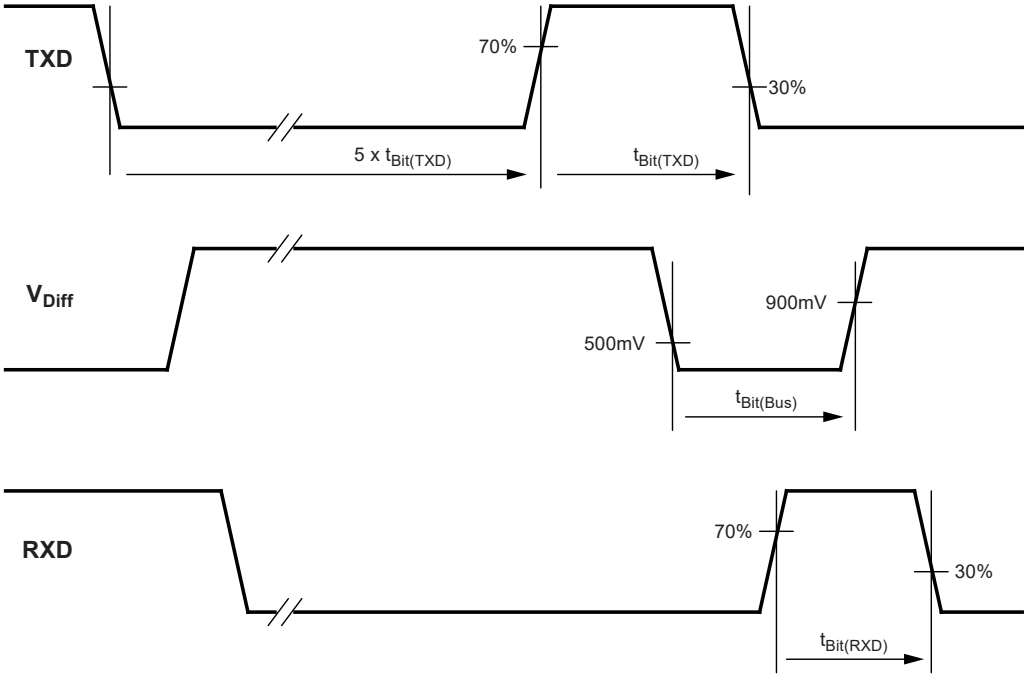
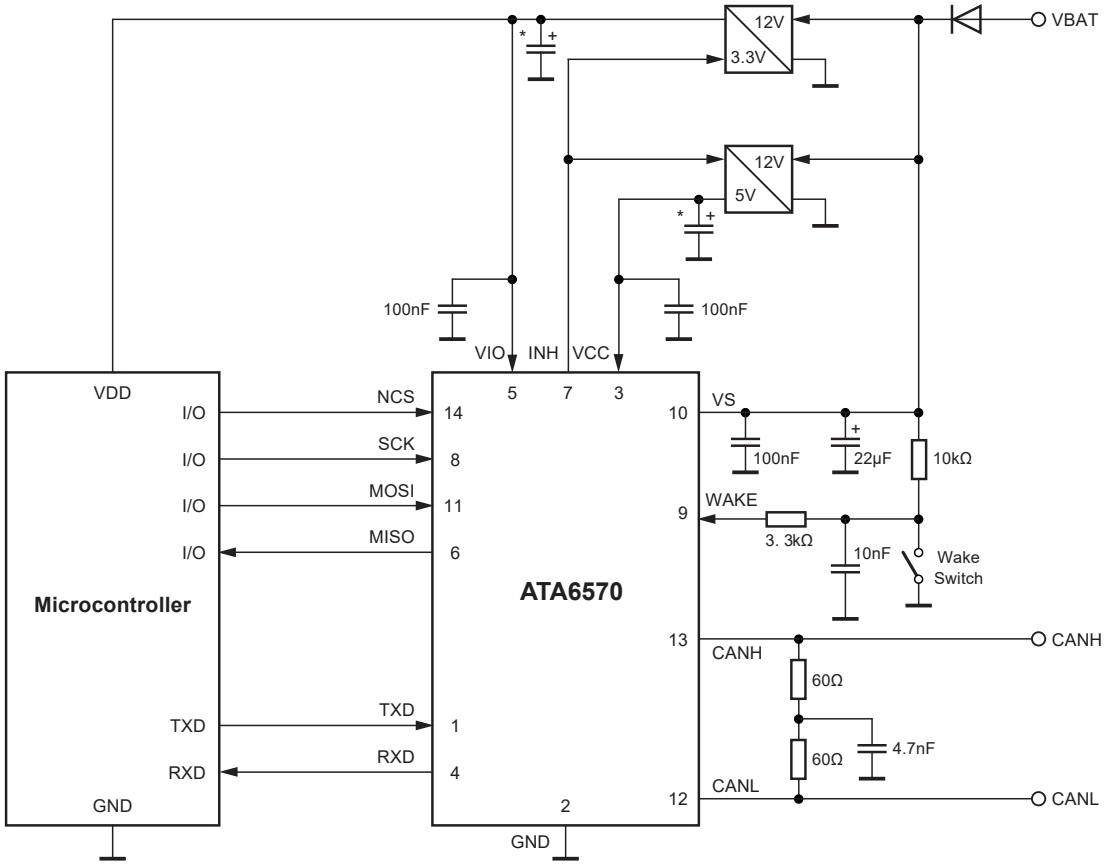


Figure 5-2. CAN Transceiver Timing Diagram 2



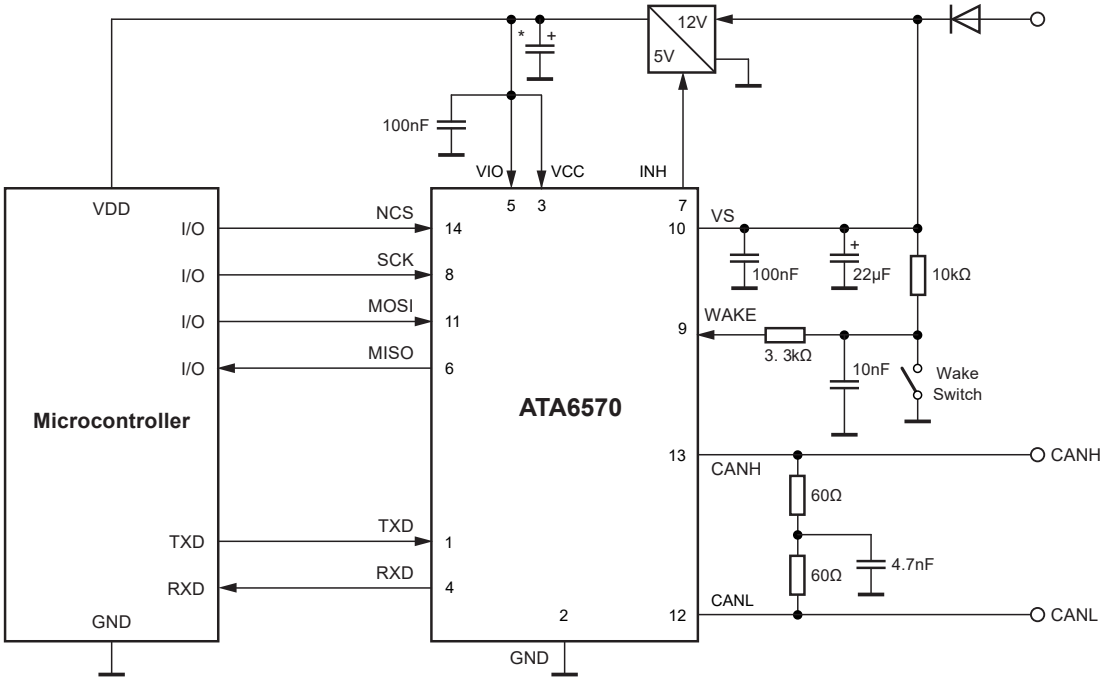
6. Application Circuits

Figure 6-1. Typical Application Circuit ATA6570



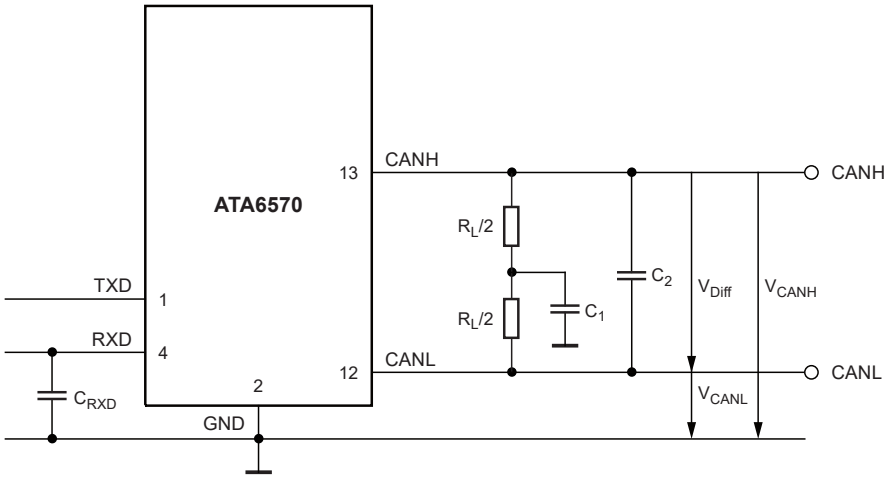
*The value of these capacitors depends on the used external voltage regulators

Figure 6-2. Typical Application Circuit 5V Only



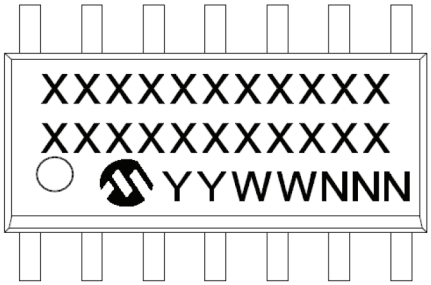
* The value of this capacitor depends on the used external voltage regulator

Figure 6-3. ATA6570 Test Circuit

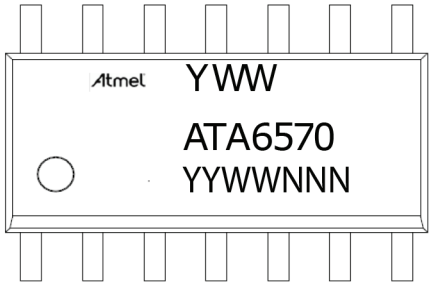


7. Package Marking Information

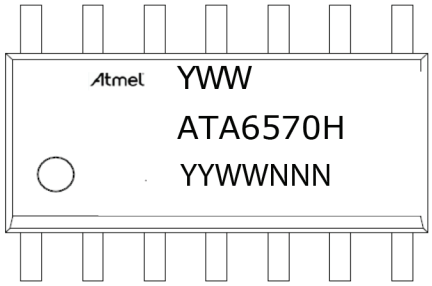
14-Lead SOIC



Example Grade 1



Example Grade 0

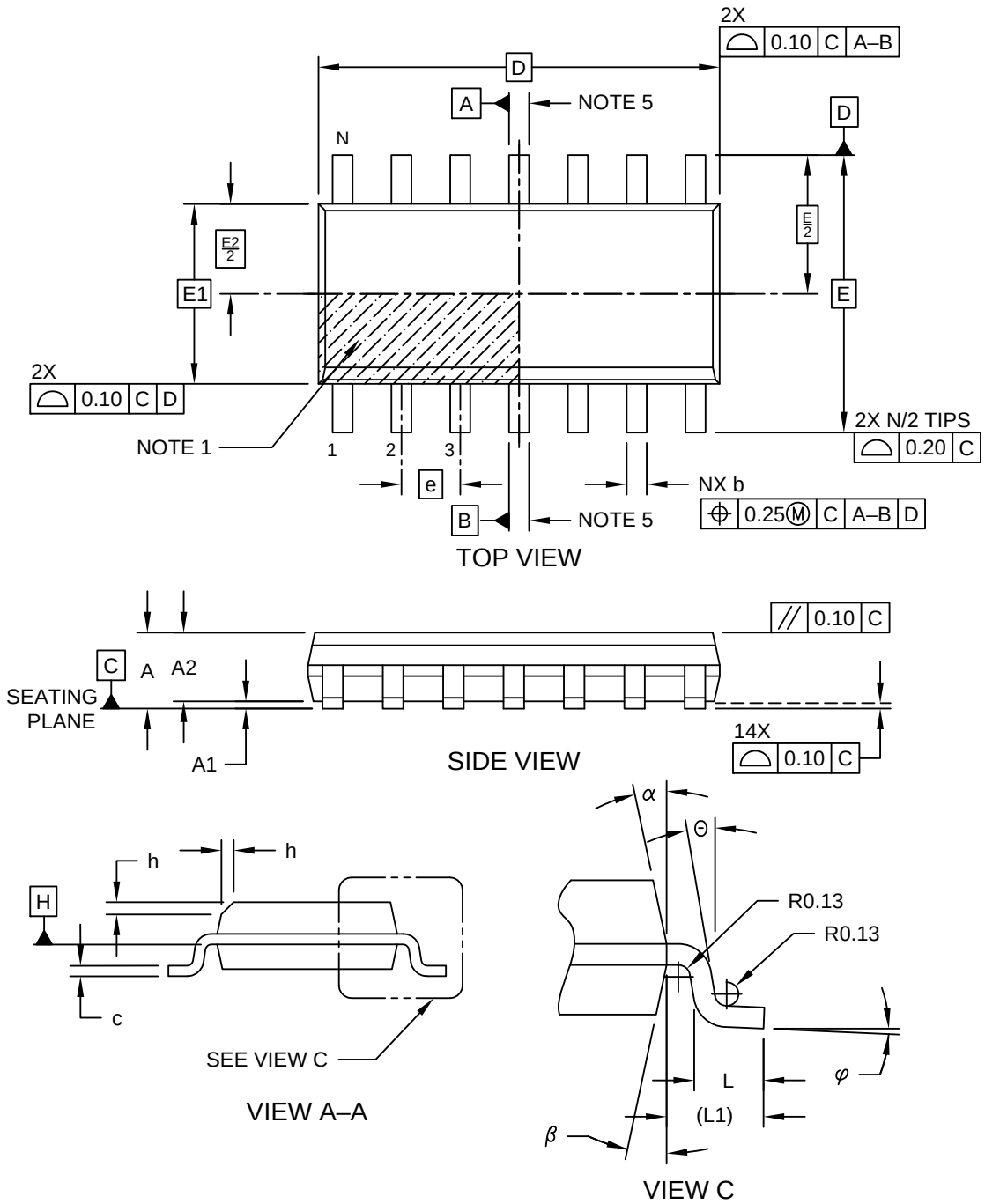


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

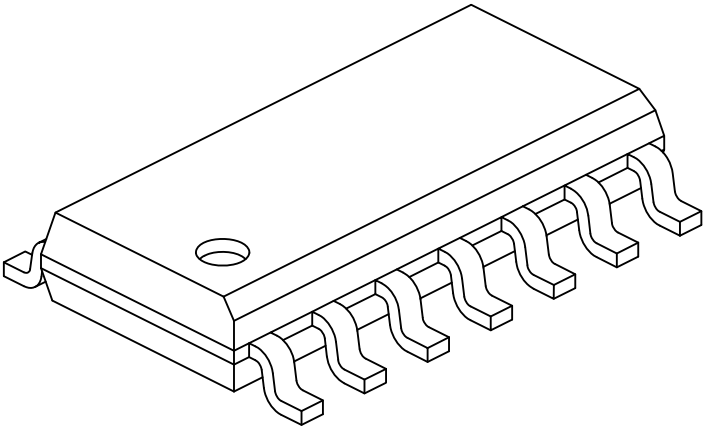
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

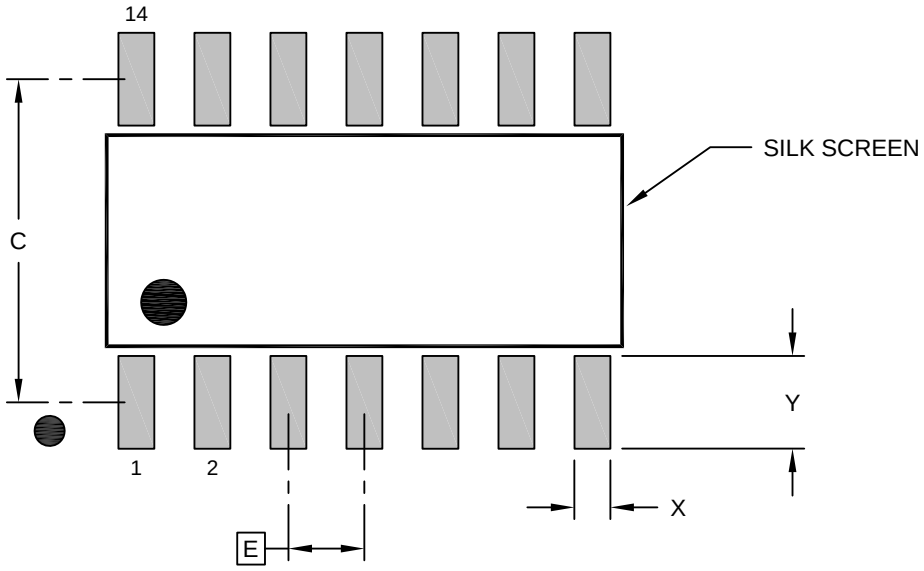
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

8. Revision History

Revision A (June 2017)
Original release of this document.

This document replaces Atmel Revision D - 9340D-11/16.

Revision B (July 2017)
Various internal updates.

Revision C (April 2018)
Various internal updates.

Revision D (December 2018)
Added the Grade 0 device and updated the related information across the document.

Added the ATA6570 Family Members table.

Updated the Application Circuits chapter.

Updated the Thermal Characteristics section.

Updated the Product Identification System chapter.

Updated Parameter 0.10, 0.40, 1.30, 1.31, 1.32, 2.20, 2.21 and 9.210.

Various typographical edits.

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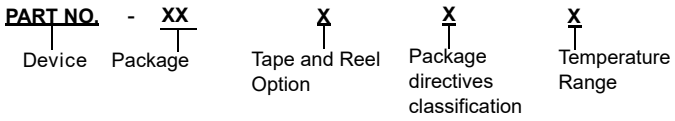

Device:	ATA6570	
Package:	GN	SOIC14, copper bonds
Tape and Reel option:	Q	330 mm diameter Tape and Reel (1)
Package directives classification:	W	Package according to RoHS (3)
Temperature range:	0	Temperature Grade 0 (-40°C to +150°C)
	1	Temperature Grade 1 (-40°C to +125°C)

Examples:

- ATA6570-GNQW0 - CAN transceiver with partial networking and watchdog (default off), CAN FD capable, SO14 package, Grade 0
- ATA6570-GNQW1 - CAN transceiver with partial networking and watchdog (default off), CAN FD capable, SO14 package, Grade 1

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check http://www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.
3. RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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ISO/TS 16949

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