dsPIC33EPXXXGM3XX/6XX/7XX Family Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXXGM3XX/6XX/7XX family devices that you have received conform functionally to the current Device Data Sheet (DS70000689**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EPXXXGM3XX/6XX/7XX family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on Page 25, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33EPXXXGM3XX/6XX/7XX family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]			
		A0	A1	A2	A3
dsPIC33EP128GM304	0x1B40	0x4000	0x4001	0x4002	0x4003
dsPIC33EP128GM604	0x1B48				
dsPIC33EP128GM306	0x1B43				
dsPIC33EP128GM706	0x1B4B				
dsPIC33EP128GM310	0x1B47				
dsPIC33EP128GM710	0x1B4F				
dsPIC33EP256GM304	0x1B80				
dsPIC33EP256GM604	0x1B88				
dsPIC33EP256GM306	0x1B83				
dsPIC33EP256GM706	0x1B8B				
dsPIC33EP256GM310	0x1B87				
dsPIC33EP256GM710	0x1B8F				
dsPIC33EP512GM304	0x1BC0				
dsPIC33EP512GM604	0x1BC8				
dsPIC33EP512GM306	0x1BC3				
dsPIC33EP512GM706	0x1BCB				
dsPIC33EP512GM310	0x1BC7				
dsPIC33EP512GM710	0x1BCF				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

2: Refer to the *“dsPIC33EPXXXGM3XX/6XX/7XX Flash Programming Specification”* (DS70000685) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]			
				A0	A1	A2	A3
Core	CPU	1.	Limited execution speed (44/64-pin and 100/121-pin devices).	X			
Core	Program Memory	2.	The address error trap may occur while accessing certain program memory locations.	X	X	X	X
SPI	Frame Sync Pulse	3.	When in SPIx Slave mode with the Frame Sync pulse set as an input, FRMDLY must be set to '0'.	X	X	X	X
SPI	Frame Master Mode	4.	Received data is right-shifted under certain conditions.	X	X	X	X
Input Capture	Synchronous Cascade mode	5.	Even numbered timer does not reset on a source clock rollover in a synchronous cascaded operation.	X	X	X	X
PWM	Immediate Update	6.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X	X	X
PWM	PWM Override	7.	Under certain circumstances, updates to the OVRENH and OVRENL bits may be ignored by the PWMx module.	X	X		
PWM	Complementary Mode	8.	With dead time greater than zero, 0% and 100% duty cycles cannot be obtained on PWMxL and PWMxH outputs.	X	X	X	X
PWM	Center-Aligned Mode	9.	Under certain conditions, the PWMxH and PWMxL outputs are deasserted.	X	X	X	X
PWM	Current Reset Mode	10.	PWM Resets only occur on alternate cycles in Current Reset mode.	X	X	X	X
PWM	Master Time Base Mode	11.	When the Immediate Update is disabled, certain changes to the PHASEx register may result in missing dead time.	X	X	X	X
PWM	Redundant/ Push-Pull Output Mode	12.	When the Immediate Update is disabled, changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to 1 PWM clock.	X	X	X	X
PWM	Complementary Mode	13.	If PWM override is turned off during dead time, then the PWM generator may not provide dead time on the corresponding PWMxH-PWMxL edge transition.	X	X	X	X
ADC	DONE bit	14.	DONE bit does not work when an external interrupt is selected as the ADC trigger source.	X	X	X	X
ADC	Analog Channel	15.	Selecting the same ANx input for CH0 and CH1 results in erroneous readings for CH1.	X	X	X	X
CAN	DMA	16.	Write collisions on a DMA-enabled CAN module do not generate DMAC error traps.	X	X	X	X
JTAG	I/O	17.	$\overline{\text{MCLR}}$ pin operation may be disabled.	X	X	X	X
JTAG	I/O	18.	Active-high logic pulse on the I/O pin with TMS function at POR.	X	X	X	X
QEI	Velocity Counter	19.	Under certain circumstances, the Velocity Counter x register (VELxCNT) misses count pulses.	X	X	X	X
FRC	FRC Accuracy	20.	Change in the FRC accuracy.	X			

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A0	A1	A2	A3
Op Amp	Op Amp Offset Voltage	21.	Drift in the op amp offset voltage.	X	X	X	X
CPU	`div.sd`	22.	When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit is not getting set when an overflow occurs.	X	X	X	X
Output Compare	PWM Mode	23.	In the scaled down timer source for the Output Compare module, the first PWM pulse may not appear on the OCx pin.	X	X	X	X
Output Compare	Interrupt	24.	Under certain circumstances, an Output Compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.	X	X	X	X
CPU	`DO` Loop	25.	PSV access, including Table Reads or Writes in the first or last instruction of a `DO` loop, is not allowed.	X	X	X	X
PWM	PWM SWAP	26.	In Center-Aligned mode, there is missing dead time when SWAP is disabled.	X	X	X	X
PWM	Center-Aligned Mode	27.	Updates to the PHASEx registers occur only at the middle of the center-aligned PWM cycle.	X	X	X	X
ADC	Integral Nonlinearity (INL) Specification	28.	The AC/DC electrical characteristic, Integral Nonlinearity error in the ADC module, is not within the specifications published in the data sheet.	X	X	X	
PWM	Push-Pull Mode	29.	Period register writes may produce back-to-back pulses under certain conditions.	X	X	X	X
PWM	Trigger Compare Match	30.	First PWM/ADC trigger event on TRIGx match may not occur under certain conditions.	X	X	X	X
Input Capture	Cascade Mode	31.	When IC is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over, but instead occurs one cycle after the rollover.	X	X	X	X
SPI	DMA	32.	The data transferred from DMA to the SPIx buffer may get corrupted if the CPU accesses the Special Function Registers (SFRs) during the data transfer.	X	X	X	X
Core	`DO` Loop	33.	`DO` loops may work incorrectly if nested interrupts are enabled and interrupts occur during the last two instructions of the `DO` loop.	X	X	X	X
Core	Variable Interrupt Latency	34.	Address error trap may occur under certain circumstances if Variable Interrupt Latency mode is enabled.	X	X	X	X
Power-Saving Mode	Doze Mode	35.	Stack error trap may occur under certain circumstances if the processor is switched between normal mode and Doze mode.	X	X	X	X
SPI	SPIx Enable	36.	When the SPIx module is enabled for the first time, there may be a spurious clock on the SCKx pin, which causes a mismatch between the clock and data lines.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A0	A1	A2	A3
Data Memory	Stack Error Trap	37.	If the CPU is assigned a lower data bus master priority level than either the DMA Controller or USB, by configuring the MSTRPR register to any value other than 0x0000, then executing an ULNK instruction will result in a stack error trap.	X	X	X	X
SPI	Master Mode	38.	Received data is shifted by 1 bit when CKP = 1 and CKE = 0.	X	X	X	X
PTG	Debug Mode	39.	Single-stepping of the command sequence queue when device is in Debug mode is not functional.	X	X	X	X
PTG	PTGADD/ PTGCOPY	40.	PTGADD and PTGCOPY commands do not change the counter limit values.	X	X	X	X
I/O	Schmitt Trigger	41.	Schmitt Trigger output may produce glitches.	X	X	X	X
CPU	Data Flash Reads	42.	Given a specific set of preconditions, when two or more data Flash read instructions (via Program Space Visibility (PSV) read or table read) are executed back-to-back, one or more subsequent instructions will be misexecuted.	X	X	X	X
Electrical Characteristics	ADC2 Gain error	43.	ADC2 module specifications Parameters AD23a and HAD23a Gain Error (GERR) are updated to ±15%.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Core

For 44/64-pin and 100/121-pin devices, code execution may be unreliable under the following conditions:

- From -40°C to +85°C for FOSC above 120 MHz (60 MIPS)
- From +85°C to +125°C for FOSC above 100 MHz (50 MIPS)
- From +125°C to +150°C for FOSC above 60 MHz (30 MIPS)

Work around

Do not use clock speeds above 120 MHz for applications operating in the industrial temperature range (-40°C to +85°C) or above 100 MHz for temperatures in the extended range (+85°C to +125°C), or above 60 MHz for the high-temperature range (+125°C to +150°C).

Affected Silicon Revisions

A0	A1	A2	A3				
X							

2. Module: Core

An unexpected address error trap may occur during accesses to program memory addresses, 001h through 200h. This has been observed when one or more interrupt requests are asserted while reading or writing program memory addresses using TBLRDH/L, TBLWTH/L or PSV-based instructions.

Work around

Before executing instructions that read or write program memory addresses, 001h through 200h, disable interrupts using the DISI instruction.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

3. Module: SPI

When in SPIx Slave mode (MSTEN bit (SPIxCON1<5>) = 0) and using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2<15>) = 1) in Slave mode (SPIFSD bit (SPIxCON2<14>) = 1), the Frame Sync Pulse Edge Select bit (FRMDLY bit (SPIxCON2<1>) = 0) must be set to '0'.

Work around

None. The Frame Sync Pulse Edge Select bit, FRMDLY, cannot be set to produce a Frame Sync pulse that coincides with the first bit clock.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

4. Module: SPI

When SPIx is operating in Master mode and Framed SPIx mode is enabled (SPIxCON1<5> = 1 and SPIxCON2<15> = 1), received data may be shifted to the right by one bit when the following conditions are also true:

- The Frame Sync pulse is configured as an output (SPISFD (SPIxCON2<14>) = 0).
- Input data is sampled at the end of data output time (SMP (SPIxCON1<9>) = 1).

Work around

Clear the SMP bit while using SPIx Frame Master mode; this changes data sampling to the start of data output time.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

5. Module: Input Capture

The even numbered timer does not reset on a source clock rollover in Synchronous Cascaded mode operation.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules), ICy and ICx form a single 32-bit module. In Synchronous Cascaded mode (IC32 = 1, ICTRIG = 0 and the SYNCSEL<4:0> bits are not equal to 0h), both timers, ICyTMR:ICxTMR, must reset on a Sync_trig input from the 32-bit source timers, but only the odd timer (ICxTMR) is getting reset on a Sync Trigger input.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

6. Module: PWM

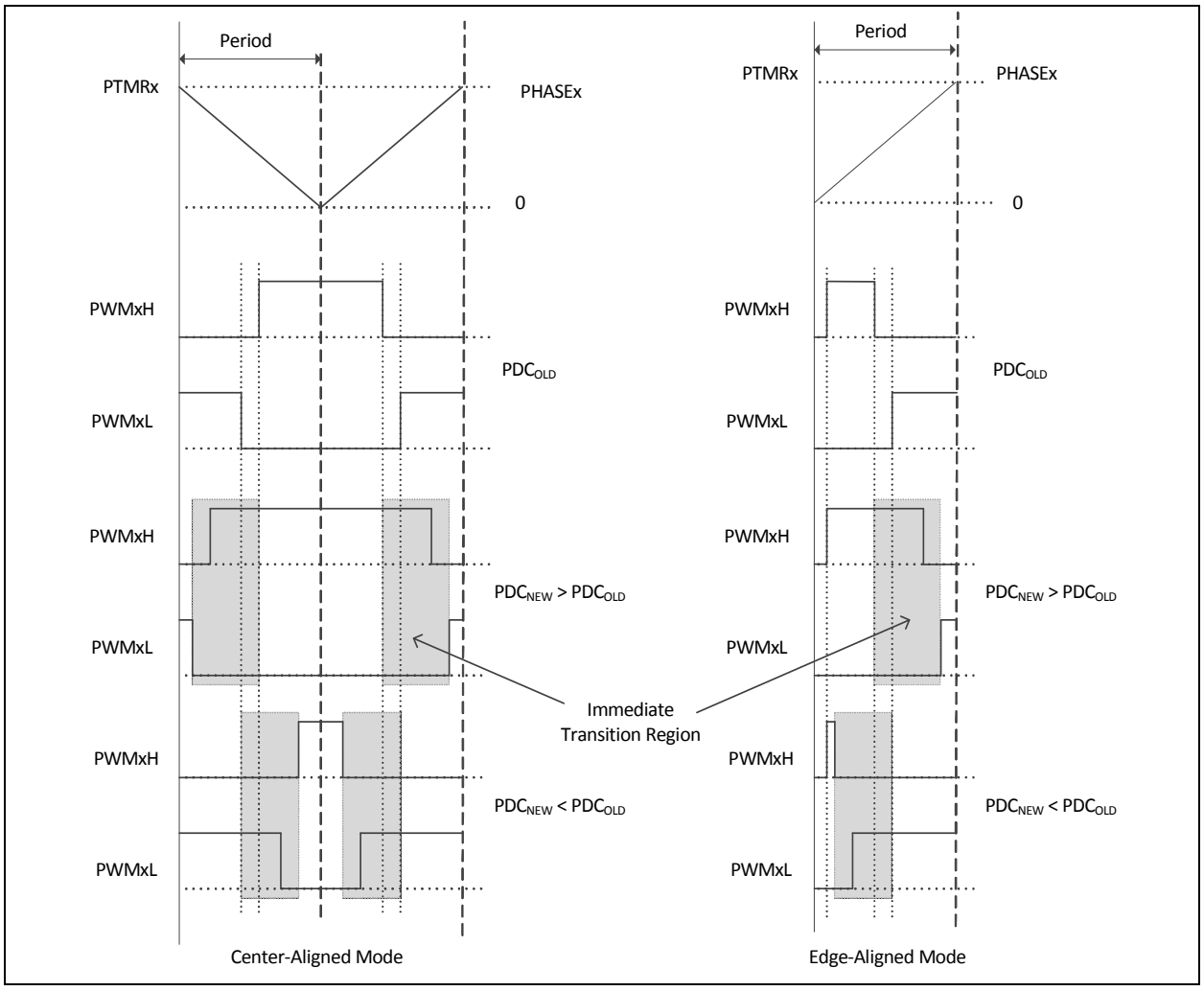
The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWM generator is configured to operate in Complementary mode with Independent Time Base (ITB) or master time base;
- Immediate update is enabled; and
- The value in the PDC register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDCOLD, newly calculated duty cycle, PDCNEW, and the point at which a write to the Duty Cycle register occurs within the PWM time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDCNEW, at a point of time when the PWM time base is counting a value that is in between PDCNEW and PDCOLD. Additionally, writing to the Duty Cycle register, close to the instant of time where dead time is being applied, may result in a reduced dead time which is effective on the PWMxH and PWMxL transition edges.

In Figure 1, if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

FIGURE 1: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES



Work around

None.

In most applications, the duty cycle update timing can be controlled using the TRIGx trigger, or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

7. Module: PWM

Under certain circumstances, an update to the IOCONx register to turn off the override will be ignored by the PWMx module. The issue has been observed to occur when the IOCONx update to turn off the override occurs close to the time when dead time is being applied.

Work around

1. Turn off the PWM dead time.
2. Alternatively, turn off the PWM override with the following procedure:
   a) Disable the PWMx module (PTEN = 0)
   b) Clear the Override Enable bits (OVRENH = 0 and OVRENL = 0)
   c) Enable the PWMx module (PTEN = 1)

Affected Silicon Revisions

A0	A1	A2	A3				
X	X						

8. Module: PWM

This issue is applicable when a PWM generator is configured to operate in Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, PWMxL is not asserted for 100% of the time when PDCx is zero. Similarly, when dead time is non-zero, PWMxH is not asserted for 100% of the time when PDCx is equal to PHASEx. This issue also applies to Master Time Base mode.

Work around

In Center-Aligned mode:

- To obtain 0% duty cycle, zero out the ALTDTRx register and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the ALTDTRx register and then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write (PHASEx + 1) to the PDCx register.

Alternatively, in both Center-Aligned and Edge-Aligned PWM modes, 0% and 100% duty cycle can be obtained by enabling the PWM override (IOCONx<9:8> = 0b11) with the Output Override Synchronization bit (IOCONx<0> = 1) set:

- For 0% duty cycle, set the value of the Override Data (IOCONx<7:6>) for the PWMxH and PWMxL pins as '0b01'
- For 100% duty cycle, set the value of the Override Data (IOCONx<7:6>) for the PWMxH and PWMxL pins as '0b10'

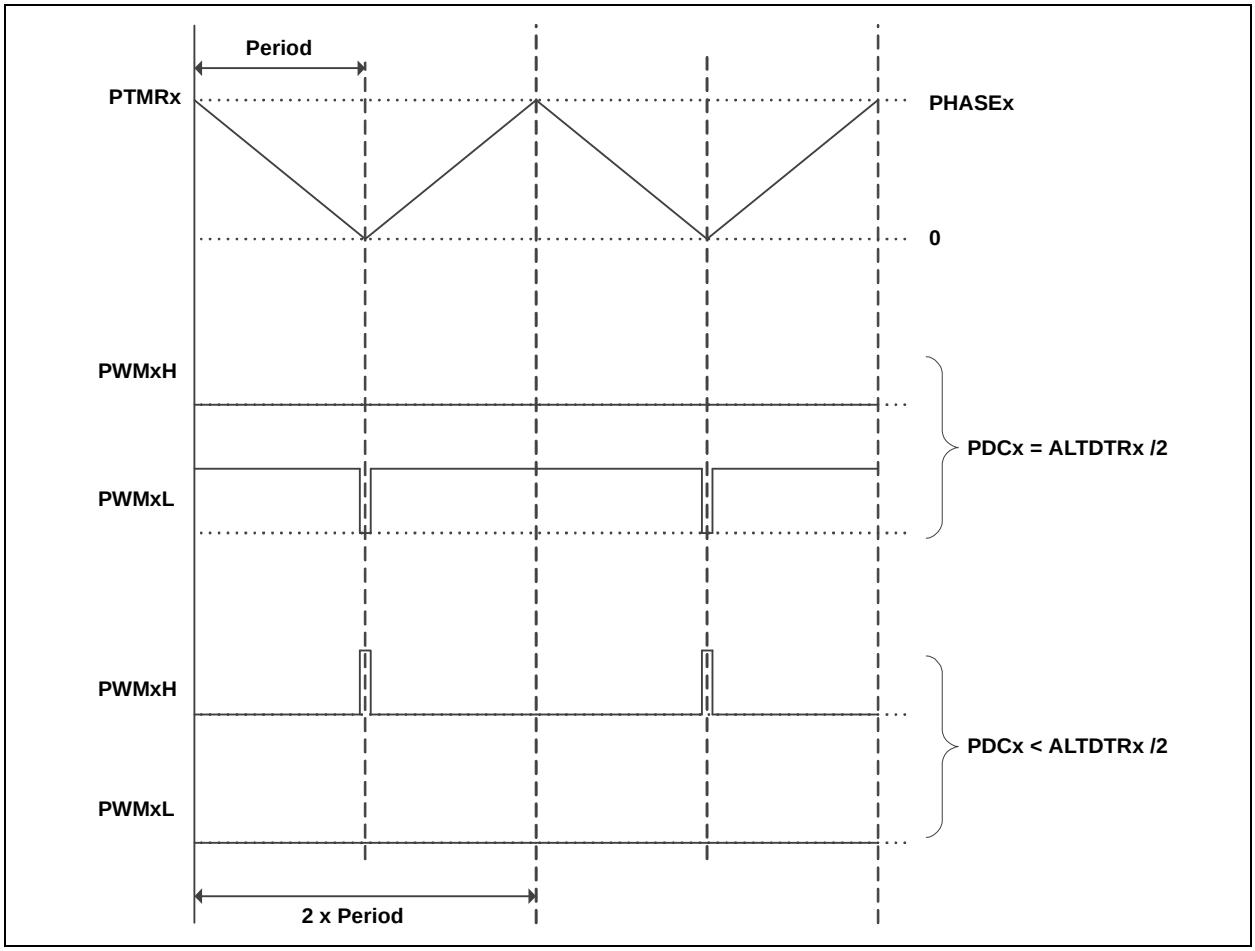
Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

9. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, if the value in the PDCx register is less than one-half the value in the ALTDTRx register, the PWM generator will force the PWMxL to low, and on the PWMxH, generates pulses of a width less than twice the dead time, as shown in Figure 2.

FIGURE 2: PWM GENERATOR TIMING DIAGRAM



Work around

Include a software routine to ensure that the duty cycle value written to the PDCx register is at least one-half of the value in ALTDTRx. Example 1 shows one method, with PDCtemp representing the variable which has the value to be written to the PDCx register. Alternatively, for duty cycle values less than half the desired dead-time value, zero out the ALTDTRx register or dynamically reduce the value in the ALTDTRx register, such that ALTDTRx is always equal to 2 * PDCx, as shown in Example 2.

EXAMPLE 1: WORK AROUND CODE

```
Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
PDCx = Altdtr_by2;
}
else
{
PDCx = PDCtemp;
}
```

EXAMPLE 2: WORK AROUND CODE

```
#define DESIRED_DEADTIME 100
if (PDCtemp < (DESIRED_DEADTIME/2))
{
ALTDTRx = PDCtemp * 2;
PDCx = PDCtemp;
}
else
{
ALTDTRx = DESIRED_DEADTIME;
PDCx = PDCtemp;
}
```

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

10. Module: PWM

When the PWM generator is configured to operate in Current Reset mode (XPRES (PWMCONx<1>) = 1 with Independent Time Base mode (ITB (PWMCONx<9>) = 1), the PWM Reset will happen only in every alternate PWM cycle.

Work around

1. Generate an interrupt when the comparator state changes. This interrupt should be high priority and could be either a comparator interrupt or PWM Fault interrupt. The current-limit interrupt does not function in this mode. Inside the interrupt, update PHASEx (period value) with a value less than the programmed duty cycle and then immediately update the PHASEx register with the value, as required by the application (PWM_period) shown in Example 3.

EXAMPLE 3: WORK AROUND CODE

```
PWMx ISR:
{
PHASEx = PDCx - 100;
PHASEx = PWM_period;
PWMxIF =0;
}
```

2. When the External Current Reset signal is applied to the PWM generator (configured using Current-Limit Signal Source Select bits (CLSRC<4:0>) in the PWM Fault Current-Limit Control registers (FCLCONx<14:10>)), depending on the PWM resolution selected, PCLKDIV<2:0> (PTCON2<2:0>), the maximum pulse width of the External Current Reset signal is to be restricted to less than the values as shown in Table 3.

TABLE 3: MAXIMUM EXTERNAL CURRENT RESET SIGNAL WIDTH

PCLKDIV<2:0>	Max. External Current Reset Signal Width (in nS)
000	20
001	40
010	80
011	160
100	320
101	640
110	1280

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

11. Module: PWM

In Edge-Aligned Complementary mode, changes to the PHASEx register under certain circumstances will result in missing dead time at the PWMxH-to-PWMxL transition. This has been observed only when all of the following are true:

- Master Time Base mode is enabled (PWMCONx<9> = 0);
- PHASEx is changed after the PWMx module is enabled; and
- The PHASEx register value is changed, so that either PHASEx < DTRx or PHASEx > PDCx.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

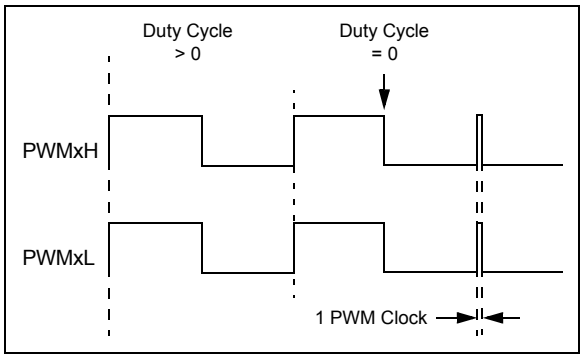
12. Module: PWM

In certain output modes, the PWMx module produces a pulse glitch of one PWM clock in width (Figure 3). This has been observed only when all of the following are true:

- Either Redundant or Push-Pull Output mode is selected (IOCONx<11:10> = 10 or 01);
- Immediate Update is disabled (PWMCONx<0> = 0); and
- The value of the current Duty Cycle register (either the PDCx or MDC register, as determined by PWMCONx<8>) is updated to zero from any non-zero value.

The pulse glitch has been observed to occur at the beginning of the following PWM boundary period.

FIGURE 3:



Work around

If the application requires a duty cycle of zero, two possible work arounds are available.

1. Use the PWM overrides to force the output to a low state, instead of writing a '0' to the Duty Cycle register. When using this method, the PWM override must be disabled when the duty cycle is a non-zero value. If output override synchronization is configured to occur on CPU clock boundaries (IOCONx<0> = 0), enabling and disabling the override must be timed to occur as closely as possible to the PWM period boundary.
2. Configure the module for Immediate Update (PWMCONx<0> = 1) *before* enabling the module. In this mode, writes to the Duty Cycle register have an immediate effect on the output. As with the previous work around, writes to the Duty Cycle register must be timed to occur as close to the PWM period boundary as possible in order to avoid distortion of the output.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

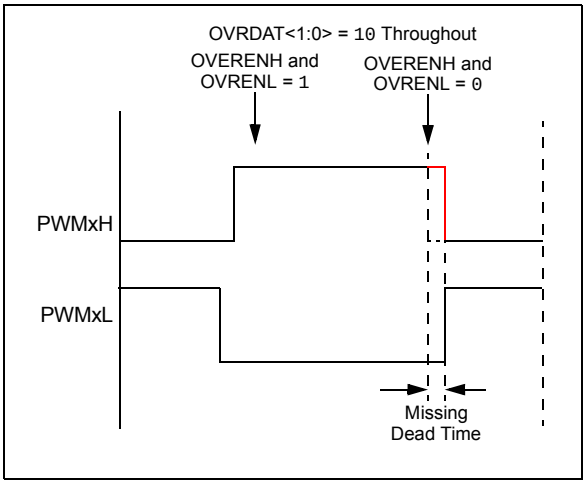
13. Module: PWM

In Complementary Output mode, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when the following occurs:

- Output override synchronization is configured to occur on the CPU clock boundary (IOCONx<0> = 0);
- Both PWMxH and PWMxL overrides are enabled prior to the event (OVRENH and OVRENL are both '1'), and
- Both overrides are disabled (OVRENH and OVRENL are both '0') at the instant the dead time should be asserted (Figure 4).

This has been observed in both Center-Aligned and Edge-Aligned modes.

FIGURE 4:



Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

14. Module: ADC

The ADC Conversion Status (DONE) bit (ADxCON1<0>) does not indicate completion of a conversion when an external interrupt is selected as the ADC trigger source (SSRC<2:0> bits (ADxCON1<7:5>) = 0x1).

Work around

Use an ADC interrupt or poll the ADxIF bit in the IFSx registers to determine the completion of the conversion.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

15. Module: ADC

Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.

Work around

Bring the analog signal into the device using both AN0 and AN3, connect externally, and then assign one input to CH0 and the other to CH1.

If selecting AN0 on CH1 (CH123Sx = 0), select AN3 on CH0 (CH0Sx = 3). Conversely, if selecting AN3 on CH1 (CH123Sx = 1), select AN0 on CH0 (CH0Sx = 0).

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

16. Module: CAN

When DMA is used with the CAN module, and the CPU and DMA write to a CAN Special Function Register (SFR) at the same time, the DMAC error trap does not occur. In addition, neither the PWCOL<3:0> bits of the DMAPWC SFR nor the DMACERR bit of the INTCON1 SFR become set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

Work around

There is no work around; however, under normal circumstances, this situation must not arise. When DMA is used with the CAN module, the application must not be writing to the CAN SFRs.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

17. Module: JTAG

The $\overline{\text{MCLR}}$ pin (normally input only) may be set as an output pin through the JTAG interface. If it is set at an output high level, subsequent device Resets are prevented until the device is powered down.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

18. Module: JTAG

At Power-on Reset (POR), when JTAG is disabled in the Configuration bits, the I/O pin with TMS function produces an active-high logic pulse with a pulse width in the order of milliseconds.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

19. Module: QEI

The Velocity Counter x (VELxCNT) is a 16-bit wide register that increments or decrements based on the signal from the quadrature decoder logic. Reading this register results in a Counter Reset. Typically, the user application must read the velocity counter at a rate of 1 kHz-4 kHz.

As a result of this issue, the velocity counter may miss a count if the user application reads the Velocity Counter x register at the same time as a (+1 or -1) count increment occurs.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

20. Module: FRC

Refer to Table 4 for a change in the FRC accuracy at FRC Frequency = 7.3728 MHz.

TABLE 4: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended -40°C ≤ TA ≤ +150°C for High Temperature					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz							
F20a	FRC	-2	0.5	2	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-3	1.5	3	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V
HF20	FRC	-4	—	4	%	-40°C ≤ TA ≤ +150°C	VDD = 3.0-3.6V

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X							

21. Module: Op Amp

When operating at lower temperatures (< 0°C), there is a drift in the op amp offset voltage. Refer to Table 5 for a change in the op amp offset voltage at different operating temperatures.

TABLE 5: OP AMP SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CM42	VOFFSET	Op Amp Offset Voltage	—	±20	±70	mV	0°C ≤ TA ≤ +125°C
CM42	VOFFSET	Op Amp Offset Voltage	—	—	±500	mV	-40°C ≤ TA < 0°C

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

22. Module: CPU

When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

This erratum only affects operations in which at least one of the following conditions is true:

a) Dividend and divisor differ in sign,

b) Dividend > 0x3FFFFFFF or

c) Dividend ≤ 0xC0000000.

Work around

The application software must perform both the following actions in order to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.

b) If the dividend and divisor differ in sign (e.g., dividend is negative and divisor is positive), then after executing the `div.sd` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient.

If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

23. Module: Output Compare

The first PWM pulse may not appear on the OCx pin if the timer source of the Output Compare x module is scaled down.

The first pulse on the OCx pin is missed in PWM mode when the timer source for the Output Compare x module is scaled down (1:8, 1:64 or 1:256) using the Timerx Input Clock Prescale Select bits, TCKPS<1:0> (TxCON<5:4>).

Work around

- Configure the prescaler for the source timer to 1:1 for Output Compare 3, 4, 5 and 6.
- The Output Compare 1 or 2 module can be used. The scaled down timer (1:8, 1:64 or 1:256) can be used as a source for the Output Compare 1 and 2 modules.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

24. Module: Output Compare

Under certain circumstances, an output compare match may cause the Output Compare Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM<2:0> = `001`, `010` or `100`);
- One of the timer modules is being used as the time base; and
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing the OCM<2:0> bits after the One-Shot mode compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing the OCM<2:0> bits. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

25. Module: CPU

Table write (TBLWTx), table read (TBLRDx) and PSV Flash read instructions should not be used in the first or last instruction locations of a DO loop.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

26. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted at all times if the SWAP (IOCONx<1>) bit setting is changed from '1' to '0' in order to remap PWMxH and PWMxL to their respective pins, after the PWM module is enabled.

Work around

None.

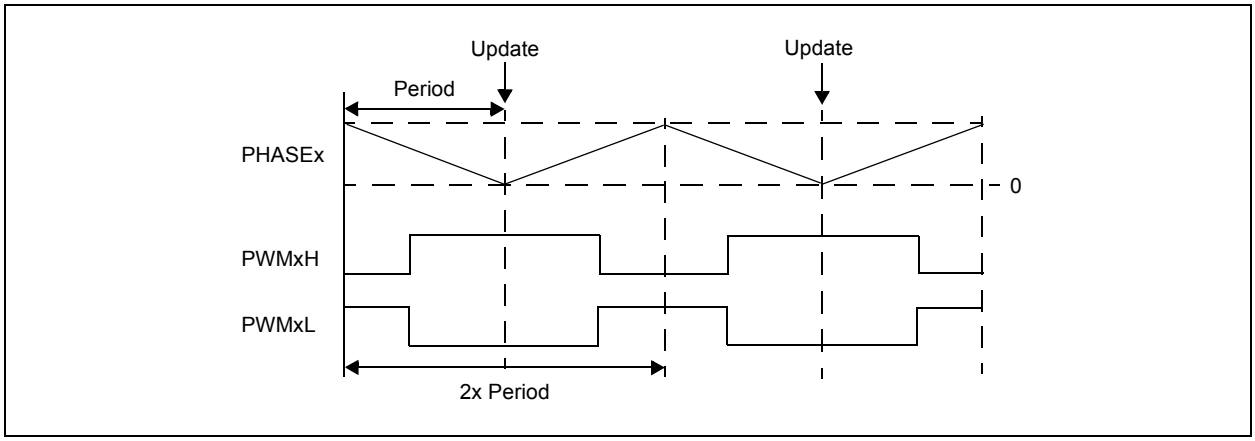
Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

27. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, updates to the PHASEx register take effect in the middle of a Center-Aligned PWM cycle, as shown in Figure 5. This occurs only when the Immediate Update feature is disabled (IUE = 0). If Immediate Update is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

FIGURE 5:



Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

28. Module: ADC

In the AC/DC electrical characteristics, the Integral Nonlinearity (INL) error for the ADC2 module differs in 12-Bit ADC mode with the operating temperature range from the specifications published in the *"dsPIC33EPXXXGM3XX/6XX/7XX Family Data Sheet"*. The updated text is shown in **bold** in Table 33-57 below:

TABLE 33-57: ADCx MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (12-Bit Mode) – VREF-							
AD20a	Nr	Resolution	12 data bits			bits	
AD21a	INL	Integral Nonlinearity	**-3.0**	—	**+3.0**	LSb	**-40°C ≤ TA ≤ +85°C Only** VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V (Note 2)
			-6.0	**—**	**6.0**	LSb	**+85°C ≤ TA ≤ +125°C Only** VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V (Note 2)

Work around

None.

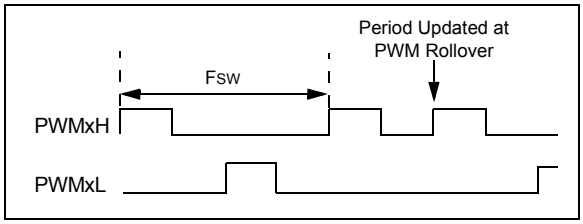
Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X					

29. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx<11:10> = 10) with the Enable Immediate Period Update bit enabled (PTCON <10> = 1), a write to the Period register that coincides with the period rollover event may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins (Figure 6).

FIGURE 6:



Work around

Ensure that the update to the PWM Period register occurs away from the PWM rollover event by setting the EIPU bit (PTCON<10> = 1). Use either the PWM Special Event Trigger (SEVTCMP) or the PWM Primary Trigger (TRIGx) to generate a PWM Interrupt Service Routine (ISR) near the start of the PWM cycle. This ISR will ensure that period writes do not occur near the PWM period rollover event.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

30. Module: PWM

The triggers generated by the PWMx Primary Trigger Compare Value register (TRIGx) will not trigger at the point defined by the TRIGx register values on the first instance for the configurations listed below. Subsequent trigger instances are not affected.

- Trigger compare values for TRIGx are less than 8 counts
- Trigger Output Divider bits, TRGDIV<3:0> (TRGCONx<15:12>), are greater than '0'
- Trigger Postscaler Start Enable Select bits, TRGSTRT<5:0> (TRGCONx<5:0>), are equal to '0'

Work around

Configure the PWMx Primary Trigger Compare Value Register (TRIGx) values to be equal to or greater than 8.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

31. Module: Input Capture

When the IC is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over, but instead occurs one cycle after the roll over.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules) form a single 32-bit module. In such a configuration, when ICx counts for 16-bit value (65535 cycles) and rolls over to zero during the next clock cycle (65536th cycle), ICy should immediately increment by one. But ICy timer remains at zero and during the next clock cycle (65537th cycle), both ICx and ICy timers increment by one.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

32. Module: SPI

The data transferred from the DMA to the SPIx buffer may get corrupted if the CPU is writing to any Special Function Registers (SFRs) during the data transfer.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

33. Module: Core

When interrupt nesting is enabled by clearing the NSTDIS bit (INTCON1<15> = 0), an interrupt that occurs during the last two instructions of the DO loop can end it prematurely. The DCOUNT is incorrectly decremented twice when:

- an interrupt occurs during the last two instructions of a DO loop, and
- the second higher priority interrupt occurs exactly four instruction cycles later.

Work around

Disable interrupt nesting by setting the NSTDIS bit (INTCON1<15> = 1).

Alternatively, for interrupts of priority levels up to 6, use the DISI instruction to disable the nested interrupts while executing the last two instructions of the DO loop.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

34. Module: Core

An address error trap may occur if the variable exception processing latency is enabled by setting the VAR bit (CORCON<15> = 1), and the same data variables are modified both within and outside the Interrupt Service Routine.

Work around

Enable the Fixed Interrupt Latency mode by clearing the VAR bit (VAR (CORCON<15>) = 0).

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

35. Module: Power-Saving Mode

A stack error trap may be generated when all of the following conditions are met:

- Device operates in Doze mode.
- The Processor Clock Reduction Select bits, DOZE<2:0> (CLKDIV<14:12>), are set to '0b011' or '0b01xx'.
- Multiple interrupts are enabled.
- In the user function, the processor speed is switched between normal speed and reduced speed (as defined by the DOZE<2:0> bits).

Work around

In Doze mode, set the Processor Clock Reduction Select bits, DOZE<2:0> (CLKDIV<14:12>), to '0b010', '0b001' or '0b000'.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

36. Module: SPI

When the SPIx module is enabled for the first time, there may be a spurious clock on the SCKx pin. This may result in one bit of data getting shifted out on the data line, resulting in a mismatch between the clock and data lines.

This issue may also occur when the SPIx module is disabled during data transmission, and subsequently enabled.

Work around

1. Disable the SPIx module after two SPIx cycles and then re-enable SPIx, this will synchronize the clock and data.
2. If the SPIx module is configured on the PPS pins, first enable the SPIx without configuring the PPS, then allow the two SPIx clocks to pass and then configure the PPS to connect to the SPIx module. This will prevent the spurious SPIx clock going out on the pin. If the SPIx module is turned off periodically, ensure that the PPS is turned off as well.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

37. Module: Data Memory

If the CPU is assigned a lower data bus master priority level than either the DMA Controller or USB, by configuring the MSTRPR register to any value other than 0x0000, then executing an ULNK instruction will result in a stack error trap.

Work around

1. Ensure that the MSTRPR register is always maintained at its default (Reset) value of 0x0000. Do not write any other value to this SFR.
2. If writing source code in assembly, the recommended work around is to replace all instances of the ULNK instruction with:

```
mov  W14,W15
mov  [--w15], W14
bclr  CORCON, #SFA
```

If using the MPLAB® XC16 compiler (XC16 v1.30 or later), specify the compiler option: `merrata=busmaster` (Project Properties >> XC16 >> xc16-gcc >> General >> Additional Options).

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

38. Module: SPI

In Master mode, the SPI device reads the data on the SDIx line incorrectly (data is shifted by one bit; e.g., if 0x37 is transmitted, it is read as 0x1B).

The issue occurs for the following configuration:

- SMP = x
- CKE = 0
- CKP = 1
- Master MIPS ≤ Slave MIPS. Issue occurred over a range of SPI clock frequencies (1 MHz to 16 MHz).

Work around

When CKE = 0 and CKP = 1, use the following sequence to initiate SPI communication:

- Set the Slave Select line to the Idle state
- Set the SCKx pin high
- Enable Master mode
- Enable the module
- Assert the Slave Select line

If the SPI slave device does not use the $\overline{SSx}$ line, the SPI slave should be enabled only after the master clock line is made high.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

39. Module: PTG

Single-stepping through the command sequence feature, which is enabled by setting the PTGSSEN bit when the device is in Debug mode, does not work. Also, the corresponding step interrupt, which generates after each step execution in the queue, doesn't work.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

40. Module: PTG

The PTGADD/PTGCOPY commands which add the contents of the PTGADJ register, or copy the contents of the PTGHOLD register to the PTG Counter Limit registers (PTGC0LIM and PTGC1LIM) does not work. Though the loop counter value gets updated, loop repletion cannot be changed dynamically after starting execution.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

41. Module: I/O

If the input signal rise or fall time is greater than 300 nS, the I/O Schmitt Trigger output may have glitches.

Work around

The rise/fall times must be less than 300 nS.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

42. Module: CPU

Note: This issue is deterministic based on the instruction sequence executed, and is not sensitive to manufacturing process, temperature, voltage or other application operating conditions that do not affect the instruction sequence.

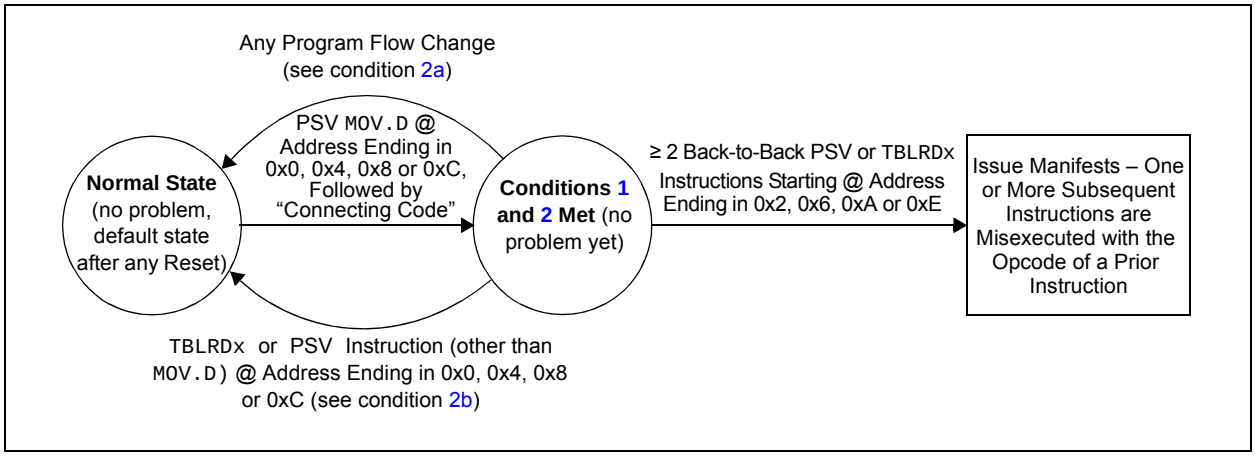
When two or more data Flash read instructions (via Program Space Visibility (PSV) read or table read) are executed back-to-back, one or more subsequent instructions can be misexecuted when all of the conditions in Table 6 occur.

TABLE 6: REQUIRED CONDITIONS

1.	A PSV `MOV.D` instruction is executed with an opcode at address ending in 0x0, 0x4, 0x8 or 0xC; and
2.	Some "connecting code" is executed (following the `MOV.D` of condition 1), with the properties: a) The connecting code does not include any program flow changes, including: taken branch instructions (including all versions of `BRA`, `CPBEQ`, `CPBGT`, `CPBLT`, `CPBNE`), `CALL`, `CALL.L`, `GOTO`, `GOTO.L`, `RCALL`, `RETLW`, `RETURN`, vectoring to an ISR, returning from an interrupt (`RETFIE`) and certain debug operations, such as `break` and `one-step`; and b) The connecting code does not include a `TBLRDx` or non-`MOV.D` PSV instruction, located at a Flash memory address ending in 0x0, 0x4, 0x8 or 0xC; and c) The connecting code is at least two instruction words in length; and d) The connecting code does not end with a `REPEAT` instruction, with count > `0`; and
3.	≥ 2 back-to-back PSV or `TBLRDx` instructions are executed (following the code of condition 2), where the first of the back-to-back instructions is located at an address ending in 0x2, 0x6, 0xA or 0xE.

Figure 7 provides an example of the effective behavior.

FIGURE 7: SIMPLIFIED BEHAVIOR



Work around

The issue can be avoided by ensuring any one or more of the requirements are not met. For example:

1. All instances of PSV `MOV.D` can be replaced with two PSV `MOV` instructions instead. Non-PSV `MOV.D` instructions acting on RAM/SFRs do not need to be modified; or
2. If not already present, a program flow change instruction (such as `BRA $+2`) can be inserted above back-to-back data Flash read sequences; or
3. Back-to-back data Flash read instruction sequences can be broken up by inserting a non-Flash read instruction (such as a `NOP`), in between the Flash read instructions; or
4. The alignment of the code can be shifted to avoid the required opcode location addresses.

C code built with MPLAB® XC16 Compiler Version 1.32, or later, implements the work around by default. However, if the application uses Assembly language routines, these should be manually modified to implement the work around. Additionally, if precompiled libraries are used, these should be built with XC16 Version 1.32 or later. For additional information, please visit: **www.microchip.com/erratum_psrd_psrd**

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

43. Module: Electrical Characteristics

The Gain Error (GERR) of the ADC2 module does not meet the specifications Parameters AD23a (Table 33-57) and HAD23a (Table 34-14). The Gain Error of ADC2 is at minimum -15 LSbs and at maximum +15 LSbs. ADC1 specifications are unaffected and adhere to Tables 33-57 and 34-14.

Work around

None.

Affected Silicon Revisions

A0	A1	A2	A3				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000689**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

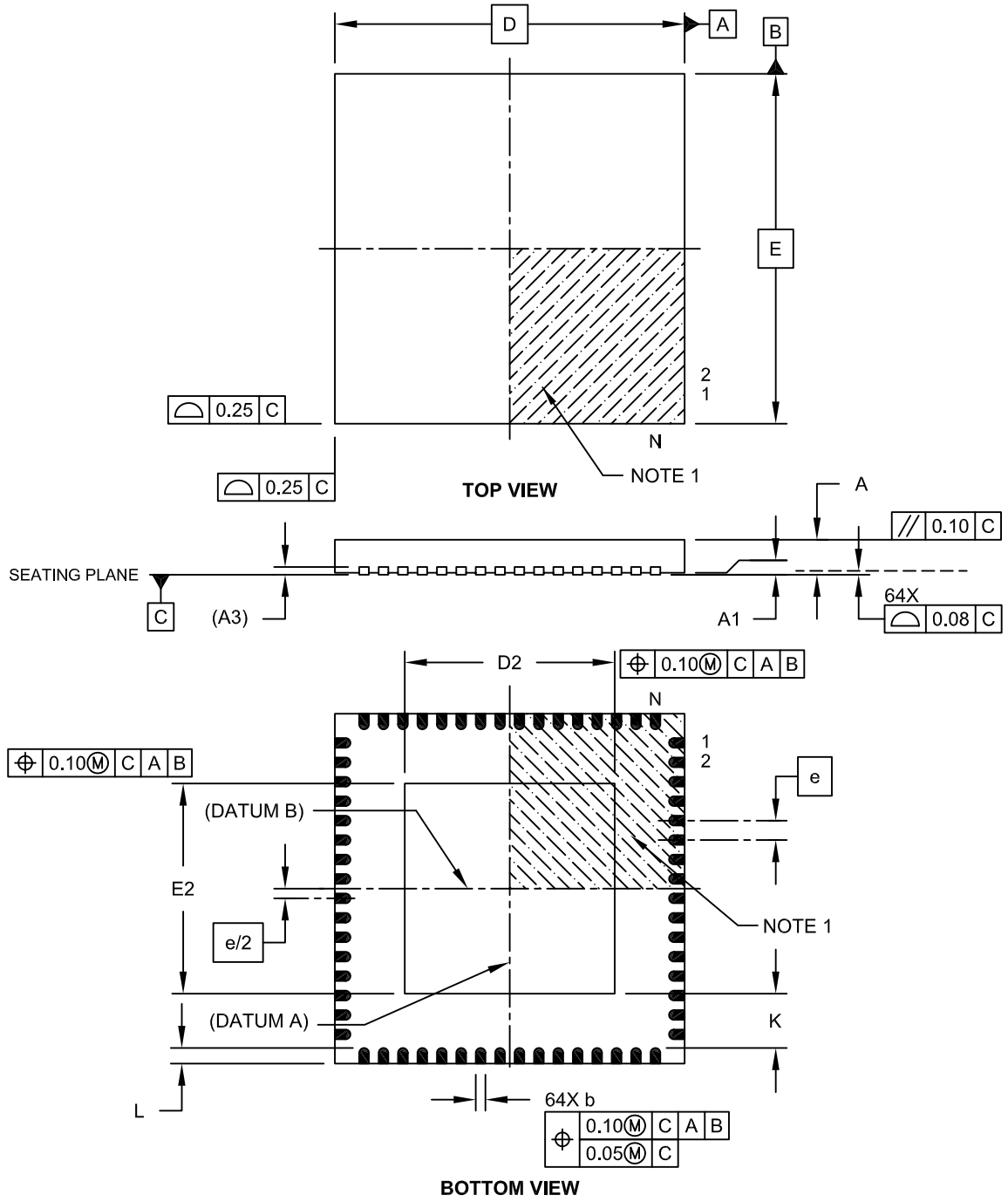
1. Module: Packaging Information

In the *"dsPIC33EPXXXGM3XX/6XX/7XX Family Data Sheet"*, **Section 35.2 "Package Details"**, dimensions for the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 7.15 x 7.15 Exposed Pad [QFN] is mentioned. However, the dsPIC33EPXXXGM3XX/6XX/7XX family devices are not available in this package.

The dsPIC33EPXXXGM3XX/6XX/7XX family devices are available in the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN], and the package dimensions are shown on the following pages.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

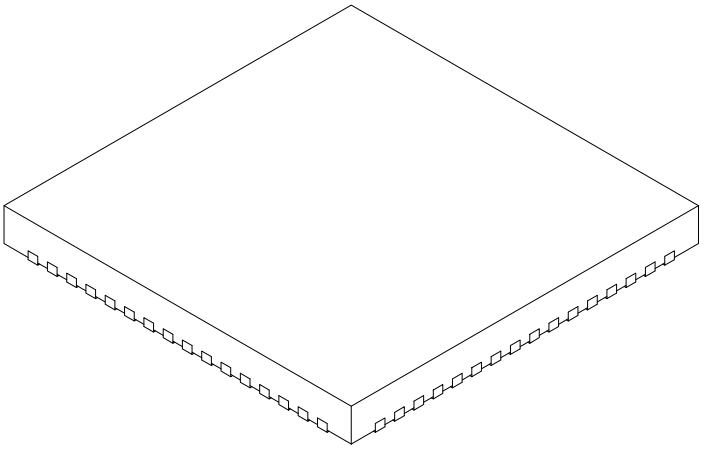
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-154A Sheet 1 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

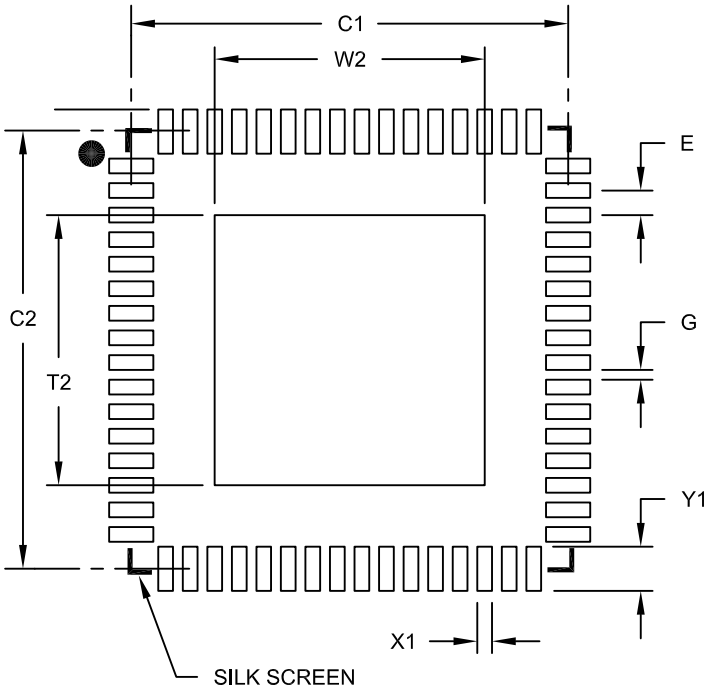
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A

2. Module: Power-Saving Features

In **Section 10.0 "Power-Saving Features"**, there are two changes included.

Change 1: Example 10-1 is modified to show a condition and a note. The changes are shown below in **bold**.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode(1)
```

Note 1: The use of PWRSV #SLEEP_MODE has limitations when the Flash Voltage Regulator bit, VREGSF (RCON<11>), is set to Standby mode. Refer to Section 10.2.1 "Sleep Mode" for more information.

Change 2: The fourth paragraph of **Section 10.2.1 "Sleep Mode"** is modified to include the condition where the Flash voltage regulator is placed in Standby mode. An additional example is added to show how to implement the SLEEP instruction in a 4-instruction word-aligned function. The modified text is added as follows:

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration). However, putting the Flash Voltage Regulator in Standby mode (VREGSF = 0) when in Sleep has the effect of corrupting the prefetched instructions placed in the instruction queue. When the part wakes up, these instructions may cause undefined behavior. To remove this problem, the instruction queue must be flushed after the part wakes up. A way to flush the instruction queue is to perform a branch. Therefore, it is required to implement the SLEEP instruction in a function with 4-instruction word alignment. The 4-instruction word alignment will assure that the SLEEP instruction is always placed on the correct address to make sure the flushing will be effective. Example 10-2 shows how this is performed.

EXAMPLE 10-2: SLEEP MODE PWRSAV INSTRUCTION SYNTAX (WITH FLASH VOLTAGE REGULATOR SET TO STANDBY MODE)

```
.global    _GoToSleep
.section   .text
.align     4

_GoToSleep:

PWRSAV  #SLEEP_MODE
BRA     TO_FLUSH_QUEUE_LABEL
TO_FLUSH_QUEUE_LABEL:
RETURN
```

3. Module: Pin Diagrams

In the **Pin Diagrams**, both the 44-Pin Diagrams for TQFP and QFN are corrected by removing the reference to U1RTS on pin number 27.

The dsPIC33EPXXXGM3XX/6XX/7XX family devices do not have U1RTS, U1CTS, U2RTS, U2CTS pins on 44-pin packages. Only U3RTS, U3CTS and U4RTS, U4CTS are available as remappable pins.

4. Module: Pin Diagrams

In the **Pin Diagrams**, the 44-Pin TQFP diagram is corrected by replacing the reference to OA4IN+ on pin 27 with OA3IN+.

5. Module: Pin Diagrams

In the **Pin Diagrams**, both the 64-Pin Diagrams for TQFP and QFN are corrected to include the following PMP Pins:

- PMA6 has been added to RB1
- PMA7 has been added to RC1
- PMP13 has been added to RC2

6. Module: Electrical Characteristics

In the AC/DC electrical characteristics, the Integral Nonlinearity (INL) error for the ADC module differs in 12-Bit ADC mode from the specifications published in the *"dsPIC33EPXXXGM3XX/6XX/7XX Family Data Sheet"*. The updated text is shown in **bold** in Table 33-57 below.

TABLE 33-57: ADCx MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (12-Bit Mode)							
AD20a	Nr	Resolution	12 data bits			bits	
AD21a	INL	Integral Nonlinearity	**-2**	—	**+2**	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V (Note 2)

7. Module: Memory Organization

In **Section 4.3 "Special Function Register Maps"**, Table 4-2 and Table 4-3 are corrected by removing the following IFSx/IPCx/IECx bits:

- FLT1IP0, FLT1IP1 and FLT1IP2 of IPC15
- FLT2IP0, FLT2IP1 and FLT2IP2 of IPC16
- FLT3IP0, FLT3IP1 and FLT3IP2 of IPC18
- FLT4IP0, FLT4IP1 and FLT4IP2 of IPC19
- FLT1IE of IEC3
- FLT2IE, FLT3IE and FLT4IE of IEC4
- FLT1IF of IFS3
- FLT2IF, FLT3IF and FLT4IF of IFS4

8. Module: Electrical Characteristics

In the AC/DC electrical characteristics, the Power-Down Current (I_{PD}) for the devices differs from the specifications published in the *"dsPIC33EPXXXGM3XX/6XX/7XX Family Data Sheet"*.

The updates for Table 33-8 of the data sheet are highlighted in **bold** in the following table.

TABLE 33-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typ.(2)	Max.	Units	Conditions		
Power-Down Current (I_{PD})(1)						
DC60d	35	**200**	µA	-40°C	3.3V	Base Power-Down Current
DC60c	40	**250**	µA	+25°C		
DC60b	250	**1500**	µA	+85°C		
DC60c	1000	**3500**	µA	+125°C		
DC61d	8	10	µA	-40°C	3.3V	Watchdog Timer Current: ΔI_{WDT}(3)
DC61c	10	15	µA	+25°C		
DC61b	12	20	µA	+85°C		
DC61c	13	25	µA	+125°C		

9. Module: Configuration Byte Register Map

In Table 30-1: Configuration Byte Register Map, configuration byte addresses published in the *"dsPIC33EPXXXGM3XX/6XX/7XX Family Data Sheet"* differ for the devices with a memory size equal to 128 Kbytes and 256 Kbytes. The corrected Configuration byte addresses are shown in bold below:

Configuration byte addresses for 128K devices are:

FICD = **0x155F0**
FPOR = **0x155F2**
FWDT = **0x155F4**
FOSC = **0x155F6**,
FOSCSEL = **0x155F8**
FGS = **0x155FA**

Configuration byte addresses for 256K devices are:

FICD = **0x2ABF0**
FPOR = **0x2ABF2**
FWDT = **0x2ABF4**
FOSC = **0x2ABF6**
FOSCSEL = **0x2ABF8**
FGS = **0x2ABFA**

10. Module: Instruction Set Overview

Modify the existing note of Table 31-2: Instruction Set Overview on pages 422 to 427 to **"Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle"**. This note should be referenced with a superscript (1) on the **"# of Cycles(1)"** column of Table 31-2.

TABLE 31-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

11. Module: Electrical Characteristics

In Table 33-10, the electrical characteristics of Parameter DI31 are updated. The parameter values are highlighted in **bold** in the following table.

TABLE 33-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI31	ICNPD	Change Notification Pull-Down Current(4)	20	**60**	**120**	µA	VDD = 3.3V, VPIN = VDD

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.

4: VIL source < (VSS – 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

12. Module: 10-Bit/12-Bit Analog-to-Digital Converter (ADC)

In Register 23-2: ADxCON2, the OFFCAL bit is unimplemented. The changes are highlighted in **bold** in the following table.

REGISTER 23-2: ADxCON2: ADCx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	**U-0**	U-0	R/W-0	R/W-0	R/W-0
VCFG2(1)	VCFG1(1)	VCFG0(1)	**—**	—	CSCNA	CHPS1	CHPS0
bit 15							bit 8

bit 12 **Unimplemented:** Read as '0'

13. Module: PTG Control Registers

In Register 25-1: PTGCST, the PTG Watchdog Timer Time-out Status bit should be referenced as **PTGWTO**. The changes are highlighted in **bold** in the following table.

REGISTER 25-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	**HS-0**	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PTGEN	**PTGWTO**	—	—	—	—	PTGITM1(1)	PTGITM0(1)
bit 7							bit 0

bit 6 **PTGWTO**: PTG Watchdog Timer Time-out Status bit
1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out.

14. Module: LED Control Registers

In Register 16-23: LEBDLYx, the LEB register bits<2:0> are unimplemented. The changes are highlighted in **bold** in the following table.

REGISTER 16-23: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER x

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	**LEB<8:5>**			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	**U-0**	**U-0**	**U-0**
LEB<4:0>					**—**	**—**	**—**
bit 7							bit 0

bit 15-12 **Unimplemented:** Read as '0'
bit 11-3 **LEB<8:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits
The value is in 8.32 ns increments.
bit 2-0 **Unimplemented:** Read as '0'

15. Module: Special Features

Brown-out Reset: The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP.

Here, VCAP should be read as **VDD**.

16. Module: Interrupt Controller Register

Updates to the INTCON2 register bits are as follows:

Table 4-2: Interrupt Controller Register Map for dsPIC33EPXXXGM6XX/7XX Devices and Table 4-3: Interrupt Controller Register Map for dsPIC33EPXXXGM3XX Devices have been updated. The changes are highlighted in **bold** in the following table.

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	**INT4EP**	**INT3EP**	INT2EP	INT1EP	IINT0EP	**8000**

Register 7-4: INTCON2 has been updated. The changes are highlighted in **bold** in the following table.

REGISTER 7-4: INTERRUPT CONTROL REGISTER 2

U-0	U-0	U-0	**R/W-0**	**R/W-0**	R/W-0	R/W-0	R/W-0
—	—	—	**INT4EP**	**INT3EP**	INT2EP	INT1EP	INT0EP
bit 7							bit 0

bit 4 **INT4EP: External Interrupt 4 Edge Detect Polarity Select bit**
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 3 **INT3EP: External Interrupt 3 Edge Detect Polarity Select bit**
1 = Interrupt on negative edge
0 = Interrupt on positive edge

17. Module: Electrical Characteristics

Note 3 referred in parameters:

- SP10 in Table 33-43: SPI1 Master Mode is updated as (changes are shown in **bold**):

The minimum clock period for SCK1 is **40 ns**. The clock generated in Master mode must not violate this specification.

- SP70 in Table 33-44: SPI1 Slave Mode is updated as (changes are shown in **bold**):

The minimum clock period for SCK1 is **40 ns**. Therefore, the SCK1 clock generated by the master must not violate this specification.

18. Module: I/O Ports

The SDO3 description in Table 11-3: Output Selection for Remappable Pins (RPn) should be read as (changes are shown in **bold**):

"RPn tied to SPI3 **Data** Output".

19. Module: Quadrature Encoder Interface (QEI) Module

In Register 17-2: QEIxIOC, the phrase, "home input", for bit 15 QCAPEN is inappropriate and should be read as (changes are shown in **bold**):

QCAPEN**:** QEIx Position Counter Input Capture Enable bit

1 = **Index match event triggers a position capture event**

0 = **Index match event does not trigger a position capture event**

20. Module: Oscillator Configuration

The OSCTUN range on the positive side is clamped to +1.45%, hence in Register 9-4: OSCTUN: FRC Oscillator Tuning Register, the following should be read as:

011111 = **Maximum frequency deviation of 1.453% (7.477 MHz)**

011110 = **Center frequency + 1.406% (7.474 MHz)**

21. Module: Memory Organization

In Table 4-2: Interrupt Controller Register Map for dsPIC33EPXXXGM6XX/7XX Devices and Table 4-3: Interrupt Controller Register Map for dsPIC33EPXXXGM3XX Devices, the changes are as follows (changes are shown in **bold**):

- SFR Name – IPC0: Bit 0 should be read as **INT0IP0**
- SFR Name – IPC1: Bit 0 should be read as **DMA0IP0**

22. Module: Timer1

In Register 12-1: T1CON: Timer1 Control Register (changes are shown in **bold**):

- bit 4 should be read as **TCKPS0**

23. Module: PWM

In Register 16-18: TRGCONx: PWMx Trigger Control Register, bits<5-0> should be read as (changes are highlighted in **bold** in the following table):

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	**TRGSTRT5(1)**	**TRGSTRT4(1)**	**TRGSTRT3(1)**	**TRGSTRT2(1)**	**TRGSTRT1(1)**	**TRGSTRT0(1)**
bit 7							bit 0

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2013)

Initial release of this document; issued for silicon revision A0.

Includes silicon issues 1 (Core, CPU), 2 (Core, Program Memory), 3-4 (SPI, Frame modes), 5 (Input Capture), 6-10 (PWM), 11-12 (ADC), 13 (ECAN), 14-15 (JTAG), and 16 (QEI).

Rev B Document (9/2013)

Adds silicon issue **20. Module: "FRC"** and updates Table 2. Adds a new bulleted list in silicon issue **20. Module: "FRC"**. Updates work around section in silicon issue **20. Module: "FRC"**.

Rev C Document (10/2013)

Updates Table 1 with new revision ID, "A1". Updates Table 2.

Rev D Document (11/2013)

Adds silicon issue **21. Module: "Op Amp"** and updates Table 2.

Rev E Document (6/2014)

Replaced silicon issue **9. Module: "PWM"**. Adds silicon issue **10. Module: "PWM"**, **11. Module: "PWM"**, **12. Module: "PWM"**, **13. Module: "PWM"** and updates Table 2.

Rev F Document (9/2014)

Updates Table 1 with new revision ID, "A2". Updates Table 2 and Table 3. Adds silicon issues **22. Module: "CPU"**, **23. Module: "Output Compare"**, **24. Module: "Output Compare"**. Replaces silicon issue **6. Module: "PWM"**.

Adds data sheet clarification **1. Module: "Packaging Information"**.

Rev G Document (12/2014)

Updates the silicon issue description of **7. Module: "PWM"**, **10. Module: "PWM"**, **11. Module: "PWM"**, **12. Module: "PWM"** and **13. Module: "PWM"**. Basic issue is unchanged.

Adds new silicon issues **25. Module: "CPU"**, **26. Module: "PWM"**, **27. Module: "PWM"** and **28. Module: "ADC"**.

Adds data sheet clarification **2. Module: "Power-Saving Features"**.

Rev H Document (5/2015)

Updates Table 1, Table 2 and all Affected Silicon Revision tables with new revision ID, "**A3**."

Replaces silicon issue **5. Module: "Input Capture"**.

Add silicon issues **29. Module: "PWM"**, **30. Module: "PWM"** and **31. Module: "Input Capture"**.

Adds data sheet clarifications **3. Module: "Pin Diagrams"**, **4. Module: "Pin Diagrams"**, **5. Module: "Pin Diagrams"** and **6. Module: "Electrical Characteristics"**.

Rev J Document (8/2015)

Adds silicon issue **32. Module: "DMA"**.

Adds data sheet clarification **7. Module: "Memory Organization"**.

Rev K Document (10/2015)

Updates silicon issue **32. Module: "SPI"**.

Adds silicon issues **33. Module: "Core"**, **34. Module: "Core"** and **35. Module: "Power-Saving Mode"**.

Adds data sheet clarification **8. Module: "Electrical Characteristics"**.

Rev L Document (5/2016)

Adds silicon issues **36. Module: "SPI"** and **37. Module: "Data Memory"**.

Adds data sheet clarification **9. Module: "Configuration Byte Register Map"**.

Rev M Document (12/2016)

Adds silicon issues **38. Module: "SPI"**, **39. Module: "PTG"** and **40. Module: "PTG"**.

Adds data sheet clarification **10. Module: "Instruction Set Overview"**.

Rev N Document (8/2017)

Updates silicon issues **22. Module: "CPU"** and **25. Module: "CPU"**.

Adds silicon issues **41. Module: "I/O"** and **42. Module: "CPU"**.

Adds data sheet clarification **11. Module: "Electrical Characteristics"**.

Rev P Document (4/2018)

Adds silicon issue **43. Module: "Electrical Characteristics"**.

Adds data sheet clarifications **12. Module: "10-Bit/ 12-Bit Analog-to-Digital Converter (ADC)"**, **13. Module: "PTG Control Registers"**, **14. Module: "LED Control Registers"**, **15. Module: "Special Features"**, **16. Module: "Interrupt Controller Register"**, **17. Module: "Electrical Characteristics"**, **18. Module: "I/O Ports"**, **19. Module: "Quadrature Encoder Interface (QEI) Module"**, **20. Module: "Oscillator Configuration"**, **21. Module: "Memory Organization"**, **22. Module: "Timer1"** and **23. Module: "PWM"**.

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