USB3318

Hi-Speed USB Transceiver with 1.8V-3.3V ULPI Interface - 13MHz Reference Clock

PRODUCT FEATURES

Datasheet

- USB-IF “Hi-Speed” compliant to the Universal Serial Bus Specification Rev 2.0
- Interface compliant with the ULPI Specification revision 1.1 as a Single Data Rate (SDR) PHY
- 1.8V to 3.3V IO Voltage (±10%)
- flexPWR® Technology
  - — Low current design ideal for battery powered applications
  - — “Sleep” mode tri-states all ULPI pins and places the part in a low current state
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep-alive pulse
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Allows host to turn VBUS off to conserve battery power in OTG applications
- Support OTG monitoring of VBUS levels with internal comparators
- “Wrapper-less” design for optimal timing performance and design ease
  - — Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- 13MHz Reference Clock Operation
  - — 0 to 3.6V input drive tolerant
  - — Able to accept “noisy” clock sources
- Internal low jitter PLL for 480MHz Hi-Speed USB operation
- Internal detection of the value of resistance to ground on the ID pin
- Integrated battery to 3.3V LDO regulator
  - — 2.2uF bypass capacitor
  - — 100mV dropout voltage
- Integrated ESD protection circuits
  - — Up to ±15kV without any external devices
- Carkit UART mode for non-USB serial data transfers
- Industrial Operating Temperature -40°C to +85°C
- Packaging Options
  - — 24 pin QFN lead-free RoHS compliant package (4 x 4 x 0.90 mm height)

Applications

The USB3318 is targeted for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

The USB3318 is well suited for:

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles
- POS Terminals

Order Number(s):

USB3318C-CP-TR FOR 24 PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (TAPE AND REEL)

REEL SIZE IS 4000 PIECES.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

0.1 Reference Documents

- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- On-The-Go Supplement to the USB 2.0 Specification, Revision 2.0, May 8, 2009
- 27% Resistor ECN
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- UTMI+ Specification, Revision 1.0, February 2, 2004
- UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, October 20, 2004
- Technical Requirements and Test Methods of Charger and Interface for Mobile Telecommunication Terminal Equipment (Chinese Charger Specification Approval Draft 11/29/2006)

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Chapter 1 General Description

The USB3318 is a highly integrated Hi-Speed USB 2.0 Transceiver (PHY) that supports systems architectures based on a 13MHz reference clock. It is designed to be used in both commercial and industrial temperature applications.

The USB3318 meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) device. In addition to the supporting USB signaling the USB3318 also provides USB UART mode

USB3318 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the Link. The industry standard ULPI interface uses a method of in-band signaling and status byte transfers between the Link and PHY, to facilitate a USB session. By using in-band signaling and status byte transfers the ULPI interface requires only 12 pins.

The USB3318 uses SMSC's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. SMSC's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

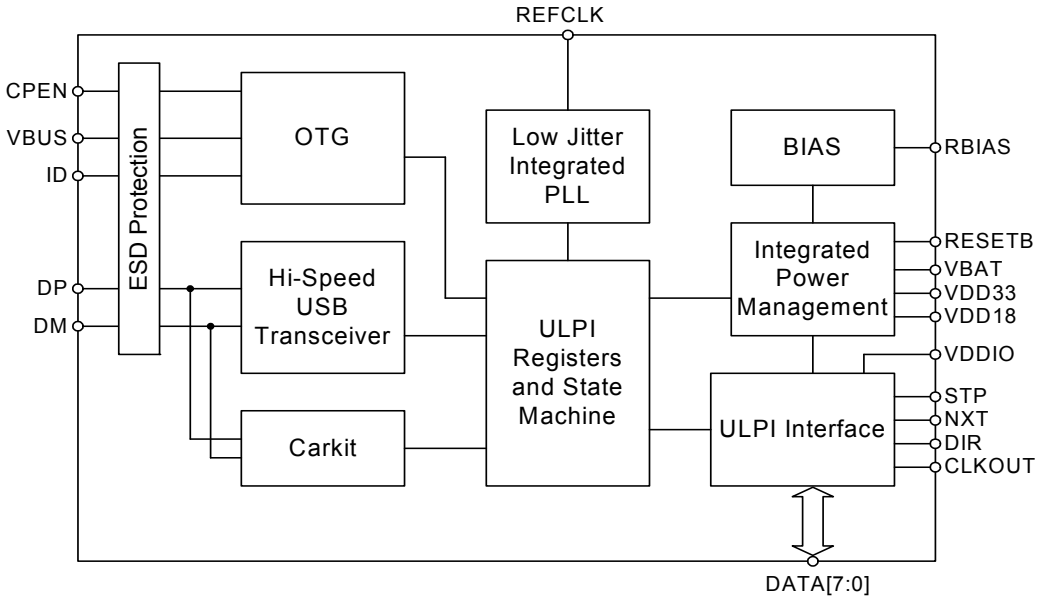

Figure 1.1 USB3318 Block Diagram

The USB3318 is designed to run with a 13MHz reference clock. By using a reference clock from the Link the USB3318 is able to remove the cost of a crystal reference from the design.

The USB3318 includes a integrated 3.3V LDO regulator to generate its own supply from power applied at the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.1 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.1V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. If the user would like to provide a 3.3V supply to the USB3318, the **VBAT** and **VDD33** pins should be connected together as described in Section 5.5.1.

The USB3318 also includes integrated pull-up resistors that can be used for detecting the attachment of a USB Charger. By sensing the attachment to a USB Charger, a product using the USB3318 can charge its battery at more than the 500mA allowed when charging from a USB Host as described in Section 8.2.

Chapter 2 USB3318 Pin Locations and Definitions

2.1 USB3318 Pin Locations and Descriptions

2.1.1 Package Diagram with Pin Locations

The pinout below is viewed from the top of the package.

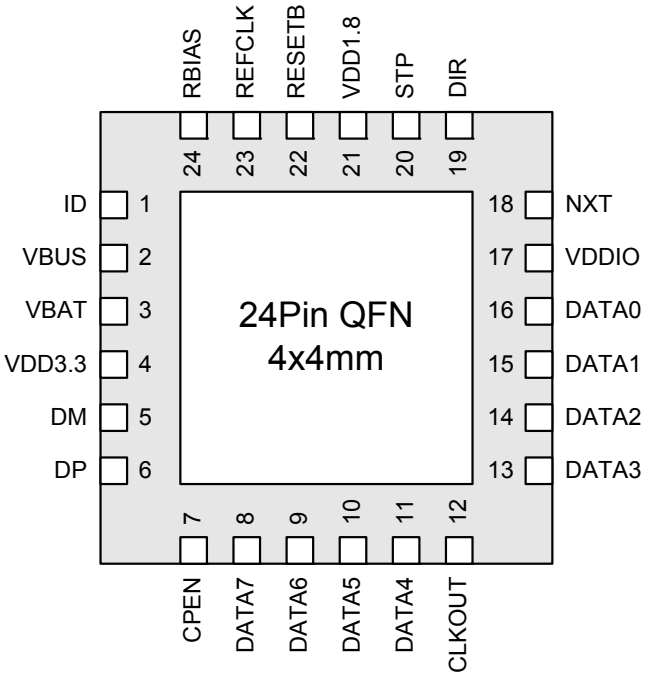

Figure 2.1 USB3318 QFN Pinout - Top View

2.1.2 Pin Definitions

The following table details the pin definitions for the figure above.

Table 2.1 USB3318 Pin Description

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
1	**ID**	Input, Analog	N/A	**ID** pin of the USB cable. For non-OTG applications this pin can be floated. For an A-Device **ID** is grounded. For a B-Device **ID** is floated.
2	**VBUS**	I/O, Analog	N/A	**VBUS** pin of the USB cable. This pin is used for the Vbus comparator inputs and for Vbus pulsing during session request protocol.
3	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.1V.

Table 2.1 USB3318 Pin Description (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
4	**VDD3.3**	Power	N/A	3.3V Regulator Output. A 2.2uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3318.
5	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
6	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
7	**CPEN**	Output, CMOS	High	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The **CPEN** pin is low on POR. This pad uses VDD3.3 logic level.
8	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
9	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
10	**DATA[5**	I/O, CMOS	N/A	ULPI bi-directional data bus.
11	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
12	**CLKOUT**	Output, CMOS	N/A	60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock. Following POR or hardware reset, the voltage at **CLKOUT** must not exceed V_{IH_ED} as provided in Table 4.4.
13	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
14	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
15	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
16	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
17	**VDDIO**	Power	N/A	1.8V to 3.3V ULPI interface supply voltage. This voltage sets the value of V_{OH} for the ULPI interface.
18	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.

Table 2.1 USB3318 Pin Description (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
19	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
20	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
21	**VDD1.8**	Power	N/A	External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3318.
22	**RESETB**	Input, CMOS,	N/A	When low, the part is suspended with all of the I/O tri-stated. When high the USB3318 will operate as a normal ULPI device.
23	**REFCLK**	Input, CMOS	N/A	13MHz Reference Clock input.
24	**RBIAS**	Analog, CMOS	N/A	Rbias pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB3318.
FLAG	**GND**	Ground	N/A	Ground. QFN only: The flag should be connected to the ground plane with a via array under the exposed flag. This is the main ground for the IC.

Chapter 3 Limiting Values

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum **VBUS**, **VBAT**, **ID**, **DP**, **DM**, and **CPEN** voltage to **GND**	V_{MAX_5V}		-0.5		+6.0	V
Maximum **VDD18** voltage to Ground	$V_{MAX\_1.8V}$		-0.5		2.5	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}	**VDD18** = V_{DD18}	-0.5		4.0	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}	**VDD18** = 0V	-0.5		0.7	V
Maximum **VDD33** voltage to Ground	$V_{MAX\_3.3V}$		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	V
QFN Package Junction to Ambient (θ_{JA})		Thermal vias per Layout Guidelines.		58		°C/W
QFN Package Junction to Case (θ_{JC})				11		°C/W
Operating Temperature	T_{MAX_OP}		-40		85	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Table 3.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT to **GND**	V_{VBAT}		3.1		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDDIO to **GND**	V_{DDIO}	**VDDIO** ≥ **VDD18**(min)	1.6	1.8-3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **CPEN**) **CPEN**,	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	V
Ambient Temperature	T_A		-40		85	C

Chapter 4 Electrical Characteristics

The following conditions are assumed unless otherwise specified:

V_{VBAT} = 3.1 to 5.5V; V_{DD18} = 1.6 to 2.0V; V_{DDIO} = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40C to +85C

The current for 3.3V circuits is sourced at the VBAT pin, except when using an external 3.3V supply as shown in Figure 5.4.

4.1 Operating Current

Table 4.1 Electrical Characteristics: Operating Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Mode Current (Default Configuration)	$I_{33AVG(SYNC)}$	Start-up sequence defined in Section 5.5.4 has completed.	5.0	5.5	8.0	mA
	$I_{18AVG(SYNC)}$		17.5	22.0	27.0	mA
	$I_{IOAVG(SYNC)}$		2.5	3.0	4.0	mA
Synchronous Mode Current (HS USB operation)	$I_{33AVG(HS)}$	Active USB Transfer	7.0	10.0	14.0	mA
	$I_{18AVG(HS)}$		23.0	28.0	34.0	mA
	$I_{IOAVG(HS)}$		2.5	3.0	4.0	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{33AVG(FS)}$	Active USB Transfer	5.0	8.5	13.0	mA
	$I_{18AVG(FS)}$		19.0	22.0	27.0	mA
	$I_{IOAVG(FS)}$		2.5	3.0	4.0	mA
Serial Mode Current (FS/LS USB) Note 4.1	$I_{33AVG(FS\_S)}$		5.0	5.5	7.0	mA
	$I_{18AVG(FS\_S)}$		1.5	2.2	3.5	mA
	$I_{IOAVG(FS\_S)}$				0.1	mA
USB UART Current Note 4.1	$I_{33AVG(UART)}$		5.0	5.5	7.0	mA
	$I_{18AVG(UART)}$		1.4	2.1	3.5	mA
	$I_{IOAVG(UART)}$				0.1	mA
Low Power Mode Note 4.2	$I_{DD33(LPM)}$	V_{VBAT} = 4.2V V_{DD18} = 1.8V V_{DDIO} = 1.8V	14.0	20.0	25.0	uA
	$I_{DD18(LPM)}$			0.3	10.0	uA
	$I_{DDIO(LPM)}$				1.5	uA
Standby Mode	$I_{DD33(RSTB)}$	RESETB = 0 V_{VBAT} = 4.2V V_{DD18} = 1.8V V_{DDIO} = 1.8V	14.0	20.0	25.0	uA
	$I_{DD18(RSTB)}$			0.3	10.0	uA
	$I_{DDIO(RSTB)}$				1.5	uA

Note 4.1 *ClockSuspendM* bit = 0.

Note 4.2 SessEnd, VbusVld, and IdFloat comparators disabled. STP Interface protection disabled.

4.2 CLKOUT Specifications

Table 4.2 Electrical Characteristics: CLKOUT Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suspend Recovery Time Note 4.3	T_{START}			2.07	3.32	ms
CLKOUT Duty Cycle	DC_{CLKOUT}		45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note 4.3 The USB3318 uses the *AutoResume* feature, Section 5.4, to allow a host start-up time of less than 1ms

4.3 ULPI Interface Timing

Table 4.3 ULPI Interface Timing

PARAMETER	SYMBOL	MIN	MAX	UNITS
Setup time (STP, data in)	T_{SC}, T_{SD}	5.0		nS
Hold time (STP, data in)	T_{HC}, T_{HD}	0.0		nS
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	1.5	3.5	nS

Note: V_{DDIO} = 1.6 to 3.6V; V_{SS} = 0V; T_A = -40C to 85C; C_{Load} = 10pF

4.4 Digital IO Pins

Table 4.4 Digital IO Characteristics: RESETB, CLKOUT, STP, DIR, NXT, DATA[7:0] and XI Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.4 * V_{DDIO}	V
High-Level Input Voltage	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage REFCLK only	V_{IH}		0.68 * V_{DD18}		V_{DD33}	V
Clock High REFCLK only	T_{HIGH}		0.3 * T_P	0.5 * T_P	0.7 * T_P	
Clock Low REFCLK only	T_{LOW}		0.3 * T_P	0.5 * T_P	0.7 * T_P	
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	V_{DDIO}- 0.4			V
High-Level Output Voltage **CPEN** Only	V_{OH}	I_{OH} = -8mA	V_{DD33} - 0.4			V
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF

Table 4.4 Digital IO Characteristics: RESETB, CLKOUT, STP, DIR, NXT, DATA[7:0] and XI Pins (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STP pull-up resistance	R_{STP}	InterfaceProtectDisable = 0	51	60	65	kΩ
DATA[7:0] pull-dn resistance	R_{DATA_PD}	ULPI Synchronous Mode	55	67	79	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

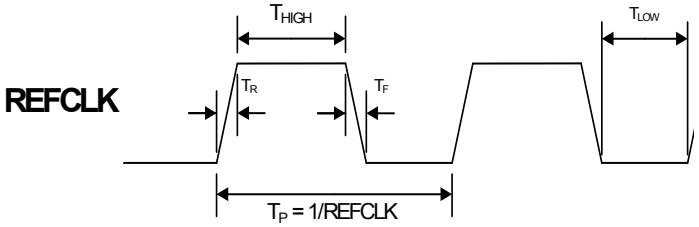

Figure 4.1 External Reference Clock

4.5 DC Characteristics: Analog I/O Pins

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4.5			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4.5	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4.5 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4.4	0.900	1.24	1.575	kΩ

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4.4	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 4.4	14.25	16.9	20	kΩ
Weak Pull-up Resistor Impedance	R_{CD}	Configured by bits 4 and 5 in USB IO & Power Management register.	128	170	212	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
High-Speed Squelch Detection Threshold (Differential Signal Amplitude)	V_{HSSQ}	Note 4.6	100		150	mV
Output Levels						
Hi-Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
Hi-Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
Hi-Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 4.4 The resistor value follows the 27% Resistor ECN published by the USB-IF.

Note 4.5 The values shown are valid when the *USB RegOutput* bits in the USB IO & Power Management register are set to the default value.

Note 4.6 An automatic waiver up to 200mV is granted to accommodate system-level elements such as measurement/test fixtures, captive cables, EMI components, and ESD suppression.

4.6 Dynamic Characteristics: Analog I/O Pins

Table 4.6 Dynamic Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
Hi-Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

4.7 OTG Electrical Characteristics

Table 4.7 OTG Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VbusVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
A-Device Impedance	R_{IdGnd}	Maximum A device Impedance to ground on **ID** pin			100	kΩ
ID Float trip point	$V_{IdFloat}$		1.9	2.2	2.5	V
Vbus Pull-Up	R_{VPU}	**VBUS** to **VDD33** (*ChargeVbus* = 1)	281	340	450	Ω

Table 4.7 OTG Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Vbus Pull-down	R_{VPD}	**VBUS** to **GND** (*DisChargeVbus* = 1)	656	850	1100	Ω
Vbus Impedance	R_{VB}	**VBUS** to **GND**	40	75	100	kΩ
ID pull-up resistance	R_{ID}	*IdPullup* = 1	80	100	120	kΩ
ID weak pull-up resistance	R_{IDW}	*IdPullup* = 0	1			MΩ
ID pull-dn resistance	R_{IDPD}	*IdGndDrv* = 1			1000	Ω

4.8 Regulator Output Voltages and Capacitor Requirement

Table 4.8 Regulator Output Voltages and Capacitor Requirement

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Output Voltage	V_{DD33}	6V > VBAT > 3.1V	3.0	3.3	3.6	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 01 6V > VBAT > 3.1V	2.7	3.0	3.3	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 10 6V > VBAT > 3.1V	2.47	2.75	3.03	V
Regulator Output Voltage	V_{DD33}	USB UART Mode & *UART RegOutput[1:0]* = 11 6V > VBAT > 3.1V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{BYP}		2.2			uF
Bypass Capacitor ESR	C_{ESR}				1	Ω

Table 4.9 ESD and LATCH-UP Performance

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	COMMENTS
ESD PERFORMANCE						
Note 4.7	Human Body Model			±8	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±8	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±15	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

Note 4.7 **REFCLK** pin ±5kV Human Body Model.

Chapter 5 Architecture Overview

The USB3318 consists of the blocks shown in the diagram below. All pull-up resistors shown in Figure 5.1 are connected to VDD33.

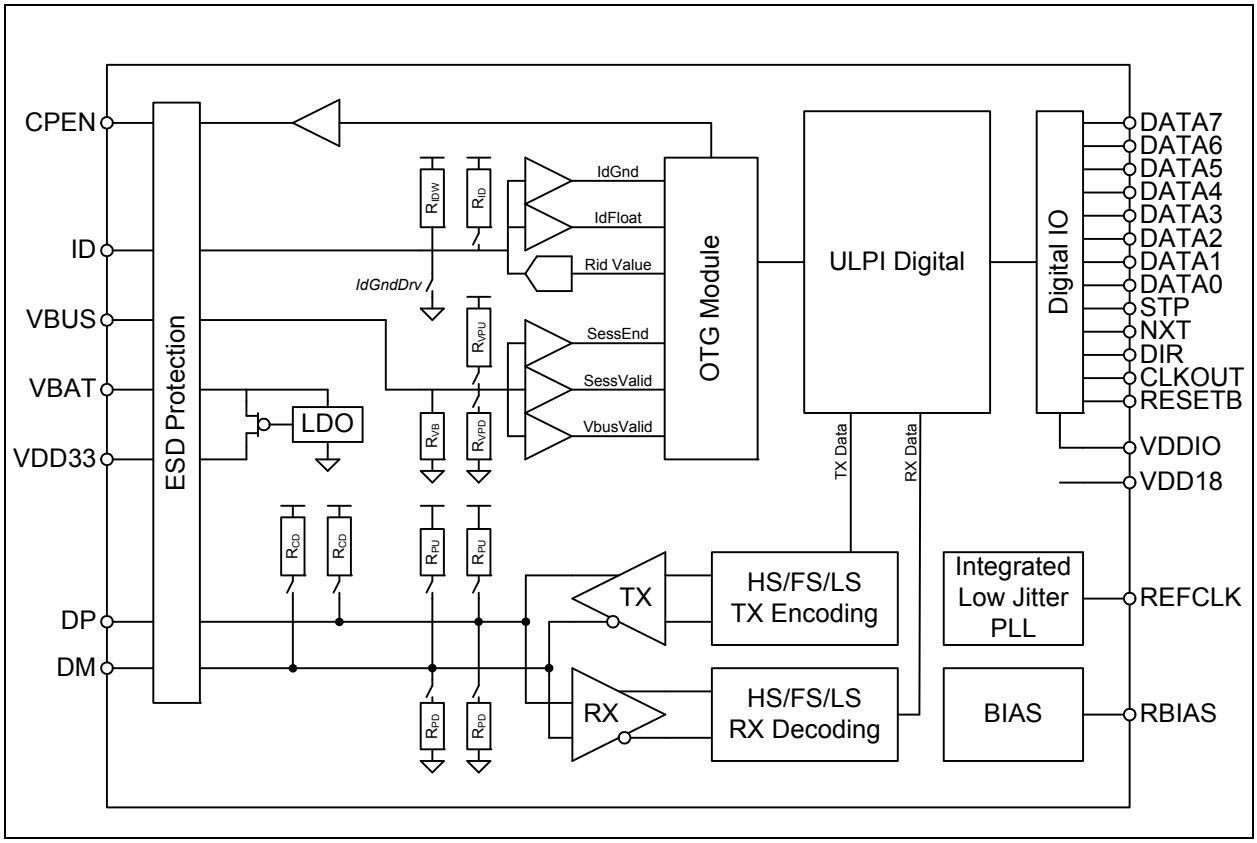

Figure 5.1 USB3318 System Diagram

5.1 ULPI Digital Operation and Interface

This section of the USB3318 is covered in detail in Chapter 6, ULPI Operation Overview.

5.2 Interface to DP/DM

The blocks in the lower left-hand corner of Figure 5.1 interface to the DP/DM pins.

5.2.1 USB Transceiver

The USB3318 transceiver includes the receivers and transmitters required to be compliant to the Universal Serial Bus Specification Rev 2.0. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The RX block consists of separate differential receivers for HS and FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the TX Logic block is encoded, bit stuffed, serialized and transmitted onto the USB cable by the TX block. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3318 TX block meets the HS signalling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector have very little loss. In some systems, it may be desirable to compensate for loss by adjusting the HS transmitter amplitude. The *Boost* bits in the HS TX Boost register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins.

5.2.2 Termination Resistors

The USB3318 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the PHY when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration. The possible valid resistor combinations are shown in Table 5.1, and operation is guaranteed in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5.1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

The USB3318 also includes two 125kΩ **DP** and **DM** pull-up resistors described in Section 5.8.

Table 5.1 DP/DM Termination vs. Signaling Mode

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3318 TERMINATION RESISTOR SETTINGS				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or Vbus < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b

Table 5.1 DP/DM Termination vs. Signaling Mode (continued)

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3318 TERMINATION RESISTOR SETTINGS				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
Host low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Any combination not defined above Note 5.1						0b	0b	0b	0b	0b

Note: This is the same as Table 40, Section 4.4 of the ULPI 1.1 specification.

Note: USB3318 does not support operation as an upstream hub port. See Section 6.2.4.3.

Note 5.1 The transceiver operation is not guaranteed in a combination that is not defined.

The USB3318 uses the 27% resistor ECN resistor tolerances. The resistor values are shown in Table 4.5.

5.3 Bias Generator

This block consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. This resistor should be placed as close as possible to the USB3318 to minimize the trace length. The nominal voltage at **RBIAS** is 0.8V and therefore the resistor will dissipate approximately 80μW of power.

5.4 Integrated Low Jitter PLL

The USB3318 uses an integrated low jitter phase locked loop (PLL) to provide a clean 480MHz clock. This clock is used by the PHY during both transmit and receive. The USB3318 requires a 13MHz reference clock to be driven on the **REFCLK** pin.

After the PLL has locked to the correct frequency, the USB3318 will de-assert **DIR** and the Link can begin using the ULPI interface. The USB3318 is guaranteed to start the clock within the time specified in Table 4.2. For Host applications, the ULPI *AutoResume* bit should be enabled. This is described in Section 6.2.4.4.

The system must not drive voltage on the CLKOUT pin following POR or hardware reset that exceeds the value of V_{IH_ED} provided in Table 4.4.

5.4.1 Reference Clock Requirements

The reference clock is connected to the REFCLK pins as shown in the application diagram, Figure 8.1. The REFCLK pin is designed to be driven with a square wave from 0V to V_{DDIO}, but can be driven with a square wave from 0V to as high as 3.6V.

When using an external reference clock, the USB3318 only uses the positive edge of the clock. The signal must comply with the V_{IH} and V_{IL} parameters provided in Table 4.4. It may be possible to AC couple the reference clock to change the common-mode voltage level when it is sourced by a device that does not comply with the V_{IH} and V_{IL} parameters. A DC bias network must be provided at the REFCLK pin when the reference clock is AC coupled. The component values provided in Figure 5.2 are for example only. The actual values should be selected to satisfy system requirements.

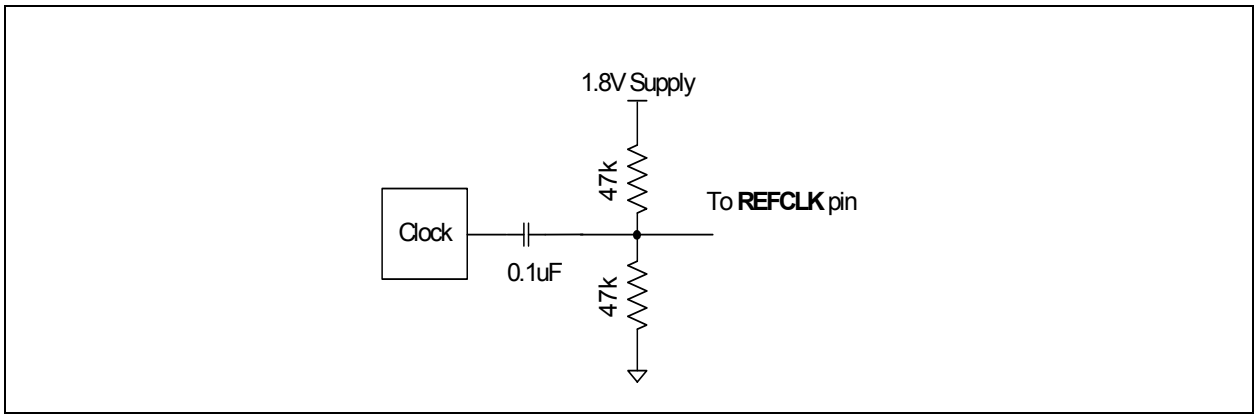

Figure 5.2 Example of circuit used to shift a reference clock common-mode voltage level.

The USB3318 is tolerant to jitter on the reference clock. The REFCLK jitter should be limited to a peak to peak jitter of less than 1nS over a 10uS time interval. If this level of jitter is exceeded the USB3318 high speed eye diagram may be degraded.

The edges of the reference clock do not need to be aligned in any way to the ULPI interface signals. The reference clock is used by a PLL to generate the 60MHz CLKOUT for the ULPI digital. There is no need to align the phase of the REFCLK and the 60MHz CLKOUT.

The REFCLK should be enabled when the RESETB pin is brought high. The ULPI interface will start running after the time specified in Table 4.2. If the REFCLK enable is delayed relative to the RESETB pin, the ULPI interface will start operation delayed by the same amount. The REFCLK can be run at anytime the RESETB pin is low without causing the USB3318 to start-up or draw current.

When the USB3318 is placed in Low Power Mode or carkit mode the REFCLK can be stopped after the final ULPI register write is complete. The STP pin is asserted to bring the USB3318 out of Low Power Mode. The REFCLK should be started at the same time STP is asserted to minimize the USB3318 start-up time.

If the REFCLK is stopped while CLKOUT is running the PLL will come out of lock and the frequency of the CLKOUT signal will decrease to the minimum allowed by the PLL design. If the REFCLK is stopped during a USB session the session may drop.

5.5 Internal Regulators and POR

The USB3318 includes integrated power management functions, including a Low-Dropout regulator that can be used to generate the 3.3V USB supply, and a POR generator.

5.5.1 Integrated Low Dropout Regulator

The USB3318 has an integrated linear regulator. Power sourced at the **VBAT** pin is regulated to 3.3V and the regulator output is on the **VDD33** pin. To ensure stability, the regulator requires an external bypass capacitor as specified in Table 4.8 placed as close to the pin as possible.

The USB3318 regulator is designed to generate a 3.3 volt supply for the USB3318 only. Using the regulator to provide current for other circuits is not recommended and SMSC does not guarantee USB performance or regulator stability.

During USB UART mode the regulator output voltage can be changed to allow the USB3318 to work with UARTs operating at different operating voltages. The regulator output voltage is controlled by the *UART RegOutput[1:0]* bits described in Section 7.1.4.4 and Table 4.8.

The USB3318 regulator can be powered in the three methods as shown below.

For USB Peripheral, Host, and OTG operations the regulator can be connected as shown in Figure 5.3 or Figure 5.4 below. For OTG operation, the **VDD33** supply on the USB3318 must be powered to detect devices attaching to the USB connector and detect a SRP during an OTG session. When using a battery to supply the USB3318 the battery voltage must be within the range of 3.1V to 5.5V

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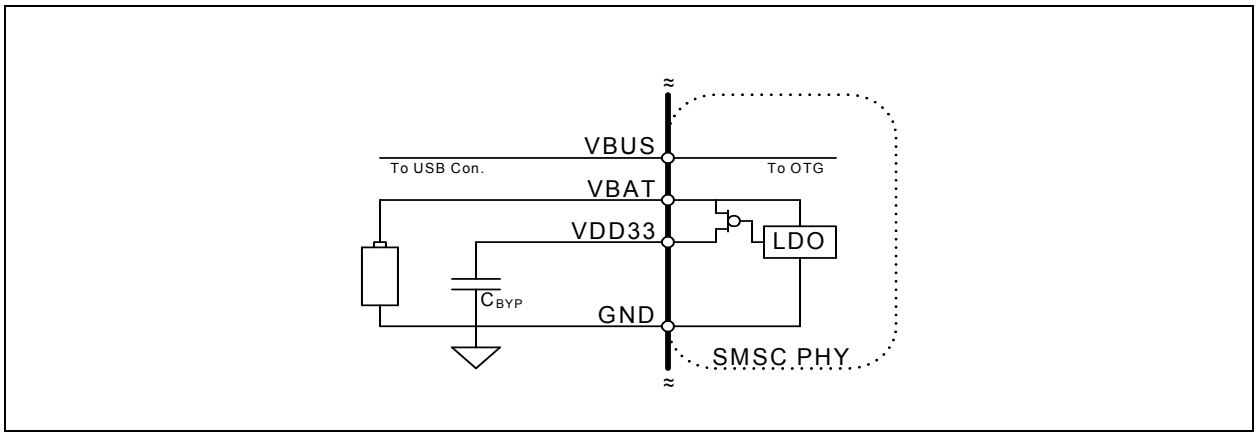


Figure 5.3 Powering the USB3318 from a Battery

The USB3318 can be powered from an external 3.3V supply as shown in Figure 5.4. When using the external supply both the **VBAT** and **VDD33** pins are connected together. The bypass capacitor should be included when using the external supply.

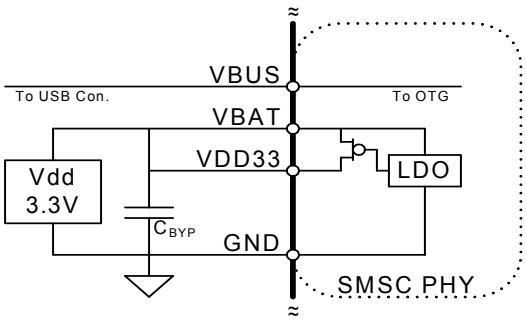


Figure 5.4 Powering the USB3318 from a 3.3V Supply

For peripheral only or host only operation the regulator can be connected as shown in Figure 5.5. This connection of the regulator requires the Vbus supply to be present any time the USB operation is desired. When a Vbus voltage is not present, the USB3318 cannot detect OTG or Carkit signaling.

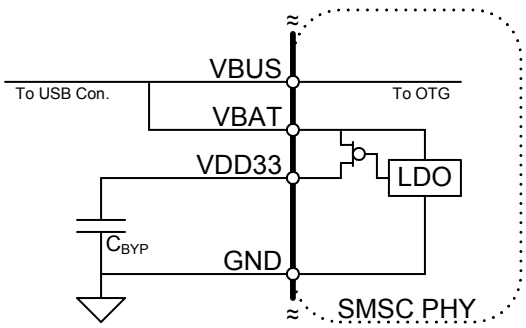


Figure 5.5 Powering the USB3318 from the USB Cable Vbus

When using the USB3318 connected as shown in Figure 5.5, the ULPI interface will operate when Vbus is removed. When Vbus is removed the USB3318 should be placed into Low Power Mode until Vbus is detected through an interrupt. While the USB3318 is in Low Power Mode the status of **VBUS**, **ID**, **DP**, and **DM** can be monitored while drawing a minimum amount of current from the **VDD18** supply as described in Section 6.2.6.4.

5.5.2 Power On Reset (POR)

The USB3318 provides an internal POR circuit that generates a reset pulse after the **VDD18** supply is stable. After the internal POR goes high and the **RESETB** pin is high, the USB3318 will release from reset and begin normal ULPI operation. Provided that REFCLK is present when the **RESETB** pin is brought high, the ULPI bus will be available in the time defined as T_{START} as given in Table 4.2.

The ULPI registers will power up in their default state summarized in Table 7.1 when the 1.8V supply is brought up. Cycling the 1.8 volt power supply will reset the ULPI registers to their default states. The **RESETB** pin can also be used to reset the ULPI registers to their default state (and reset all internal state machines) by bringing the pin low for a minimum of 1 microsecond and then high.

The Link is not required to assert the **RESETB** pin. A pull-down resistor is not present on the **RESETB** pin and therefore the Link must drive the **RESETB** pin to the desired state at all times (including system start-up) or connect the **RESETB** pin to **VDDIO.**

5.5.3 Recommended Power Supply Sequence

For USB operation the USB3318 requires the **VBAT**, **VDD33**, **VDD18**, and **VDDIO** supples. The **VDDIO** supply should be powered up at the same time or after the **VDD18** supply is turned on and stable.

When the **VBAT** supply is applied the integrated regulator will automatically start-up and regulate **VBAT** to **VDD33**. If the **VDD33** supply is powered and the **VDD18** supply is not powered, the 3.3V circuits are powered off and the **VDD33** current will be limited to 20uA.

The ULPI interface will start operating after the **VDD18** and **VDDIO** supplies are applied and the **RESETB** pin is brought high. The **RESETB** pin must be held low until the VDD18 supply is stable. If the Link is not ready to interface the USB3318 the Link may choose to hold the **RESETB** pin low until it is ready to control the ULPI interface.

Table 5.2 Operating Mode vs. Power Supply Configuration

VDD33 (Note 5.2)	VDD18	RESETB	OPERATING MODES AVAILABLE
0	0	0	Powered Off
0	1	0	Standby Mode. VDD18 Current <1uA
0	1	1	All operating modes described in Chapter 6. Note: The USB3318 will only allow ULPI register access in this configuration.
1	1	1	Full USB operation as described in Chapter 6.
1	0	X	In this mode the ULPI interface is not active and the circuits powered from the **VDD33** are turned off and the current will be limited to 20uA.

Note 5.2 Anytime **VBAT** is powered the **VDD33** pin will be powered up. This column assumes the **VBAT** pin is powered as described above.

5.5.4 Start-Up

The power on default state of the USB3318 is ULPI Synchronous mode. The USB3318 requires the following conditions to begin operation: the power supplies must be stable, the **REFCLK** must be present and the **RESETB** pin must be high. After these conditions are met, the USB3318 will begin ULPI operation that is described in Section 6.1.

Figure 5.6 below shows a timing diagram to illustrate the start-up of the USB3318. At T0, the supplies are stable and the USB3318 is held in reset mode. At T1, the Link drives **RESETB** high after the **REFCLK** has started. The **RESETB** pin may be brought high asynchronously to **REFCLK**. At this point the USB3318 will drive idle on the data bus and assert **DIR** until the internal PLL has locked. After the PLL has locked, the USB3318 will check that the Link has de-asserted **STP** and at T2 it will de-assert **DIR** and begin ULPI operation.

The ULPI bus will be available as shown in Figure 5.6 in the time defined as T_{START} given in Table 4.2. If the **REFCLK** signal starts after the **RESETB** pin is brought high, then time T0 will begin when **REFCLK** starts. T_{START} also assumes that the Link has de-asserted **STP**. If the Link has held **STP** high the USB3318 will hold **DIR** high until **STP** is de-asserted. When the LINK de-asserts STP, it must drive a ULPI IDLE one cycle after **DIR** de-asserts.

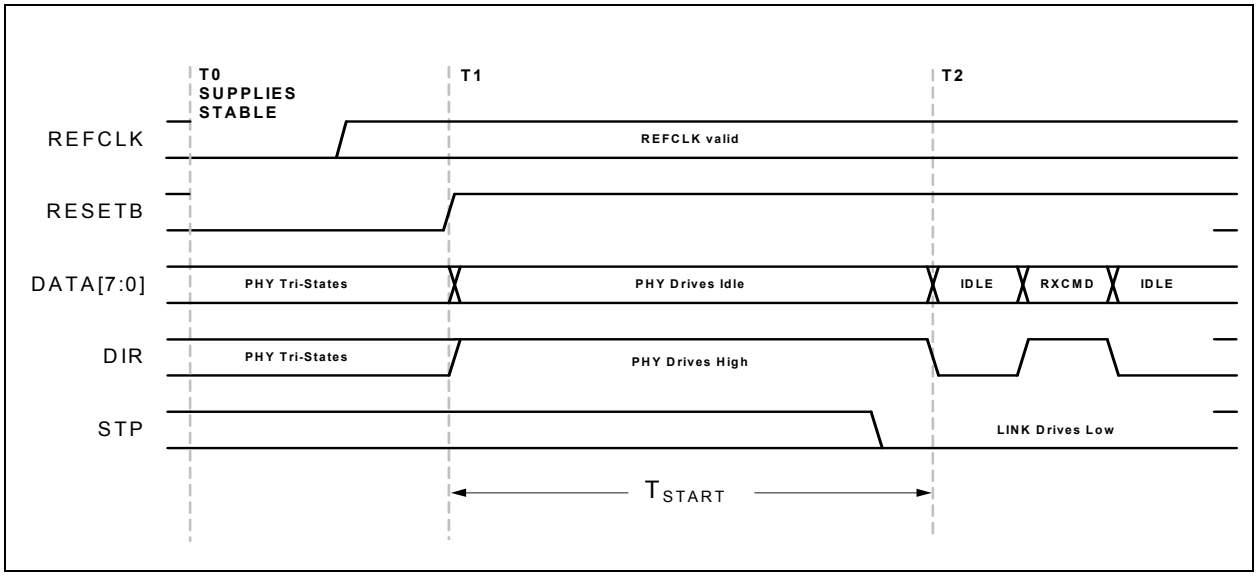


Figure 5.6 ULPI Start-up Timing

5.6 USB On-The-Go (OTG)

The USB3318 provides full support for USB OTG protocol. OTG allows the USB3318 to be dynamically configured as a host or device depending on the type of cable inserted into the Micro-AB receptacle. When the Micro-A plug of a cable is inserted into the Micro-AB receptacle, the USB device becomes the A-device. When a Micro-B plug is inserted, the device becomes the B-device. The OTG A-device behaves similar to a Host while the B-device behaves similar to a peripheral. The differences are covered in the OTG the “On-The-Go Supplement to the USB 2.0 Specification”. In applications where only Host or Device is required, the OTG Module is unused.

The OTG Module is described in the following sections.

5.6.1 ID Resistor Detection

The ID pin of the USB connector is monitored by the **ID** pin of the USB3318 to detect the attachment of different types of USB devices and cables. The block diagram of the ID detection circuitry is shown in Figure 5.7 and the related parameters are given in Table 4.7.

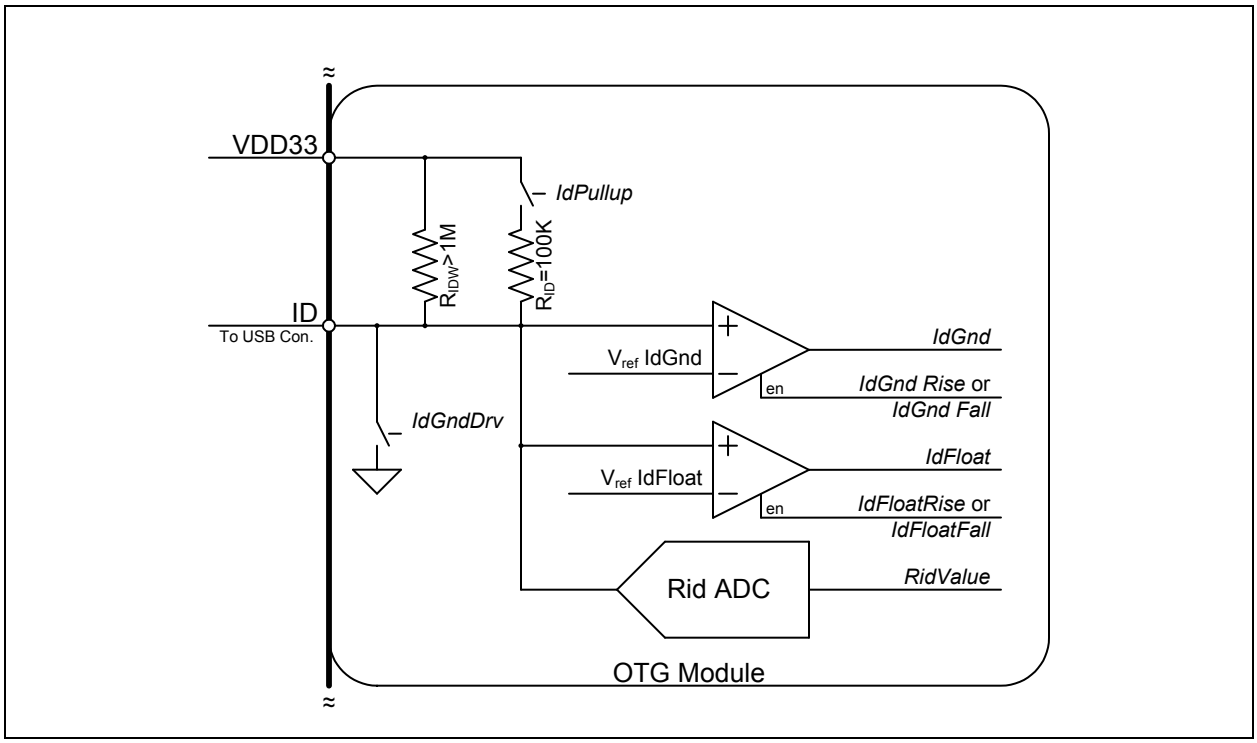


Figure 5.7 USB3318 ID Resistor Detection Circuitry

5.6.1.1 USB OTG Operation

The USB3318 can detect **ID** grounded and **ID** floating to determine if an A or B cable has been inserted. The A plug will ground the **ID** pin while the B plug will float the **ID** pin. These are the only two valid states allowed in the OTG Protocol.

To monitor the status of the **ID** pin, the Link activates the *idPullup* bit in the OTG Control register, waits 50mS and then reads the status of the *IdGnd* bit in the USB Interrupt Status register. If an A cable has been inserted the *IdGnd* bit will read 0. If a B cable is inserted, the **ID** pin is floating and the *IdGnd* bit will read 1.

The USB3318 provides an integrated weak pull-up resistor on the **ID** pin, R_{IDW}. This resistor is present to keep the **ID** pin in a known state when the *IdPullup* bit is disabled and the **ID** pin is floated. In addition to keeping the **ID** pin in a known state, it enables the USB3318 to generate an interrupt to inform the link when a cable with a resistor to ground has been attached to the **ID** pin. The weak pull-up is small enough that the largest valid Rid resistor pulls the **ID** pin low and causes the IdGnd comparator to go low.

After the link has detected an **ID** pin state change, the RID converter can be used to determine the resistor value as described in Section 5.6.1.2.

5.6.1.2 Measuring ID Resistance to Ground

The Link can used the integrated resistance measurement capabilities to determine the value of an ID resistance to ground. The following table details the valid values of resistance to ground that the USB3318 can detect.

Table 5.3 Valid Values of ID Resistance to Ground

ID RESISTANCE TO GROUND	RID VALUE
Ground	000
75Ω +/-1%	001
102kΩ +/-1%	010
200kΩ+/-1%	011
440kΩ +/-1%	100
Floating	101

Note: IdPullUp = 0

The Rid resistance can be read while the USB3318 is in Synchronous Mode. When a resistor to ground is attached to the **ID** pin, the state of the IdGnd comparator will change. After the Link has detected **ID** transition to ground, it can use the methods described in Section 6.5 to operate the Rid converter.

5.6.1.3 Using IdFloat Comparator (not recommended)

Note: The ULPI specification details a method to detect a 102kΩ resistance to ground using the IdFloat comparator. This method can only detect 0ohms, 102kΩ, and floating terminations of the **ID** pin. Due to this limitation it is recommended to use the RID Converter as described in Section 5.6.1.2.

The **ID** pin can be either grounded, floated, or connected to ground with a 102kΩ external resistor. To detect the 102K resistor, set the *idPullup* bit in the OTG Control register, causing the USB3318 to apply the 100K internal pull-up connected between the **ID** pin and VDD33. Set the *idFloatRise* and *idFloatFall* bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers to enable the IdFloat comparator to generate an RXCMD to the Link when the state of the IdFloat changes. As described in Figure 6.3, the alt_int bit of the RXCMD will be set. The values of IdGnd and IdFloat are shown for the three types cables that can attach to the USB Connector in Table 5.4.

Table 5.4 IdGnd and IdFloat vs. ID Resistance to Ground

ID RESISTANCE	IDGND	IDFLOAT
Float	0	1
102K	1	0
GND	1	0

Note: The ULPI register bits *IdPullUp*, *IdFloatRise,* and *IdFloatFall* should be enabled.

To save current when an A Plug is inserted, the internal 102kΩ pull-up resistor can be disabled by clearing the *IdPullUp* bit in the OTG Control register and the *IdFloatRise* and *IdFloatFall* bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. If the cable is removed the weak R_{IDW} will pull the **ID** pin high.

The *IdGnd* value can be read using the ULPI USB Interrupt Status register, bit 4. In host mode, it can be set to generate an interrupt when *IdGnd* changes by setting the appropriate bits in the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. The *IdFloat* value can be read by reading the ULPI Carkit Interrupt Status register bit 0.

Note: The IdGnd switch has been provided to ground the **ID** pin for future applications.

5.6.2 VBUS Monitor and Pulsing

The USB3318 includes all of the Vbus comparators required for OTG. The VbusVld, SessVld, and SessEnd comparators shown in Figure 5.8 are fully integrated into the USB3318. These comparators are used to monitor changes in the Vbus voltage, and the state of each comparator can be read from the USB Interrupt Status register.

The VbusVld comparator is used by the Link, when configured as an A device, to ensure that the Vbus voltage on the cable is valid. The SessVld comparator is used by the Link when configured as both an A or B device to indicate a session is requested or valid. Finally the SessEnd comparator is used by the B-device to indicate a USB session has ended.

Also included in the VBUS Monitor and Pulsing block are the resistors used for Vbus pulsing in SRP. The resistors used for VBUS pulsing include a pull-down to ground and a pull-up to VDD33 as shown in Figure 5.8.

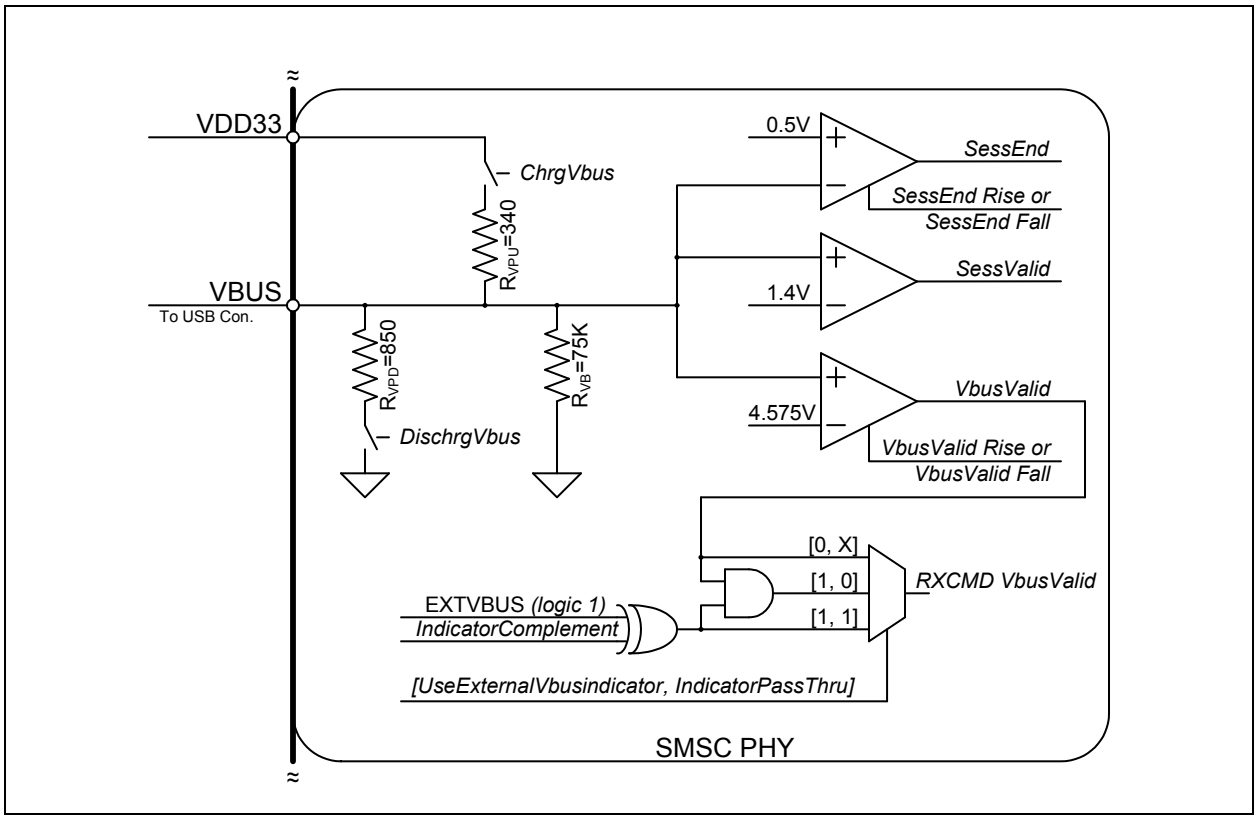


Figure 5.8 USB3318 OTG Vbus Block

5.6.2.1 SessEnd Comparator

The SessEnd comparator is designed to trip when Vbus is less than 0.5 volts. When Vbus goes below 0.5 volts the USB session is considered to be ended, and SessEnd will transition from 0 to 1. The SessEnd comparator can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When disabled, the SessEnd bit in the USB Interrupt Status register will read 0. The SessEnd comparator trip points are detailed in Table 4.7.

5.6.2.2 SessVld Comparator

The SessVld comparator is used when the PHY is configured as both an A and B device. When configured as an A device, the SessVld is used to detect Session Request protocol (SRP). When configured as a B device, SessVld is used to detect the presence of Vbus. The SessVld interrupts can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When the interrupts are disabled, the SessVld comparator is not disabled and its state can be read in the USB Interrupt Status register. The SessVld comparator trip point is detailed in Table 4.7.

Note: The OTG Supplement specifies a voltage range for A-Device Session Valid and B-Device Session Valid comparator. The USB3318 PHY combines the two comparators into one and uses the narrower threshold range.

5.6.2.3 VbusVld Comparator

The final Vbus comparator is the VbusVld comparator. This comparator is only used when the USB3318 is configured as an A-device. In the USB protocol the A-device supplies the VBUS voltage and is responsible to ensure it remains within a specified voltage range. The VbusVld comparator can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When disabled, bit 1 of the USB Interrupt Status register will return a 0. The VbusVld comparator trip points are detailed in Table 4.7.

The internal VbusValid comparator is designed to ensure the Vbus voltage remains above 4.4V.

The USB3318 includes the external vbus valid indicator logic as detail in the ULPI Specification. The external vbus valid indicator is tied to a logic one. The decoding of this logic is shown in Table 5.5 below. By default this logic is disabled.

Table 5.5 External Vbus Indicator Logic

TYPICAL APPLICATION	USE EXTERNAL VBUS INDICATOR	INDICATOR PASS THRU	INDICATOR COMPLEMENT	RXCMD VBUS VALID ENCODING SOURCE
OTG Device	0	X	X	Internal VbusVld comparator (Default)
	1	1	0	Fixed 1
	1	1	1	Fixed 0
	1	0	0	Internal VbusVld comparator.
	1	0	1	Fixed 0
Standard Host	1	1	0	Fixed 1
	1	1	1	Fixed 0
Standard Peripheral	0	X	X	Internal VbusVld comparator. This information should not be used by the Link. (Note 5.3)

Note 5.3 A peripheral should not use VbusVld to begin operation. The peripheral should use SessVld because the internal VbusVld threshold can be above the Vbus voltage required for USB peripheral operation.

5.6.2.4 Vbus Pulsing with Pull-up and Pull-down Resistors

In addition to the internal Vbus comparators, the USB3318 also includes the integrated Vbus pull-up and pull-down resistors used for Vbus Pulsing. To discharge the Vbus voltage so that a Session Request can begin, the USB3318 provides a pull-down resistor from Vbus to Ground. This resistor is controlled by the *DischargeVbus* bit 3 of the OTG Control register. The pull-up resistor is connected between Vbus and VDD33. This resistor is used to pull Vbus above 2.1 volts so that the A-Device knows that a USB session has been requested. The state of the pull-up resistor is controlled by the bit 4 *ChargeVbus* of the OTG Control register. The Pull-Up and Pull-Down resistor values are detailed in Table 4.7.

5.6.2.5 Vbus Input Impedance

The OTG Supplement requires an A-Device that supports Session Request Protocol to have a VBUS input impedance less than 100kΩ and greater the 40kΩ to ground. The USB3318 provides a 75kΩ resistance to ground, R_{VB}. The R_{VB} resistor tolerance is detailed in Table 4.7.

5.6.3 Driving External Vbus

A system that is operating as a host is required to source 5 volts on VBUS. The USB3318 fully supports VBUS power control using external devices. The USB3318 provides an active high control signal, **CPEN**, which is dedicated to controlling the Vbus supply when configured as an A-Device.

CPEN is asserted by setting the *DrvVbus* or *DrvVbusExternal* bit of the OTG Control register. To be compatible with Link designs that support both internal and external Vbus supplies the *DrvVbus* and *DrvVbusExternal* bits in the OTG Control Register are or'd together. This enables the Link to set either bit to access the external Vbus enable (**CPEN**.) This logic is shown in Figure 5.9. *DrvVbus* and *DrvVbusExternal* are set to 0 on POR.

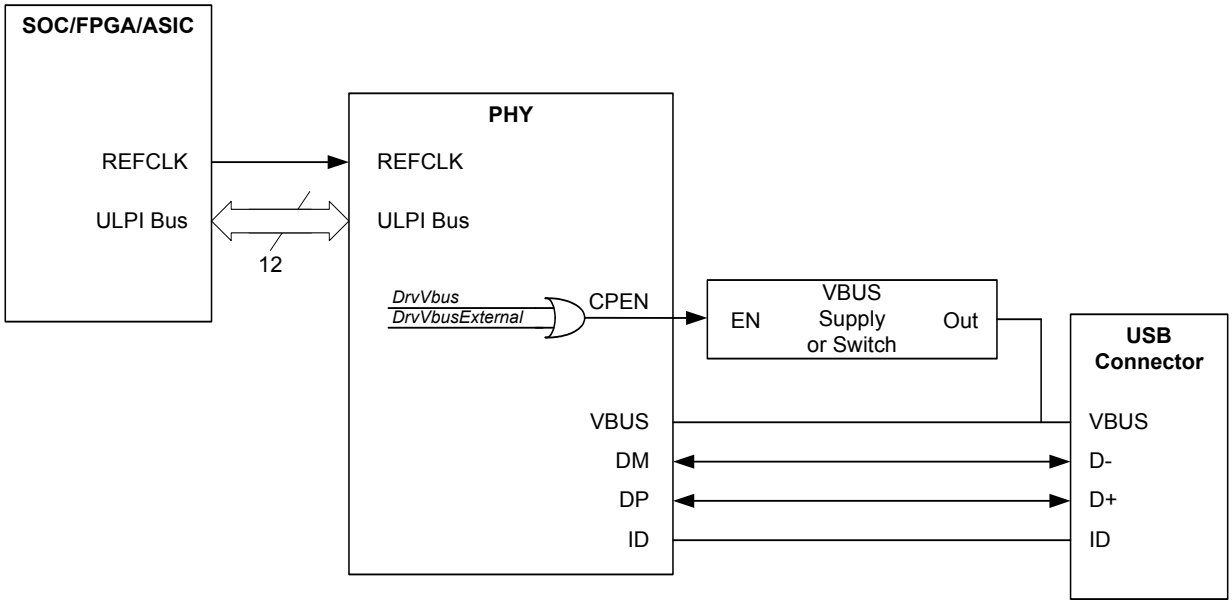


Figure 5.9 USB3318 Drives External Vbus Supply or Switch

5.7 USB UART Support

The USB3318 provides support for the USB UART interface as detailed in the ULPI specification and the CEA-936A specification. The USB3318 can be placed in UART Mode using the method described in Section 6.4, and the regulator output will automatically switch to the value configured by the *UART RegOutput* bits in the USB IO & Power Management register. While in UART mode, the Linestate signals cannot be monitored on the DATA[0] and DATA[1] pins.

5.8 USB Charger Detection Support

To support the detection and identification of different types of USB chargers the USB3318 provides integrated pull-up resistors, R_{CD}, on both DP and DM. These pull-up resistors along with the single ended receivers can be used to help determine the type of USB charger attached. Reference information on implementing charger detection is provided in Section 8.2.

Table 5.6 USB Weak Pull-up Enable

RESETB	DP PULLUP ENABLE	DM PULLUP ENABLE
0	0	0
1	*ChargerPullupEnableDP*	*ChargerPullupEnableDM*

Note: *ChargerPullupEnableDP* and *ChargerPullupEnableDM* are enabled in the USB IO & Power Management register.

Chapter 6 ULPI Operation Overview

The USB3318 uses the industry standard ULPI digital interface to facilitate communication between the PHY and Link (device controller). The ULPI interface is designed to reduce the number of pins required to connect a discrete USB PHY to an ASIC or digital controller. For example, a full UTMI+ Level 3 OTG interface requires 54 signals while a ULPI interface requires only 12 signals.

The ULPI interface is documented completely in the "UTMI+ Low Pin Interface (ULPI) Specification Revision 1.1" (www.ulpi.org). The following sections highlight the key operating modes of the USB3318 digital interface.

6.1 Overview

Figure 6.1 illustrates the block diagram of the ULPI digital functions. It should be noted that this USB3318 does not use a "ULPI wrapper" around a UTMI+ PHY core as the ULPI specification implies.

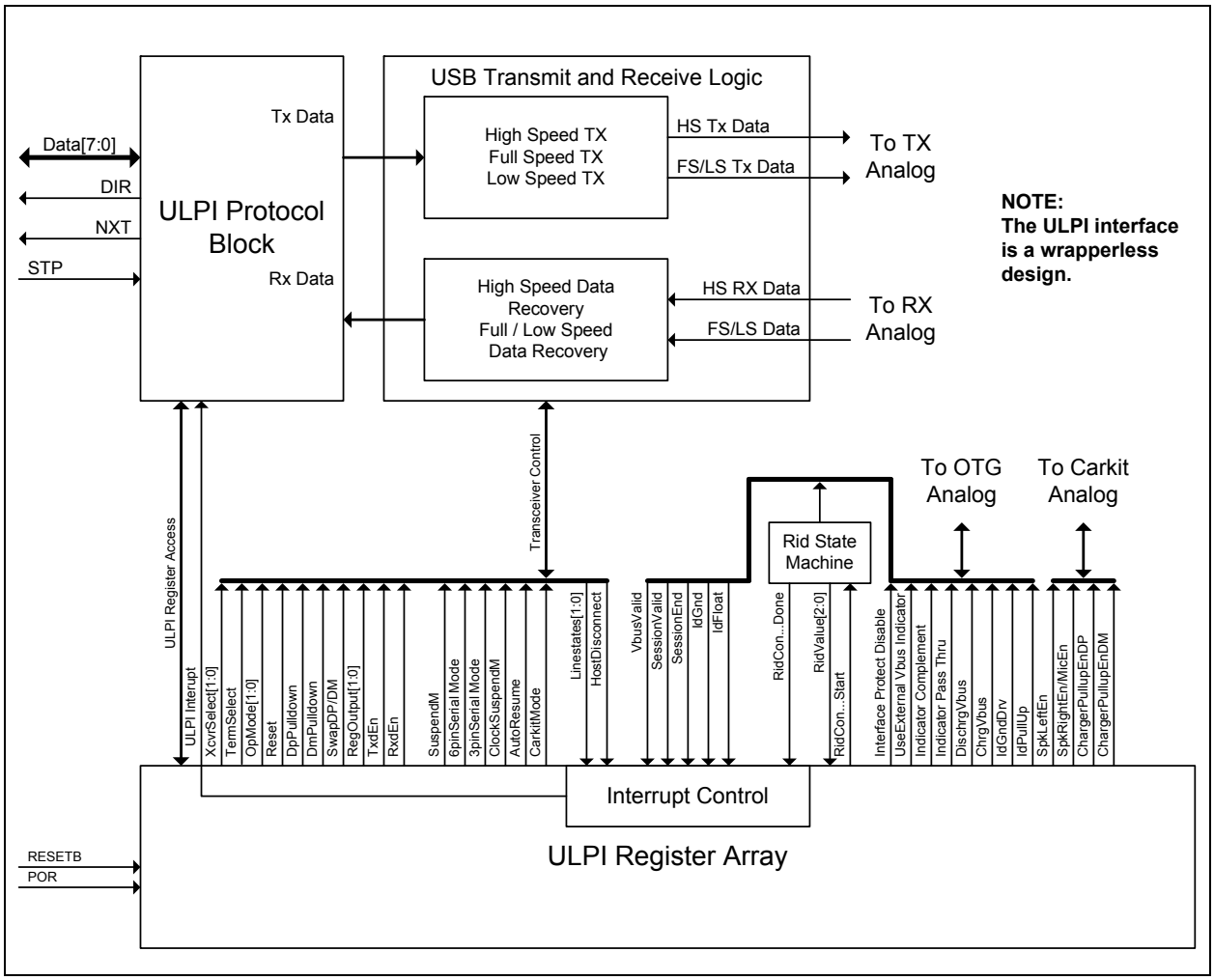


Figure 6.1 ULPI Digital Block Diagram

The advantage of a "wrapper less" architecture is that the USB3318 has a lower USB latency than a design which must first register signals into the PHY's wrapper before the transfer to the PHY core. A low latency PHY allows a Link to use a wrapper around a UTMI Link and still make the required USB turn-around timing given in the USB 2.0 specification.

RxEndDelay maximum allowed by the UTMI+/ULPI for 8-bit data is 63 high speed clocks. USB3318 uses a low latency high speed receiver path to lower the RxEndDelay to 43 high speed clocks. This low latency design gives the Link more cycles to make decisions and reduces the Link complexity. This is the result of the “wrapper less” architecture of the USB3318. This low RxEndDelay should allow legacy UTMI Links to use a “wrapper” to convert the UTMI+ interface to a ULPI interface.

In Figure 6.1, a single ULPI Protocol Block decodes the ULPI 8-bit bi-directional bus when the Link addresses the PHY. The Link must use the **DIR** output to determine direction of the ULPI data bus. The USB3318 is the “bus arbitrator”. The ULPI Protocol Block will route data/commands to the transmitter or the ULPI register array.

6.1.1 ULPI Interface Signals

The UTIM+ Low Pin Interface (ULPI) uses 12-pins to connect a full OTG Host / Device PHY to an SOC. A reduction of external pins on the PHY is accomplished by realizing that many of the relatively static configuration pins (xcvrselect[1:0], termselect, opmode[1:0], and DpPullDown DmPulldown to list a few,) can be implemented by having an internal static register array.

An 8-bit bi-directional data bus clocked at 60MHz allows the Link to access this internal register array and transfer USB packets to and from the PHY. The remaining 3 pins function to control the data flow and arbitrate the data bus.

Direction of the 8-bit data bus is controlled by the **DIR** output from the PHY. Another output, **NXT**, is used to control data flow into and out of the device. Finally, **STP**, which is in input to the PHY, terminates transfers and is used to start up and resume from Low Power Mode.

The 12 signals are described below in Table 6.1.

Table 6.1 ULPI Interface Signals

SIGNAL	DIRECTION	DESCRIPTION
CLKOUT	OUT	60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock.
DATA[7:0]	I/O	8-bit bi-directional data bus. Bus ownership is determined by DIR. The Link and PHY initiate data transfers by driving a non-zero pattern onto the data bus. ULPI defines interface timing for a single-edge data transfers with respect to rising edge of **CLKOUT**.
DIR	OUT	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link. The PHY will pull **DIR** high whenever the interface cannot accept data from the Link, such as during PLL start-up.
STP	IN	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
NXT	OUT	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.

USB3318 implements a Single Data Rate (SDR) ULPI interface with all data transfers happening on the rising edge of the **CLKOUT** signal supplied by the PHY.

The ULPI interface supports the two basic modes of operation: Synchronous Mode and Low Power Mode. In Synchronous Mode, all signals change synchronously with the 60MHz CLKOUT. In Low Power Mode the clock is off and the lower two bits of the data bus contain the linestate[1:0] signals. Interrupt outputs are generated while in Low Power Mode to enable the Link to receive an asynchronous interrupt when the Linestate, Vbus state, or ID state changes.

Data is transferred on the rising edge of **CLKOUT** while operating in Synchronous Mode. The direction of the data bus is determined by the state of **DIR**. When **DIR** is high, the PHY is driving **DATA[7:0]**. When **DIR** is low, the Link is driving **DATA[7:0]**.

Each time DIR changes, a “turn-around” cycle occurs where neither the Link nor PHY drive the data bus for one clock cycle. During the “turn–around“cycle, the state of **DATA[7:0]** is unknown and the PHY will not read the data bus.

Because USB uses a bit-stuffing encoding, some means of allowing the PHY to throttle the USB transmit data is needed. The ULPI signal NXT is used to request the next byte to be placed on the data bus by the Link layer.

6.1.2 ULPI Interface Timing in Synchronous Mode

The control and data timing relationships are given in Figure 6.2 and Table 4.3. The USB3318 provides **CLKOUT** and all timing is relative to the rising clock edge.

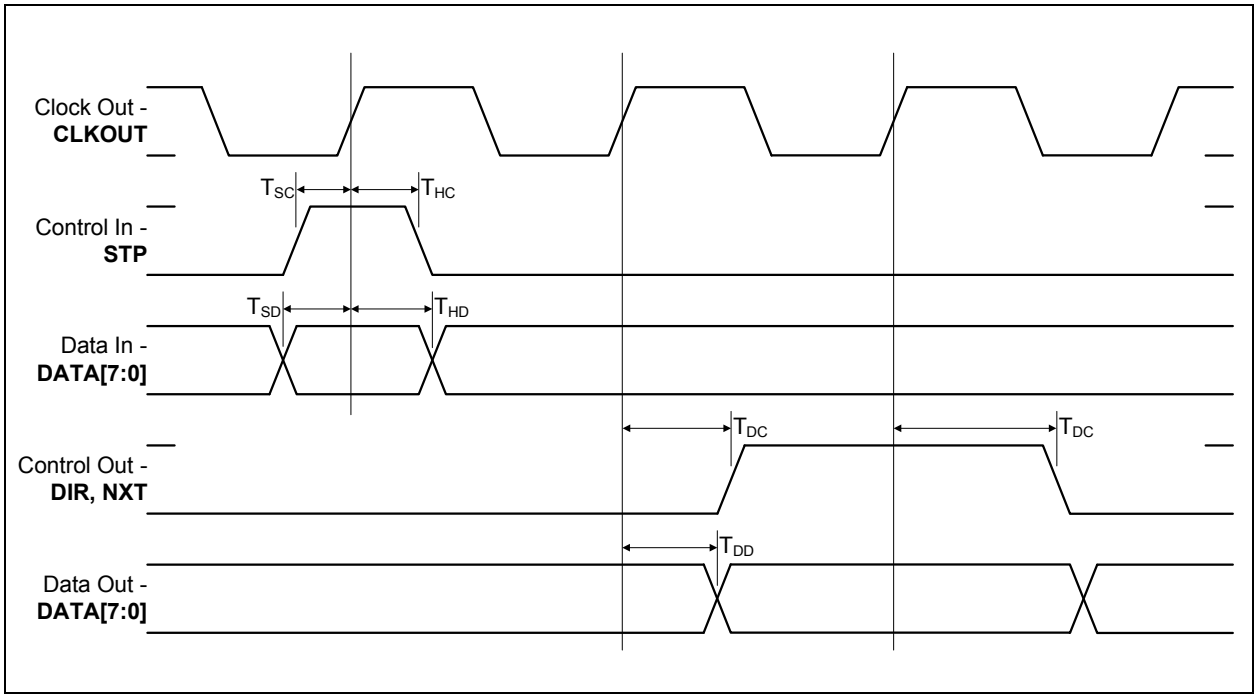


Figure 6.2 ULPI Single Data Rate Timing Diagram in Synchronous Mode

6.2 ULPI Register Access

A command from the Link begins a ULPI transfer from the Link to the USB3318. Before reading a ULPI register, the Link must wait until DIR is low, and then send a Transmit Command Byte (TXD CMD) byte. The TXD CMD byte informs the USB3318 of the type of data being sent. The TXD CMD is followed by a data transfer to or from the USB3318. Table 6.2 gives the TXD command byte (TXD CMD) encoding for the USB3318. The upper two bits of the TX CMD instruct the PHY as to what type

of packet the Link is transmitting. The ULPI registers retain their contents when the PHY is in Low Power Mode, Full Speed/Low Speed Serial Mode, or Carkit Mode.

Table 6.2 ULPI TXD CMD Byte Encoding

COMMAND NAME	CMD BITS[7:6]	CMD BITS[5:0]	COMMAND DESCRIPTION
Idle	00b	000000b	ULPI Idle
Transmit	01b	000000b	USB Transmit Packet with No Packet Identifier (NOPID)
		00XXXXb	USB Transmit Packet Identifier (PID) where DATA[3:0] is equal to the 4-bit PID. $P_3P_2P_1P_0$ where P_3 is the MSB.
Register Write	10b	XXXXXXb	Immediate Register Write Command where: **DATA[5:0]** = 6-bit register address
		101111b	Extended Register Write Command where the 8-bit register address is available on the next cycle.
Register Read	11b	XXXXXXb	Immediate Register Read Command where: **DATA[5:0]** = 6-bit register address
		101111b	Extended Register Read Command where the 8-bit register address is available on the next cycle.

6.2.1 ULPI Register Write

A ULPI register write operation is given in Figure 6.3. The TXD command with a register write DATA[7:6] = 10b is driven by the Link at T0. The register address is encoded into **DATA[5:0]** of the TXD CMD byte.

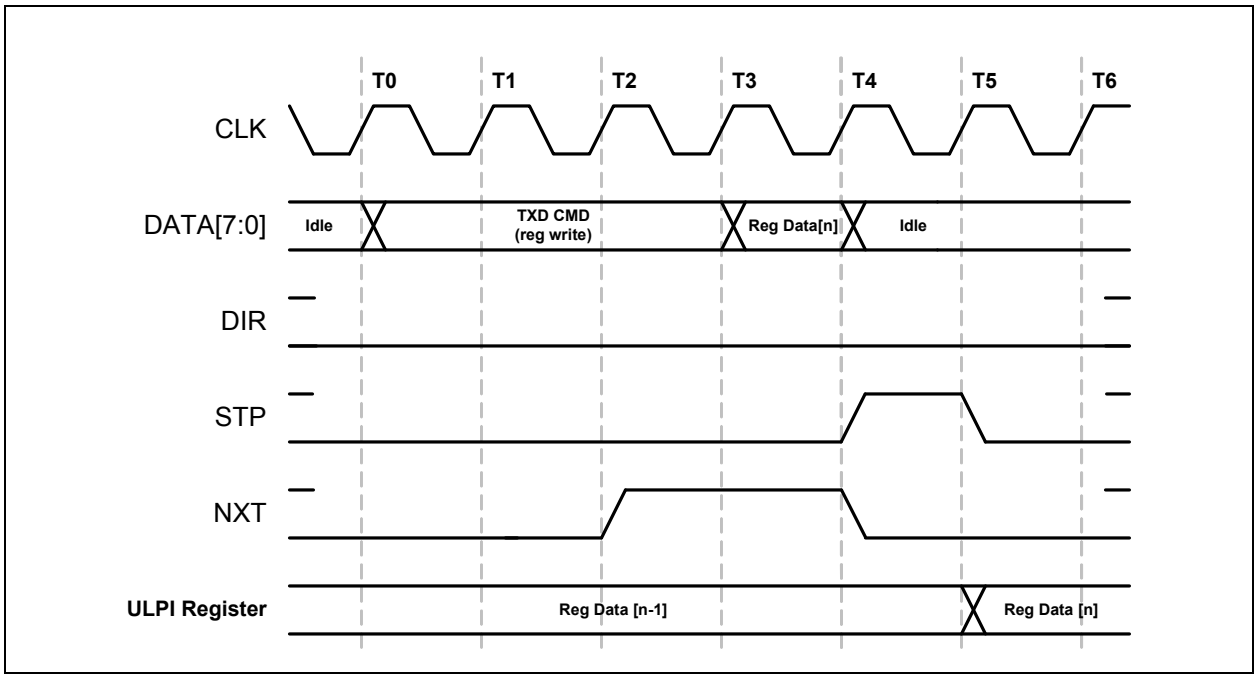


Figure 6.3 ULPI Register Write in Synchronous Mode

To write a register, the Link will wait until **DIR** is low, and at T0, drive the TXD CMD on the data bus. At T2 the PHY will drive **NXT** high. On the next rising clock edge, T3, the Link will write the register data. At T4, the PHY will accept the register data and the Link will drive an Idle on the bus and drive **STP** high to signal the end of the data packet. Finally, at T5, the PHY will latch the data into the register and drive **NXT** low. The Link will pull **STP** low.

NXT is used to control when the Link drives the register data on the bus. **DIR** is low throughout this transaction since the PHY is receiving data from the Link. **STP** is used to end the transaction and data is registered after the de-assertion of **STP**. After the write operation completes, the Link must drive a ULPI Idle (00h) on the data bus or the USB3318 may decode the bus value as a ULPI command.

A ULPI extended register write operation is shown in Figure 6.4. To write an extended register, the Link will wait until **DIR** is low, and at T0, drive the TXD CMD on the data bus. At T2 the PHY will drive **NXT** high. On the next clock T3 the Link will drive the extended address. On the next rising clock edge, T4, the Link will write the register data. At T5, the PHY will accept the register data and drive **NXT** low. The Link will drive an Idle on the bus and drive **STP** high to signal the end of the data packet. Finally, at T5, the PHY will latch the data into the register. The Link will pull **STP** low.

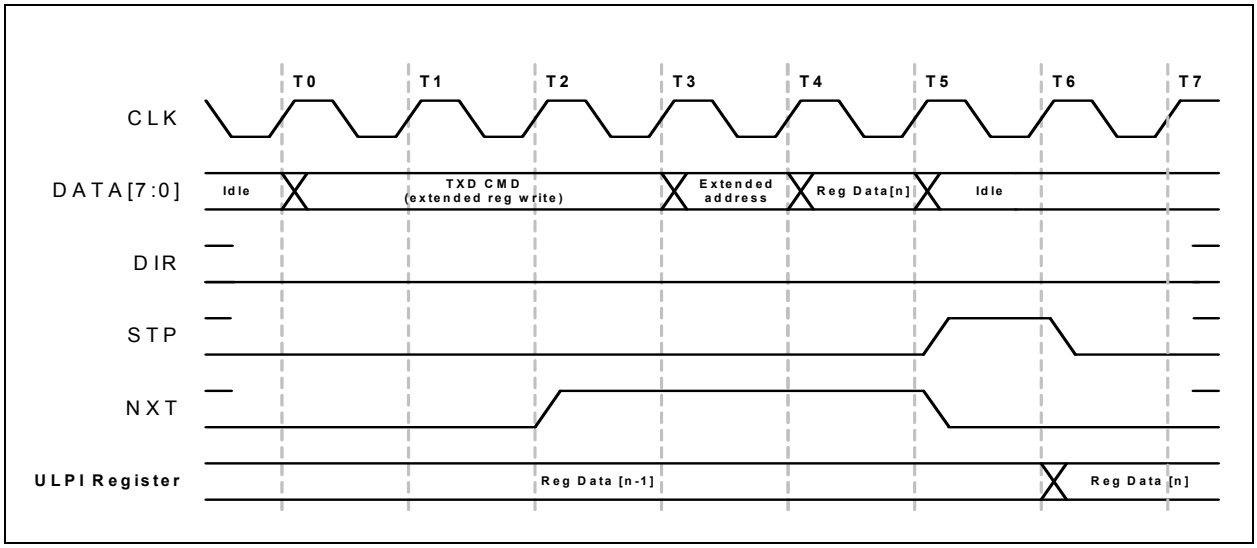


Figure 6.4 ULPI Extended Register Write in Synchronous Mode

6.2.2 ULPI Register Read

A ULPI register read operation is given in Figure 6.5. The Link drives a TXD CMD byte with **DATA[7:6]** = 11h for a register read. **DATA[5:0]** of the ULPI TXD command bye contain the register address.

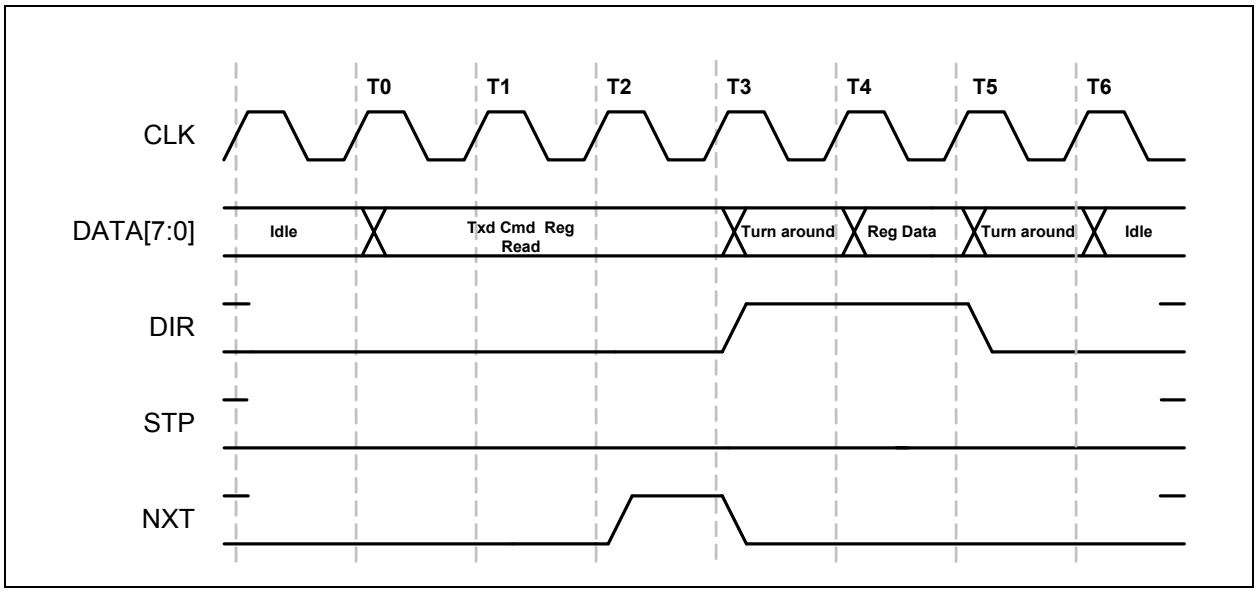


Figure 6.5 ULPI Register Read in Synchronous Mode

At T0, the Link will place the TXD CMD on the data bus. At T2, the PHY will bring **NXT** high, signaling that the Link it is ready to accept the data transfer. At T3, the PHY reads the TXD CMD, determines it is a register read, and asserts **DIR** to gain control of the bus. The PHY will also de-assert **NXT**. At T4, the bus ownership has transferred back to the PHY and the PHY drives the requested register onto the data bus. At T5, the Link will read the data bus and the PHY will drop **DIR** low returning control of the bus back to the Link. After the turn around cycle, the Link must drive a ULPI Idle command at T6.

A ULPI extended register read operation is shown in Figure 6.6.To read an extended register, the Link writes the TX CMD with the address set to 2Fh. At T2, the PHY will assert **NXT**, signaling the Link it is ready to accept the extended address. At T3, the Link places the extended register address on the bus. At T4, the PHY reads the extended address, and asserts **DIR** to gain control of the bus. The PHY will also de-assert **NXT**. At T5, the bus ownership has transferred back to the PHY and the PHY drives the requested register onto the data bus. At T6, the Link will read the data bus and the PHY will de-assert **DIR** returning control of the bus back to the Link. After the turn around cycle, the Link must drive a ULPI Idle command at T6.

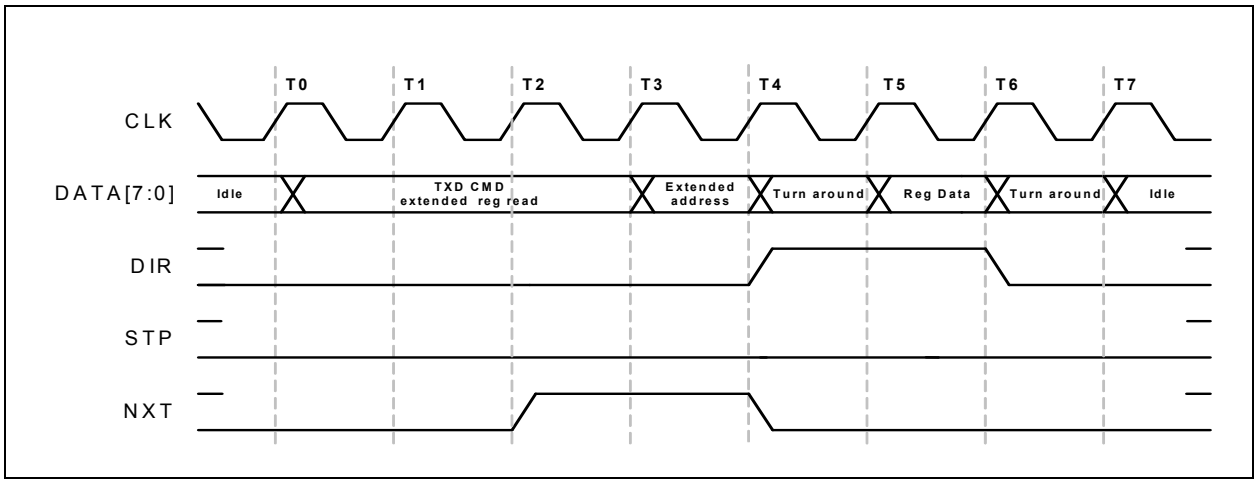


Figure 6.6 ULPI Extended Register Read in Synchronous Mode

6.2.3 ULPI RXCMD

The ULPI Link needs information which was provided by the following pins in a UTMI implementation: linestate[1:0], rxactive, rxvalid and rxerror. When implementing the OTG functions the **VBUS** and **ID** pin states must also be transferred to the Link.

ULPI defines a Receive Command Byte (RXCMD) that contains this information. The Encoding of the RXCMD byte is given in the Table 6.3.

Transfer of the RXCMD byte occurs in Synchronous Mode when the PHY has control of the bus. The ULPI Protocol Block shown in Figure 6.1 determines when to send an RXCMD. When a linestate change occurs, the RXCMD is sent immediately if the **DIR** output is low.

When a USB Receive is occurring, RXCMD's are sent whenever **NXT** = 0 and **DIR** = 1. During a USB Transmit, the RXCMD's are returned to the Link after **STP** is asserted.

To summarize a RXCMD transfer occurs:

- When **DIR** is low and a linestate change occurs.
- When Vbus and/or ID comparators change state.
- During a USB receive when **NXT** is low.
- After **STP** is asserted during a USB transmit command.
- After the USB3318 deasserts **DIR** and **STP** is low during start-up
- After the USB3318 exits Low Power Mode, Serial Modes, or Carkit Modes after detecting that the Link has asserted **STP**.

Table 6.3 ULPI RX CMD Encoding

DATA[7:0]	NAME	DESCRIPTION AND VALUE				
[1:0]	Linestate	UTMI Linestate Signals Note 6.1				
[3:2]	Encoded Vbus State	**ENCODED VBUS VOLTAGE STATES**				
		VALUE	**VBUS VOLTAGE**	**SESSEND**	**SESSVLD**	**$VBUSVLD_2$**
		00	$V_{VBUS} < V_{SESS\_END}$	1	0	0
		01	$V_{SESS\_END} < V_{VBUS} < V_{SESS\_VLD}$	0	0	0
		10	$V_{SESS\_VLD} < V_{VBUS} < V_{VBUS\_VLD}$	X	1	0
		11	$V_{VBUS\_VLD} < V_{VBUS}$	X	X	1
[5:4]	Rx Event Encoding	**ENCODED UTMI EVENT SIGNALS**				
		VALUE	**RXACTIVE**	**RXERROR**	**HOSTDISCONNECT**	
		00	0	0	0	
		01	1	0	0	
		11	1	1	0	
		10	X	X	1	
[6]	State of **ID** pin	Set to the logic state of the **ID** pin. A logic low indicates an A device. A logic high indicates a B device.				
[7]	alt_int	Asserted when a non-USB interrupt occurs. This bit is set when an unmasked event occurs on any bit in the Carkit Interrupt Latch register. The Link must read the Carkit Interrupt Latch register to determine the source of the interrupt. Section 5.6.1.3 describes how a change on the **ID** pin can generate an interrupt. Section 6.5 describes how an interrupt can be generated when the *RidConversionDone* bit is set.				

Notes:

1. An ‘X’ is a do not care and can be either a logic 0 or 1.
2. The value of VbusValid is defined in Table 5.5.

Note 6.1 LineState: These bits in the RXCMD byte reflect the current state of the Full-Speed single ended receivers. LineState[0] directly reflects the current state of **DP**. LineState[1] directly reflects the current state of **DM**. When **DP**=**DM**=0 this is called "Single Ended Zero" (SE0). When **DP**=**DM**=1, this is called "Single Ended One" (SE1).

6.2.4 USB3318 Transmitter

The USB3318 ULPI transmitter fully supports HS, FS, and LS transmit operations. Figure 6.1 shows the high speed, full speed, and low speed transmitter block controlled by ULPI Protocol Block. Encoding of the USB packet follows the bit-stuffing and NRZI outlined in the USB 2.0 specification. Many of these functions are re-used between the HS and FS/LS transmitters. When using the USB3318, Table 5.1 should always be used as a guideline on how to configure for various modes of operation. The transmitter decodes the inputs of *XcvrSelect[1:0]*, *TermSelect*, *OpMode[1:0]*, *DpPulldown,* and *DmPulldown* to determine what operation is expected. Users must strictly adhere to the modes of operation given in Table 5.1.

Several important functions for a device and host are designed into the transmitter blocks.

The USB3318 transmitter will transmit a 32-bit long high speed sync before every high speed packet. In full and low speed modes a 8-bit sync is transmitted.

When the device or host needs to chirp for high speed port negotiation, the *OpMode* = 10 setting will turn off the bit-stuffing and NRZI encoding in the transmitter. At the end of a chirp, the USB3318 *OpMode* register bits should be changed only after the RXCMD linestate encoding indicates that the transmitter has completed transmitting. Should the opmode be switched to normal bit-stuffing and NRZI encoding before the transmit pipeline is empty, the remaining data in the pipeline may be transmitted in an bit-stuff encoding format.

Please refer to the ULPI specification for a detailed discussion of USB reset and HS chirp.

6.2.4.1 High Speed Long EOP

When operating as a Hi-Speed host, the USB3318 will automatically generate a 40 bit long End of Packet (EOP) after a SOF PID (A5h). The USB3318 determines when to send the 40-bit long EOP by decoding the ULPI TXD CMD bits [3:0] for the SOF. The 40-bit long EOP is only transmitted when the *DpPulldown* and *DmPulldown* bits in the OTG Control register are asserted. The Hi-Speed 40-bit long EOP is used to detect a disconnect in high speed mode.

In device mode, the USB3318 will not send a long EOP after a SOF PID.

6.2.4.2 Low Speed Keep-Alive

Low speed keep alive is supported by the USB3318. When in Low speed (10b), the USB3318 will send out two Low speed bit times of SE0 when a SOF PID is received.

6.2.4.3 UTMI+ Level 3

Pre-amble is supported for UTMI+ Level 3 compatibility. When *XcvrSelect* is set to (11b) in host mode, (*DpPulldown* and *DmPulldown* both asserted) the USB3318 will pre-pend a full speed pre-amble before the low speed packet. Full speed rise and fall times are used in this mode. The pre-amble consists of the following: Full speed sync, the encoded pre-PID (C3h) and then full speed idle (DP=1 and DM = 0). A low speed packet follows with a sync, data and a LS EOP.

The USB3318 will only support UTMI+ Level 3 as a host. The USB3318 does not support UTMI+ Level 3 as a peripheral. A UTMI+ Level 3 peripheral is an upstream hub port. The USB3318 will not decode a pre-amble packet intended for a LS device when the USB3318 is configured as the upstream port of a FS hub, *XcvrSelect* = 11b, *DpPulldown* = 0b, *DmPulldown* =0b.

6.2.4.4 Host Resume K

Resume K generation is supported by the USB3318. When the USB3318 exits the suspended (Low Power Mode), the USB3318, when operating as a host, will transmit a K on DP/DM. The transmitters will end the K with SE0 for two Low Speed bit times. If the USB3318 was operating in high speed mode before the suspend, the host must change to high speed mode before the SE0 ends. SE0 is two low speed bit times which is about 1.2 us. For more details please see sections 7.1.77 and 7.9 of the USB Specification.

In device mode, the resume K will not append an SE0, but release the bus to the correct idle state, depending upon the operational mode as shown in Table 5.1.

The ULPI specification includes a detailed discussion of the resume sequence and the order of operations required. To support Host start-up of less than 1mS the USB3318 implements the ULPI *AutoResume* bit in the Interface Control register. The default *AutoResume* state is 0 and this bit should be enabled for Host applications.

6.2.4.5 No SYNC and EOP Generation (*OpMode* = 11)

UTMI+ defines O*pMode* = 11 where no sync and EOP generation occurs in Hi-Speed operation. This is an option to the ULPI specification and not implemented in the USB3318.

6.2.4.6 Typical USB Transmit with ULPI

Figure 6.7 shows a typical USB transmit sequence. A transmit sequence starts by the Link sending a TXD CMD where **DATA[7:6]** = 01b, **DATA[5:4]** = 00b, and **Data[3:0]** = PID. The TX CMD with the PID is followed by transmit data.

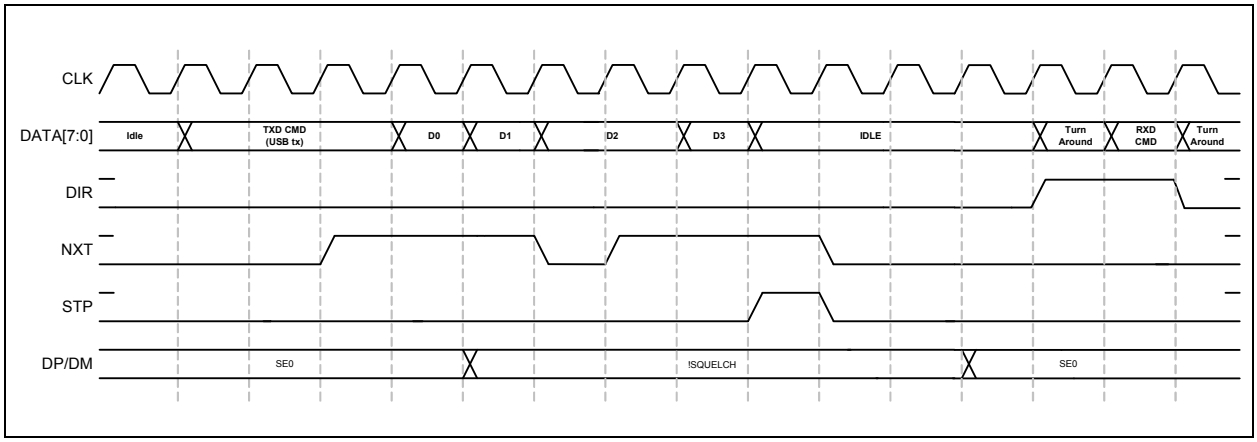


Figure 6.7 ULPI Transmit in Synchronous Mode

During transmit the PHY will use **NXT** to control the rate of data flow into the PHY. If the USB3318 pipeline is full or bit-stuffing causes the data pipeline to overfill **NXT** is de-asserted and the Link will hold the value on Data until **NXT** is asserted. The USB Transmit ends when the Link asserts **STP** while **NXT** is asserted.

Note: The Link cannot assert **STP** with **NXT** de-asserted since the USB3318 is expecting to fetch another byte from the Link.

After the USB3318 completes transmitting, the DP/DM lines return to idle and a RXCMD is returned to the Link so the inter-packet timers may be updated by linestate.

While operating in Full Speed or Low Speed, an End-of-Packet (EOP) is defined as SE0 for approximately two bit times, followed by J for one bit time. The transceiver drives a J state for one bit time following the SE0 to complete the EOP. The Link must wait for one bit time following line state indication of the SE0 to J transition to allow the transceiver to complete the one bit time J state. All bit times are relative to the speed of transmission.

In the case of Full Speed or Low Speed, after **STP** is asserted each FS/LS bit transition will generate a RXCMD since the bit times are relatively slow.

6.2.5 USB Receiver

The USB3318 ULPI receiver fully supports HS, FS, and LS transmit operations. In all three modes the receiver detects the start of packet and synchronizes to the incoming data packet. In the ULPI protocol, a received packet has the priority and will immediately follow register reads and RXCMD transfers. Figure 6.8 shows a basic USB packet received by the USB3318 over the ULPI interface.

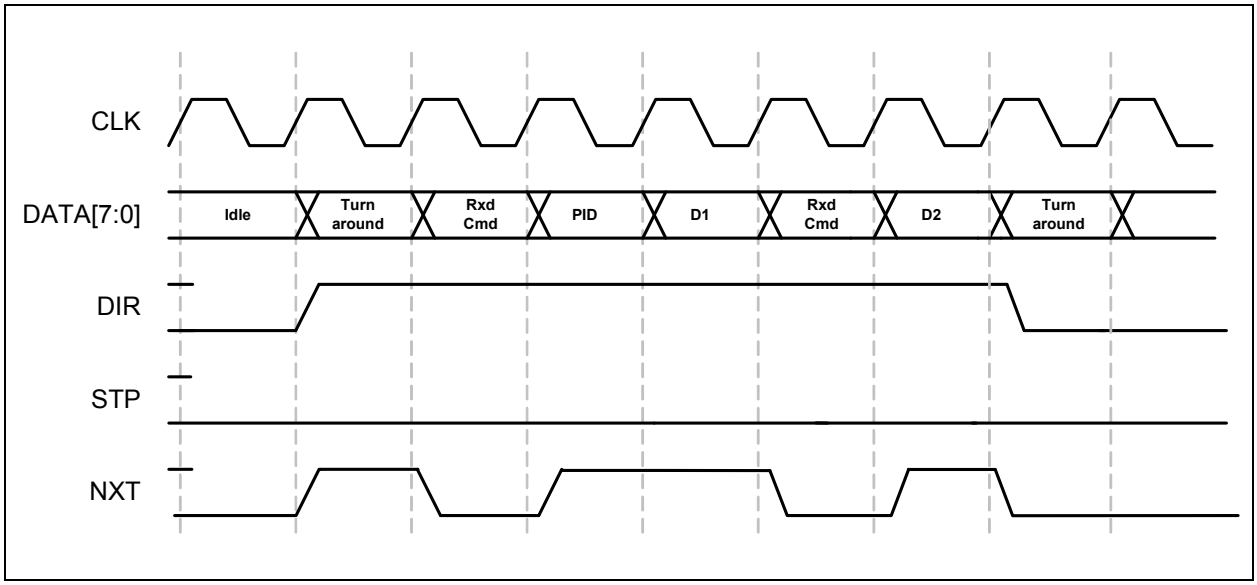


Figure 6.8 ULPI Receive in Synchronous Mode

In Figure 6.8 the PHY asserts **DIR** to take control of the data bus from the Link. The assertion of **DIR** and **NXT** in the same cycle contains additional information that Rxactive has been asserted. When **NXT** is de-asserted and **DIR** is asserted, the RXCMD data is transferred to the Link. After the last byte of the USB receive packet is transferred to the PHY, the linestate will return to idle.

The ULPI full speed receiver operates according to the UTMI / ULPI specification. In the full speed case, the **NXT** signal will assert only when the Data bus has a valid received data byte. When **NXT** is low with **DIR** high, the RXCMD is driven on the data bus.

In full speed, the USB3318 will not issue a Rxactive de-assertion in the RXCMD until the DP/DM linestate transitions to idle. This prevents the Link from violating the two full speed bit times minimum turn around time.

6.2.5.1 Disconnect Detection

A High Speed host must detect a disconnect by sampling the transmitter outputs during the long EOP transmitted during a SOF packet. The USB3318 only looks for a high speed disconnect during the long EOP where the period is long enough for the disconnect reflection to return to the host PHY. When a high speed disconnect occurs, the USB3318 will return a RXCMD and set the host disconnect bit in the USB Interrupt Status register.

When in FS or LS modes, the Link is expected to handle all disconnect detection.

6.2.6 Low Power Mode

Low Power Mode is a power down state to save current when the USB session is suspended. The Link controls when the PHY is placed into or out of Low Power Mode. In Low Power Mode all of the circuits are powered down except the interface pins, full speed receiver, VBUS comparators, and IdGnd comparator.

Before entering Low Power Mode, the USB3318 must be configured to set the desired state of the USB transceiver. The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration as shown in Table 5.1. The **DP** and **DM** pins are configured to a high impedance state by configuring *OpMode[1:0]* = 01. Pull-down resistors with a value of approximately 2MΩ are present

on the **DP** and **DM** pins to avoid false linestate indications that could result if the pins were allowed to float.

6.2.6.1 Entering Low Power/Suspend Mode

To enter Low Power Mode, the Link will write a 0 or clear the *SuspendM* bit in the Function Control register. After this write is complete, the PHY will assert **DIR** high and after a minimum of five rising edges of **CLKOUT**, drive the clock low. After the clock is stopped, the PHY will enter a low power state to conserve current. Placing the PHY in Suspend Mode is not related to USB Suspend. To clarify this point, USB Suspend is initiated when a USB host stops data transmissions and enters Full-Speed mode with 15KΩ pull-down resistors on **DP** and **DM**. The suspended device goes to Full-Speed mode with a pull-up on **DP**. Both the host and device remain in this state until one of them drives **DM** high (this is called a resume).

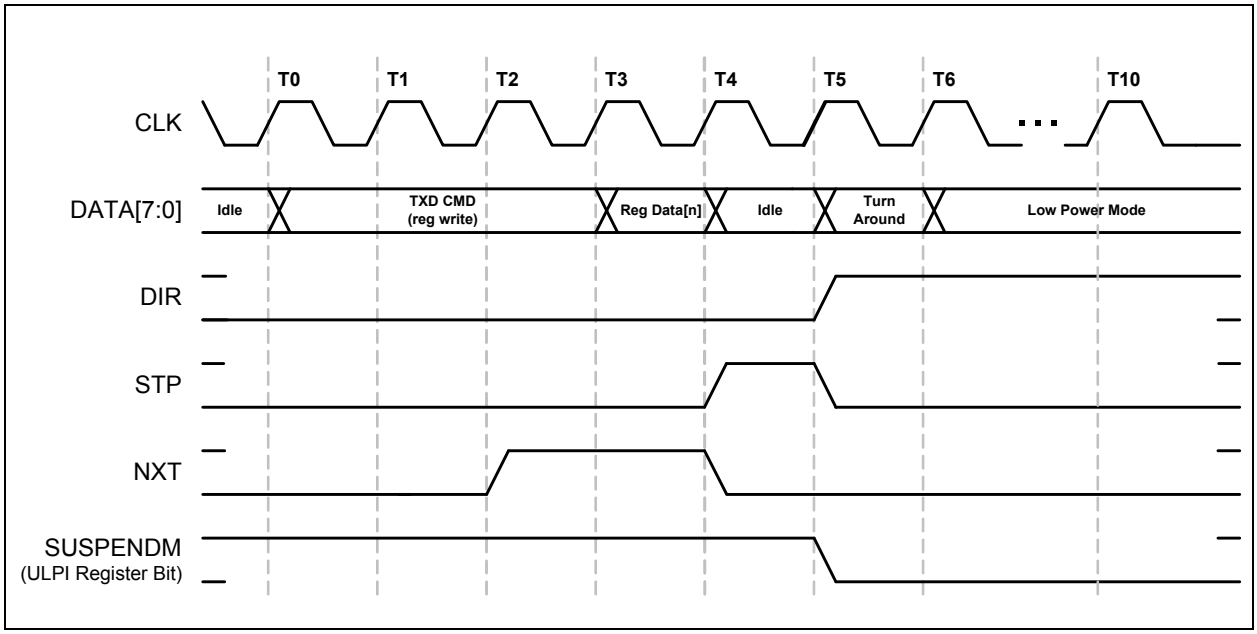


Figure 6.9 Entering Low Power Mode from Synchronous Mode

While in Low Power Mode, the Data interface is redefined so that the Link can monitor Linestate and the Vbus voltage. In Low Power Mode **DATA[3:0]** are redefined as shown in Table 6.4. Linestate[1:0] is the combinational output of the Single-Ended Receivers. The “int” or interrupt signal indicates an unmasked interrupt has occurred. When an unmasked interrupt or linestate change has occurred, the Link is notified and can determine if it should wake-up the PHY.

Table 6.4 Interface Signal Mapping During Low Power Mode

SIGNAL	MAPS TO	DIRECTION	DESCRIPTION
linestate[0]	DATA[0]	OUT	Combinatorial linestate[0] driven directly by FS analog receiver.
linestate[1]	DATA[1]	OUT	Combinatorial linestate[1] driven directly by FS analog receiver.
reserved	DATA[2]	OUT	Driven Low
int	DATA[3]	OUT	Active high interrupt indication. Must be asserted whenever any unmasked interrupt occurs.
reserved	DATA[7:4]	OUT	Driven Low

An unmasked interrupt can be caused by the following comparators changing state: VbusVld, SessVld, SessEnd, and IdGnd. If any of these signals change state during Low Power Mode and the bits are enabled in either the USB Interrupt Enable Rising or USB Interrupt Enable Falling registers, **DATA[3]**

will assert. During Low Power Mode, the VbusVld and SessEnd comparators can have their interrupts masked to lower the suspend current as described in Section 6.2.6.4.

While in Low Power Mode, the Data bus is driven asynchronously because all of the PHY clocks are stopped during Low Power Mode.

6.2.6.2 Exiting Low Power Mode

To exit Low Power Mode, the Link will assert **STP**. Upon the assertion of **STP**, the USB3318 will begin its start-up procedure. After the PHY start-up is complete, the PHY will start the clock on **CLKOUT** and de-assert **DIR**. After **DIR** has been de-asserted, the Link can de-assert **STP** when ready and start operating in Synchronous Mode. The PHY will automatically set the *SuspendM* bit to a 1 in the Function Control register.

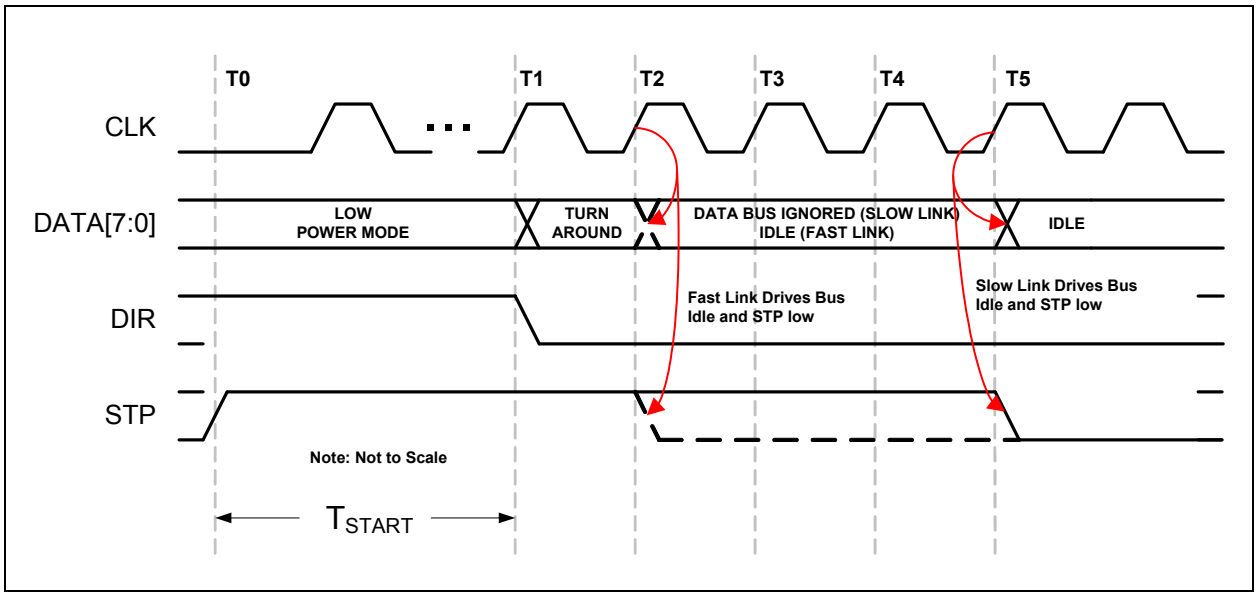


Figure 6.10 Exiting Low Power Mode

The value for T_{START} is given in Table 4.2.

Should the Link de-assert **STP** before **DIR** is de-asserted, the USB3318 will detect this as a false resume request and return to Low Power Mode. This is detailed in section 3.9.4 of the ULPI 1.1 specification.

6.2.6.3 Interface Protection

ULPI protocol assumes that both the Link and PHY will keep the ULPI data bus driven by either the Link when **DIR** is low or the PHY when **DIR** is high. The only exception is when **DIR** has changed state and a turn around cycle occurs for 1 clock period.

In the design of a USB system, there can be cases where the Link may not be driving the ULPI bus to a known state while **DIR** is low. Two examples where this can happen is because of a slow Link start-up or a hardware reset.

START UP PROTECTION

Upon start-up, when the PHY de-asserts **DIR**, the Link must be ready to receive commands and drive Idle on the data bus. If the Link is not ready to receive commands or drive Idle, it must assert **STP** before **DIR** is de-asserted. The Link can then de-assert **STP** when it has completed its start-up. If the Link doesn't assert **STP** before it can receive commands, the **PHY** may interpret the data bus state as a TX CMD and transmit invalid data onto the **USB** bus, or make invalid register writes.

When the USB3318 sends a RXCMD the Link is required to drive the data bus back to idle at the end of the turn around cycle. If the Link does not drive the databus to idle the USB3318 may take the information on the data bus as a TXCMD and transmit data on **DP** and **DM** until the Link asserts stop. If the **ID** pin is floated the last RXCMD from the USB3318 will remain on the bus after **DIR** is de-asserted and the USB3318 will take this in as a TXCMD.

A Link should be designed to have the default POR state of the **STP** output high and the data bus tri-stated. The USB3318 has weak pull-downs on the data bus to prevent these inputs from floating when not driven. These resistors are only used to prevent the ULPI interface from floating during events when the link ULPI pins may be tri-stated. The strength of the pull down resistors can be found in Table 4.4. The pull downs are not strong enough to pull the data bus low after a ULPI RXCMD, the Link must drive the data bus to idle after **DIR** is de-asserted.

In some cases, a Link may be software configured and not have control of its **STP** pin until after the PHY has started. In this case, the USB3318 has in internal pull-up on the **STP** input pad which will pull **STP** high while the Link's **STP** output is tri-stated. The **STP** pull-up resistor is enabled on POR and can be disabled by setting the *InterfaceProtectDisable* bit 7 of the Interface Control register.

The **STP** pull-up resistor will pull-up the Link's **STP** input high until the Link configures and drives **STP** high. After the Link completes its start-up, **STP** can be synchronously driven low.

A Link design which drives **STP** high during POR can disable the pull-up resistor on **STP** by setting *InterfaceProtectDisable* bit to 1. A motivation for this is to reduce the suspend current. In Low Power Mode, **STP** is held low, which would draw current through the pull-up resistor on **STP**.

WARM RESET

Designers should also consider the case of a warm restart of a Link with a PHY in Low Power Mode. After the PHY enters Low Power Mode, **DIR** is asserted and the clock is stopped. The USB3318 looks for **STP** to be asserted to re-start the clock and then resume normal synchronous operation.

Should the USB3318 be suspended in Low Power Mode, and the Link receives a hardware reset, the PHY must be able to recover from Low Power Mode and start its clock. If the Link asserts **STP** on reset, the PHY will exit Low Power Mode and start its clock.

If the Link does not assert **STP** on reset, the interface protection pull-up can be used. When the Link is reset, its **STP** output will tri-state and the pull-up resistor will pull **STP** high, signaling the PHY to restart its clock.

6.2.6.4 Minimizing Current in Low Power Mode

In order to minimize the suspend current in Low Power Mode, the OTG comparators can be disabled to reduce suspend current. In Low Power Mode, the VbusVld and SessEnd comparators are not needed and can be disabled by clearing the associated bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. By disabling the interrupt in BOTH the rise and fall registers, the SessEnd and VbusVld comparators are turned off. The *IdFloatRise* and *IdFloatFall* bits in Carkit Interrupt Enable register should also be disabled if they were set. When exiting Low Power Mode, the Link should immediately re-enable the VbusVld and SessEnd comparators if host or OTG functionality is required.

In addition to disabling the OTG comparators in Low Power Mode, the Link may choose to disable the Interface Protect Circuit. By setting the *InterfaceProtectDisable* bit high in the Interface Control register, the Link can disable the pull-up resistor on **STP**. When **RESETB** is low the Interface Protect Circuit will be disabled.

6.3 Full Speed/Low Speed Serial Modes

The USB3318 includes two serial modes to support legacy Links which use either the 3pin or 6pin serial format. To enter either serial mode, the Link will need to write a 1 to the *6-pin FsLsSerialMode* or the *3-pin FsLsSerialMode* bits in the Interface control register. Serial Mode may be used to conserve power when attached to a device that is not capable of operating in Hi-Speed.

The serial modes are entered in the same manner as the entry into Low Power Mode. The Link writes the Interface Control register bit for the specific serial mode. The USB3318 will assert **DIR** and shut off the clock after at least five clock cycles. Then the data bus goes to the format of the serial mode selected. Before entering either serial mode, the Link must set the ULPI transceiver to the appropriate mode as defined in Table 5.1.

By default, the PHY will shut off the 60MHz clock to conserve power. Should the Link need the 60MHz clock to continue during the serial mode of operation, the *ClockSuspendM* bit[3] of the Interface Control Register should be set before entering a serial mode. If set, the 60 MHz clock will be present during serial modes.

In serial mode, interrupts are possible from unmasked sources. The state of each interrupt source is sampled prior to the assertion of **DIR** and this is compared against the asynchronous level from interrupt source.

Exiting the serial modes is the same as exiting Low Power Mode. The Link must assert **STP** to signal the PHY to exit serial mode. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB3318 and return it to Synchronous Mode.

6.3.1 3pin FS/LS Serial Mode

Three pin serial mode utilizes the data bus pins for the serial functions shown in Table 6.5.

Table 6.5 Pin Definitions in 3 pin Serial Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
tx_enable	**DATA[0]**	IN	Active High transmit enable.
data	**DATA[1]**	I/O	TX differential data on DP/DM when tx_enable is high. RX differential data from DP/DM when tx_enable is low.
SE0	**DATA[2]**	I/O	TX SE0 on DP/DM when tx_enable is high. RX SE0_b from DP/DM when tx_enable is low.
interrupt	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
Reserved	**DATA[7:4]**	OUT	Driven Low.

6.3.2 6pin FS/LS Serial Mode

Six pin serial mode utilizes the data bus pins for the serial functions shown in Table 6.6.

Table 6.6 Pin Definitions in 6 pin Serial Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
tx_enable	**DATA[0]**	IN	Active High transmit enable.
tx_data	**DATA[1]**	IN	Tx differential data on DP/DM when tx_enable is high.
tx_se0	**DATA[2]**	IN	Tx SE0 on DP/DM when tx_enable is high.
interrupt	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
rx_dp	**DATA[4]**	OUT	Single ended receive data on DP.
rx_dm	**DATA[5]**	OUT	Single ended receive data on DM.

Table 6.6 Pin Definitions in 6 pin Serial Mode (continued)

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
rx_rcv	**DATA[6]**	OUT	Differential receive data from DP and DM.
Reserved	**DATA[7]**	OUT	Driven Low.

6.4 Carkit Mode

The USB3318 includes Carkit Mode to support a USB UART Mode.

60MHz clock is stopped to conserve power by default. The Link may configure the 60MHz clock to continue by setting the *ClockSuspendM* bit of Interface Control before entering Carkit Mode. If set, the 60 MHz clock will continue during the of operation.

In Carkit Mode, interrupts are possible from unmasked sources. The state of each interrupt source is sampled prior to the assertion of **DIR** and this is compared against the asynchronous level from interrupt source. In Carkit Mode, the Linestate signals are not available per the ULPI specification.

Exiting Carkit Mode is the same as exiting Low Power Mode as described in Section 6.2.6.2. The Link must assert **STP** to signal the PHY to exit serial mode. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB3318 and return it to Synchronous Mode.

6.4.1 USB UART Mode

The USB3318 can be placed into UART Mode by first setting the *TxdEn* and *RxdEn* bits in the Carkit Control register. Then the Link can set the *CarkitMode* bit in the Interface Control register. The *TxdEn* and *RxdEn* bits must be written before the *CarkitMode* bit. After the *CarkitMode* bit is set, the ULPI interface will become redefined as described in Table 6.7, and the USB3318 will transmit data through the **DATA[0]** to **DM** of the USB connector and receive data on **DP** and pass the information the Link on **DATA[1]**.

When entering UART mode, the regulator output will automatically switch to the value configured by the *UART RegOutput bits in the* USB IO & Power Management register and a 125K R_{CD} pull-up will be applied internally to **DP** and **DM**. This will hold the UART in its default operating state.

While in UART mode, the transmit edge rates can be set to either the Full Speed USB or Low Speed USB edge rates by using the *XcvrSelect[1:0]* bits in the Function Control register.

Table 6.7 Pin Definitions in Carkit Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
txd	**DATA[0]**	IN	UART TXD signal that is routed to the **DM** pin if the *TxdEn* is set in the Carkit Control register.
rxd	**DATA[1]**	OUT	UART RXD signal that is routed to the **DP** pin if the *RxdEn* bit is set in the Carkit Control register.
reserved	**DATA[2]**	OUT	Driven Low.
int	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
reserved	**DATA[4:7]**	OUT	Driven Low.

6.5 RID Converter Operation

The RID converter is designed to read the value of the ID resistance to ground and report back its value through the ULPI interface.

When a resistor to ground is applied to the **ID** pin the state of the IdGnd comparator will change from a 1 to a 0 as described in Section 5.6.1. If the USB3318 is in ULPI mode, an RXCMD will be generated with bit 6 low. If the USB3318 is in Low Power Mode (or one of the other non-ULPI modes), the DATA[3] interrupt signal will go high.

After the USB3318 has detected the change of state on the **ID** pin, the RID converter can be used to determine the value of ID resistance. To start a ID resistance measurement, the *RidConversionStart* bit is set in the Vendor Rid Conversion register.

The Link can use one of two methods to determine when the RID Conversion is complete. One method is polling the *RidConversionStart* bit as described in Section 7.1.4.3. The preferred method is to set the *RidIntEn* bit in the Vendor Rid Conversion register. When *RidIntEn* is set, an RXCMD will be generated after the RID conversion is complete. As described in Table 6.3, the alt_int bit of the RXCMD will be set.

After the RID Conversion is complete, the Link can read *RidValue* from the Vendor Rid Conversion register.

6.6 Headset Audio Mode

This mode is designed to allow a user to view the status of several signals while using an analog audio headset with a USB connector. This feature, exclusive to SMSC, is provided as an alternate mode to the CarKit Mode defined in Section 6.4. In the CarKit Mode, the Link is unable to view the source of the interrupt on **ID**, except by returning to synchronous mode to read the ULPI registers. This forces the audio switches to be deactivated, and may glitch the audio signals. In addition, the Link cannot change the resistance on the **ID** pin without starting up the PHY to access the ULPI registers.

The Headset Audio Mode is entered by writing to the Headset Audio Mode register, and allows the Link access to the state of the **VBUS** and **ID** pins during audio without glitching the audio connection. The Headset Audio mode also enables the Link to change the resistance on the **ID** pin and to change the audio headset attached from mono to stereo.

The ULPI interface is redefined as shown in Table 6.8 when Headset Audio Mode is entered.

Table 6.8 Pin Definitions in Headset Audio Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
SessVld	**DATA[0]**	OUT	Output of SessVld comparator
VbusVld	**DATA[1]**	OUT	Output of VbusVld Comparator (interrupt must be enabled)
IdGndDrv	**DATA[2]**	IN	Drives **ID** pin to ground when asserted 0b: Not connected 1b: Connects **ID** to ground.
	DATA[3]	OUT	Driven low
IdGround	**DATA[4]**	OUT	Asserted when the **ID** pin is grounded. 0b: **ID** pin is grounded 1b: **ID** pin is floating
IdFloat	**DATA[5]**	OUT	Asserted when the **ID** pin is floating. *IdPullup* or *d_pullup330* must be enabled as shown below.

Table 6.8 Pin Definitions in Headset Audio Mode (continued)

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
IdPullup330	**DATA[6]**	IN	When enabled a 330kΩpullup is applied to the **ID** pin. 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor
IdPullup	**DATA[7]**	IN	Connects the 100kΩ pull-up resistor from the **ID** pin to **VDD3.3** 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor

Exiting Headset Audio Mode is the same as exiting Low Power Mode as described in Section 6.2.6.2. The Link must assert **STP** to signal the PHY to exit. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB3318 and return it to Synchronous Mode.

Chapter 7 ULPI Register Map

7.1 ULPI Register Array

The USB3318 PHY implements all of the ULPI registers detailed in the ULPI revision 1.1 specification. The complete USB3318 ULPI register set is shown in Table 7.1. All registers are 8 bits. This table also includes the default states of the register upon POR, as described in Section 5.5.2. The RESET bit in the Function Control Register does not reset the bits of the ULPI register array. The Link should not read or write to any registers not listed in this table.

The USB3318 supports extended register access. The immediate register set (00-3Fh) can be accessed through either an immediate address or an extended register address..

Table 7.1 ULPI Register Map

REGISTER NAME	DEFAULT STATE	ADDRESS (6BIT)			
		READ	WRITE	SET	CLEAR
Vendor ID Low	24h	00h	-	-	-
Vendor ID High	04h	01h	-	-	-
Product ID Low	06h	02h	-	-	-
Product ID High	00h	03h	-	-	-
Function Control	41h	04-06h	04h	05h	06h
Interface Control	00h	07-09h	07h	08h	09h
OTG Control	06h	0A-0Ch	0Ah	0Bh	0Ch
USB Interrupt Enable Rising	1Fh	0D-0Fh	0Dh	0Eh	0Fh
USB Interrupt Enable Falling	1Fh	10-12h	10h	11h	12h
USB Interrupt Status	00h	13h	-	-	-
USB Interrupt Latch	00h	14h	-	-	-
Debug	00h	15h	-	-	-
Scratch Register	00h	16-18h	16h	17h	18h
Carkit Control	00h	19-1Bh	19h	1Ah	1Bh
Reserved	00h	1Ch			
Carkit Interrupt Enable	00h	1D-1Fh	1Dh	1Eh	1Fh
Carkit Interrupt Status	00h	20h	-	-	-
Carkit Interrupt Latch	00h	21h	-	-	-
Reserved	00h	22-30h			
HS TX Boost	00h	31h	31h	-	-
Reserved	00h	32h	32h	-	-
Headset Audio Mode	00h	33h	33h	-	-

Table 7.1 ULPI Register Map (continued)

REGISTER NAME	DEFAULT STATE	ADDRESS (6BIT)			
		READ	WRITE	SET	CLEAR
Reserved	00h	34-35h			
Vendor Rid Conversion	00h	36-38h	36h	37h	38h
USB IO & Power Management	04h	39-3Bh	39h	3Ah	3Bh
Reserved	00h	3C-3Fh			

7.1.1 ULPI Register Set

The following registers are used for the ULPI interface.

7.1.1.1 Vendor ID Low

Address = 00h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Vendor ID Low	7:0	rd	24h	SMSC Vendor ID

7.1.1.2 Vendor ID High

Address = 01h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Vendor ID High	7:0	rd	04h	SMSC Vendor ID

7.1.1.3 Product ID Low

Address = 02h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Product ID Low	7:0	rd	06h	SMSC Product ID

7.1.1.4 Product ID High

Address = 03h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Product ID High	7:0	rd	00h	SMSC Product ID

7.1.1.5 Function Control

Address = 04-06h (read), 04h (write), 05h (set), 06h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
XcvrSelect[1:0]	1:0	rd/w/s/c	01b	Selects the required transceiver speed. 00b: Enables HS transceiver 01b: Enables FS transceiver 10b: Enables LS transceiver 11b: Enables FS transceiver for LS packets (FS preamble automatically pre-pended)
TermSelect	2	rd/w/s/c	0b	Controls the DP and DM termination depending on *XcvrSelect*, *OpMode*, *DpPulldown*, and *DmPulldown*. The DP and DM termination is detailed in Table 5.1.
OpMode	4:3	rd/w/s/c	00b	Selects the required bit encoding style during transmit. 00b: Normal Operation 01b: Non-Driving 10b: Disable bit-stuff and NRZI encoding 11b: Reserved
Reset	5	rd/w/s/c	0b	Active high transceiver reset. This reset does not reset the ULPI interface or register set. Automatically clears after reset is complete.
SuspendM	6	rd/w/s/c	1b	Active low PHY suspend. When cleared the PHY will enter Low Power Mode as detailed in 6.2.6. Automatically set when exiting Low Power Mode.
Reserved	7	rd	0b	Read only, 0.

7.1.1.6 Interface Control

Address = 07-09h (read), 07h (write), 08h (set), 09h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
6-pin FsLsSerialMode	0	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the 6-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode.
3-pin FsLsSerialMode	1	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the 3-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode.
CarkitMode	2	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the Carkit interface. The PHY will automatically clear this bit when exiting carkit mode.
ClockSuspendM	3	rd/w/s/c	0b	Enables Link to turn on 60MHz CLKOUT in serial or carkit mode. 0b: Disable clock in serial or carkit mode. 1b: Enable clock in serial or carkit mode.
AutoResume	4	rd/w/s/c	0b	Only applicable in Host mode. Enables the PHY to automatically transmit resume signaling. This function is detailed in Section 6.2.4.4.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IndicatorComplement	5	rd/w/s/c	0b	Inverts the EXTVBUS signal. This function is detailed in Section 5.6.2. **Note:** The EXTVBUS input is always high on the USB3318.
IndicatorPassThru	6	rd/w/s/c	0b	Disables and'ing the internal VBUS comparator with the EXTVBUS input when asserted. This function is detailed in Section 5.6.2. **Note:** The EXTVBUS input is always high on the USB3318.
InterfaceProtectDisable	7	rd/w/s/c	0b	Used to disable the integrated **STP** pull-up resistor used for interface protection. This function is detailed in Section 6.2.6.3.

7.1.1.7 OTG Control

Address = 0A-0Ch (read), 0Ah (write), 0Bh (set), 0Ch (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdPullup	0	rd/w/s/c	0b	Connects a 100kΩ pull-up resistor from the **ID** pin to **VDD33** 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor
DpPulldown	1	rd/w/s/c	1b	Enables the 15k Ohm pull-down resistor on **DP**. 0b: Pull-down resistor not connected 1b: Pull-down resistor connected
DmPulldown	2	rd/w/s/c	1b	Enables the 15k Ohm pull-down resistor on **DM**. 0b: Pull-down resistor not connected 1b: Pull-down resistor connected
DischrgVbus	3	rd/w/s/c	0b	This bit is only used during SRP. Connects a resistor from VBUS to ground to discharge **VBUS**. 0b: disconnect resistor from **VBUS** to ground 1b: connect resistor from **VBUS** to ground
ChrgVbus	4	rd/w/s/c	0b	This bit is only used during SRP. Connects a resistor from **VBUS** to **VDD33** to charge **VBUS** above the SessValid threshold. 0b: disconnect resistor from **VBUS** to **VDD33** 1b: connect resistor from **VBUS** to **VDD33**
DrvVbus	5	rd/w/s/c	0b	Used to enable external 5 volt supply to drive 5 volts on VBUS. This signal is or'ed with *DrvVbusExternal*. 0b: do not drive Vbus, **CPEN** driven low. 1b: drive Vbus, **CPEN** driven high.
DrvVbusExternal	6	rd/w/s/c	0b	Used to enable external 5 volt supply to drive 5 volts on Vbus. This signal is or'ed with *DrvVbus*. 0b: do not drive Vbus, **CPEN** driven low. 1b: drive Vbus, **CPEN** driven high

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
UseExternalVbus Indicator	7	rd/w/s/c	0b	Tells the PHY to use an external VBUS over-current or voltage indicator. This function is detailed in Section 5.6.2. 0b: Use the internal VbusValid comparator 1b: Use the EXTVBUS input as for VbusValid signal. **Note:** The EXTVBUS input is always high on the USB3318.

7.1.1.8 USB Interrupt Enable Rising

Address = 0D-0Fh (read), 0Dh (write), 0Eh (set), 0Fh (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect Rise	0	rd/w/s/c	1b	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode.
VbusValid Rise	1	rd/w/s/c	1b	Generate an interrupt event notification when Vbusvalid changes from low to high.
SessValid Rise	2	rd/w/s/c	1b	Generate an interrupt event notification when SessValid changes from low to high.
SessEnd Rise	3	rd/w/s/c	1b	Generate an interrupt event notification when SessEnd changes from low to high.
IdGnd Rise	4	rd/w/s/c	1b	Generate an interrupt event notification when IdGnd changes from low to high.
Reserved	7:5	rd	0h	Read only, 0.

7.1.1.9 USB Interrupt Enable Falling

Address = 10-12h (read), 10h (write), 11h (set), 12h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect Fall	0	rd/w/s/c	1b	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode.
VbusValid Fall	1	rd/w/s/c	1b	Generate an interrupt event notification when Vbusvalid changes from high to low.
SessValid Fall	2	rd/w/s/c	1b	Generate an interrupt event notification when SessValid changes from high to low.
SessEnd Fall	3	rd/w/s/c	1b	Generate an interrupt event notification when SessEnd changes from high to low.
IdGnd Fall	4	rd/w/s/c	1b	Generate an interrupt event notification when IdGnd changes from high to low.
Reserved	7:5	rd	0h	Read only, 0.

7.1.1.10 USB Interrupt Status

Address = 13h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect	0		0b Note 7.1	Current value of the UTMI+ Hi-Speed Hostdisconnect output. Applicable only in host mode.
VbusValid	1		0b Note 7.1	Current value of the UTMI+ Vbusvalid output.
SessValid	2		0b Note 7.1	Current value of the UTMI+ SessValid output.
SessEnd	3		0b Note 7.1	Current value of the UTMI+ SessEnd output.
IdGnd	4		0b Note 7.1	Current value of the UTMI+ IdGnd output.
Reserved	7:5		0h	Read only, 0.

Note 7.1 The default conditions will match the current status of the comparators. The values shown are for an unattached OTG device.

7.1.1.11 USB Interrupt Latch

Address = 14h (read only with auto clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect Latch	0	Note 7.2	0b	Set to 1b by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.
VbusValid Latch	1		0b	Set to 1b by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.
SessValid Latch	2		0b	Set to 1b by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read.
SessEnd Latch	3		0b	Set to 1b by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.
IdGnd Latch	4		0b	Set to 1b by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.
Reserved	7:5		0h	Read only, 0.

Note 7.2 Read Only with auto clear.

7.1.1.12 Debug

Address = 15h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Linestate0	0	rd	0b	Contains the current value of Linestate[0].
Linestate1	1	rd	0b	Contains the current value of Linestate[1].
Reserved	7:2	rd	000000b	Read only, 0.

7.1.1.13 Scratch Register

Address = 16-18h (read), 16h (write), 17h (set), 18h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Scratch	7:0	rd/w/s/c	00h	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.

7.1.2 Carkit Control Registers

The following registers are used to set-up and enable the USB UART functions.

7.1.2.1 Carkit Control

Address = 19-1Bh (read), 19h (write), 1Ah (set), 1Bh (clear)

This register is used to program the USB3318 into and out of the carkit modes. When entering the carkit UART mode the Link must first set the desired *TxdEn* and the *RxdEn* bits and then transition to Carkit Mode by setting the *CarkitMode* bit in the Interface Control Register. When *RxdEn* is not set then the DATA[1] pin is held to a logic high.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
CarkitPwr	0	rd	0b	Read only, 0.
IdGndDrv	1	rd/w/s/c	0b	Drives **ID** pin to ground
TxdEn	2	rd/w/s/c	0b	Connects UART TXD (**DATA[0]**) to **DM**
RxdEn	3	rd/w/s/c	0b	Connects UART RXD (**DATA[1]**) to **DP**
Reserved	4-7	rd	0b	Read only, 0.

7.1.2.2 Carkit Interrupt Enable

Address = 1D-1Fh (read), 1Dh (write), 1Eh (set), 1Fh (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdFloatRise	0	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when the **ID** pin transitions from non-floating to floating. The *IdPullup* bit in the OTG Control register should be set.
IdFloatFall	1	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when the **ID** pin transitions from floating to non-floating. The *IdPullup* bit in the OTG Control register should be set.
CarIntDet	2	rd	0b	Not Implemented. Reads as 0b.
CarDpRise	3	rd	0b	Not Implemented. Reads as 0b.
CarDpFall	4	rd	0b	Not Implemented. Reads as 0b.
RidIntEn	5	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when *RidConversionDone* bit is asserted. **Note:** This register bit is or'ed with the *RidIntEn* bit of the Vendor Rid Conversion register described in Section 7.1.4.3.
Reserved	7:6	rd	0b	Read only, 0.

7.1.2.3 Carkit Interrupt Status

Address = 20h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdFloat	0	rd	0b	Asserted when the **ID** pin is floating. *IdPullup* must be enabled.
CarIntDet	1	rd	0b	Not Implemented. Reads as 0b.
CarDp	2	rd	0b	Not Implemented. Reads as 0b.
RidValue	5:3	rd	000b	Conversion value of Rid resistor 000: 0 ohms 001: 75 ohms 010: 102K ohms 011: 200K ohms 100: 440K ohms 101: ID floating 111: Error **Note:** *RidValue* can also be read from the Vendor Rid Conversion register described in Section 7.1.4.3.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
RidConversionDone	6	rd	0b	Automatically asserted by the USB3318 when the Rid Conversion is finished. The conversion will take 282uS. This bit will auto clear when the *RidValue* is read from the Rid Conversion Register. Reading the *RidValue* from the Carkit interrupt Status register will not clear either *RidConversionDone* status bit. **Note:** *RidConversionDone* can also be read from the Vendor Rid Conversion register described in Section 7.1.4.3.
Reserved	7	rd	0b	Read only, 0.

7.1.2.4 Carkit Interrupt Latch

Address = 21h (read only with auto-clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdFloat Latch	0	rd*	0b	Asserted if the state of the **ID** pin changes from non-floating to floating while the *IdFloatRise* bit is enabled or if the state of the **ID** pin changes from floating to non-floating while the *IdFloatFall* bit is enabled.
CarIntDet Latch	1	rd	0b	Not Implemented. Reads as 0b.
CarDp Latch	2	rd	0b	Not Implemented. Reads as 0b.
RidConversionLatch	3	rd*	0b	If *RidIntEn* is set and the state of the *RidConversionDone* bit changes from a 0 to 1 this bit will be asserted.
Reserved		rd	00000b	Read only, 0.

Note: rd*: Read Only with auto clear.

7.1.3 Extended Register Access

The USB3318 supports extended register access. The immediate register set (00-3Fh) can be accessed through either a immediate address or an extended register address.

7.1.4 Vendor Register Access

The vendor specific registers include the range from 30h to 3Fh. These can be accessed by the ULPI immediate register read / write.

7.1.4.1 HS TX Boost

Address = 31h (read / write)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Reserved	4:0	rd	00000b	Read only, 0.
Boost	6:5	rd/w	00b	Sets the HS transmitter amplitude as described in Section 5.2.1. 00b: Nominal 01b: Reserved 10b: Enables 7.4% increased drive strength 11b: Enables 3.7% increased drive strength
Reserved	7	rd	0b	Read only, 0.

7.1.4.2 Headset Audio Mode

Address = 33h (read / write)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HeadsetAudioEn	3:0	rd/w	0000b	When this field is set to a value of 1010, the Headset Audio Mode is enabled as described in Section 6.6.
Reserved	7:4	rd	0h	Read only, 0.

7.1.4.3 Vendor Rid Conversion

Address = 36-38h (read), 36h (write), 37h (set), 38h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
RidValue	2:0	rd/w	000b	Conversion value of Rid resistor 000: 0 ohms 001: 75 ohms 010: 100K ohms 011: 200K ohms 100: 440K ohms 101: ID floating 111: Error **Note:** *RidValue* can also be read from the Carkit Interrupt Status register described in Section 7.1.2.3.
RidConversionDone	3	rd*	0b	Automatically asserted by the USB3318 when the Rid Conversion is finished. The conversion will take 282uS. This bit will auto clear when the *RidValue* is read from the Rid Conversion Register. Reading the *RidValue* from the Carkit interrupt Status register will not clear either *RidConversionDone* status bit. **Note:** *RidConversionDone* can also be read from the Carkit Interrupt Status register described in Section 7.1.2.3.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
RidConversionStart	4	rd/w/s/c	0b	When this bit is asserted either through a register write or set, the Rid converter will read the value of the ID resistor. When the conversion is complete this bit will auto clear.
Reserved	5	rd/w/s/c	0b	This bit must remain at 0.
RidIntEn	6	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when *RidConversionDone* bit is asserted. **Note:** This register bit is or'ed with the *RidIntEn* bit of the Carkit Interrupt Status register.
Reserved	7	rd	0b	Read only, 0.

Note: rd*: Read Only with auto clear.

7.1.4.4 USB IO & Power Management

Address = 39-3Bh (read), 39h (write), 3Ah (set), 3Bh (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Reserved	0	rd/w/s/c	0b	Read only, 0.
SwapDP/DM	1	rd/w/s/c	0b	When asserted, the **DP** and **DM** pins of the USB PHY are swapped. This bit can be used to prevent crossing the DP/DM traces on the board. In UART mode, it swaps the routing to the **DP** and **DM** pins.
UART RegOutput	3:2	rd/w/s/c	01b	Controls the output voltage of the **VBAT** to **VDD33** regulator in UART mode. When the PHY is switched from USB mode to UART mode regulator output will automatically change to the value specified in this register when *TxdEn* is asserted. 00: 3.3V 01: 3.0V (default) 10: 2.75V 11: 2.5V
ChargerPullupEnDP	4	rd/w/s/c	0b	Enables a 125K Pull-up for USB Charger Detection when set on the **DP** pin. (The pull-up is automatically enabled in UART mode)
ChargerPullupEnDM	5	rd/w/s/c	0b	Enables a 125K Pull-up for USB Charger Detection when set on the **DM** pin. (The pull-up is automatically enabled in UART mode)
USB RegOutput	7:6	rd/w/s/c	00b	Controls the output voltage of the **VBAT** to **VDD33** regulator in USB mode. When the PHY is in Synchronous Mode, Serial Mode, or Low Power Mode the regulator output will be the value specified in this register. 00: 3.3V (default) 01: 3.0V 10: 2.75V 11: 2.5V

Chapter 8 Application Notes

8.1 Application Diagram

The USB3318 requires few external components as shown in the application diagram. In some applications, the power supplied on the VBUS pin of the USB connector is used as the source of system power. The USB 2.0 Specification restricts the voltage at the VBUS pin to a maximum value of 5.25V. In some applications, it may be required to provide protection to the USB331x VBUS pin and VBAT pin if the VBUS voltage exceeds USB 2.0 specifications.

One method of protecting the **VBUS** pin from excessive voltage transients is to place a resistor (R_{VBUS}) in series as shown in the application diagram. The resistor provides some protection against transients that exceed the value of V_{VMAX} provided in Table 3.2. This resistor can be used when the USB3318 is powered from a Battery as shown in Figure 5.3 or from a 3.3V Supply as shown in Figure 5.4. When R_{VBUS} is installed, the transient must not be allowed to exceed the value of V_{VBUS} for longer than 500 µs.

To protect the **VBUS** pin against a steady state voltage on the USB connector that exceed the value of V_{VMAX} provided in Table 3.2, an Over Voltage Protection (OVP) component could be used in the place of R_{VBUS}.

Following POR or hardware reset, the voltage at **CLKOUT** must not exceed V_{IH_ED} as provided in Table 4.4.

Table 8.1 Component Values in Application Diagrams

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	NOTES
C_{OUT}	2.2µF	Bypass capacitor to ground (<1Ω ESR) for regulator stability.	Place as close as possible to the PHY.
C_{VBUS}	See Table 8.2	Capacitor to ground required by the USB Specification. SMSC recommends <1Ω ESR.	Place near the USB connector.
C_{BYP}	System dependent.	Bypass capacitor to ground. Typical values used are 0.1 or 0.01 µF.	Place as close as possible to the PHY.
C_{DC_LOAD}	System dependent.	The USB connector housing may be AC-coupled to the device ground.	Industry convention is to ground only the host side of the cable shield.
R_{VBUS}	820Ω or 10kΩ	Series resistor to reduce transient voltage on VBUS. 820Ω in Host or OTG applications. 10kΩ may be used only in device mode applications.	Cannot be used when the USB3318 is powered from the VBUS at the USB connector. This method of powering is shown in Figure 5.5.

Table 8.2 Capacitance Values at VBUS of USB Connector

MODE	MIN VALUE	MAX VALUE
Host	120µF	
Device	1µF	10µF
OTG	1µF	6.5µF

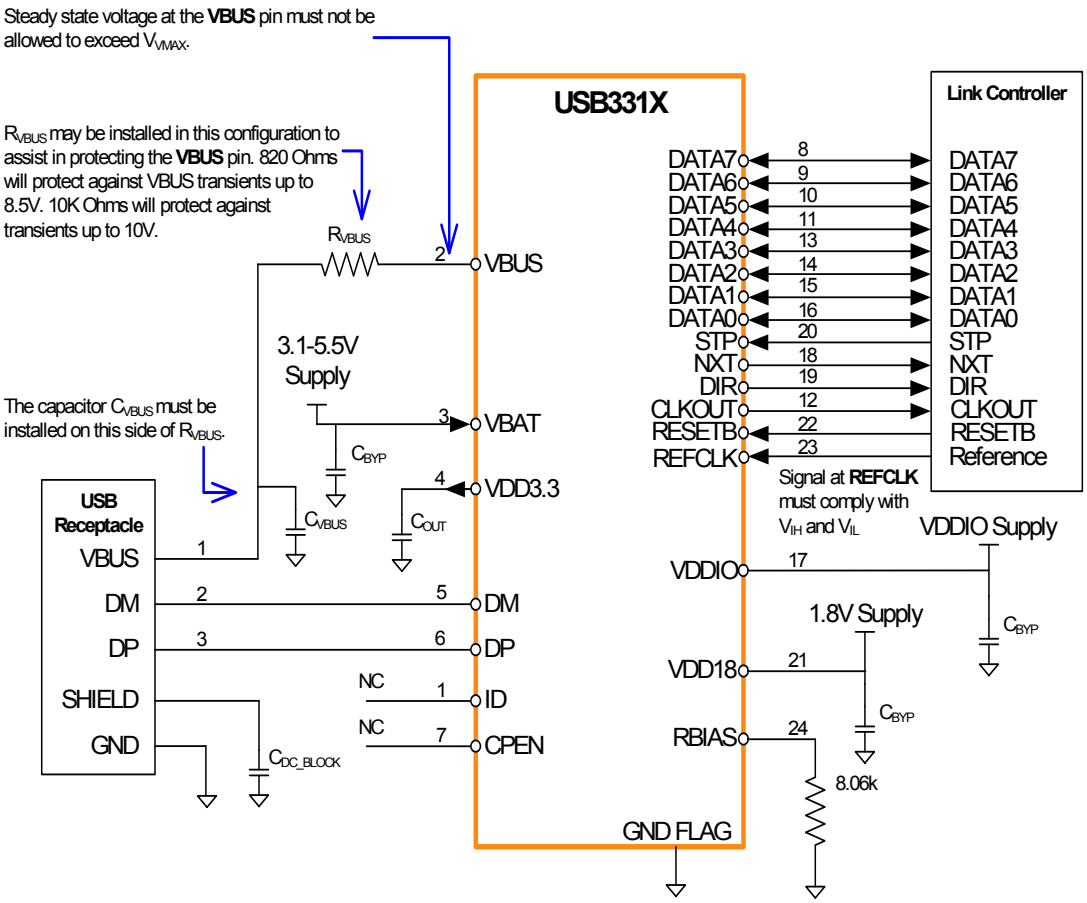


Figure 8.1 USB3318 QFN Application Diagram (Device)

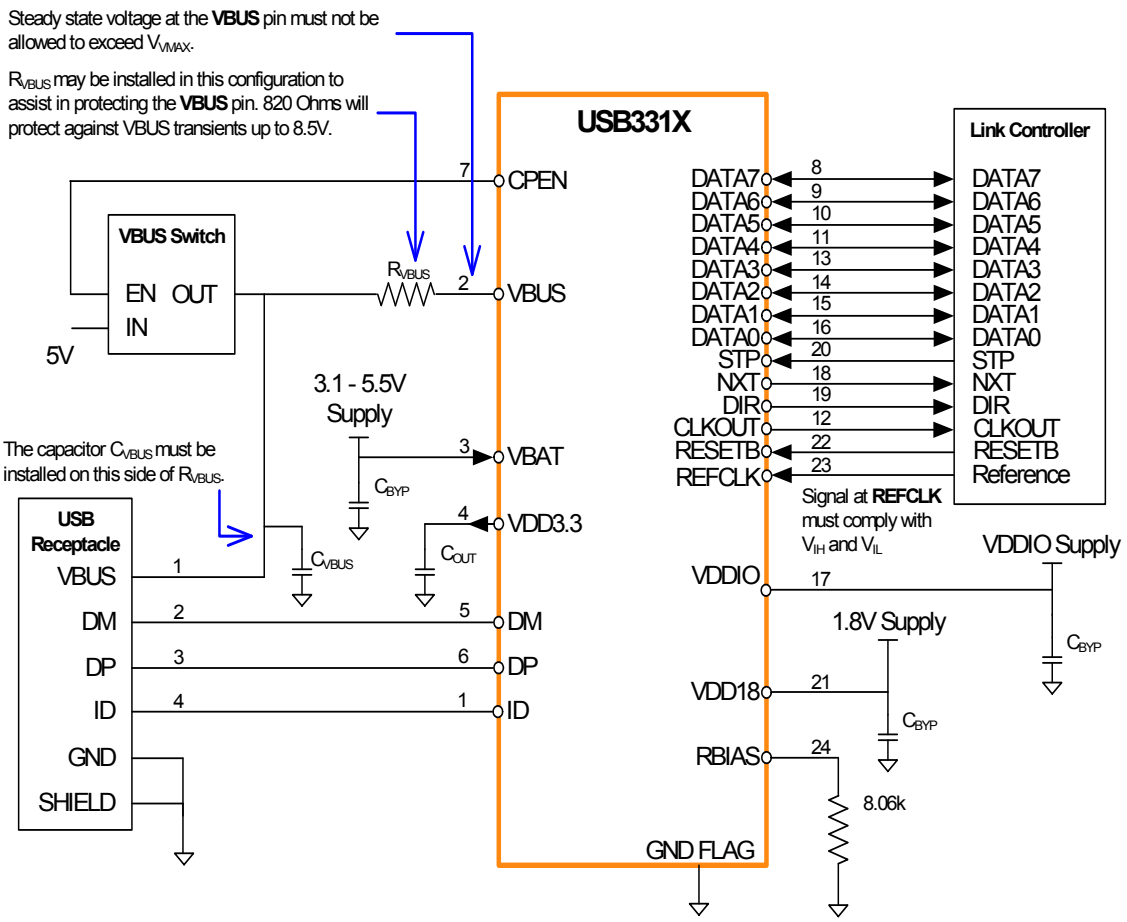


Figure 8.2 USB3318 QFN Application Diagram (Host or OTG)

8.2 USB Charger Detection

Note: SMSC does not build, specify, design, or sell USB chargers. The following section is provided as a reference to the end user so that they may implement a USB Charger detection method that will work with the chargers selected to work with their end product.

The examples below are illustrated for reference only and are not intended to dictate a standard for a USB Charger. The charger and detection method must be chosen to work together.

When attached to a USB Host the device is only allowed to draw 100mA until the completion of USB enumeration. The USB3318 includes features that can be used to differentiate between a USB Host and a Charger.

8.2.1 Detecting the ID Resistor in a Charger

The ID Resistor Detection feature of the USB3318 described in Section 5.6.1.2 may be used to detect a resistor to ground. Some charger manufacturers use 100kΩ to ground at the ID pin of the USB connector.

Pseudo Algorithm for detecting resistor to ground and reading value

```
Wait for IdGnd
Enable IdPullup
Set RidConversionStart
Wait for RidConversionDone
Read RidValue
```

8.2.2 Detecting DP Shorted to DM

USB Chargers and USB Hosts will present 5V nominal onto the Vbus terminal of the USB connector at all times. While in synchronous mode, the Link can detect SessVld in the RXCMD byte as shown in Table 6.3. In any of the non-synchronous modes, the Link must monitor the interrupt signal on DATA[3] as described in Table 6.4. When an interrupt occurs, the Link commands the USB3318 to exit Low Power Mode and reads registers to discover what caused the interrupt.

In preparation for testing if a charger has connected the DP and DM pins in the USB connector, the **DP** and **DM** pins of the USB3318 must be placed into Non-Driving, FS mode using the Full Speed transceivers. This is done by writing 49h to the Function Control register at address 04h. Next, pull-up resistors can be enabled on the **DP** and **DM** pins. As described in Section 5.8, the pull-up resistors may be enabled individually. For example, setting bit 4 in the USB IO & Power Management register at address 3Ah will connect the *ChargerPullupEnableDP* resistor. Likewise, a write to the USB IO & Power Management register at address 3Ah with a 20h will connect the *ChargerPullupEnableDM* resistor.

The linestate signals are monitored to determine whether the **DP** and **DM** pins are shorted. While in synchronous mode, the Link can monitor *Linestate0 and Linestate1* in the RXCMD byte as shown in Table 6.3, or by reading the Debug register. In any of the non-synchronous modes, the Link can monitor linestate on DATA[0] and DATA[1] as described in Table 6.3. The DC Electrical Characteristics of the Single-Ended Receivers used to generate the linestate signals are provided in Table 4.6.

Pseudo Algorithm for detecting voltage at Vbus and detecting DP shorted to DM

```
Wait for SessVld
Tri-State DP/DM and select FS transceivers
Enable ChargerPullupEnableDP resistor
Enable ChargerPullupEnableDM resistor
If the linestates show a SE1 the charger has been detected.
If the linestates show an SE0 you are connected to a host.
```

8.3 Reference Designs

SMSC has generated reference designs for connecting the USB3318 to SOCs with a ULPI port. Please contact the SMSC sales office for more details.

8.4 ESD Performance

The USB3318 is protected from ESD strikes. By eliminating the requirement for external ESD protection devices, board space is conserved, and the board manufacturer is enabled to reduce cost. The advanced ESD structures integrated into the USB3318 protect the device whether or not it is powered up.

8.4.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand the ESD strikes like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event. All pins on the USB3318 except the **REFCLK** pin provide ±8kV HBM protection, as shown in Table 4.9.

8.4.2 EN/IEC 61000-4-2 Performance

The EN/IEC 61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. In contrast, the HBM ESD tests are performed at the device level with the device powered down.

SMSC contracts with Independent laboratories to test the USB3318 to EN/IEC 61000-4-2 in a working system. Reports are available upon request. Please contact your SMSC representative, and request information on 3rd party ESD test results. The reports show that systems designed with the USB3318 can safely provide the ESD performance shown in Table 4.9 without additional board level protection.

In addition to defining the ESD tests, EN/IEC 61000-4-2 also categorizes the impact to equipment operation when the strike occurs (ESD Result Classification). The USB3318 maintains an ESD Result Classification 1 or 2 when subjected to an EN/IEC 61000-4-2 (level 4) ESD strike.

Both air discharge and contact discharge test techniques for applying stress conditions are defined by the EN/IEC 61000-4-2 ESD document.

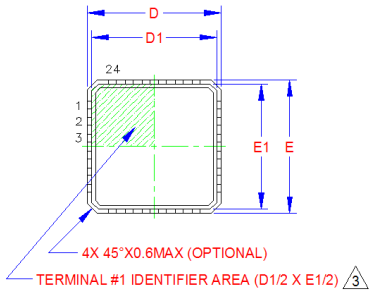
8.4.3 Air Discharge

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

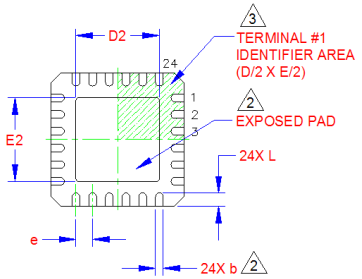
8.4.4 Contact Discharge

The uncharged electrode first contacts the USB connector to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. The independent test laboratories contracted by SMSC provide test results for both types of discharge methods.

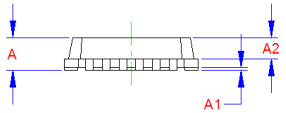
Chapter 9 Package Outline, Tape & Reel Drawings, Package Markings



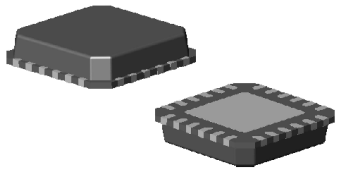
TOP VIEW



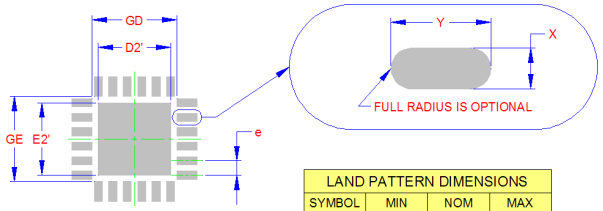
BOTTOM VIEW



SIDE VIEW



3-D VIEWS



THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.93	-	-
D2'/E2'	-	2.50	-
X	-	-	0.28
Y	-	-	0.69
e		0.50	

RECOMMENDED PCB LAND PATTERN

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	-	0.90	-	MOLD CAP THICKNESS
D/E	3.85	4.00	4.15	-	X/Y BODY SIZE
D1/E1	3.55	-	3.95	-	X/Y MOLD CAP SIZE
D2/E2	2.40	2.50	2.60	2	X/Y EXPOSED PAD SIZE
L	0.30	-	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 9.1 24-pin QFN, 4x4mm Body, 0.5mm Pitch

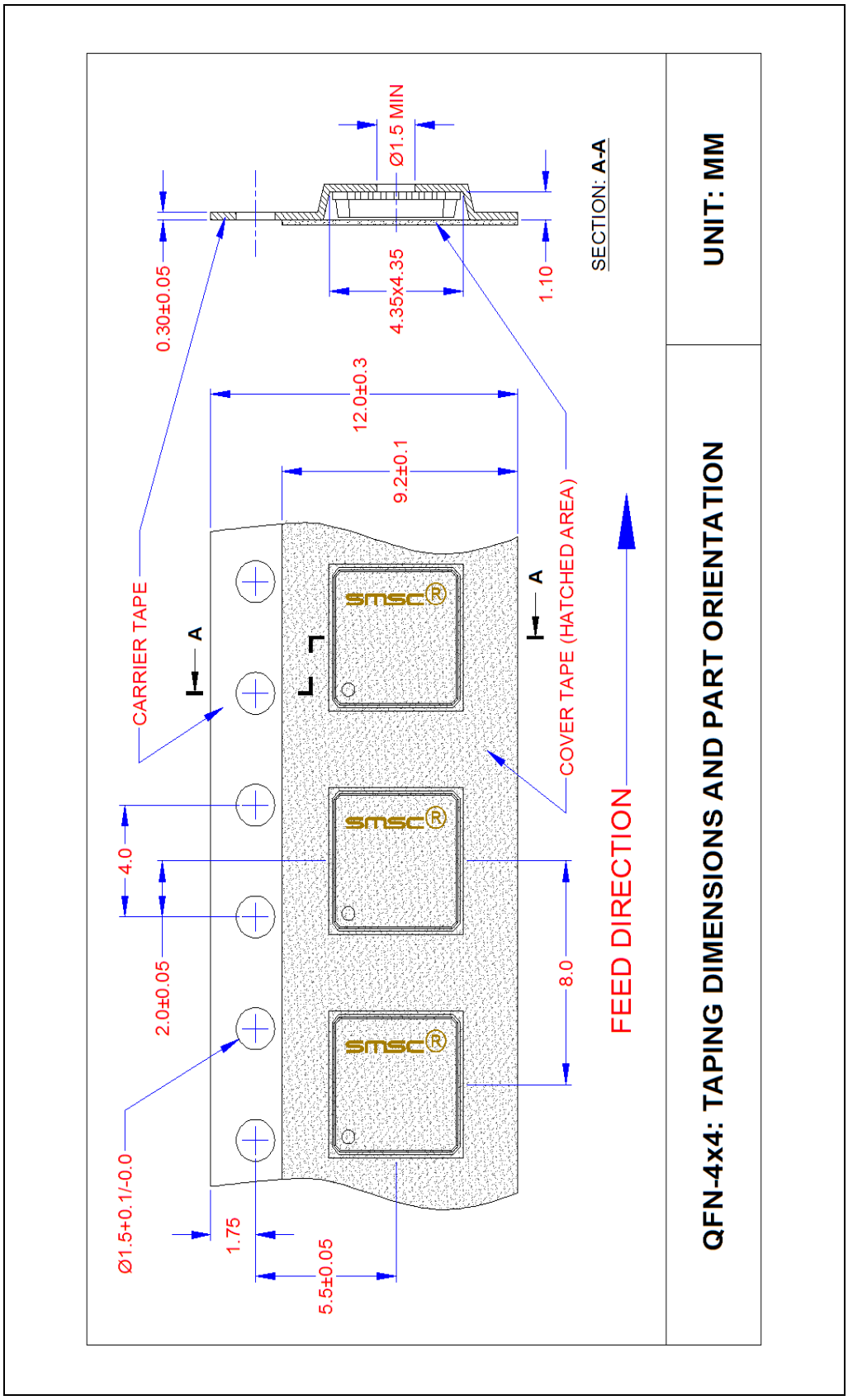


Figure 9.2 QFN, 4x4 Tape & Reel

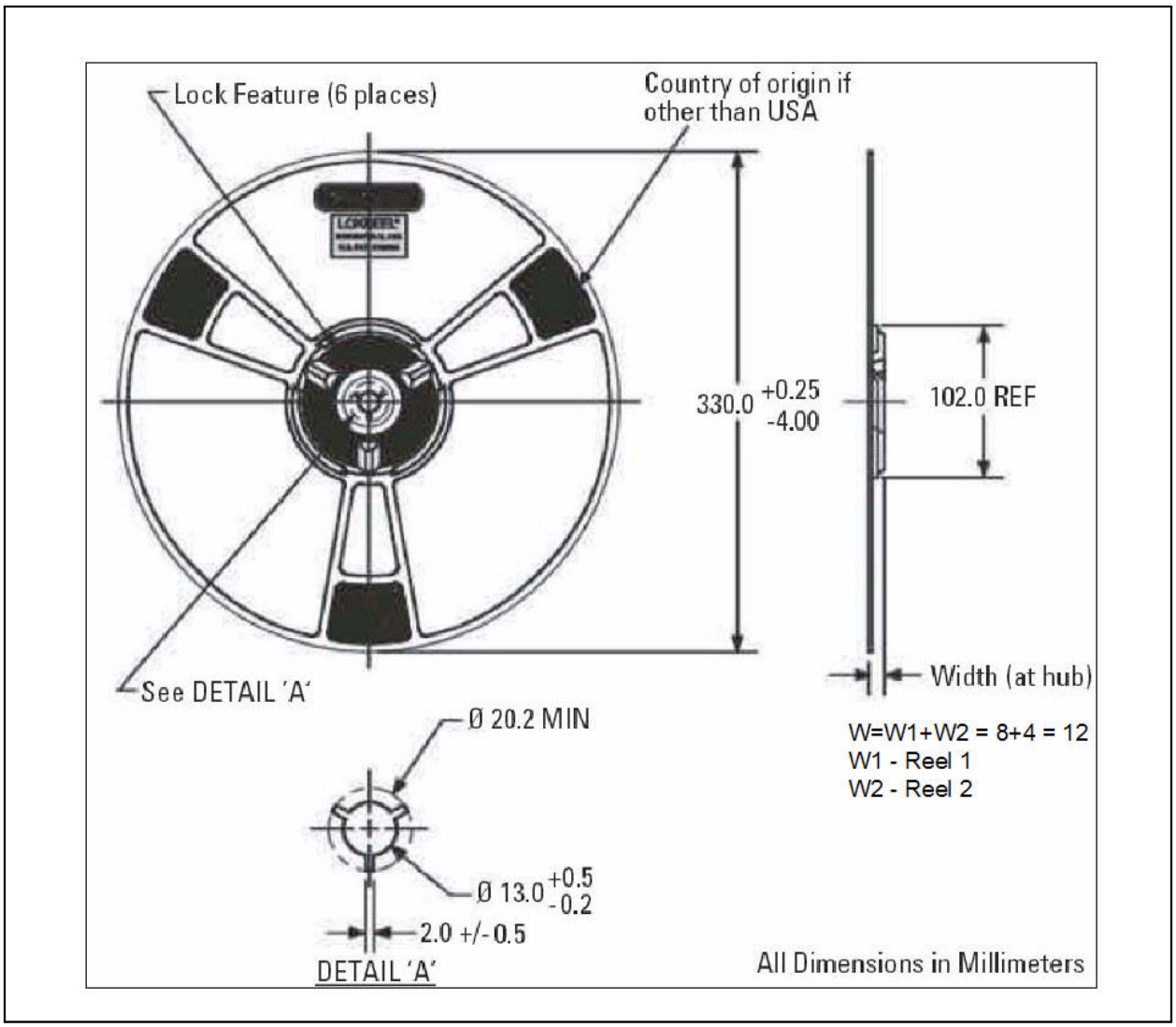


Figure 9.3 Reel Dimensions

Note: Standard reel size is 4000 pieces per reel.

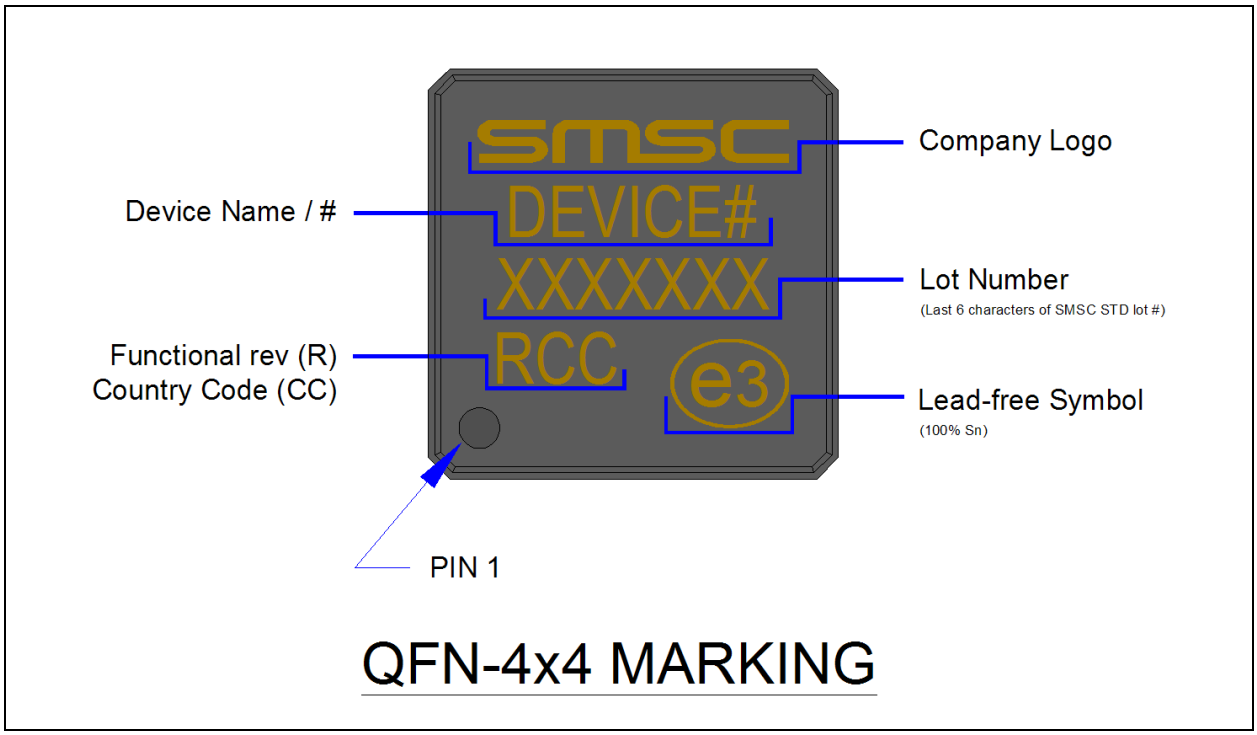


Figure 9.4 QFN, 4x4 Package Marking

Chapter 10 Datasheet Revision History

Table 10.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev 2.1 (06-02-10)	Cover Section	Changed references to OTG Specification Revision 1.3 to Revision 2.0.
	Chapter 5	Removed Note 5.3.
	Section 7.1.4.1	Removed -3.7% TX Boost.
	Section 6.6, Section 7.1	Added Headset Audio Mode definition.
Rev 2.0 (08-03-09)	Table 4.3	Changed Tdc,Tdd MIN to 1.5ns.
	Table 5.2	Added note.
	Figure 5.7	Corrected polarity of IdGnd Comparator.
	Table 5.4	Corrections made to column “IDGND”.
	Table 6.3	Modified definition of ID bit.
Rev. 1.11 (10-31-08)	Table 4.4	Formula in MAX column for CLKOUT External Drive changed from “0.68 * V_{DDIO}“ to “0.4 * V_{DDIO}”
Rev. 1.11 (10-28-08)	Pin Definitions table	Added the following note in description for CLKOUT: “Following POR or hardware reset, the voltage at **CLKOUT** must not exceed V_{IH_ED} as provided in Table 4.4.”
Rev. 1.11 (10-28-08)	Section 8.1, "Application Diagram"	Paragraph added: Following POR or hardware reset, the voltage at **CLKOUT** must not exceed V_{IH_ED} as provided in Table 4.4.
Rev. 1.11 (10-28-08)	Section 5.4, "Integrated Low Jitter PLL"	Paragraph added: “The system must not drive voltage on the CLKOUT pin following POR or hardware reset that exceeds the value of V_{IH_ED} provided in Table 4.4.”
Rev. 1.11 (10-28-08)	Table 4.4	Table title changed from “Electrical Characteristics - Digital IO Pins: RESETB, STP, DIR, NXT, DATA[7:0] & REFCLK Pins" to: "Digital IO Characteristics: RESETB, CLKOUT, STP, DIR, NXT, DATA[7:0] and XI Pins" Row added - “CLKOUT External Drive”
Rev. 1.11 (10-27-08)	Section 5.2.1, "USB Transceiver"	Added paragraph for further clarification
Rev. 1.11 (10-27-08)	Table 7.1, "ULPI Register Map" and Section 7.1.4.1, "HS TX Boost"	Added “HS TX Boost” register
Rev. 1.11 (10-27-08)	Section 8.2.2, "Detecting DP Shorted to DM"	Section modified
Rev. 1.10 (08-08-08)	Initial Release	

Table 10.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.10 (07-25-08)	Section 7.1.1.3, "Product ID Low"	Default column changed from “01h” to “06h”
Rev. 1.10 (07-09-08)	Section 7.1.1.10, "USB Interrupt Status"	Changed from : “Address = 13h (read only with auto clear)” to: “Address = 13h (read only)”; Note removed
Rev. 1.9 (06-23-08)		Changed conditions for synchronous mode to: Start-up sequence defined in Section 5.5.4, "Start-Up" has completed.
Rev. 1.9 (06-19-08)	Chapter 4, Electrical Characteristics	Changed conditions at beginning of chapter to include V_{VBAT}.
Rev. 1.9 (06-19-08)	Table 3.2, "Recommended Operating Conditions"	Made separate entry for V_{VBAT} and V_{BUS}. For normal operation, V_{VBAT} cannot be zero.
Rev. 1.8 (05-02-08)	Section 5.6, "USB On-The-Go (OTG)"	Changed Mini-AB connector to Micro-AB receptacle.