LC823450

Low Power & High-Resolution Audio Processing System LSI for Portable Sound Solution

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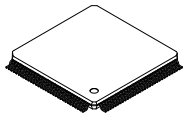
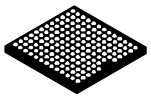
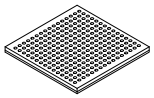


TQFP128 14 x 14/ TQFP128L
CASE 932BA



WLCSP154 5.52 x 5.33
CASE 567LD



LFBGA240 11 x 11
CASE 566EY

ORDERING INFORMATION

See detailed ordering and shipping information on page 53 of this data sheet.

Description

LC823450 is an ultra−low power, 32−bit, 192 kHz high−resolution audio−capable signal processing system−on−chip (SoC). It consists of dual ARM Cortex−M3, 32−bit DSP (LPDSP32) core, hard wired MP3 encoder/decoder, and integrated SRAM. It is also equipped with analog peripheral functionality, such as PLLs, class−D stereo HP amplifier, 6−band equalizer and ADCs/DACs. Our proprietary LPDSP32 supports Noise/Echo cancellation, and playback speed control capability for MP3, WMA, AAC and PCM with VBR. With fine−tuned power management and dedicated hard wired audio blocks, LC823450 provides a significantly longer battery life without compromising audio quality, for voice recorders and wearable audio applications.

This document describes features, basic functions, electrical specifications, characteristics, application diagram and package dimension of this LSI.

Features

- Ultra Low Power Consumption
- Arm® Cortex®−M3 Dual Core
- Proprietary 32−bit DSP Core (LPDSP32)
- Internal Large Scale Size SRAM: 1656 kB (1.5 MB + 120 kB)
- High−Resolution 32−bit & 192 kHz Audio Processing Capability
- Several DSP Codes Available for Audio Functions
- Hard Wired Audio Functions Built−in MP3 Decoder, MP3 Encoder 6 Band Equalizer Synchronous SRC, Asynchronous SRC, etc.
- Analog Blocks Built−in
  System PLL, Audio PLL
  16−bit DAC, Class−D amp, etc.
- USB2.0 Device and USB2.0 Host with a Integrated PHY
  eMMC and SD card I/F
  Serial Flash I/F(Quad) with Cache Memory
  SPI, UART, I^2C, etc.

Typical Applications

- Sound Recorders
- Wearable Audio Players
- Bluetooth Headsets
- Smart Phone Accessories

ABSTRACT

Features

- Cortex−M3 Dual Core, AMBA® (AHB/APB) System
  - Internal SRAM (1.5M-byte)
  - Internal ROM (256k-byte). Boot code, Standard Functions
  - SDRAM Controller (1 * CS)
    64M to 256Mbit SDRAM / Mobile SDRAM
  - External Memory Controller (2 * CS)
    NOR FLASH, SRAM, ROM supported, 8/16 bit I/F
    LCD controller supported
    Internal ROM boot and External memory device boot available
  - DMA Controller (8ch)
  - Interrupt Controller (External 90ch, Internal 82ch)
  - SPI (1ch)
  - Serial Flash I/F (1ch)
    Quad SPI, cache memory (16k-byte, 4way set associative, 128line) function available
    1.8V dedicated power supply
  - UART (3ch)
    UART1: w/flow control (CTS, RTS)
    UART0, UART2: w/o flow control
  - I^2C (2ch) Single Master, Full/Standard
  - GPIO (90ch)
  - Plain Timer w/ Watch Dog Timer (1ch×3)
  - Multiple Timer (2ch×4)
  - 10bit ADC (6ch)
  - SD Card I/F (3ch)
    eSD/eMMC, UHS−I, w/o CPRM
    - SD0: eSD/eMMC boot supported (Internal ROM Boot function) 1.8 V dedicated power supply
    - SD1: Multiplexed w/ Memory Stick I/F
      1.8 V dedicated power supply
    - SD2: 1.8 V dedicated power supply
  - Memory Stick I/F (1ch)
    Multiplexed w/ SD1
  - USB2.0 Host (HS/FS/LS) Controller, Device (HS/FS) Controller. Integrated PHY
    Xtal (XT1) is required for USB function.
    48 MHz for Host, and 12,20,24,48 MHz for device w/o OTG function. Host and Device share an integrated PHY.
  - Real Time Clock
    2 modes below are available
    - General RTC mode: RTC w/o key input
    - KeyInt RTC mode: RTC w/ key input which enables power on function
  - SWD (Serial Wire Debug) is supported as the debug interface.
    SWV (Serial Wire Viewer) is supported as the trace interfaceOnly one of Cortex−M3 Dual Core can be traced.

Availability of features explained here depends on products.

- MP3[1] Hard Wired Encoder/Decoder
  - MP3 MPEG1, MPEG2, MPEG2.5
    - Sampling rate: 8 kHz,11.025 kHz,12 kHz,16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz
    - Bit rate:8 Kbps to 320 Kbps (Decoder−VBR supported)
- LPDSP32 System
  - Internal SRAM (120 kbyte)
  - Internal ROM (220 kbyte)
  - WMA[2] (Microsoft WMA Decoder Profile Level3)
    - Sampling rate: 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz
    - Bit rate: 5 Kbps to 320 Kbps (VBR supported)
  - AAC (MPEG4 LC−AAC)
    - Bit rate: 8 Kbps to 320 Kbps (VBR supported)
  - Variable Speed Control playback
    (0.5 to 4.0 times speed)
    - While WMA and AAC playback, up to 2.0 time speed
    - While PCM playback, up to 4.0 times speed
    - While MP3 playback w/ hard wired decoder, up to 4.0 times speed
  - Noise Canceller, etc.
  - JTAG ICE

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1 MPEG Layer−3 audio coding technology licensed from Fraunhofer IIS and Thomson.
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2 This product contain technology of Microsoft company ownership, and you cannot distribute or use without getting license from Microsoft Licensing company.

- Bluetooth Protocol Stack Available[3]
- Other Audio Functions Available:
  - 6band Equalizer (EQ3)
  - Volume, Mute
  - Level Meter
  - Audio Timer w/ interrupt generation
  - 16/24/32bit 192 kHz PCM I/F (2ch×2). Master/slave, I2S
  - SSRC (Synchronous Sampling Rate Converter) 0.25 to 64 conversion capable
  - ASRC (Asynchronous Sampling Rate Converter) jitter reducing function supporting USB audio class and Bluetooth streaming
  - Beep generator
  - Digital Microphone I/F (2ch×1)
  - 16bit Audio DAC (2ch) w/ Class−D Amplifier for Head Phone (2ch). Need external LC LPF
- Audio Clock Generation
  - Dedicated PLL for audio(PLL2:1 V and PLL3:3 V operation integrated)
  - Selectable PLL reference clock
    XT1 (1 to 50 MHz Main xtal)
    XTRTC (32.768 KHz RTC xtal)
    PCM I/F MCLK0 (/MCLK1), BCK0, BCK1
- Power Supply
  - Typical voltage:
    - LOGIC(Vdd1), XT1(VddXT1), PLL1(AVddPLL1), PLL2(AVddPLL2) = 1.0 V
    - PLL3(AVddPLL3) = 3.3 V
    - RTC(VddRTC) = 1.0 V
    - I/O(Vdd2) = 1.8 V or 3.3 V
    - SD0(VddSD0) = 1.8 V or 3.3 V
    - SD1(VddSD1) = 1.8 V or 3.3 V
    - SD2(VddSD2) = 1.8 V or 3.3 V
    - S−Flash I/F(VddQSPI) = 1.8 V or 3.3 V
    - ADC(AVddADC) = 3.3 V
    - USB PHY1(AVddUSBPHY1, DVddUSBPHY1) = 1.0 V(w/o USB connection) or 1.2 V (w/ USB connection)
    - USB PHY2(AVddUSBPHY2) = 2.8 V (w/o USB connection) or 3.3 V (w/ USB connection)
    - Class−D Amplifier(AVddDAMPL,AVddDAMPR) = 1.2 V

[3] The product name for which Bluetooth Protocol Stack is available is determined. Please contact our representative for license fee for the Stack.

Package Code and Functional Difference

Table 1. FUNCTIONAL DIFFERENCE

Function	Package Code			
	TA	XA, XC	XB, XD	RA, RB
Package	**TQFP128L**	**WLP154**		**LFBGA240**
Cortex−M3 Dual Core	Single	Single	Dual	Dual
SDRAM Controller				Available
External Memory Controller		8bit I/F (LCD I/F, etc.)	8bit I/F (LCD I/F, etc.)	Available
SD2	Available		Available	Available
10bit ADC Conversion Speed	MAX 5 Mhz (Note 2)			MAX 20 MHz (Note 4)
10bit ADC Reference Voltage	VRH = AvddADC VRL = AVssADC (Note 3)			VRH = AVddADC and lower VRL = AVssADC and higher
PCM1(PCM I/F ch1)	BCK1/LRCK1 share pins with other function	Available	Available	Available
MP3 Hard Wired Encoder	Available		Available	Available
16bit Audio DAC, Class−D AMP	Available		Available	Available
PLL2 (1 V PLL) PLL3 (3 V PLL)	Only PLL2	Available	Available	Only PLL2
XTALINFO[1:0] Input	“00” (24 MHz)	Available	Available	Available
RTCMODE Input	“1” (General RTC mode)	Available	Available	Available
KEYINT[2:0] Input		Available	Available	Available
External Interrupt	45 ch	61 ch	61 ch	90 ch
GPIO	45 ch	61 ch	61 ch	90 ch

1. Pin shared for multiple function. Refer to Terminal Functions for details.
2. VR is open inside.
3. VRH = AvddADC, VRL = AVssADC inside.
4. While there is decoupling capacitor. If not, it should be 5 MHz.

Block Diagram

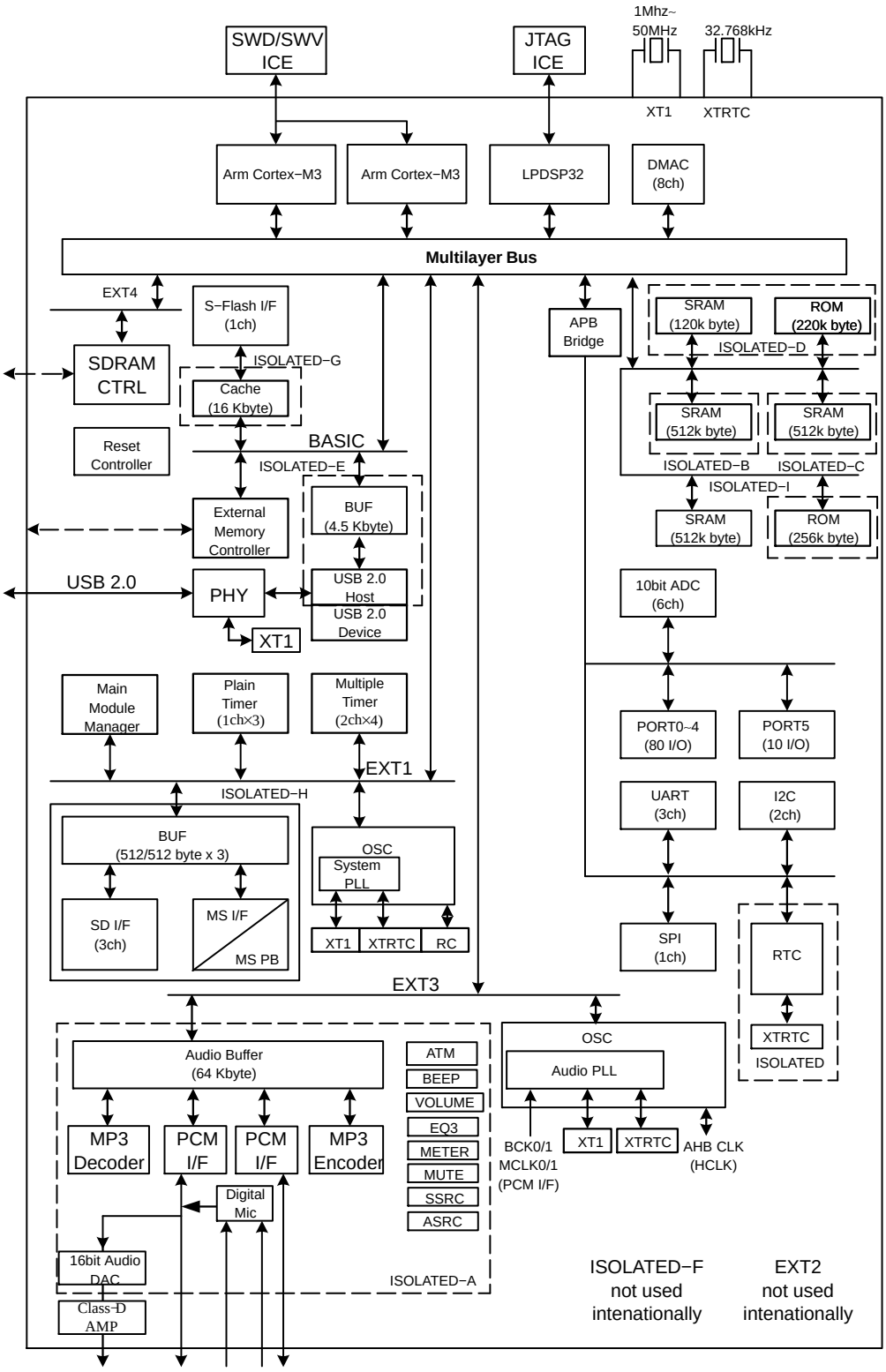


Figure 1. Top

Bus Matrix

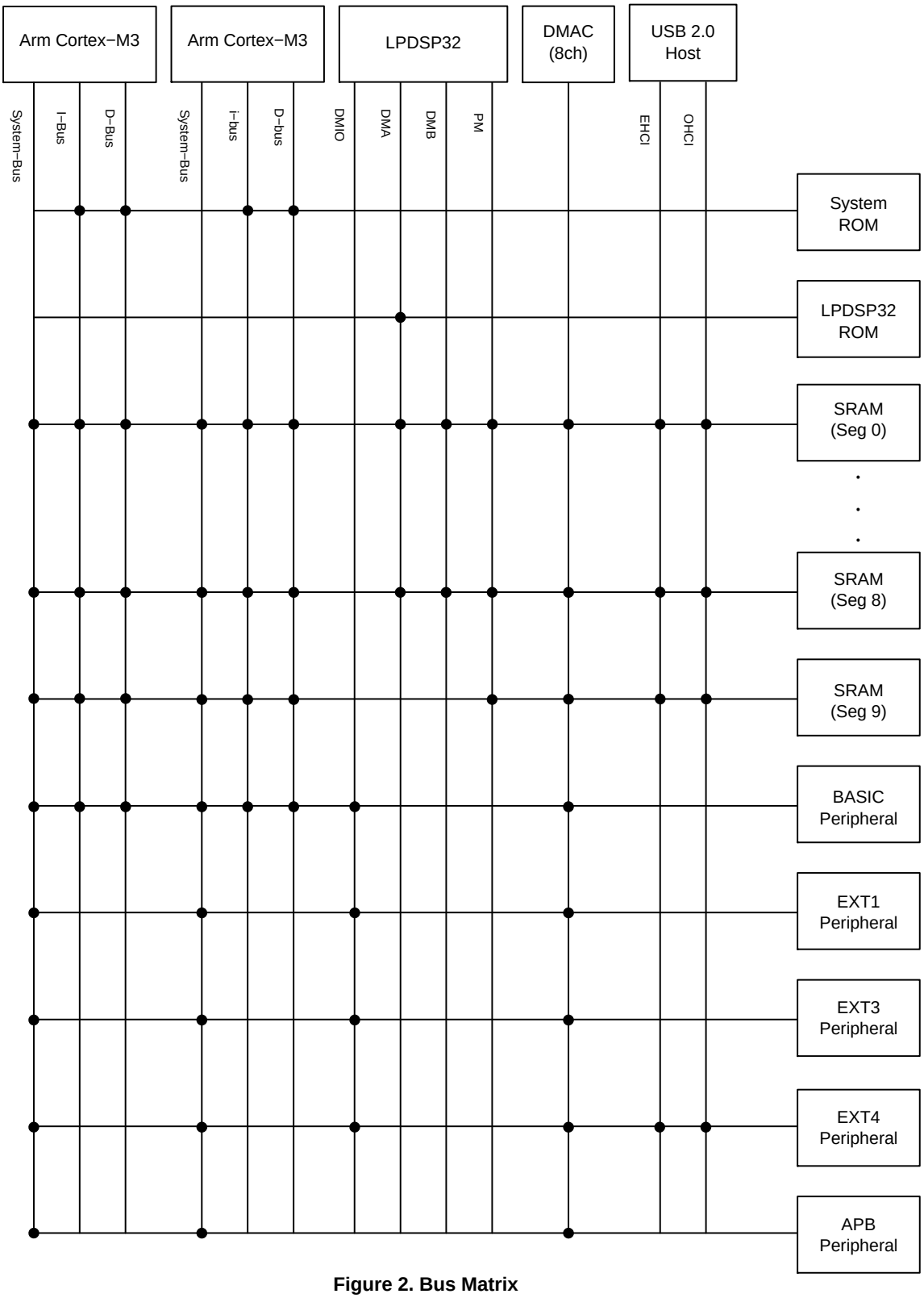


Figure 2. Bus Matrix

Audio

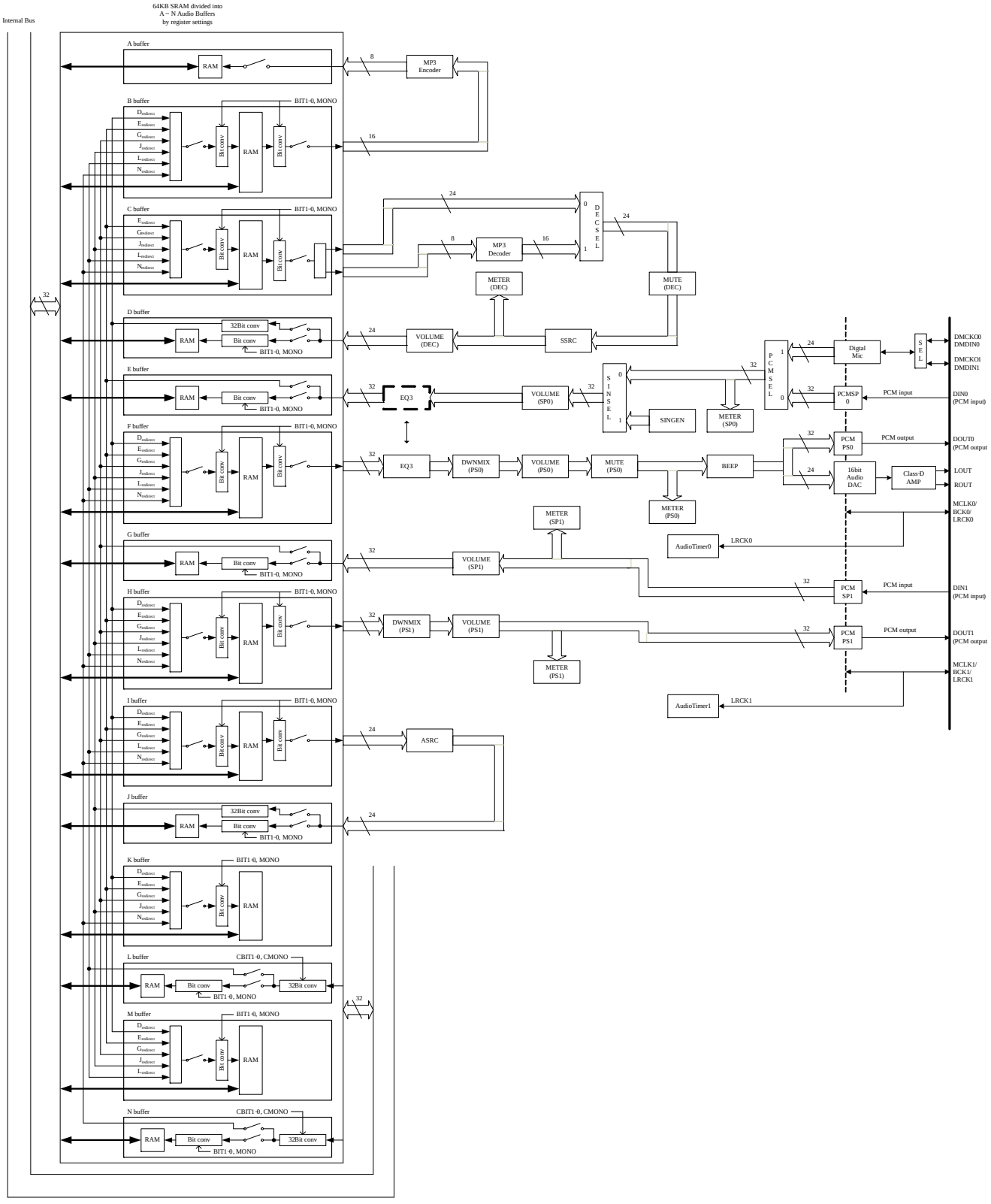


Figure 3. Audio

Clock Hierarchy

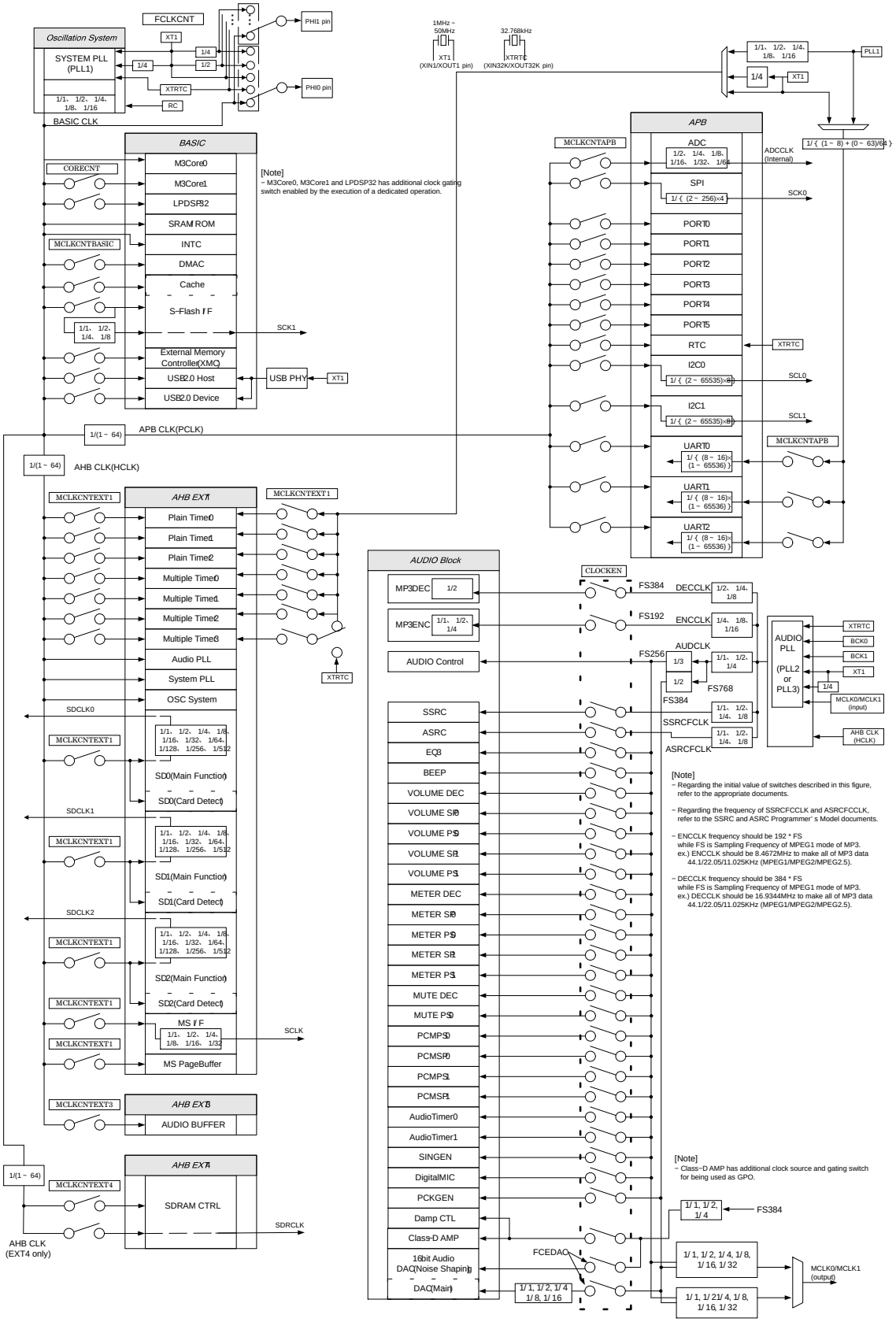


Figure 4. Clock Hierarchy

Memory Map

All Area (Cortex−M3)

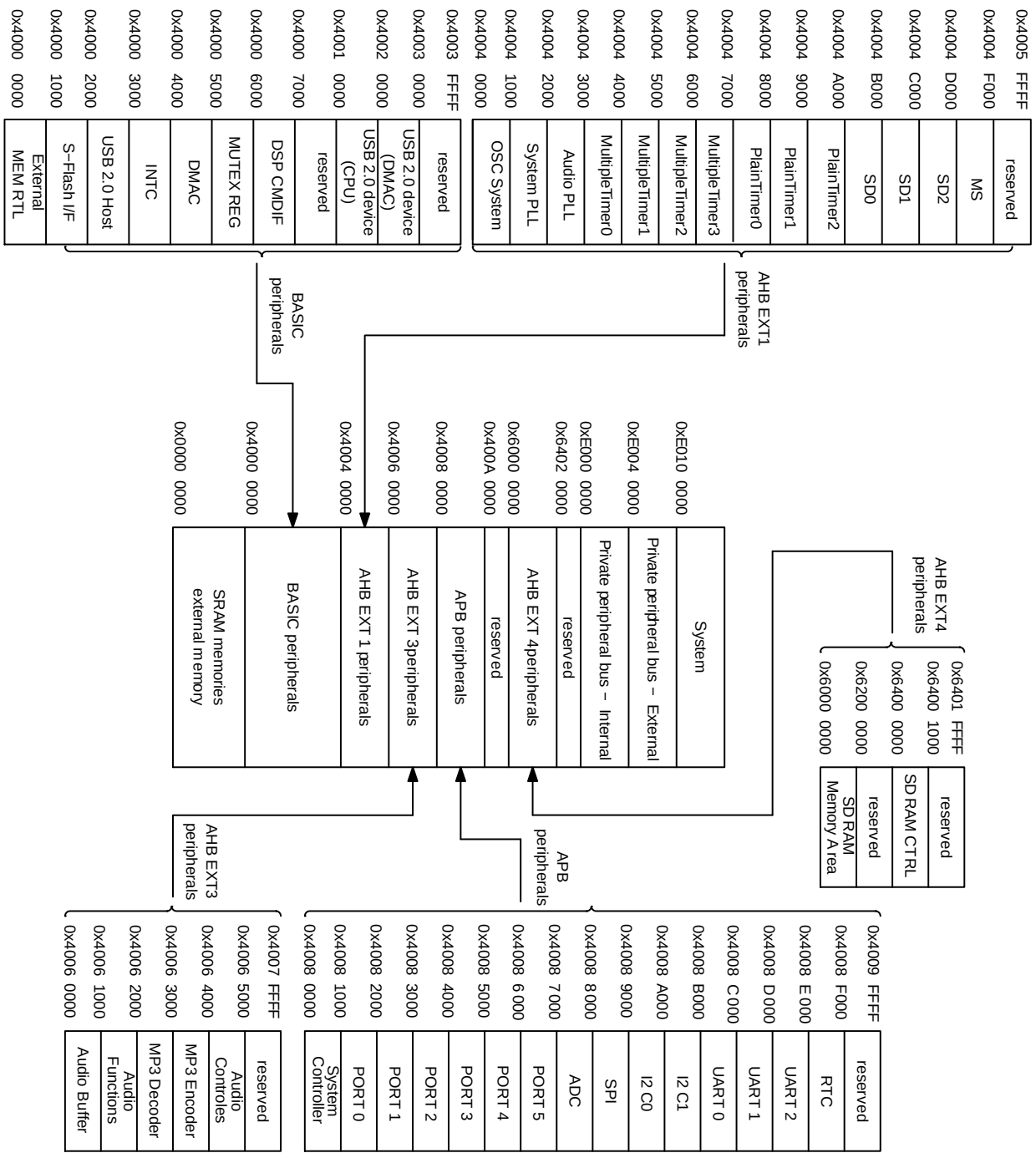


Figure 5. All Area (Cortex−M3)

Code Area (Cortex−M3)

Table 2. CODE AREA (CORTEX−M3) − UNREMAPPED (AFTER RESET)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0x1C00 0000	Reserved									
0x1A00 0000	External Memory 1		○			○				
0x1800 0000	External Memory 0		○			○				
0x0600 0000	Reserved									
0x0500 0000	S−Flash I/F (Memory, Cache)		○			○				
0x0224 0000	Reserved									
0x0220 0000	256 KB Internal ROM		○			○				
0x0219 E000	Reserved									
0x0218 0000	120 KB Internal SRAM (seg 9)		○			○				
0x0217 8000	32 KB Internal SRAM (seg 8)		○			○				
0x0214 0000	224 KB Internal SRAM (seg 7)		○			○				
0x0210 0000	256 KB Internal SRAM (seg 6)		○			○				
0x020C 0000	256 KB Internal SRAM (seg 5)		○			○				
0x020A 0000	128 KB Internal SRAM (seg 4)		○			○				
0x0208 0000	128KB Internal SRAM (seg 3)		○			○				
0x0204 0000	256 KB Internal SRAM (seg 2)		○			○				
0x0202 0000	128 KB Internal SRAM (seg 1)		○			○				
0x0200 0000	128 KB Internal SRAM (seg 0)		○			○				
0x0004 0000	Reserved									
0x0000 0000	256 KB Internal ROM Shadow Area		○			○				

Table 3. CODE AREA (CORTEX−M3) − REMAPPED (REMAP[1:0] = 2'B01)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0x1C00 0000	Reserved									
0x1A00 0000	External Memory 1		○			○				
0x1800 0000	External Memory 0		○			○				
0x0600 0000	Reserved									
0x0500 0000	S−Flash I/F (Memory, Cache)		○			○				
0x0224 0000	Reserved									
0x0220 0000	256 KB Internal ROM		○			○				
0x0219 E000	Reserved									
0x0218 0000	120 KB Internal SRAM (seg 9)		○			○				
0x0217 8000	32 KB Internal SRAM (seg 8)		○			○				
0x0214 0000	224 KB Internal SRAM (seg 7)		○			○				
0x0210 0000	256 KB Internal SRAM (seg 6)		○			○				
0x020C 0000	256 KB Internal SRAM (seg 5)		○			○				
0x020A 0000	128 KB Internal SRAM (seg 4)		○			○				
0x0208 0000	128 KB Internal SRAM (seg 3)		○			○				
0x0204 0000	256 KB Internal SRAM (seg 2)		○			○				
0x0202 0000	128 KB Internal SRAM (seg 1)		○			○				
0x0200 0000	128 KB Internal SRAM (seg 0)		○			○				
0x0002 0000	Reserved									
0x0000 0000	128 KB Internal SRAM (seg 0) Shadow Area		○			○				
0x1C00 0000	Reserved									

Table 3. CODE AREA (CORTEX−M3) − REMAPPED (REMAP[1:0] = 2'B01) (continued)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0x1A00 0000	External Memory 1		○			○				
0x1800 0000	External Memory 0		○			○				
0x0600 0000	Reserved									
0x0500 0000	S−Flash I/F (Memory, Cache)		○			○				
0x0224 0000	Reserved									
0x0220 0000	256 KB Internal ROM		○			○				
0x0219 E000	Reserved									
0x0218 0000	120 KB Internal SRAM (seg 9)		○			○				
0x0217 8000	32 KB Internal SRAM (seg 8)		○			○				
0x0214 0000	224 KB Internal SRAM (seg 7)		○			○				
0x0210 0000	256 KB Internal SRAM (seg 6)		○			○				
0x020C 0000	256 KB Internal SRAM (seg 5)		○			○				
0x020A 0000	128 KB Internal SRAM (seg 4)		○			○				
0x0208 0000	128 KB Internal SRAM (seg 3)		○			○				
0x0204 0000	256 KB Internal SRAM (seg 2)		○			○				
0x0202 0000	128 KB Internal SRAM (seg 1)		○			○				
0x0200 0000	128 KB Internal SRAM (seg 0)		○			○				
0x0000 0000	External Memory 0 Shadow Area		○			○				

SRAM Area (Cortex−M3)

Table 4. SRAM AREA (CORTEX−M3)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0x2600 0000	Reserved									
0x2500 0000	S−Flash I/F (Memory, Cache)	○			○			○		
0x2400 0000	S−Flash I/F (Memory, No Cache)	○			○			○		
0x2019 E000	Reserved									
0x2018 0000	120 KB Internal SRAM (seg 9) Shadow Area	○			○			○		
0x2017 8000	32 KB Internal SRAM (seg 8) Shadow Area	○			○			○		
0x2014 0000	224 KB Internal SRAM (seg 7) Shadow Area	○			○			○		
0x2010 0000	256 KB Internal SRAM (seg 6) Shadow Area	○			○			○		
0x200C 0000	256 KB Internal SRAM (seg 5) Shadow Area	○			○			○		
0x200A 0000	128 KB Internal SRAM (seg 4) Shadow Area	○			○			○		
0x2008 0000	128 KB Internal SRAM (seg 3) Shadow Area	○			○			○		
0x2004 0000	256 KB Internal SRAM (seg 2) Shadow Area	○			○			○		
0x2002 0000	128 KB Internal SRAM (seg 1) Shadow Area	○			○			○		
0x2000 0000	128 KB Internal SRAM (seg 0) Shadow Area	○			○			○		

Other Area (Cortex−M3)

Table 5. OTHER AREA (CORTEX−M3)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0xE010 0000	Reserved									
0xE00F F000	ROM Table	○ (Note 5)			○ (Note 5)					
0xE00F E000	CORE REG	○ (Note 5)			○ (Note 5)					
0xE004 1000	Reserved									
0xE004 0000	TPIU	○ (Note 5)			○ (Note 5)					
0xE000 F000	Reserved									
0xE000 E000	NVIC	○ (Note 5)			○ (Note 5)					
0xE000 3000	Reserved									
0xE000 2000	FPB	○ (Note 5)			○ (Note 5)					
0xE000 1000	DWT	○ (Note 5)			○ (Note 5)					
0xE000 0000	ITM	○ (Note 5)			○ (Note 5)					
0x6400 1000	Reserved									
0x6400 0000	SDRAM CTRL	○			○					
0x6200 0000	Reserved									
0x6000 0000	SDRAM Memory Area	○			○			○		
0x4008 F000	Reserved									
0x4008 E000	RTC	○			○					
0x4008 D000	UART2	○			○			○		
0x4008 C000	UART1	○			○			○		
0x4008 B000	UART0	○			○			○		
0x4008 A000	I2C1	○			○					
0x4008 9000	I2C0	○			○					
0x4008 8000	SPI	○			○			○		
0x4008 7000	ADC	○			○			○		

Table 5. OTHER AREA (CORTEX−M3) (continued)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0x4008 6000	PORT5	○			○					
0x4008 5000	PORT4	○			○					
0x4008 4000	PORT3	○			○					
0x4008 3000	PORT2	○			○					
0x4008 2000	PORT1	○			○					
0x4008 1000	PORT0	○			○					
0x4008 0000	System Controller	○			○					
0x4006 5000	Reserved									
0x4006 4000	Audio Controls	○			○					
0x4006 3000	MP3 Encoder	○			○					
0x4006 2000	MP3 Decoder	○			○					
0x4006 1000	Audio Functions	○			○					
0x4006 0000	Audio Buffer	○			○			○		
0x4004 D000	MS	○			○			○		
0x4004 C000	SD2	○			○			○		
0x4004 B000	SD1	○			○			○		
0x4004 A000	SD0	○			○			○		
0x4004 9000	Plain Timer2	○			○					
0x4004 8000	Plain Timer1	○			○					
0x4004 7000	Plain Timer0	○			○					
0x4004 6000	Multiple Timer3	○			○					
0x4004 5000	Multiple Timer2	○			○					
0x4004 4000	Multiple Timer1	○			○					
0x4004 3000	Multiple Timer0	○			○					
0x4004 2000	Audio PLL	○			○					
0x4004 1000	System PLL	○			○					

Table 5. OTHER AREA (CORTEX−M3) (continued)

Address	Master/Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20HC	
		System − Bus	I−Bus	D−Bus	System − Bus	I−Bus	D−Bus		EHCI	OHCI
0x4004 0000	OSC System	○			○					
0x4003 0000	Reserved									
0x4002 0000	USB2.0 Device(DMAC)	○			○			○		
0x4001 0000	USB2.0 Device(CPU)	○			○			○		
0x4000 7000	Reserved									
0x4000 6000	DSP CMDIF	○			○					
0x4000 5000	MUTEX REG	○			○					
0x4000 4000	DMAC	○			○					
0x4000 3000	INTC	○			○					
0x4000 2000	USB2.0 Host	○			○			○		
0x4000 1000	S−Flash I/F	○			○					
0x4000 0000	External MEM CTL	○			○					

5. Access from internal peripheral bus(AHB/APB).

LPDSP32

Table 6. LPDSP32 − DMA

Address	Master/Slave	LPDSP32
		DMA
0x23 7000	Reserved	
0x20 0000	220 KB LPDSP32 ROM	○
0x18 0000	Reserved	○
0x17 8000	32 KB Internal SRAM (seg 8)	○
0x14 0000	224 KB Internal SRAM (seg 7)	○
0x10 0000	256 KB Internal SRAM (seg 6)	○
0x0C 0000	256 KB Internal SRAM (seg 5)	○
0x0A 0000	128 KB Internal SRAM (seg 4)	○
0x08 0000	128 KB Internal SRAM (seg 3)	○
0x04 0000	256 KB Internal SRAM (seg 2)	○
0x02 0000	128 KB Internal SRAM (seg 1)	○
0x00 0000	128 KB Internal SRAM (seg 0)	○

Table 7. LPDSP32 − DMB

Address	Master/Slave	LPDSP32
		DMB
0x98 0000	reserved	
0x97 8000	32 KB Internal SRAM (seg 8) Shadow Area	○
0x94 0000	224 KB Internal SRAM (seg 7) Shadow Area	○
0x90 0000	256 KB Internal SRAM (seg 6) Shadow Area	○
0x8C 0000	256 KB Internal SRAM (seg 5) Shadow Area	○
0x8A 0000	128 KB Internal SRAM (seg 4) Shadow Area	○
0x88 0000	128 KB Internal SRAM (seg 3) Shadow Area	○
0x84 0000	256 KB Internal SRAM (seg 2) Shadow Area	○
0x82 0000	128 KB Internal SRAM (seg 1) Shadow Area	○
0x80 0000	128 KB Internal SRAM (seg 0) Shadow Area	○

Table 8. LPDSP32 − DMIO

Address	Master/Slave	LPDSP32
		DMIO
0xF0 1000	reserved	
0xF0 0000	SDRAM CTRL	○
0xD0 0000	SDRAM Memory Area	○
0xC6 5000	reserved	
0xC6 4000	Audio Controls	○
0xC6 3000	MP3 Encoder	○
0xC6 2000	MP3 Decoder	○
0xC6 1000	Audio Functions	○
0xC6 0000	Audio Buffer	○
0xC4 A000	Reserved	
0xC4 9000	Plain Timer2	○
0xC4 8000	Plain Timer1	○
0xC4 7000	Plain Timer0	○
0xC4 6000	Multiple Timer3	○
0xC4 5000	Multiple Timer2	○
0xC4 4000	Multiple Timer1	○
0xC4 3000	Multiple Timer0	○
0xC4 2000	Audio PLL	○
0xC4 1000	System PLL	○
0xC4 0000	OSC System	○
0xC0 7000	Reserved	
0xC0 6000	DSP CMDIF	○

Table 8. LPDSP32 − DMIO (continued)

Address	Master/Slave	LPDSP32
		DMIO
0xC0 5000	MUTEX REG	○
0xC0 4000	DMAC	○
0xC0 3000	INTC	○
0xC0 0000	Reserved	

Table 9. LPDSP32 − PM

Address	Master/Slave	LPDSP32
		PM
0x48 3332	Reserved	
0x48 0000	32 KB Internal SRAM (seg 8)	○
0x41 6666	Reserved	
0x40 0000	224 KB Internal SRAM (seg 7)	○
0x39 9998	Reserved	
0x38 0000	256 KB Internal SRAM (seg 6)	○
0x31 9998	Reserved	
0x30 0000	256 KB Internal SRAM (seg 5)	○
0x28 CCCC	Reserved	
0x28 0000	128 KB Internal SRAM (seg 4)	○
0x20 CCCC	Reserved	
0x20 0000	128 KB Internal SRAM (seg 3)	○
0x19 9998	Reserved	
0x18 0000	256 KB Internal SRAM (seg 2)	○
0x10 CCCC	Reserved	
0x10 0000	128 KB Internal SRAM (seg 1)	○
0x08 CCCC	Reserved	
0x08 0000	128 KB Internal SRAM (seg 0)	○
0x00 C000	Reserved	
0x00 0000	120 KB Internal SRAM (seg 9)	○

TERMINAL FUNCTIONS

TA: Package Code = “TA”
XA: Package Code = “XA”
XB: Package Code = “XB”
XC: Package Code = “XC”
XD: Package Code = “XD”
RA: Package Code = “RA”
RB: Package Code = “RB”

Table 10. TERMINAL FUNCTIONS

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
JTAG/SWD								
TDO	−	O	JTAG test data outputSD	VddSD1	○	○	○	○
SDWP1	Pos	I	SD I/F Ch1 write protect		○	○	○	○
INS	Neg	I	Memory Stick INS		○	○	○	○
GPIO21	−	B	GPIO		○	○	○	○
EXTINT21	−	I	External Interrupt 2−bit1		○	○	○	○
TDI	−	I	JTAG test data input	VddSD1	○	○	○	○
SDCD1	Neg	I	SD I/F Ch2 write protect		○	○	○	○
SWO	−	O	Serial wire view data		○	○	○	○
GPIO20	−	B	GPIO		○	○	○	○
EXTINT20	−	I	External Interrupt 2−bit0		○	○	○	○
TMS	−	I	JTAG test data select	VddSD2	○	○	○	○
SDWP2	Pos	I	SD I/F Ch2 write protect		○	(Note 6)	○	○
GPIO28	−	B	GPIO		○	○	○	○
EXTINT28	−	I	External Interrupt 2−bit8		○	○	○	○
TCK	Pos	I	JTAG test clock	VddSD2	○	○	○	○
SDCD2	Neg	I	SD I/F Ch2 detect		○	(Note 6)	○	○
GPIO29	−	B	GPIO		○	○	○	○
EXTINT29	−	I	External Interrupt 2−bit9		○	○	○	○
SWDCLK	Pos	I	Serial wire clock	Vdd2	○	○	○	○
DMCKO1	−	O	Digital MicCh1Clock Output		○	○	○	○
GPIO58	−	B	GPIO		○	○	○	○
EXTINT58	−	I	External Interrupt 5−bit8		○	○	○	○
SWDIO	−	B	Serial wire Data	Vdd2	○	○	○	○
DMDIN1	−	I	Digital MicCh1 Data Input		○	○	○	○
GPIO59	−	B	GPIO		○	○	○	○
EXTINT59	−	I	External Interrupt 5−bit9		○	○	○	○
Sum					6	6	6	6
RTC								
XIN32K	Pos	I	32.768 kHz XTAL Input (XTRTC)	VddRTC	○	○	○	○
XOUT32K	−	O	32.768 kHz XTAL Output (XTRTC)		○	○	○	○
VDET	Neg	I	RTC power detect Input		○	○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
RTC								
RTCINT	Neg	O	RTC Interrupt Output (Normal:HiZ, Interrupt enabled: Low Output)	VddRTC	○	○	○	○
BACKUPB	Neg	I	RTC backup mode input		○	○	○	○
KEYINT[2:0]	−	I	RTC KEY input can be used when KeyInt RTC mode	VddRTC		○	○	○
RTCMODE	−	I	RTC mode input (Note 7) Set General RTC or KeyInt RTC mode RTCMODE = G “0”: KeyInt RTC mode G “1”: General RTC mode Bonding internally for “TA” product	VddRTC		○	○	○
VddRTC	−	P	RTC power supply	−	○	○	○	○
VssRTC	−	P	RTC ground	−	○	○	○	○
Sum					7	11	11	11
EXTERNAL INTERRUPT/GPIO								
SDRADDR12	−	O	SDRAM address	Vdd2				○
GPIO2A	−	B	GPIO					○
EXTINT2A	−	I	External Interrupt 2−bit10					○
SCL1	−	O	I^2C ch1 Clock (open drain output)	Vdd2	○	○	○	○
GPIO2B	−	B	GPIO		○	○	○	○
EXTINT2B	−	I	External Interrupt 2−bit11		○	○	○	○
SDA1	−	B	I^2C ch1 Clock (open drain output)	Vdd2	○	○	○	○
GPIO2C	−	B	GPIO		○	○	○	○
EXTINT2C	−	I	External Interrupt 2−bit12		○	○	○	○
SDRADDR11	−	O	SDRAM address	Vdd2				○
DMCKO0	−	O	Digital Mic Clock Ch0 Output		○	○	○	○
GPIO2D	−	B	GPIO		○	○	○	○
EXTINT2D	−	I	External Interrupt 2−bit13		○	○	○	○
EXTINT2E	−	I	External Interrupt 2−bit14	Vdd2	○	○	○	○
GPIO2E	−	B	GPIO *While Internal ROM boot, this terminal is used as boot monitor signal.		○	○	○	○
EXTINT2F	−	I	External Interrupt 2−bit14	Vdd2	○	○	○	○
GPIO2F	−	B	GPIO *While Internal ROM boot, this terminal is used as boot monitor signal.		○	○	○	○
Sum					5	5	5	6
SPI (SERIAL I/F CH0)/S−FLASH I/F (SERIAL I/F CH1)								
SCK0	Neg	B	Serial I/F Ch0 Clock	Vdd2	○	○	○	○
GPIO1D	−	B	GPIO		○	○	○	○
EXTINT1D	−	I	External Interrupt 1−bit13		○	○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
SPI (SERIAL I/F CH0)/S−FLASH I/F (SERIAL I/F CH1)								
SDI0	−	I	Serial I/F Ch0 Data Input	Vdd2	○	○	○	○
GPIO1E	−	B	GPIO		○	○	○	○
EXTINT1E	−	I	External Interrupt 1−bit14		○	○	○	○
SDO0	−	O	Serial I/F Ch0 Data Output	Vdd2	○	○	○	○
GPIO1F	−	B	GPIO		○	○	○	○
EXTINT1F	−	I	External Interrupt 1−bit15		○	○	○	○
SCK1	Neg	O	Serial I/F Ch1 Clock (QSPI Clock)	VddQSPI	○	○	○	○
GPIO0D	−	B	GPIO		○	○	○	○
EXTINT0D	−	I	External Interrupt 0 bit13		○	○	○	○
SDI1(QIO0)	−	O(B)	Serial I/F Ch1 Data Input (QSPI Data 1)	VddQSPI	○	○	○	○
GPIO0E	−	B	GPIO		○	○	○	○
EXTINT0E	−	I	External Interrupt 0−bit14		○	○	○	○
SDO1(QIO1)	−	I(B)	Serial I/F Ch1 Data Output (QSPI Data 1)	VddQSPI	○	○	○	○
GPIO0F	−	B	GPIO		○	○	○	○
EXTINT0F	−	I	External Interrupt 0−bit15		○	○	○	○
SWP1(QIO2)	Neg	O(B)	Serial I/F Ch1 write protect (QSPI Data 2)	VddQSPI	○	○	○	○
GPIO11	−	B	GPIO		○	○	○	○
EXTINT11	−	I	External Interrupt 1−bit1		○	○	○	○
SHOLD1(QIO3)	Neg	O(B)	Serial I/F Ch1 hold (QSPI Data 3)	VddQSPI	○	○	○	○
GPIO12	−	B	GPIO		○	○	○	○
EXTINT12	−	I	External Interrupt 1−bit2		○	○	○	○
Sum					8	8	8	8
I^2C								
SCL0	−	O	I^2C ch0 Clock (open drain output)	Vdd2	○	○	○	○
GPIO07	−	B	GPIO		○	○	○	○
EXTINT07	−	I	External Interrupt 0−bit7		○	○	○	○
SDA0	−	B	I^2C ch0 Data (open drain output)	Vdd2	○	○	○	○
GPIO08	−	B	GPIO		○	○	○	○
EXTINT08	−	I	External Interrupt 0−bit8		○	○	○	○
Sum					2	2	2	2
UART								
TXD1	−	O	UART Ch1 transmit Data	VddSD2	○	○	○	○
SDAT20	−	B	SD I/F Ch2 Data 0		○	(Note 6)	○	○
GPIO04	−	B	GPIO		○	○	○	○
EXTINT04	−	I	External Interrupt 0−bit4		○	○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
UART								
RXD1	−	I	UART Ch1 receive Data	VddSD2	○	○	○	○
SDAT21	−	B	SD I/F Ch2 Data 1		○	(Note 6)	○	○
GPIO05	−	B	GPIO		○	○	○	○
EXTINT05	−	I	External Interrupt 0−bit5		○	○	○	○
CTS1	Neg	I	UART Ch1 clear to send	VddSD2	○	○	○	○
SDAT22	−	B	SD I/F Ch2 Data 2		○	(Note 6)	○	○
RXD0	−	I	UART Ch0 receive Data		○	○	○	○
GPIO56	−	B	GPIO		○	○	○	○
EXTINT56	−	I	External Interrupt 5−bit6		○	○	○	○
RTS1	Neg	O	UART Ch1 request to send	VddSD2	○	○	○	○
SDAT23	−	B	SD I/F Ch2 Data 3		○	(Note 6)	○	○
TXD0	−	O	UART Ch0 transmit Data		○	○	○	○
GPIO57	−	B	GPIO		○	○	○	○
EXTINT57	−	I	External Interrupt 5−bit7		○	○	○	○
TXD2	−	O	UART Ch2 transmit Data	VddQSPI	○	○	○	○
TIOCA10	−	B	MTM1 Ch0A − target signal of pulse−length−reader function − output of sentinel−inform−function − output of PWM output		○	○	○	○
GPIO0B	−	B	GPIO		○	○	○	○
EXTINT0B	−	I	External Interrupt 0−bit11		○	○	○	○
RXD2	−	I	UART ch2 receive Data	VddQSPI	○	○	○	○
TIOCA11	−	B	MTM1 Ch1A − target signal of pulse−length−reader function − output of sentinel−inform−function − output of PWM output		○	○	○	○
GPIO0C	−	B	GPIO		○	○	○	○
EXTINT0C	−	I	External Interrupt 0−bit12		○	○	○	○
Sum					6	6	6	6
TIMER								
TIOCA00	−	B	MTM0 Ch0A − target signal of pulse−length−reader function − output of sentinel−inform−function − output of PWM output	VddSD2	○	○	○	○
SDCLK2	−	O	SD I/F Ch2 Clock Output		○	(Note 6)	○	○
PHI0	−	O	System Clock Output 0		○	○	○	○
GPIO09	−	B	GPIO		○	○	○	○
EXTINT09	−	I	External Interrupt 0−bit9		○	○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
TIMER								
TIOCA01	−	B	MTM0 Ch1A − target signal of pulse−length−reader function − output of sentinel−inform−function − output of PWM output	VddSD2	○	○	○	○
SDCMD2	−	B	SD I/F Ch2 command line		○	(Note 6)	○	○
PHI1	−	O	System Clock Output 1		○	○	○	○
GPIO0A	−	B	GPIO		○	○	○	○
EXTINT0A	−	I	External Interrupt 0−bit10		○	○	○	○
TIOCB00	−	B	MTM0 Ch0B − target signal of pulse−length−reader function − output of sentinel−inform−function	Vdd2	○	○	○	○
DIN1	−	I	PCM1 Data Input		○	○	○	○
DMDIN0	−	I	Digital Mic Data Ch0 Input		○	○	○	○
GPIO02	−	B	GPIO		○	○	○	○
EXTINT02	−	I	External Interrupt 0−bit2		○	○	○	○
TIOCB01	−	B	MTM0 Ch1B − target signal of pulse−length−reader function − output of sentinel−inform−function	VddQSPI	○	○	○	○
DMCKO0	−	O	Digital Mic Clock Ch0 Output		○	○	○	○
QSCS	Neg	O	Serial I/Fch1 QSPI chip select *While Serial Flash Boot, this is used as chip select of Serial Flash		○	○	○	○
GPIO03	−	B	GPIO		○	○	○	○
EXTINT03	−	I	External Interrupt 0−bit3		○	○	○	○
TCLKA0	−	I	MTM0 external Clock A	Vdd2	○	○	○	○
BCK1	−	B	PCM1 bit Clock		○	○	○	○
GPIO00	−	B	GPIO		○	○	○	○
EXTINT00	−	I	External Interrupt 0−bit0		○	○	○	○
TCLKB0	−	I	MTM0 external Clock B	Vdd2	○	○	○	○
LRCK1	−	B	PCM1 LR Clock		○	○	○	○
GPIO01	−	B	GPIO		○	○	○	○
EXTINT01	−	I	External Interrupt 0−bit1		○	○	○	○
Sum					6	6	6	6
PCM I/F								
MCLK0	Pos	B	PCM0 master Clock	Vdd2	○	○	○	○
MCLK1	Pos	B	PCM1 master Clock		○	○	○	○
GPIO18	−	B	GPIO		○	○	○	○
EXTINT18	−	I	External Interrupt 1−bit8		○	○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
PCM I/F								
BCK0	−	B	PCM0 bit Clock	Vdd2	○	○	○	○
DMCKO1	−	O	Digital Mic Ch1 Clock Output		○	○	○	○
GPIO19	−	B	GPIO		○	○	○	○
EXTINT19	−	I	External Interrupt 1−bit9		○	○	○	○
LRCK0	−	B	PCM0 LR Clock	Vdd2	○	○	○	○
DMDIN1	−	I	Digital Mic ch1 Data Input		○	○	○	○
GPIO1A	−	B	GPIO		○	○	○	○
EXTINT1A	−	I	External Interrupt 1−bit10		○	○	○	○
DIN0	−	I	PCM0 Data Input	Vdd2	○	○	○	○
DMDIN0	−	I	Digital Mic Ch0 Data Input		○	○	○	○
GPIO1B	−	B	GPIO		○	○	○	○
EXTINT1B	−	I	External Interrupt 1−bit11		○	○	○	○
DOUT0	−	O	PCM0 Data Output	Vdd2	○	○	○	○
DMCKO0	−	O	Digital Mic Ch0 Data Output		○	○	○	○
GPIO1C	−	B	GPIO		○	○	○	○
EXTINT1C	−	I	External Interrupt 1−bit12		○	○	○	○
BCK1	−	B	PCM1 bit Clock	Vdd2		○	○	○
GPIO13	−	B	GPIO			○	○	○
EXTINT13	−	I	External Interrupt 1−bit3			○	○	○
LRCK1	−	B	PCM1 LR Clock	Vdd2		○	○	○
GPIO14	−	B	GPIO			○	○	○
EXTINT14	−	I	External Interrupt 1−bit4			○	○	○
DOUT1	−	O	PCM1 Data Output	Vdd2	○	○	○	○
GPIO15	−	B	GPIO		○	○	○	○
EXTINT15	−	I	External Interrupt 1−bit5		○	○	○	○
Sum					6	8	8	8
SD IF/MS IF								
SDCLK0	−	O	SD I/F Ch0 Clock Output	VddSD0	○	○	○	○
SDCMD0	−	B	SD I/F Ch0 command line		○	○	○	○
SDAT0[3:0]	−	B	SD I/F Ch0 Data		○	○	○	○
SDCLK1	−	O	SD I/F Ch1 Clock Output	VddSD1	○	○	○	○
SCLK	−	O	Memory Stick Clock Output		○	○	○	○
GPIO22	−	B	GPIO		○	○	○	○
EXTINT22	−	I	External Interrupt 2−bit2		○	○	○	○
SDCMD1	−	B	SD I/F Ch1 command line	VddSD1	○	○	○	○
BS	−	O	Memory Stick BS		○	○	○	○
GPIO23	−	B	GPIO		○	○	○	○
EXTINT23	−	I	External Interrupt 2−bit3		○	○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
SD IF/MS IF								
SDAT1[3:0]	−	B	SD I/F Ch1 Data	VddSD1	○	○	○	○
DATA[3:0]	−	B	Memory Stick Data		○	○	○	○
GPIO2[7:4]	−	B	GPIO		○	○	○	○
EXTINT2[7:4]	−	I	External Interrupt 2−bit7 to bit4		○	○	○	○
Sum					12	12	12	12
SDRAM I/F								
SDRCLK	Neg	O	SDRAM Clock Output	Vdd2				○
SDRCKE	Pos	O	SDRAM Clock enable Output					○
SDRCS	Neg	O	SDRAM chip select Output					○
SDRWE	Neg	O	SDRAM write enable Output	Vdd2				○
SDRCAS	Neg	O	SDRAM CAS Output					○
SDRRAS	Neg	O	SDRAM RAS Output					○
SDRDQM[1:0]	Pos	O	SDRAM Data mask byte lane select					○
SDRADDR[10:0]	−	O	SDRAM address (Note 8)	Vdd2				○
SDRBA[1:0]	−	O	SDRAM bank select					○
SDRDATA[15:0]	−	B	SDRAM Data					○
Sum					0	0	0	37
EXTERNAL MEMORY I/F								
NCS0	Neg	O	Chip select0	Vdd2		○	○	○
GPIO06	−	B	GPIO			○	○	○
EXTINT06	−	I	External Interrupt 0−bit6			○	○	○
NCS1	Neg	O	Chip select1	Vdd2		○	○	○
RXD0	−	I	UART Ch0 receive Data			○	○	○
GPIO10	−	B	GPIO			○	○	○
EXTINT10	−	I	External Interrupt 1−bit0			○	○	○
NRD	Neg	O	Read enable	Vdd2		○	○	○
GPIO17	−	B	GPIO			○	○	○
EXTINT17	−	I	External Interrupt 1−bit7			○	○	○
NWRENWRL	Neg	O	Write enable, write enable low	Vdd2		○	○	○
GPIO30	−	B	GPIO			○	○	○
EXTINT30	−	I	External Interrupt 3−bit0			○	○	○
NHBNWRH	−	O	High byte select, write enable high	Vdd2		○	○	○
TXD0	−	O	UART Ch0 transmit Data			○	○	○
GPIO31	−	B	GPIO			○	○	○
EXTINT31	−	I	External Interrupt 3−bit1			○	○	○
NLBEXA0	−	O	Low byte select, address0	Vdd2		○	○	○
GPIO16	−	B	GPIO			○	○	○
EXTINT16	−	I	External Interrupt 1−bit6			○	○	○

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
EXTERNAL MEMORY I/F								
EXA[20:15]	−	O	Address	Vdd2				○
GPIO4[5:0]	−	B	GPIO					○
EXTINT4[5:0]	−	I	External Interrupt 4−bit5 to bit0					○
EXA[14:9]	−	O	Address	Vdd2				○
GPIO3[F:A]	−	B	GPIO					○
EXTINT3[F:A]	−	I	External Interrupt 3−bit15 to bit10					○
EXA[8:1]	−	O	Address	Vdd2				○
GPIO3[9:2]	−	B	GPIO					○
EXTINT3[9:2]	−	I	External Interrupt 3−bit9 to bit2					○
EXD[7:0]	−	B	Data	Vdd2		○	○	○
GPIO4[D:6]	−	B	GPIO			○	○	○
EXTINT4[D:6]	−	I	External Interrupt 4−bit13 to bit6			○	○	○
EXD[15:8]	−	B	Data	Vdd2				○
GPIO5[5:0] GPIO4[F:E]	−	B	GPIO					○
EXTINT5[5:0] EXTINT4[F:E]	−	I	External Interrupt 5−bit5 to bit0, External Interrupt 4−bit15 to bit14					○
Sum					0	14	14	42
Xtal, PLL								
XIN1	−	I	XTAL input (XT1)	VddXT1	○	○	○	○
XOUT1	−	O	XTAL output (XT1)	VddXT1	○	○	○	○
VddXT1	−	P	XTAL power supply (XT1)	−	○	○	○	○
VssXT1	−	P	XTAL ground (XT1)	−	○	○	○	○
XTALINFO[1:0]	−	B	XTAL frequency input (Note 9) XTALINFO[1:0] = • “00”: 24 MHz • “01”: 12 MHz • “10”: 20 MHz • “11”: 48 MHz Used for determining clock frequency setting while internal ROM boot. Bonding internally for “TA” product	Vdd2		○	○	○
VCNT1	−	O	PLL1 VCO control	AvddPLL1	○	○	○	○
AvddPLL1	−	P	PLL1 analog power supply	−	○	○	○	○
AvssPLL1	−	P	PLL1 analog ground	−	○	○	○	○
VCNT2	−	O	PLL2 VCO control	AvddPLL2	○ (Note 10)	○	○	○ (Note 10)
AvddPLL2	−	P	PLL2 analog power supply	−	○ (Note 10)	○	○	○ (Note 10)
VCNT3	−	O	PLL3 VCO control	AvddPLL3	○ (Note 11)	○	○	○ (Note 11)

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name / Multiplexed Function	Polarity	Direction	Function	IO POWER	Available (○) TA	XA,XC	XB,XD	RA, RB
Xtal, PLL								
AvddPLL3	−	P	PLL3 analog power supply	−	○ (Note 11)	○	○	○ (Note 11)
AvssPLL2	−	P	PLL2/3 analog ground (Note 12)	−	○	○	○	○
Sum					10	14	14	12
USB−PHY								
USBDP	−	B	USB D+	AVddUSBPHY2 or AVddUSBPHY1	○	○	○	○
USBDM	−	B	USB D−	AVddUSBPHY2 or AVddUSBPHY1	○	○	○	○
USBEXT12	−	O	USB−PHY reference resister	AVddUSBPHY2	○	○	○	○
AvddUSBPHY1	−	P	USB−PHY 1.0V analog power supply	−	○ 2	○ 2	○ 2	○ 2
DVddUSBPHY1	−	P	USB−PHY 1.0V digital power supply. Connected to AVddUSBPHY1 internally in case of no DVddUSBPHY1 port available	−				○ 2
AvddUSBPHY2	−	P	USB−PHY 3.3V analog power supply	−	○ 2	○ 2	○ 2	○ 2
AvddUSBPHY	−	P	USB−PHY analog ground	−	○ 4	○ 4	○ 4	○ 4
Sum					11	11	11	13
10BIT ADC								
AN[5:0]	−	I	ADC Input	AVddADC	○	○	○	○
VRH	−	I	ADC High reference	AVddADC				○
VRL	−	I	ADC Low reference	AVddADC				○
VR	−	O	ADC reference voltage	AVddADC				○
AVddADC	−	P	ADC analog power	−	○	○	○	○
AVssADC	−	P	ADC analog ground	−	○	○	○	○
Sum					8	8	8	11
CLASS−D AMP								
LOUT	−	O	Lch Class D AMP Output	Avdd−DAMPL	○		○	○
GPLOUT	−	O	Genereal purpose Output (GPO)		○	○	○	○
ROUT	−	O	Rch Class D AMP Output	Avdd−DAMPR	○		○	○
GPROUT	−	O	Genereal purpose Output (GPO)		○	○	○	○
AVddDAMPL	−	P	Lch Class D AMP analog power supply	−	○	○	○	○
AVddDAMPR	−	P	Rch Class D AMP analog power supply	−	○	○	○	○
AVssDAMPL	−	P	Lch Class D AMP analog power supply	−	○	○	○	○
AVssDAMPR	−	P	Rch Class D AMP analog power supply	−	○	○	○	○
Sum					6	6	6	6

Table 10. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)			
Multiplexed Function					TA	XA,XC	XB,XD	RA, RB
OTHER, POWER								
BMODE[1:0]	−	B	Bootmodeselect	Vdd2	○	○	○	○
TEST	Pos	I	Test mode (normally connect to ground)	Vdd2	○	○	○	○
NRES	Neg	I	LSI reset Input	Vdd2	○	○	○	○
Vdd1	−	P	Digital core power	−	○ 7	○ 7	○ 7	○ 8
Vdd2	−	P	Digital IO power	−	○ 8	○ 8	○ 8	○ 15
VddSD0	−	P	Digital IO power (SDI/F Ch0)	−	○	○	○	○
VddSD1	−	P	Digital IO power (SD(MS)I/F Ch1)	−	○	○	○	○
VddSD2	−	P	Digital IO power (SDI/F Ch2)	−	○	○	○	○
VddQSPI	−	P	Digital IO power (QSPI)	−	○ 12	○ 14	○ 14	○ 23
Sum					35	37	37	54
All Sum					128	154	154	240

6. This function is not available
7. Set according to the General RTC mode or KeyInt RTC mode. Bonding internally for “TA” product as described on Page 7.
8. SDRAM address bit is 13bit including SDRADDR [12:11].
9. Set according to the frequency of XT1 (12/20/24/48 MHz).
   Bonding internally for “TA’’ product as described on Page 5.
10. Audio clock is generated by one of PLL2 (1 V) or PLL3 (3 V).
    One of PLL2 or PLL3 is available for “TA”, “RA” and “RB” products. Please refer to Page 5 for more information.
    Both of PLL2 and PLL3 are available for “XA”,“XB”, “XC” and “XD” products.
11. Audio clock is generated by one of PLL2 (1 V) or PLL3 (3 V).
    One of PLL2 or PLL3 is available for “TA”, “RA” and “RB” products. Please refer to Page 5 for more information.
    Both of PLL2 and PLL3 are available for “XA”,“XB”, “XC” and “XD” products.
12. Analog ground is shared by PLL2 and PLL3.
13. Unused Input terminals and input state terminals of bidirectional should be set Pull−up/Down resister ON or connect to digital power supply or ground (don’t let open).

Boot Mode

Boot modes available depend on BMODE[1:0] port status.

Table 11. BOOT MODE

IPL Mode	BMODE1	BMODE0	Explanation
Physical Boot USB	PD 470 kΩ	PD 470 kΩ	Internal ROM boot(eMMC Physical Boot with USB download – SD card I/F Ch0 + USB Device + EXTINT2E + EXTINT2F)
			By using Boot operation mode of eMMC, load IPL2(program) from eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through USB.
Physical Boot SD	PD 470 kΩ	PU 470 kΩ	Internal ROM boot (eMMC Physical Boot with SD Ch1 download – SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2E + EXTINT2F)
			By using Boot operation mode of eMMC, load IPL2(program) from eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through SD1.
User Area Boot USB	PD 1 kΩ	PU or PD 470 kΩ	Internal ROM boot(User Area Boot with USB download – SD card I/F Ch0 + USB Device + EXTINT2E + EXTINT2F)
			Load IPL2(program) from user area of eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through USB.
User Area Boot SD	PU 470 kΩ	PD 1 kΩ	Internal ROM boot(User Area Boot with SD Ch1 download – SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2E + EXTINT2F)
			Load IPL2(program) from user area of eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through SD1.
SPI Boot USB	PU 470 kΩ	PU 470 kΩ	Internal ROM boot(external Serial Flash SPI Boot with USB down-load – S−Flash I/F + USB Device + EXTINT2E + EXTINT2F + TI-OCB01)
			Load IPL2(program) from Serial Flash connected to S−Flash I/F to internal SRAM and jump to IPL2. IPL2 is written through USB.
SPI Boot SD	PD 470 kΩ	PU 1 kΩ	Internal ROM boot(external Serial Flash SPI Boot with SD Ch1 download − S−Flash I/F + SD card I/F Ch1 + EXTINT2E + EXTINT2F + TIOCB01)
			Load IPL2 (program) from Serial Flash connected to S−Flash I/F to internal SRAM and jump to IPL2. IPL2 is written through SD1.
QSPI Boot USB	PU 1 kΩ	PU 470 kΩ	Internal ROM boot (external Serial Flash QSPI Boot with USB download – S−Flash I/F(QSPI) + USB Device + EXTINT2E + EXTINT2F + TIOCB01)
			Fetch IPL2 (program) from Serial Flash connected to S−Flash I/F. IPL2 is written by using DO command directly through USB.
QSPI Boot SD	PU 1 kΩ	PD 470 kΩ	Internal ROM boot (external Serial Flash QSPI Boot with SD Ch1 download – S−Flash I/F(QSPI) + SD card I/F Ch1 + EXTINT2E + EXTINT2F + TIOCB01)
			Fetch IPL2 (program) from Serial Flash connected to S−Flash I/F. IPL2 is written through SD1.
User Area Delete	PD 1 kΩ	PU 1 kΩ	Internal ROM boot (User Area IPL2 delete – SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			After deleting IPL2 by using this mode, IPL2 can be written again while User Area Boot mode.

Table 11. BOOT MODE (continued)

IPL Mode	BMODE1	BMODE0	Explanation
Partition Delete	PD 470 kΩ	PD 1 kΩ	Internal ROM boot (Partition Area IPL2 delete – SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			After deleting IPL2 by using this mode, IPL2 can be written again while eMMC Physical Boot mode.
SPI All Erase	PU 470 kΩ	PU 1 kΩ	Internal ROM boot(external Serial Flash SPI all area delete – S−Flash I/F + EXTINT2E + EXTINT2F + TIOCB01)
			Delete all content of Serial Flash. This mode should be used in case of SPI mode operation of Serial Flash
SDCH0 All Erase	PD 1 kΩ	PD 1 kΩ	Internal ROM boot(all area delete – SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			Delete all content of eMMC including Partition area. Take a lot of time to delete. Trim also processed in case of eMMC supporting Trim function.
QSPI All Erase	PU 1 kΩ	PD 1 kΩ	Internal ROM boot(external Serial Flash QSPI all area delete – S−Flash I/F(QSPI) + EXTINT2E + EXTINT2F + TIOCB01)
			Delete all content of Serial Flash. This mode should be used in case of QSPI fetch mode operation of Serial Flash
External ROM Boot	PU 470 kΩ	PD 470 kΩ	External memory boot(External−0)
			Fetch from external memory(External0) connected to XMC(external memory controller)
Hi−z	PU 1 kΩ	PU 1 kΩ	External I/F ports below forced to Hi−z – EXA[20:1], EXD[15:0], NCS[1:0], NRD, NWRENWRL, NHBNWRH, NLBEXA0 – SDCLK0, SDCMD0, SDAT0[3:0] – CK1, SDI1(QIO0), SDO1(QIO1), SWP1(QIO2), SHOLD1(QIO3), TIOCB01

14. In case of TQFP128L, WLP154, don’t use external memory boot (External−0)

Boot Port

Some ports are used in internal ROM code while booting as below.

- EXTINT2E(GPIO2E): OUT for power supply control
- EXTINT2F(GPIO2F): OUT for indicating status of boot, start of USB connection and USB disconnection, error status by Low/High of this port.
- Use SDCMD1, SDAT1[3:0], SDCLK1 as SD1. SDCD1 and SDWP1 are not used. Port function switch is processed during write from SD1.
- SPI Boot/SPI All Erase is processed by using 4 ports SCK1, QSCS, SDO1,SDI1. SHOLD1 and SWP1 are not used.
- QSPI Boot/QSPI All Erase is processed by using SCK1, QSCS, SDO1, SDI1, SHOLD1, SWP1.
- External ROM Boot is processed by using NCS0 and external memory controller ports. GPIO2E is not used.
- In case of External I/F ports Hi−z mode, external memory interface ports such as NCS0, NCS1 and external memory controller ports is used. GPIO2E is used as input port.

Table 12. PORTS USED DURING IPL

IPL Mode	**Ports Used** (Note 15)
Physical Boot USB	P2E(power supply control), P2F(status monitoring)
Physical Boot SD	P2E(power supply control), P2F(status monitoring) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
User Area Boot USB	P2E(power supply control), P2F(status monitoring)
User Area Boot SD	P2E(power supply control), P2F(status monitoring) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
SPI Boot USB	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1)
SPI Boot SD	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
QSPI Boot USB	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P011(SWP1) P12(SHOLD1)
User Area Delete	P2E(power supply control), P2F(status monitoring)
Partition Delete	P2E(power supply control), P2F(status monitoring)
SPI Erase	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SPIOUT) P0E(SDI1)
SDCH0 All Erase	P2E(power supply control), P2F(status monitoring)
QSPI All Erase	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P11(SWP1) P12(SHOLD1)
External ROM Boot	P06(NCS0) P17(NRD) P30(NWRENWRL) P31(NHBNWRH) P16(NLBEXA0) P32(EXA01) P33(EXA02) P34(EXA03) P35(EXA06) P36(EXA05) P37(EXA06) P38(EXA07) P39(EXA08) P3A(EXA09) P3B(EXA10) P3C(EXA11) P3D(EXA12) P3E(EXA13) P3F(EXA14) P40(EXA15) P41(EXA16) P42(EXA17) P43(EXA18) P44(EXA19) P45(EXA20) P46(EXD00) P47(EXD01) P48(EXD02) P49(EXD03) P4A(EXD04) P4B(EXD05) P4C(EXD06) P4D(EXD07) P4E(EXD08) P4F(EXD09) P50(EXD10) P51(EXD11) P52(EXD12) P53(EXD13) P54(EXD14) P55(EXD15)
HI-z	SDCLK0 Hi-z state

15. In this table “Pxx” means “GPIOxx”. For example “P2E” means “GPIO2E”.

SDIF PullUp

In case of boot mode using SDIF port, internal PullUp resistor is used (SDCMD0, SDAT0[3:0] / SDCMD1, SDAT1[3:0]). So, external PullUp resistor is not required on board.

QSCS PullUp

In case of boot mode using QSCS, PullUp of GPIO03(QSCS) is active by the hard reset. After GPIO2E is set to high, GPIO03 set to QSCS and PullUp set to inactive.

In case of Hi−z boot, PullUp is forced to inactive.

GPIO2F

During boot, GPIO2F is used as GPIO and indicates boot status and error occurrence by output of Low/High.

When errors occur during boot sequences, for example writing of IPL2, GPIO2F reports the sort of error. GPIO0F can indicate the status of USB connection and the completion of USB file transfer. And Delete Mode, completion of Erase, and status of Erase can be reported by sequence of Low/High.

For more detail about the behavior of ports used during boot, refer to the document LC823450 Series IPL specification.

PIN ASSIGNMENT

Table 13. PIN ASSIGNMENT

I/O		Input Type		Output Type	
I	Input	CMOS	CMOS Input	3−State	Tristate Output
O	Output	schmitt	schmitt Input	OD	Open Drain Output
B	Bidirectional	X	Xtal	X	Xtal
P	Power	3A	3.3 V analog	3A	3.3 V analog
NC	Non Connect	1A	1.0 V analog	1A	1.0/1.2 V analog

Drive (example)		PU/PD		IO Circuit Type	
4 mA	3.3 V 4 mA Output	PU	Pull−up resister	Refer to Page 30 for circuit diagram	
4/8 mA	3.3 V with 4 mA, 8 mA output drivability switch	PD	Pull−down resister		
0.3 mA−OD	1.0 V 0.3 mA open drain Output	PU/PD	Pull−up, pull−down resister		

Table 14.

LFBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
1	R16	−	−		SDRDATA2	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
2	N14	1	1	M11	Vss	G						
3	P15	2	2	N12	Vdd2	P						
4	P16	3	3	H8	TCLKA0/ BCK1/ GPIO00/ EXTINT00	I/ B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
5	N15	−	−		SDRDATA3	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
6	N16	4	4	L10	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	I/ B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
7	M16	−	5	K9	NHBNWRH/ TXD0/ GPIO31/ EXTINT31	O/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
8	M15	−	6	N11	NCS1/ RXD0/ GPIO10/ EXTINT10	O/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)

Table 14.

LFBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
9	M14	−	−		SDRDATA4	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
10	M13	−	7	M10	NCS0/ GPIO06/ EXTINT06	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
11	L16	−	−		GPIO2A/ EXTINT2A/ SDRADDR12	B/ I/ O	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
12	L15	−	−		Vdd2	P						
13	L14	−	−		Vss	G						
14	L13	5	8	L9	Vdd1	P						
15	L12	−	9	N10	NRD/ GPIO17/ EXTINT17	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
16	K16	−	−		SDRADDR5	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
17	K15	−	−		SDRADDR6	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
18	K14	−	10	M9	NWRENWRL/ GPIO30/ EXTINT30	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
19	K13	−	11	N9	EXD0/ GPIO46/ EXTINT46	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
20	K12	−	−		SDRADDR7	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
21	H13	−	−		SDRDATA5	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
22	J14	−	−		SDRDATA6	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
23	J13	−	−		Vdd2	P						
24	H10	−	−		Vss	G						
25	J12	−	−		SDRDATA7	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
26	J11	−	−		SDRDATA8	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
27	H11	−	−		SDRDATA9	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
28	H16	6	12	J8	SCK1/ GPIO0D/ EXTINT0D	O/ B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)
29	H14	7	13	N8	TIOCB01/ DMCKO0/ QSCS/ GPIO03/ EXTINT03	B/ O/ O/ B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)
30	J16	8	14	M8	SDO1(QIO1)/ GPIO0F/ EXTINT0F	I(B)/ B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)
31	G14	9	15	L8	VddQSPI	P						
32	H15	10	16	K8	SDI1(QIO0)/ GPIO0E/ EXTINT0E	O(B) / B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)
33	J15	11	17	N7	Vss	G						
34	G16	12	18	M7	SWP1(QIO2)/ GPIO11/ EXTINT11	O(B) / B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)
35	G15	13	19	L7	SHOLD1(QIO3)/ GPIO12/ EXTINT12	O(B) / B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)
36	H12	14	20	K7	TXD2/ TIOCA10/ GPIO0B/ EXTINT0B	O/ B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	VddQSPI	3ISUD/3T1 (2)(4)

Table 14.

LFBGA240		TQFP128L	WLP154								
No.	Ball	No.	No	Ball	Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
37	G13	15	21	J7	RXD2/ TIOCA11/ GPIO0C/ EXTINT0C	I/ B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	VddQSPI	3ISUD/3T1 (2)(4)
38	G12	16	22	N6	TDI/ SDCD1/ SWO/ GPIO20/ EXTINT20	I/ I/ O/ B/ I	Schmitt	3−State	2 mA	PU/PD	VddSD1	3ISUD/3T2
39	G11	17	23	M6	TDO/ SDWP1/ INS/ GPIO21/ EXTINT21	O/ I/ I/ B/ I	Schmitt	3−State	2 mA	PU/PD	VddSD1	3ISUD/3T2
40	F16	18	24	L6	SDCMD1/ BS/ GPIO23/ EXTINT23	B/ O/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
41	F15	19	25	K6	SDAT10/ DATA0/ GPIO24/ EXTINT24	B/ B/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
42	F14	20	26	N5	VddSD1	P						
43	E14	21	27	M5	SDAT11/ DATA1/ GPIO25/ EXTINT25	B/ B/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
44	F13	22	28	L5	Vss	G						
45	E16	23	29	J6	SDAT12/ DATA2/ GPIO26/ EXTINT26	B/ B/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
46	E15	24	30	N4	SDAT13/ DATA3/ GPIO27/ EXTINT27	B/ B/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
47	D16	25	31	M4	SDCLK1/ SCLK/ GPIO22/ EXTINT22	O/ O/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
48	F12	−	−		SDRADDR8	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
49	E12	−	−		SDRADDR9	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
50	F11	−	−		SDRADDR10	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
51	E13	26	32	L4	Vdd1	P						
52	D13	27	33	N3	Vss	G						
53	D14	28	34	N2	Vdd2	P						
54	D15	−	−		SDRBA0	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
55	C16	−	−		SDRBA1	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
56	C15	−	−		SDRCAS	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
57	C14	−	−		SDRRAS	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
58	B16	−	−		Vdd2	P						
59	B15	−	−		Vss	G						
60	A16	−	−		SDRCKE	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
61	A15	−	−		SDRCLK	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
62	A14	29	35	M3	SDCLK0	O	CMOS	3−State	6/8/10 mA		VddSD0	3IC/3T6 (8)(10)
63	B14	30	36	K5	SDCMD0	B	CMOS	3−State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
64	C12	31	37	N1	VddSD0	P						
65	B13	32	38	L3	SDAT00	B	CMOS	3−State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
66	C13	33	39	M2	Vss	G						

Table 14.

LFBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
67	A13	34	40	K4	SDAT01	B	CMOS	3−State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
68	A12	35	41	M1	SDAT02	B	CMOS	3−State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
69	B12	36	42	J5	SDAT03	B	CMOS	3−State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
70	C11	37	43	K3	TIOCA01/ SDCMD2/ PHI1/ GPIO0A/ EXTINT0A	B/ B/ O/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
71	A11	38	44	L2	TXD1/ SDAT20/ GPIO04/ EXTINT04	O/ B/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
72	B11	39	45	J4	RXD1/ SDAT21/ GPIO05/ EXTINT05	I/ B/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
73	D12	40	46	L1	VddSD2	P						
74	C10	41	47	H6	CTS1/ SDAT22/ RXD0/ GPIO56/ EXTINT56	I/ B/ I/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
75	E11	42	48	K2	Vss	G						
76	B10	43	49	K1	RTS1/ SDAT23/ TXD0/ GPIO57/ EXTINT57	O/ B/ O/ B/ I	CMOS	3−State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
77	D11	44	50	J3	TCK/ SDCD2/ GPIO29/ EXTINT29	I/ I/ B/ I	Schmitt	3−State	1/2/4mA	PU/PD	VddSD2	3ISUD/3T1 (2)(4)
78	D10	45	51	H5	TMS/ SDWP2/ GPIO28/ EXTINT28	I/ I/ B/ I	Schmitt	3−State	1/2/4mA	PU/PD	VddSD2	3ISUD/3T1 (2)(4)
79	A10	46	52	J2	TIOCA00/ SDCLK2/ PHI0/ GPIO09/ EXTINT09	B/ O/ O/ B/ I	Schmitt	3−State	6/8/10 mA	PU/PD	VddSD2	3ISUD/3T6 (8)(10)
80	E10	−	−		SDRCS	O	−	3−State	2/4/8mA		Vdd2	3T2 (4)(8)
81	F10	−	−		SDRWE	O	−	3−State	2/4/8mA		Vdd2	3T2 (4)(8)
82	G10	−	−		SDRDQM0	O	−	3−State	2/4/8mA		Vdd2	3T2 (4)(8)
83	D9	−	−		SDRDQM1	O	−	3−State	2/4/8mA		Vdd2	3T2 (4)(8)
84	E9	−	−		SDRDATA10	B	CMOS	3−State	2/4/8mA	PD	Vdd2	3ICD/3T2 (4)(8)
85	F9	−	−		SDRDATA11	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
86	A9	47	53	J1	Vdd1	P						
87	B9	48	54	H4	Vss	G						
88	G9	−	55	G5	XTALINFO0	B	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
89	C9	49	56	H1	Vdd2	P						
90	H9	−	−		SDRDATA12	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
91	G8	−	−		SDRDATA13	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
92	F8	−	−		SDRDATA14	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
93	E8	−	−		SDRDATA15	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)

Table 14.

LFBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
94	D8	50	57	H2	VddRTC	P						
95	A7	−	58	H3	RTCMODE	I	CMOS	−	−	−	VddRTC	1IC
96	B8	51	59	G2	VssRTC	G						
97	A8	52	60	G1	XIN32K	I	X	−	−	−	VddRTC	X
98	C8	53	61	G3	XOUT32K	O	−	X	−	−	VddRTC	X
99	B7	54	62	F1	VDET	I	CMOS	−	−	−	VddRTC	1IC
100	C7	55	63	G4	RTCINT(Note 16)	O	−	OD	0.3 mA−OD	−	VddRTC	OD3
101	D7	56	64	F2	BACKUPB	I	Schmitt	−	−	−	VddRTC	1IS
102	E7	−	65	F3	KEYINT0	I	Schmitt	−	−	PD	VddRTC	1ISD
103	F7	−	66	F4	KEYINT1	I	Schmitt	−	−	PD	VddRTC	1ISD
104	G7	−	67	E1	KEYINT2	I	Schmitt	−	−	PD	VddRTC	1ISD
105	A6	57	68	E2	AVddADC	P						
106	B6	−	−		VRH	I	3A	−	−	−	AVddADC	3A
107	C6	−	−		VR	O	−	3A	−	−	AVddADC	3A
108	D6	−	−		VRL	I	3A	−	−	−	AVddADC	3A
109	E6	58	69	D1	AVssADC	G						
110	C5	59	70	E3	AN5	I	3A	−	−	−	AVddADC	3A
111	B5	60	71	D2	AN4	I	3A	−	−	−	AVddADC	3A
112	A5	61	72	D3	AN3	I	3A	−	−	−	AVddADC	3A
113	C4	62	73	C1	AN2	I	3A	−	−	−	AVddADC	3A
114	B4	63	74	C2	AN1	I	3A	−	−	−	AVddADC	3A
115	A4	64	75	B1	AN0	I	3A	−	−	−	AVddADC	3A
116	D5	−	76	F5	NLBEXA0/ GPIO16/ EXTINT16	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
117	F6	−	77	E4	EXD1/ GPIO47/ EXTINT47	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
118	A3	−	−		EXA1/ GPIO32/ EXTINT32	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
119	B3	−	−		EXA2/ GPIO33/ EXTINT33	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
120	A2	−	−		EXA3/ GPIO34/ EXTINT34	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
121	A1	−	−		Vss	G						
122	B2	−	−		Vdd2	P						
123	B1	−	−		EXA4/ GPIO35/ EXTINT35	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
124	C1	−	−		EXA5/ GPIO36/ EXTINT36	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
125	C2	−	−		EXA6/ GPIO37/ EXTINT37	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
126	C3	65	78	A1	SCL0/ GPIO07/ EXTINT07	O/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
127	D3	−	−		EXA7/ GPIO38/ EXTINT38	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
128	D4	66	79	B2	SDA0/ GPIO08/ EXTINT08	B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)

Table 14.

LFBGA240		TQFP128L	WLP154									
No.	Ball	No.	No	Ball	Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
129	E4	−	−		EXA8/ GPIO39/ EXTINT39	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
130	E5	67	80	C3	SDO0/ GPIO1F/ EXTINT1F	O/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
131	D1	68	81	D4	Vss	G						
132	D2	69	82	A2	Vdd2	P						
133	F4	−	−		EXA9/ GPIO3A/ EXTINT3A	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
134	F5	−	−		EXA10/ GPIO3B/ EXTINT3B	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
135	G5	−	−		EXA11/ GPIO3C/ EXTINT3C	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
136	G4	70	83	B3	SCK0/ GPIO1D/ EXTINT1D	B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
137	G6	−	−		EXA12/ GPIO3D/ EXTINT3D	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
138	H4	71	84	A3	SWDCLK/ GPIO58/ EXTINT58/ DMCKO1	I/ B/ I/ O	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
139	H5	−	−		EXA13/ GPIO3E/ EXTINT3E	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
140	H6	72	85	F6	SDI0/ GPIO1E/ EXTINT1E	I/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
141	J4	−	−		EXA14/ GPIO3F/ EXTINT3F	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
142	J5	73	86	C4	SWDIO/ GPIO59/ EXTINT59/ DMDIN1	B/ B/ I/ I	Schmitt	3−State	2 mA	PU	Vdd2	3ISU/3T2
143	H7	−	87	E5	EXD2/ GPIO48/ EXTINT48	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
144	J6	−	88	A4	EXD3/ GPIO49/ EXTINT49	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
145	E3	74	89	B4	Vdd1	P						
146	F3	−	−		Vdd2	P						
147	G3	−	90	D5	Vss	G						
148	K6	−	−		EXA15/ GPIO40/ EXTINT40	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
149	K5	−	−		EXA16/ GPIO41/ EXTINT41	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
150	L5	−	−		EXA17/ GPIO42/ EXTINT42	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
151	M4	−	−		EXA18/ GPIO43/ EXTINT43	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
152	K4	−	−		Vss	G						
153	E2	−	−		DVddUSBPHY1	P						
154	F2	75	91	A5	AVddUSBPHY1	P						
155	G2	76	92	C5	AVssUSBPHY	G						

Table 14.

LFBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
156	E1	77	93	B5	USBDM	B	3A	3A	−	−	AVddUSB PHY2	3A
157	F1	78	94	B6	USBDP	B	3A	3A	−	−	AVddUSB PHY2	3A
158	G1	79	95	C6	AVssUSBPHY	G						
159	H2	80	96	D6	AVddUSBPHY2	P						
160	J1	81	97	E6	AVssUSBPHY	G						
161	H1	82	98	B7	USBEXT12	O	−	3A	−	−	AVddUSB PHY2	3A
162	J2	83	99	C7	AVddUSBPHY2	P						
163	H3	84	100	D7	AVddUSBPHY1	P						
164	J3	85	101	E7	AVssUSBPHY	G						
165	K3	−	−		DVddUSBPHY1	P						
166	L1	−	−		Vss	G						
167	K2	86	102	B8	VddXT1	P						
168	K1	87	103	A8	XIN1	I	X	−	−	−	VddXT1	X
169	L2	88	104	D8	VssXT1	G						
170	L3	89	105	C8	XOUT1	O	−	X	−	−	VddXT1	X
171	L4	90	106	E8	Vdd1	P						
172	M3	−	−		Vss	G						
173	M2	91	107	A9	AVddPLL1	P						
174	M1	92	108	B9	VCNT1	O	−	1A	−	−	AVddPLL1	1A
175	N1	93	109	C9	AVssPLL1	G						
176	N3	−	110	A10	EXD4/ GPIO4A/ EXTINT4A	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
177	N2	−	−		Vss	G						
178	P1	−	−		Vdd2	P						
179	P2	−	111	B10	EXD5/ GPIO4B/ EXTINT4B	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
180	R1	−	112	D9	EXD6/ GPIO4C/ EXTINT4C	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
181	R2	−	−		EXA19/ GPIO44/ EXTINT44	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
182	R3	−	−		EXA20/ GPIO45/ EXTINT45	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
183	P3	−	113	A11	EXD7/ GPIO4D/ EXTINT4D	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
184	N4	94	114	F7	TIOCB00/ DMDIN0/ DIN1/ GPIO02/ EXTINT02	B/ I/ I/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
185	R4	−	115	B11	Vss	G						
186	P4	95	116	A12	Vdd2	P						
187	M6	96	117	C10	DOUT1/ GPIO15/ EXTINT15	O/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
188	N5	−	−		EXD8/ GPIO4E/ EXTINT4E	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
189	M5	−	−		EXD9/ GPIO4F/ EXTINT4F	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)

Table 14.

LFBGA240		TQFP128L	WLP154								
No.	Ball	No.	No	Ball	Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
190	L6	−	118	G6	BCK1/ GPIO13/ EXTINT13	B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
191	M7	−	−		EXD10/ GPIO50/ EXTINT50	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
192	N7	−	119	G7	LRCK1/ GPIO14/ EXTINT14	B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
193	N6	97	120	B12	MCLK0/ MCLK1/ GPIO18/ EXTINT18	B/ B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
194	L7	−	−		EXD11/ GPIO51/ EXTINT51	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
195	M8	98	121	H7	BCK0/ DMCKO1/ GPIO19/ EXTINT19	B/ O/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
196	K7	−	−		EXD12/ GPIO52/ EXTINT52	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
197	P5	99	122	C11	Vdd2	P						
198	J7	−	123	D10	XTALINFO1	B	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
199	P6	100	124	C12	Vss	G						
200	L8	−	−		EXD13/ GPIO53/ EXTINT53	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
201	K8	101	125	E9	LRCK0/ DMDIN1/ GPIO1A/ EXTINT1A	B/ I/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
202	J8	−	−		EXD14/ GPIO54/ EXTINT54	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
203	N9	102	126	F8	DIN0/ DMDIN0/ GPIO1B/ EXTINT1B	I/ I/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
204	M9	−	−		EXD15/ GPIO55/ EXTINT55	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
205	N8	103	127	E10	DOUT0/ DMCKO0/ GPIO1C/ EXTINT1C	O/ O/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
206	P7	104	128	D11	NRES	I	Schmitt	−	−	−	Vdd2	3IS
207	L9	105	129	D12	BMODE0	B	Schmitt	3−State	2 mA	PU/PD	Vdd2	3ISUD/3T2
208	K9	106	130	F9	BMODE1	B	Schmitt	3−State	2 mA	PU/PD	Vdd2	3ISUD/3T2
209	J9	107	131	F10	TEST	I	Schmitt	−	−		Vdd2	3IS
210	P8	108	132	E11	Vdd2	P						
211	H8	109	133	E12	Vss	G						
212	P9	110	134	G10	Vdd1	P						
213	R5	111	135	F11	AVssDAMPR	G						
214	R6	112	136	F12	ROUT/ GPROUT	O/ O	−	1A	−	−	AVddDAM PR	1A
215	R7	113	137	G11	AVddDAMPR	P						
216	R8	114	138	G12	AVddDAMPL	P						
217	R9	115	139	H12	LOUT/ GPLOUT	O/ O	−	1A	−	−	AVddDAM PL	1A
218	R10	116	140	H11	AVssDAMPL	G						

Table 14.

LFBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
219	P10	−	−		Vdd1	P						
220	N11	117	141	H10	Vss	G						
(Note 18)		(Note 17)	142	J12	AVddPLL3	P						
			143	J11	VCNT3	O	−	3A	−	−	AVddPLL3	3A
221	P12	118	144	J10	AVssPLL2	G						
222	R12	119	145	K11	VCNT2	O	−	1A	−	−	AVddPLL2	1A
223	R13	120	146	K12	AVddPLL2	P						
224	P11	121	147	G9	Vdd1	P						
225	R11	−	−		Vss	G						
226	N12	−	−		Vdd2	P						
227	M10	122	148	H9	GPIO2D/ EXTINT2D/ DMCKO0/ SDRADDR11	B/ I/ O/ O	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T (4)(8)
228	L10	−	−		SDRADDR0	O	−	3−State	2/4/8 mA		Vdd2	3T2(4)(8)
229	K10	123	149	G8	GPIO2E/ EXTINT2E	B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
230	J10	−	−		SDRADDR1	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
231	N10	−	−		SDRADDR2	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
232	M11	124	150	L12	GPIO2F/ EXTINT2F	B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
233	P13	125	151	L11	Vss	G						
234	L11	126	152	K10	SCL1/ GPIO2B/ EXTINT2B	O/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
235	R14	127	153	M12	Vdd2	P						
236	K11	128	154	J9	SDA1/ GPIO2C/ EXTINT2C	B/ B/ I	Schmitt	3−State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
237	M12	−	−		SDRDATA0	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
238	N13	−	−		SDRDATA1	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
239	P14	−	−		SDRADDR3	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)
240	R15	−	−		SDRADDR4	O	−	3−State	2/4/8 mA		Vdd2	3T2 (4)(8)

16. RTCINT (open drain Output) 3.6 V tolerant.
17. Pin assignment of TQFP128L which can use PLL3 is as below.

PLL3	
118	AvddPLL3
119	VCNT3
120	AVssPLL2

18. Pin assignment of LFBGA240 which can use PLL3 is as below.

PLL3	
221	AvddPLL3
222	VCNT3
223	AVssPLL2

Input/Output Circuit

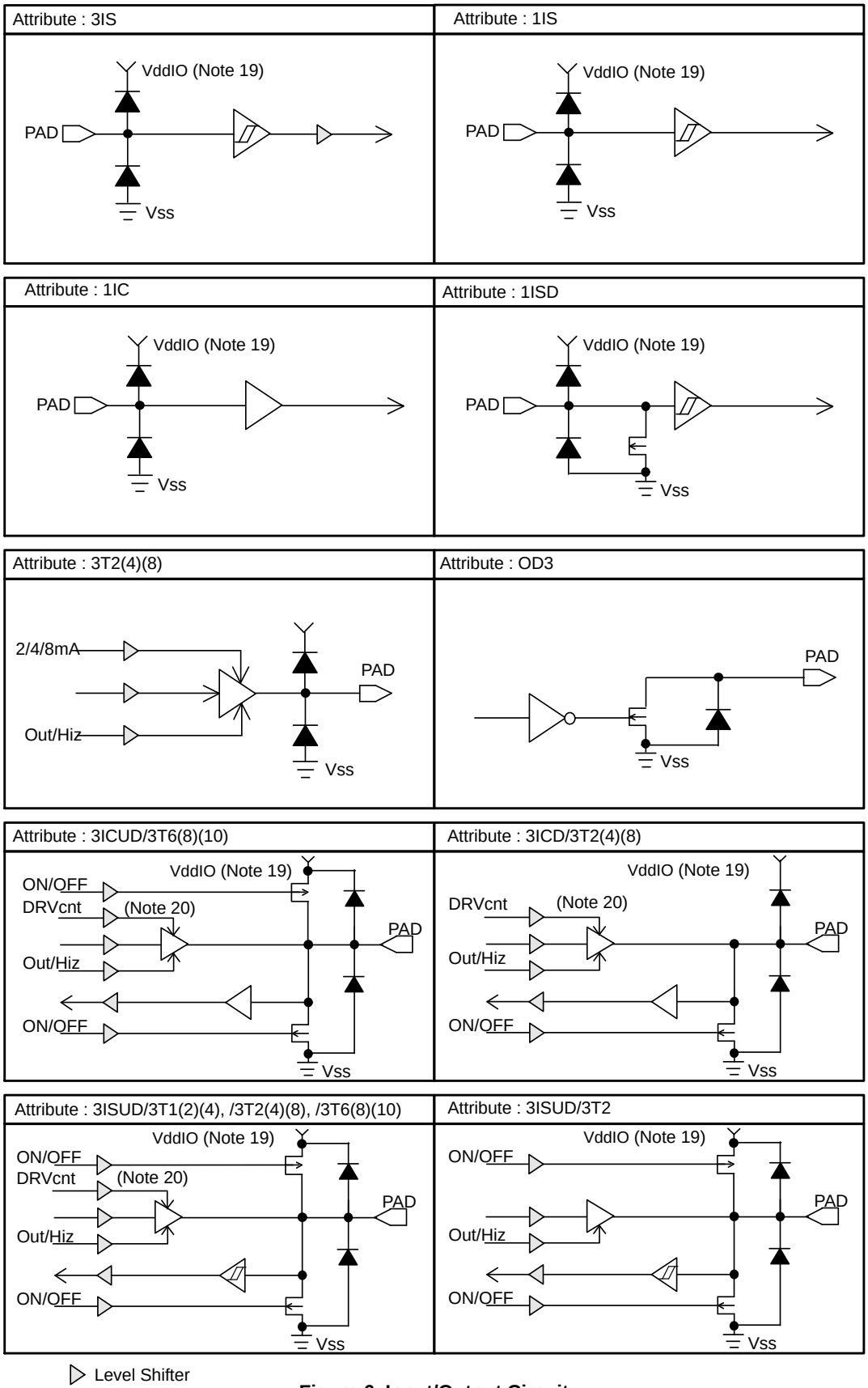
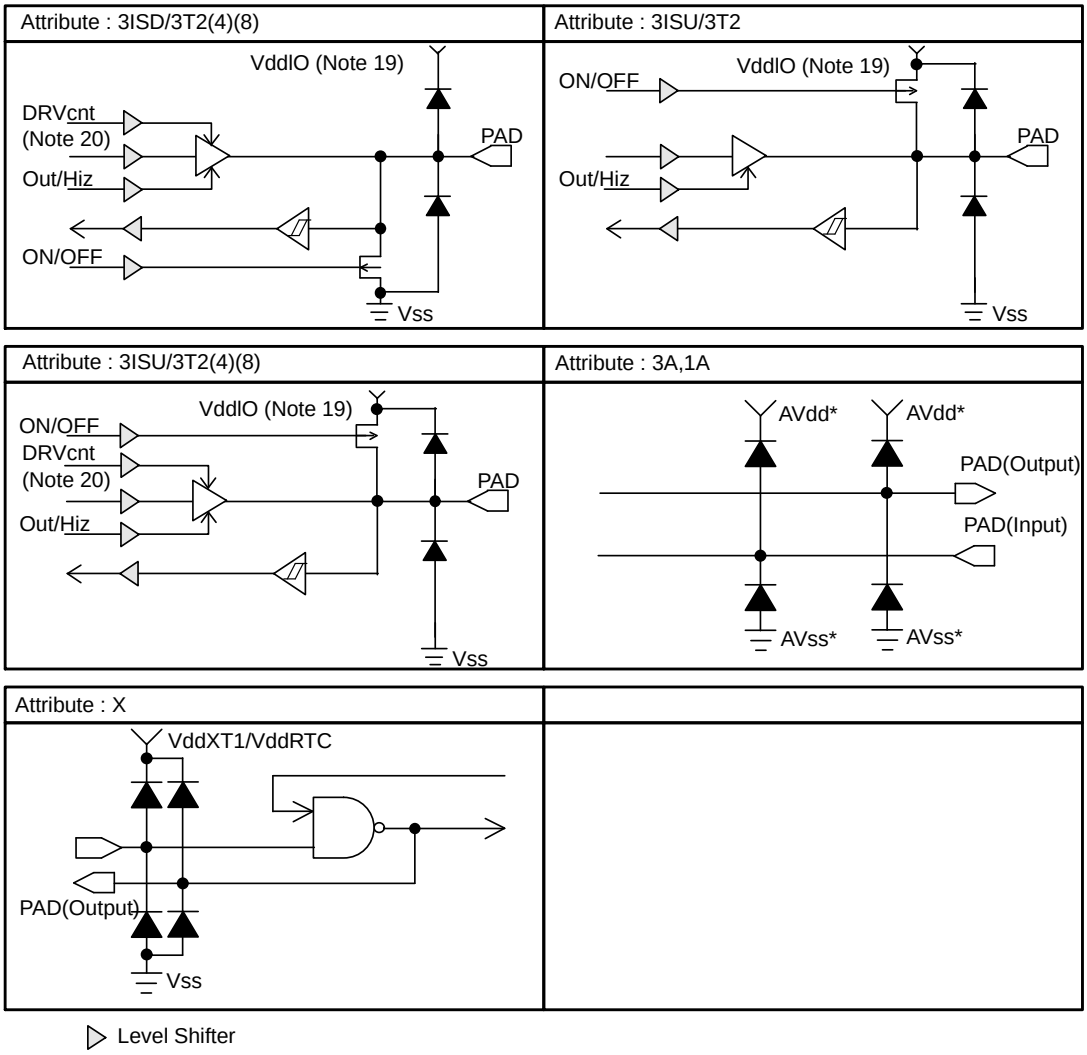


Figure 6. Input/Output Circuit



19. Vdd2, VddSD0, VddSD1, VddSD2, VddQSPI (IO Pwr Grp of 3−1 Pin Assignment)
20. DRVcnt: 1/2/4 mA, 2/4/8 mA. 4/8/10 mA, etc. Drivability switch control signal

Figure 7. Input/Output Circuit (Continued)

Table 15. PORT STATE TABLE

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	TCLKA0/ BCK1/ GPIO00/ EXTINT00	GPIO00	Hiz	Hiz
•	•	•	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	GPIO01	Hiz	Hiz
•	•	•	TIOCB00/ DMDIN0 DIN1/ GPIO02/ EXTINT02/	GPIO02	Hiz	Hiz
•	•	•	TIOCB01/ DMCKO0/ QSCS/ GPIO03/ EXTINT03	GPIO03	PU	PU (Note 24)
•	•	•	TXD1/ SDAT20/ GPIO04/ EXTINT04	GPIO04	Hiz	Hiz
•	•	•	RXD1/ SDAT21/ GPIO05/ EXTINT05	GPIO05	Hiz	Hiz
•		•	NCS0/ GPIO06/ EXTINT06	GPIO06	Hiz	Hiz
•	•	•	SCL0/ GPIO07/ EXTINT07	GPIO07	Hiz	Hiz
•	•	•	SDA0/ GPIO08/ EXTINT08	GPIO08	Hiz	Hiz
•	•	•	TIOCA00/ SDCLK2/ PHI0/ GPIO09/ EXTINT09	GPIO09	Hiz	Hiz
•	•	•	TIOCA01/ SDCMD2/ PHI1/ GPIO0A/ EXTINT0A	GPIO0A	Hiz	Hiz
•	•	•	TXD2/ TIOCA10/ GPIO0B/ EXTINT0B	GPIO0B	Hiz	Hiz
•	•	•	RXD2/ TIOCA11/ GPIO0C/ EXTINT0C	GPIO0C	Hiz	Hiz
•	•	•	SCK1/ GPIO0D/ EXTINT0D	GPIO0D	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	SDI1(QIO0)/ GPIO0E/ EXTINT0E	GPIO0E	Hiz	Hiz
•	•	•	SDO1(QIO1)/ GPIO0F/ EXTINT0F	GPIO0F	Hiz	Hiz
•		•	NCS1/ RXD0/ GPIO10/ EXTINT10	GPIO10	Hiz	Hiz
•	•	•	SWP1(QIO2)/ GPIO11/ EXTINT11	GPIO11	Hiz	Hiz
•	•	•	SHOLD1(QIO3)/ GPIO12/ EXTINT12	GPIO12	Hiz	Hiz
•		•	BCK1/ GPIO13/ EXTINT13	GPIO13	Hiz	Hiz
•		•	LRCK1/ GPIO14/ EXTINT14	GPIO14	Hiz	Hiz
•	•	•	DOUT1/ GPIO15/ EXTINT15	GPIO15	Hiz	Hiz
•		•	NLBEXA0/ GPIO16/ EXTINT16	GPIO16	Hiz	Hiz
•		•	NRD/ GPIO17/ EXTINT17	GPIO17	Hiz	Hiz
•	•	•	MCLK0/ MCLK1/ GPIO18/ EXTINT18	GPIO18	Hiz	Hiz
•	•	•	BCK0/ DMCKO1/ GPIO19/ EXTINT19	GPIO19	Hiz	Hiz
•	•	•	LRCK0/ DMDIN1/ GPIO1A/ EXTINT1A	GPIO1A	Hiz	Hiz
•	•	•	DIN0/ DMDIN0/ GPIO1B/ EXTINT1B	GPIO1B	Hiz	Hiz
•	•	•	DOUT0/ DMCKO0/ GPIO1C/ EXTINT1C	GPIO1C	Hiz	Hiz
•	•	•	SCK0/ GPIO1D/ EXTINT1D	GPIO1D	Hiz	Hiz
•	•	•	SDI0/ GPIO1E/ EXTINT1E	GPIO1E	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	SDO0/ GPIO1F/ EXTINT1F	GPIO1F	Hiz	Hiz
•	•	•	TDI/ SDCD1/ SWO/ GPIO20/ EXTINT20	GPIO20	Hiz	Hiz
•	•	•	TDO/ SDWP1/ INS/ GPIO21/ EXTINT21	GPIO21	Hiz	Hiz
•	•	•	SDCLK1/ SCLK/ GPIO22/ EXTINT22	GPIO22	Hiz	Hiz
•	•	•	SDCMD1/ BS/ GPIO23/ EXTINT23	GPIO23	Hiz	Hiz
•	•	•	SDAT10/ DATA0/ GPIO24/ EXTINT24	GPIO24	Hiz	Hiz
•	•	•	SDAT11/ DATA1/ GPIO25/ EXTINT25	GPIO25	Hiz	Hiz
•	•	•	SDAT12/ DATA2/ GPIO26/ EXTINT26	GPIO26	Hiz	Hiz
•	•	•	SDAT13/ DATA3/ GPIO27/ EXTINT27	GPIO27	Hiz	Hiz
•	•	•	TMS/ SDWP2/ GPIO28/ EXTINT28	GPIO28	Hiz	Hiz
•	•	•	TCK/ SDCD2/ GPIO29/ EXTINT29	GPIO29	Hiz	Hiz
•			GPIO2A/ EXTINT2A/ SDRADDR12	GPIO2A	Hiz	Hiz
•	•	•	SCL1/ GPIO2B/ EXTINT2B	GPIO2B	Hiz	Hiz
•	•	•	SDA1/ GPIO2C/ EXTINT2C	GPIO2C	Hiz	Hiz
•	•	•	GPIO2D/ EXTINT2D/ DMCKO0/ SDRADDR11	GPIO2D	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	GPIO2E/ EXTINT2E	GPIO2E	Hiz	Hiz(Note 25)
•	•	•	GPIO2F/ EXTINT2F	GPIO2F	Hiz	Hiz(Note 26)
•		•	NWRENWRL/ GPIO30/ EXTINT30	GPIO30	Hiz	Hiz
•		•	NHBNWRH/ TXD0/ GPIO31/ EXTINT31	GPIO31	Hiz	Hiz
•			EXA1/ GPIO32/ EXTINT32	GPIO32	Hiz	Hiz
•			EXA2/ GPIO33/ EXTINT33	GPIO33	Hiz	Hiz
•			EXA3/ GPIO34/ EXTINT34	GPIO34	Hiz	Hiz
•			EXA4/ GPIO35/ EXTINT35	GPIO35	Hiz	Hiz
•			EXA5/ GPIO36/ EXTINT36	GPIO36	Hiz	Hiz
•			EXA6/ GPIO37/ EXTINT37	GPIO37	Hiz	Hiz
•			EXA7/ GPIO38/ EXTINT38	GPIO38	Hiz	Hiz
•			EXA8/ GPIO39/ EXTINT39	GPIO39	Hiz	Hiz
•			EXA9/ GPIO3A/ EXTINT3A	GPIO3A	Hiz	Hiz
•			EXA10/ GPIO3B/ EXTINT3B	GPIO3B	Hiz	Hiz
•			EXA11/ GPIO3C/ EXTINT3C	GPIO3C	Hiz	Hiz
•			EXA12/ GPIO3D/ EXTINT3D	GPIO3D	Hiz	Hiz
•			EXA13/ GPIO3E/ EXTINT3E	GPIO3E	Hiz	Hiz
•			EXA14/ GPIO3F/ EXTINT3F	GPIO3F	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•			EXA15/ GPIO40/ EXTINT40	GPIO40	Hiz	Hiz
•			EXA16/ GPIO41/ EXTINT41	GPIO41	Hiz	Hiz
•			EXA17/ GPIO42/ EXTINT42	GPIO42	Hiz	Hiz
•			EXA18/ GPIO43/ EXTINT43	GPIO43	Hiz	Hiz
•			EXA19/ GPIO44/ EXTINT44	GPIO44	Hiz	Hiz
•			EXA20/ GPIO45/ EXTINT45	GPIO45	Hiz	Hiz
•		•	EXD0/ GPIO46/ EXTINT46	GPIO46	Hiz	Hiz
•		•	EXD1/ GPIO47/ EXTINT47	GPIO47	Hiz	Hiz
•		•	EXD2/ GPIO48/ EXTINT48	GPIO48	Hiz	Hiz
•		•	EXD3/ GPIO49/ EXTINT49	GPIO49	Hiz	Hiz
•		•	EXD4/ GPIO4A/ EXTINT4A	GPIO4A	Hiz	Hiz
•		•	EXD5/ GPIO4B/ EXTINT4B	GPIO4B	Hiz	Hiz
•		•	EXD6/ GPIO4C/ EXTINT4C	GPIO4C	Hiz	Hiz
•		•	EXD7/ GPIO4D/ EXTINT4D	GPIO4D	Hiz	Hiz
•			EXD8/ GPIO4E/ EXTINT4E	GPIO4E	Hiz	Hiz
•			EXD9/ GPIO4F/ EXTINT4F	GPIO4F	Hiz	Hiz
•			EXD10/ GPIO50/ EXTINT50	GPIO50	Hiz	Hiz
•			EXD11/ GPIO51/ EXTINT51	GPIO51	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•			EXD12/ GPIO52/ EXTINT52	GPIO52	Hiz	Hiz
•			EXD13/ GPIO53/ EXTINT53	GPIO53	Hiz	Hiz
•			EXD14/ GPIO54/ EXTINT54	GPIO54	Hiz	Hiz
•			EXD15/ GPIO55/ EXTINT55	GPIO55	Hiz	Hiz
•	•	•	CTS1/ SDAT22/ RXD0/ GPIO56/ EXTINT56	GPIO56	Hiz	Hiz
•	•	•	RTS1/ SDAT23/ TXD0/ GPIO57/ EXTINT57	GPIO57	Hiz	Hiz
•	•	•	SDAT00	SDAT00	Hiz	Hiz
•	•	•	SDAT01	SDAT01	Hiz	Hiz
•	•	•	SDAT02	SDAT02	Hiz	Hiz
•	•	•	SDAT03	SDAT03	Hiz	Hiz
•	•	•	SDCLK0	SDCLK0	Low	Low
•	•	•	SDCMD0	SDCMD0	Hiz	Hiz
•			SDRADDR0	SDRADDR0	Low	Low
•			SDRADDR1	SDRADDR1	Low	Low
•			SDRADDR10	SDRADDR10	Low	Low
•			SDRADDR2	SDRADDR2	Low	Low
•			SDRADDR3	SDRADDR3	Low	Low
•			SDRADDR4	SDRADDR4	Low	Low
•			SDRADDR5	SDRADDR5	Low	Low
•			SDRADDR6	SDRADDR6	Low	Low
•			SDRADDR7	SDRADDR7	Low	Low
•			SDRADDR8	SDRADDR8	Low	Low
•			SDRADDR9	SDRADDR9	Low	Low
•			SDRBA0	SDRBA0	Low	Low
•			SDRBA1	SDRBA1	Low	Low
•			SDRCAS	SDRCAS	High	High
•			SDRCKE	SDRCKE	High	High
•			SDRCLK	SDRCLK	Low	Low
•			SDRCS	SDRCS	High	High
•			SDRDATA0	SDRDATA0	Hiz	Hiz
•			SDRDATA1	SDRDATA1	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•			SDRDATA10	SDRDATA10	Hiz	Hiz
•			SDRDATA11	SDRDATA11	Hiz	Hiz
•			SDRDATA12	SDRDATA12	Hiz	Hiz
•			SDRDATA13	SDRDATA13	Hiz	Hiz
•			SDRDATA14	SDRDATA14	Hiz	Hiz
•			SDRDATA15	SDRDATA15	Hiz	Hiz
•			SDRDATA2	SDRDATA2	Hiz	Hiz
•			SDRDATA3	SDRDATA3	Hiz	Hiz
•			SDRDATA4	SDRDATA4	Hiz	Hiz
•			SDRDATA5	SDRDATA5	Hiz	Hiz
•			SDRDATA6	SDRDATA6	Hiz	Hiz
•			SDRDATA7	SDRDATA7	Hiz	Hiz
•			SDRDATA8	SDRDATA8	Hiz	Hiz
•			SDRDATA9	SDRDATA9	Hiz	Hiz
•			SDRDQM0	SDRDQM0	High	High
•			SDRDQM1	SDRDQM1	High	High
•			SDRRAS	SDRRAS	High	High
•			SDRWE	SDRWE	High	High
•	•	•	SWDCLK/ GPIO58/ EXTINT58/ DMCKO1	SWDCLK	Hiz	Hiz
•	•	•	SWDIO/ GPIO59/ EXTINT59/ DMDIN1	SWDIO	Hiz	Hiz
•	•	•	NRES	NRES	Hiz	Hiz
•	•	•	TEST	TEST	Hiz	Hiz
•		•	XTALINFO0	XTALINFO0	Hiz	Hiz
•		•	XTALINFO1	XTALINFO1	Hiz	Hiz
•	•	•	BMODE0	BMODE0	Hiz	Hiz
•	•	•	BMODE1	BMODE1	Hiz	Hiz
•		•	RTCMODE	RTCMODE	Hiz	Hiz
•		•	KEYINT0	KEYINT0	PD	PD
•		•	KEYINT1	KEYINT1	PD	PD
•		•	KEYINT2	KEYINT2	PD	PD
•	•	•	BACKUPB	BACKUPB	Hiz	Hiz
•	•	•	RTCINT	RTCINT	(Not Determined)	(Not Determined)
•	•	•	VDET	VDET	Hiz	Hiz
•	•	•	LOUT/ GPLOUT	LOUT	Hiz	Hiz
•	•	•	ROUT/ GPROUT	ROUT	Hiz	Hiz

Table 15. PORT STATE TABLE (continued)

LFBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	USBDM	USBDM	Hiz	Hiz
•	•	•	USBDP	USBDP	Hiz	Hiz
•	•	•	USBEXT12	USBEXT12	(Not Applicable)	(Not Applicable)
•	•	•	VCNT1	VCNT1	(Not Applicable)	(Not Applicable)
• (Note 27)	• (Note 27)	•	VCNT2	VCNT2	(Not Applicable)	(Not Applicable)
		•	VCNT3	VCNT3	(Not Applicable)	(Not Applicable)
•	•	•	AN0	AN0	(Not Applicable)	(Not Applicable)
•	•	•	AN1	AN1	(Not Applicable)	(Not Applicable)
•	•	•	AN2	AN2	(Not Applicable)	(Not Applicable)
•	•	•	AN3	AN3	(Not Applicable)	(Not Applicable)
•	•	•	AN4	AN4	(Not Applicable)	(Not Applicable)
•	•	•	AN5	AN5	(Not Applicable)	(Not Applicable)
•			VR	VR	(Not Applicable)	(Not Applicable)
•			VRH	VRH	(Not Applicable)	(Not Applicable)
•			VRL	VRL	(Not Applicable)	(Not Applicable)
•	•	•	XIN1	XIN1	(Not Applicable)	(Not Applicable)
•	•	•	XIN32K	XIN32K	(Not Applicable)	(Not Applicable)
•	•	•	XOUT1	XOUT1	(Not Applicable)	(Not Applicable)
•	•	•	XOUT32K	XOUT32K	(Not Applicable)	(Not Applicable)

21. Means a port is available for each package. “PD” means pull down
22. Default function is port function set by NRES = Low
23. NRES = High (ii) occurs just after NRES = Low(i)
24. This port is set to output port and PU is disabled to be used as QSCS for SPI I/F chip select during serial flash boot mode.
25. This port is set to output port to be used as external power control during Internal ROM boot.
26. This port is set to output port to be used as boot monitor port during Internal ROM boot.
27. One of VCNT2 or VCNT3 is available

ELECTRICAL SPECIFICATION

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 16. MAXIMUM RATINGS (*Vss* = 0 V)

Item	Symbol	Condition	Ratings	Unit
Maximum Power Supply Voltage	Vdd1 VddRTC VddXT1 AVddUSBPHY1 DvddUSBPHY1 AvddPLL1 AVddPLL2		−0.5 to 1.8	V
	AvddDAMPL AVddDAMPR		−0.5 to 2.5	V
	Vdd2 VddSD0 VddSD1 VddSD2 VddQSPI AvddPLL3 AvddADC AVddUSBPHY2		−0.5 to 4.6	V
Input Voltage	V_I		−0.5 to *Vdd* + 0.5	V
	V_{IUSB}	USBDP, USBDM Terminal	−0.5 to AVddUSBPHY2 + 0.5 (< 4.6)	V
Operating Ambient Temperature	Topr		−20 to +65	°C
Ambient Ttemperature of Preservation	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 17. RECOMMENDED OPERATING CONDITIONS (Ta = −20°C to +65°C)

Item	Symbol	Condition	Low Voltage Operation (Note 28)			High Voltage Operation (Note 28)			Unit
			Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	Vdd1		0.93	1.0	1.27	1.1	1.2	1.27	V
	VddXT1	(Note 29)	0.93	1.0	1.3	0.93	1.2	1.3	V
	AVddPLL1		0.93	1.0	1.3	1.1	1.2	1.3	V
	AVddPLL2		0.9	1.0	1.3	0.9	1.2	1.3	V
	AVddPLL3		2.7	3.3	3.6	Same as left			V
	VddRTC		0.9	1.0	1.1	Same as left			V
	Vdd2		2.7	3.3	3.6	Same as left			V
			1.7	1.8	1.95	Same as left			V
	VddSD0		2.7	3.3	3.6	Same as left			V
			1.7	1.8	1.95	Same as left			V
	VddSD1		2.7	3.3	3.6	Same as left			V
			1.7	1.8	1.95	Same as left			V
	VddSD2		2.7	3.3	3.6	Same as left			V
			1.7	1.8	1.95	Same as left			V
	VddQSPI		2.7	3.3	3.6	Same as left			V
			1.7	1.8	1.95	Same as left			V
	AVddADC		2.7	3.3	3.6	Same as left			V
	AVddUSBPHY1	(Note 30)	0.93	1.2	1.3	Same as left			V
		(Note 31)	1.08	1.2	1.3	Same as left			V
	DVddUSBPHY1	(Note 30)	0.93	1.2	1.3	Same as left			V
		(Note 31)	1.08	1.2	1.3	Same as left			V
	AVddUSBPHY2	(Note 30)	2.7	3.3	3.6	Same as left			V
		(Note 31)	3.0	3.3	3.6	Same as left			V
	AVddDAMPL		0.93	1.2	1.65	Same as left			V
		(Note 32)	0.93	1.2	1.95	Same as left			V
	AVddDAMPR		0.93	1.2	1.65	Same as left			V
		(Note 32)	0.93	1.2	1.95	Same as left			V
Input Range	VIN		0		*Vdd*	Same as left			V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

28. Follow the operating frequency specifications because the operating frequency ranges are specified according to the operating voltage ranges.
29. Regarding Xtal frequency range, refer to the detailed datasheet.
30. While USB is not used.
31. While USB is used (including USB suspend mode).
32. While used as GPO (general purpose output) the output of which can be controlled by registers.
33. Power domains of Vdd1, AVddUSBPHY1 = DVddUSBPHY1, AVddPLL1, AVddPLL2, AVddPLL3, VddXT1 are divided, and different voltage can be supplied.
    Power domains of Vdd2, VddSD0, VddSD1, VddSD2, VddQSPI, AVddADC, AVddUSBPHY2, AVddPLL3, AvddDAMPL = AVddDAMPR are divided, and difference voltage can be supplied.
    If power is supplied to one of the power supply pins above, all of other power supply pins should be supplied.
    VddRTC can be supplied if BACKUPB is set to low, while other power supply pins are not supplied.

Table 18. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Function	Low Voltage Operation			High Voltage Operation			Unit
Xtal Input Frequency	Fxin1	System, Audio clock (XT1 oscillator)	12 MHz or 20 MHz tolerance : ±200 ppm or less Jitter : ±50 ps or less (Note 37)			12 MHz or 20 MHz or 24 MHz or 48 MHz tolerance : ±200 ppm or less Jitter : ±50 ps or less (Note 37)			−
	FxinRTC	RTC clock (XTRTC oscillator)	32.768 kHz Jitter : ±500 ps or less			Same as left			−
	Frc	RC (RC oscillator)	0.4 (Note 38)	1 (Note 38)	2 (Note 38)	Same as left			MHz
Time for Xtal Stable	Txin1				3 (Note 40)	Same as left			ms
	TxinRTC				1000 (Note 40)	Same as left			ms
Internal Clock Frequency	Farm	Cortex−M3	0		100	0		160 (Note 39)	MHz
	Fahb	AHB	0		100	0		160 (Note 39)	MHz
	Fapb	APB	0		100	0		160 (Note 39)	MHz
	Fdsp	DSP	0		100	0		160 (Note 39)	MHz
	Faud (Note 34)	AUDCLK(768fs)	0	33.8688	147.456	Same as left			MHz
	Fdec	DECCLK(Note 35) (MP3 Decoder)	0	16.9344	73.728	Same as left			MHz
	Fenc	ENCCLK(Note 36) (MP3 Encoder)	0	8.4672	36.864	Same as left			MHz

34. Audio blocks run on 256 * Fs (sampling frequency) clock.
    However, Class−D AMP, etc run on 384 * Fs (sampling frequency).
    These clocks are generated from 768 * Fs (Base Clock) divided by 3 and 2 respectively.
35. MP3 Decoder runs on clock of 384 * Fs (sampling frequency of MPEG1 mode).
    It runs on the clock of the same frequency as MPEG1 mode during MPEG2 / 2.5 mode. For example, even when operating in MPEG 2 / 2.5 mode (Fs = 22.05 / 11.025 KHz as an example), please supplies 16.9344 MHz(= 384 * 44.1 kHz) clock which is the same clock frequency as MPEG1 mode.
36. MP3 Encoder runs on clock of 192 * Fs(sampling frequency of MPEG1 mode).
    It runs on the clock of the same frequency as MPEG1 mode during MPEG2 / 2.5 mode. For example, even when operating in MPEG2 / 2.5 mode (Fs = 22.05 / 11.025 KHz as an example), please supplies 8.4672 Mhz (= 192 * 44.1 kHz) clock which is the same clock frequency as MPEG1 mode.
37. Refer to the detailed datasheet. If USB function is not used, the specification required may be relaxed. Please contact our representative in detail.
38. Vdd1 = 0.93 V to 1.27 V, Ta = −20°C to 65°C.
39. When Farm, Fdsp are over 100 MHz, 1 * Wait is required for Cortex−M3 and LPDSP32 to access internal ROM by the register described in the ProgrammersModel_SystemController as memory access control register4.
40. These are just reference values under Ta = 25°C, and need to be adjusted to customer board situation.

Table 19. DC CHARACTERISTICS

(Vdd2= 2.7 V to 3.6V, VddRTC = 0.9 V to 1.1 V, VddSD0 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6V, VddSD2 = 2.7 V to 3.6 V, VddQSPI = 2.7 V to 3.6 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H Voltage	V_{IH}	(1)	CMOS	0.7 × Vdd2			V
		(2)		0.7 × VddSD0			V
		(3)		0.7 × VddSD1			V
		(4)		0.7 × VddSD2			V
		(5)	Schmitt	0.75 × Vdd2			V
		(21)		0.75 × VddSD1			V
		(6)		0.75 × VddSD2			V
		(7)		0.75 × VddQSPI			V
		(8)	CMOS	0.7 × VddRTC			V
		(9)	Schmitt	0.7 × VddRTC			V
Input L Voltage	V_{IL}	(1)	CMOS			0.3 × Vdd2	V
		(2)				0.3 × VddSD0	V
		(3)				0.3 × VddSD1	V
		(4)				0.3 × VddSD2	V
		(5)	Schmitt			0.25 × Vdd2	V
		(21)				0.25 × VddSD1	V
		(6)				0.25 × VddSD2	V
		(7)				0.25 × VddQSPI	V
		(8)	CMOS			0.2 × VddRTC	V
		(9)	Schmitt			0.2 × VddRTC	V

Table 19. DC CHARACTERISTICS (continued)
(Vdd2= 2.7 V to 3.6V, VddRTC = 0.9 V to 1.1 V, VddSD0 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6V, VddSD2 = 2.7 V to 3.6 V, VddQSPI = 2.7 V to 3.6 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output H Voltage	V_{OH}	(10)(12)	I_{OH} = –1 mA	Vdd2 – 0.4			V
		(11)		VddQSPI – 0.4			V
		(10)(13)(14)	I_{OH} = –2 mA	Vdd2 – 0.4			V
		(11)		VddQSPI – 0.4			V
		(15)		VddSD1 – 0.4			V
		(12)		VddSD2 – 0.4			V
		(10)(13)	I_{OH} = –4 mA	Vdd2 – 0.4			V
		(11)		VddQSPI – 0.4			V
		(12)		VddSD2 – 0.4			V
		(16)	I_{OH} = –6 mA	VddQSPI – 0.4			V
		(17)		VddSD0 – 0.4			V
		(18)		VddSD1 – 0.4			V
		(19)		VddSD2 – 0.4			V
		(13)	I_{OH} = –8 mA	Vdd2 – 0.4			V
		(16)		VddQSPI – 0.4			V
		(17)		VddSD0 – 0.4			V
		(18)		VddSD1 – 0.4			V
		(19)		VddSD2 – 0.4			V
		(16)	I_{OH} = –10 mA	VddQSP – 0.4			V
		(17)		VddSD0 − 0.4			V
		(18)		VddSD1 − 0.4			V
		(19)		VddSD2 − 0.4			V

Table 19. DC CHARACTERISTICS (continued)
(Vdd2= 2.7 V to 3.6V, VddRTC = 0.9 V to 1.1 V, VddSD0 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6V, VddSD2 = 2.7 V to 3.6 V, VddQSPI = 2.7 V to 3.6 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output L Voltage	V_{OL}	(10)(12)	I_{OL} = 1 mA			0.4	V
		(11)				0.4	V
		(10)(13)(14)	I_{OL} = 2 mA			0.4	V
		(11)				0.4	V
		(15)				0.4	V
		(12)				0.4	V
		(10)(13)	I_{OL} = 4 mA			0.4	V
		(11)				0.4	V
		(12)				0.4	V
		(16)	I_{OL} = 6 mA			0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(13)	I_{OL} = 8 mA			0.4	V
		(16)				0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(16)	I_{OL} = 10 mA			0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(20)	I_{OL} = 0.3 mA			0.3	V
Pull−up Resister	Rup	(28)		25		75	kΩ
		(29)		10		100	kΩ
		(30)		18		50	kΩ
Pull−down Resister	Rdn	(25)		25		75	kΩ
		(26)		10		100	kΩ
		(27)		10		100	kΩ
Input Leak Current	I_{IL}	(1)(2)(3)(4) (5)(6)(7)(8) (9)(21)	VI = Vdd* = Vss	−10		10	μA
Output Leak Current	I_{OZ}	(10)(11)(12)(13) (14)(15)(16)(17) (18)(19)(20)	HiZ output	−10		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 20. DC CHARACTERISTICS

(Vdd2 = 1.7 V to 1.95 V, VddSD0 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, VddSD2 = 1.7 V to 1.95 V, VddQSPI = 1.7 V to 1.95 V, AVddDAMPL = 0.93 V to 1.95 V, AVddDAMPR = 0.93 V to 1.95 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H Voltage	V_{IH}	(1)	CMOS	0.7 × Vdd2			V
		(2)		0.7 × VddSD0			V
		(3)		0.7 × VddSD1			V
		(4)		0.7 × VddSD2			V
		(5)	Schmitt	0.75 × Vdd2			V
		(21)		0.75 × VddSD1			V
		(6)		0.75 × VddSD2			V
		(7)		0.75 × VddQSPI			V
Input L Voltage	V_{IL}	(1)	CMOS			0.3 × Vdd2	V
		(2)				0.3 × VddSD0	V
		(3)				0.3 × VddSD1	V
		(4)				0.3 × VddSD2	V
		(5)	Schmitt			0.25 × Vdd2	V
		(21)				0.25 × VddSD1	V
		(6)				0.25 × VddSD2	V
		(7)				0.25 × VddQSPI	V

Table 20. DC CHARACTERISTICS (continued)
(Vdd2 = 1.7 V to 1.95 V, VddSD0 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, VddSD2 = 1.7 V to 1.95 V, VddQSPI = 1.7 V to 1.95 V, AVddDAMPL = 0.93 V to 1.95 V, AVddDAMPR = 0.93 V to 1.95 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output H Voltage	V_{OH}	(10)(12)	I_{OH} = −0.5 mA	Vdd2 – 0.4			V
		(11)		VddQSPI – 0.4			V
		(10)(13)(14)	I_{OH} = –1 mA	Vdd2 – 0.4			V
		(11)		VddQSPI – 0.4			V
		(15)		VddSD1 – 0.4			V
		(12)		VddSD2 – 0.4			V
		(10)(13)	I_{OH} = –2 mA	Vdd2 – 0.4			V
		(11)		VddQSPI – 0.4			V
		(12)		VddSD2 – 0.4			V
		(16)	I_{OH} = –3 mA	VddQSPI – 0.4			V
		(17)		VddSD0 – 0.4			V
		(18)		VddSD1 – 0.4			V
		(19)		VddSD2 – 0.4			V
		(13)	I_{OH} = –4 mA	Vdd2 – 0.4			V
		(16)		VddQSPI – 0.4			V
		(17)		VddSD0 – 0.4			V
		(18)		VddSD1 – 0.4			V
		(19)		VddSD2 – 0.4			V
		(23)	I_{OH} = –8 mA (Note 46)	AvddDAMPL – 0.4			V
		(24)	I_{OH} = –8 mA (Note 46)	AvddDAMPR – 0.4			V
		(16)	I_{OH} = –5 mA	VddQSPI – 0.4			V
		(17)		VddSD0 – 0.4			V
		(18)		VddSD1 – 0.4			V
		(19)		VddSD2 – 0.4			V

Table 20. DC CHARACTERISTICS (continued)
(Vdd2 = 1.7 V to 1.95 V, VddSD0 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, VddSD2 = 1.7 V to 1.95 V, VddQSPI = 1.7 V to 1.95 V, AVddDAMPL = 0.93 V to 1.95 V, AVddDAMPR = 0.93 V to 1.95 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output L Voltage	V_{OL}	(10)(11)(12)	I_{OL} = 0.5 mA			0.4	V
		(10)(13)(14)	I_{OL} = 1 mA			0.4	V
		(11)				0.4	V
		(15)				0.4	V
		(12)				0.4	V
		(10)(13)	I_{OL} = 2 mA			0.4	V
		(11)				0.4	V
		(12)				0.4	V
		(16)	I_{OL} = 3 mA			0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(13)	I_{OL} = 4 mA			0.4	V
		(16)				0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(23)	I_{OL} = 8 mA (Note 41)			0.4	V
		(24)	I_{OL} = 8 mA (Note 41)			0.4	V
		(16)	I_{OL} = 5 mA			0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
Pull−up Resister	Rup	(28)		25		75	kΩ
		(29)		30		200	kΩ
		(30)		18		50	kΩ
Pull−down Resister	Rdn	(25)		25		75	kΩ
		(26)		30		200	kΩ
Input Leak Current	I_{IL}	(1)(2)(3)(4) (5)(6)(7)(8) (9)(21)	VI = Vdd* = Vss	−10		10	μA
Output Leak Current	I_{OZ}	(10)(11)(12)(13) (14)(15)(16)(17) (18)(19)	HiZ output	−10		10	μA
		(23)(24)		−10		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

41. Set DAMPCTL register as below.
    − DZCTL: DSLEEP=1. (don't care DSL value)
    − G DZINP: DZINP14=1, other DZINPx=0
    This DC characteristics can be applied while Class−D AMP used as GPO.

(1) SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA1, SDRDATA0
(2) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00
(3) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27)
(4) TXD1(GPIO04), RXD1(GPIO05), TIOCA01(GPIO0A), CTS1(GPIO56), RTS1(GPIO57)
(5) TEST, NRES, BMODE1, BMODE0, TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), NCS0(GPIO06), SCL0(GPIO07), SDA0(GPIO08), NCS1(GPIO10), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), NLBEXA0(GPIO16), NRD(GPIO17), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), SDRADDR12(GPIO2A), SCL1(GPIO2B), SDA1(GPIO2C), SDRADDR11(GPIO2D), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), NWRENWRL(GPIO30), NHBNWRH(GPIO31), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), SWDCLK(GPIO58), SWDIO(GPIO59), XTALINFO1, XTALINFO0
(6) TIOCA00(GPIO09), TMS(GPIO28), TCK(GPIO29)
(7) SCK1(GPIO0D), SDI1(GPIO0E), SDO1(GPIO0F), SWP1(GPIO11), SHOLD1(GPIO12), TIOCB01(GPIO03), TXD2(GPIO0B), RXD2(GPIO0C)
(8) VDET, RTCMODE
(9) BACKUPB, KEYINT2, KEYINT1, KEYINT0
(10) TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), SCL0(GPIO07), SDA0(GPIO08), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), SCL1(GPIO2B), SDA1(GPIO2C), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), SWDCLK(GPIO58)
(11) TXD2(GPIO0B), RXD2(GPIO0C)
(12) TMS(GPIO28), TCK(GPIO29)
(13) SDRWE, SDRRAS, SDRDQM1, SDRDQM0, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA1, SDRDATA0, SDRCS, SDRCLK, SDRCKE, SDRCAS, SDRBA1, SDRBA0, SDRADDR9, SDRADDR8, SDRADDR7, SDRADDR6, SDRADDR5, SDRADDR4, SDRADDR3, SDRADDR2, SDRADDR10, SDRADDR1, SDRADDR0, NCS0(GPIO06), NCS1(GPIO10), NLBEXA0(GPIO16), NRD(GPIO17), SDRADDR12(GPIO2A), SDRADDR11(GPIO2D), NWRENWRL(GPIO30), NHBNWRH(GPIO31), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), XTALINFO1, XTALINFO0
(14) BMODE1, BMODE0, SWDIO(GPIO59)
(15) TDI(GPIO20), TDO(GPIO21)
(16) TIOCB01(GPIO03), SCK1(GPIO0D), SDI1(GPIO0E), SDO1(GPIO0F), SWP1(GPIO11), SHOLD1(GPIO12)
(17) SDCMD0, SDCLK0, SDAT03, SDAT02, SDAT01, SDAT00
(18) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27)
(19) TXD1(GPIO04), RXD1(GPIO05), TIOCA00(GPIO09), TIOCA01(GPIO0A), CTS1(GPIO56), RTS1(GPIO57)
(20) RTCINT
(21) TDI(GPIO20), TDO(GPIO21)
(23) LOUT(used as GPLOUT)
(24) ROUT(used as GPROUT)
(25) BMODE1, BMODE0
(26) SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA1, SDRDATA0, SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), TIOCB01(GPIO03), TXD1(GPIO04), RXD1(GPIO05), SCL0(GPIO07), SDA0(GPIO08), TIOCA00(GPIO09), TIOCA01(GPIO0A), TXD2(GPIO0B), RXD2(GPIO0C), SCK1(GPIO0D), SDI1(QIO0)(GPIO0E), SDO1(QIO1)(GPIO0F), SWP1(QIO2)(GPIO11), SHOLD1(QIO3)(GPIO12), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), NLBEXA0(GPIO16), NRD(GPIO17), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), TDI(GPIO20), TDO(GPIO21), SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27), TMS(GPIO28), TCK(GPIO29), SDRADDR12(GPIO2A), SCL1(GPIO2B), SDA1(GPIO2C), SDRADDR11(GPIO2D), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), NWRENWRL(GPIO30), NHBNWRH(GPIO31), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), CTS1(GPIO56), RTS1(GPIO57), SWDCLK(GPIO58)
(27) KEYINT2, KEYINT1, KEYINT0
(28) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, BMODE1, BMODE0, TXD1(GPIO04), RXD1(GPIO05), TIOCA00(GPIO09), TIOCA01(GPIO0A), SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27), CTS1(GPIO56), RTS1(GPIO57)
(29) TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), TIOCB01(GPIO03), NCS0(GPIO06), SCL0(GPIO07), SDA0(GPIO08), TXD2(GPIO0B), RXD2(GPIO0C), SCK1(GPIO0D), SDI1(QIO0)(GPIO0E), SDO1(QIO1)(GPIO0F), NCS1(GPIO10), SWP1(QIO2)(GPIO11), SHOLD1(QIO3)(GPIO12), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), TDI(GPIO20), TDO(GPIO21), TMS(GPIO28), TCK(GPIO29), SDRADDR12(GPIO2A), SCL1(GPIO2B), SDA1(GPIO2C), SDRADDR11(GPIO2D), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), SWDCLK(GPIO58), SWDIO(GPIO59), XTALINFO1, XTALINFO0
(30) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00

PLL Characteristics

PLL1 (System)

Table 21. PLL1 (SYSTEM) ($V_{DD}1$ (Note 42) = 0.93 to 1.27 V, T_A = −20°C to +65°C)

Item	Symbol	Condition	AV_{DD}PLL1 = 0.93 to 1.1 V			AV_{DD}PLL1 = 1.1 to 1.3 V			Unit
			Min	Typ	Max	Min	Typ	Max	
VCO Voltage	VCNT1		0		AV_{DD} PLL1	same as left			V
The VCO Highest Oscillation Frequency	Fmax		200			360			MHz
The VCO Lowest Oscillation Frequency	Fmin				90			180	MHz
Phase Comparison Frequency	Fref				48	same as left			MHz
PLL Lock Time	Tlock1 (Note 44)	Fref >= 32.768 KHz		38	52	same as left			ms
	Tlock2 (Note 44)	Fref >= 1 MHz		3.5	5	same as left			ms
Jitter (Note 43)	Jitter			±3.19	±5.42		±4.28	±7.28	%

42. Power up and power down timing of AV_{DD}PLL1 and Vdd1 should be as close as possible.
43. Result of simulation
44. PLL lock time and appropriate LPF circuit depend on Phase comparison frequency (Fref).
    Refer to 5−2 PLL1(System) for appropriate LPF circuit

PLL2 (Audio)

Table 22. PLL2 (AUDIO) ($V_{DD}1$ (Note 45) = 0.93 to 1.27 V, T_A = −20°C to +65°C)

Item	Symbol	Condition	AV_{DD}PLL2 = 0.93 to 1.1 V			Unit
			Min	Typ	Max	
VCO voltage	VCNT2		0		AV_{DD}PLL2	V
The VCO Highest Oscillation Frequency	Fmax		150			MHz
The VCO Lowest Oscillation Frequency	Fmin				95	MHz
Phase Comparison Frequency	Fref				1	MHz
PLL Lock Time	Tlock1 (Note 47)	Fref ≥ 6.4 KHz		37	50	ms
	Tlock2 (Note 47)	Fref ≥ 38.4 KHz		14	20	ms
Jitter (Note 46)	Jitter			±3.28	±5.58	%

45. Power up and power down timing of AV_{DD}PLL2 and Vdd1 should be as close as possible
46. Result of simulation
47. Phase comparison frequency(Fref) depends on frequency of xtal oscillation as described in the table below.
    PLL lock time and appropriate LPF circuit depend on Fref.
    − Tlock1 is derived from the case when XT1 is one of 12, 20, 24, 48 MHz.
    − Tlock2 is derived from the case when XT1 is 24 MHz.
    Refer to 5 − 3 PLL2(Audio) for appropriate LPF circuit

Table 23.

XT1 Frequency [MHz]	VCO Frequency [MHz] (Note 48)	Sampling Frequency F_S	PLL2 Divide	PLL2 Multiply	Phase Comparison Frequency Fref [KHz]
12	147.456	48 KHz	125	1536	96
	135.4752	44.1 KHz	625	7056	19.2
	98.304	32 KHz	125	1024	96
20	147.456	48 KHz	625	4608	32
	135.4752	44.1 KHz	3125	21168	6.4
	98.304	32 KHz	625	3072	32
24	147.456	48 KHz	125	768	192
	135.4752	44.1 KHz	625	3528	38.4
	98.304	32 KHz	125	512	192
48	147.456	48 KHz	125	384	384
	135.4752	44.1 KHz	625	1764	76.8
	98.304	32 KHz	125	256	384

48. VCO frequency = $768 \times F_S \times 4$

PLL3 (Audio)

Table 24. PLL3 (AUDIO) ($V_{DD}1$ = 0.93 to 1.27 V, T_A = −20°C to +65°C)

Item	Symbol	Condition	AV_{DD}PLL3 = 0.93 to 1.1 V			Unit
			Min	Typ	Max	
VCO Voltage	VCNT3		0		AV_{DD}PLL3	V
The VCO Highest Oscillation Frequency	Fmax		150			MHz
The VCO Lowest Oscillation Frequency	Fmin				95	MHz
Phase Comparison Frequency	Fref				1	MHz
PLL Lock Time	Tlock			32	42	ms
Jitter (Note 49)	Jitter			±3.37	±4.38	%

49. Result of simulation.

Class−D AMP

Table 25. CLASS−D AMP ($V_{DD}1$ = 0.93 to 1.27 V, T_A = −20°C to +65°C)

Item	Symbol	Condition	AV_{DD}DAMPL = AV_{DD}DAMPR = 0.93 to 1.65 V			Unit
			Min	Typ	Max	
On Resistance	Ron	On resistance is set to minimum by register. (Note 50)	0.5	1.5	4.0	Ω

50. Set 0x3ff00 to Drivability set register ZINP of ProgrammersModel_DAMPCTL.

XTAL Characteristics

Table 26. XTAL CHARACTERISTICS ($V_{DD}1$ (Note 51) = 0.93 to 1.27 V, T_A = −20°C to +65°C)

Item	Symbol	Condition	VddXT1 = 0.93 to 1.1V			VddXT1 = 1.1 to 1.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
Frequency	Fmax		1		20	1		50	MHz

51. Power up and power down timing of VddXT1 and Vdd1 should be as close as possible.
Note that the oscillation frequency of XT1 that can be used with this product depends on the function used. Please refer to the following table. For example, only 48 MHz is available for USB Host function.

Table 27.

Function to be Used	Available Frequency of XT1 (X means available)				
	12 MHz	20 MHz	24 MHz	48 MHz	Other than the Left
USB Device	x	x	x	x	
USB Host				x	
ROM boot	x	x	x	x	(Note 52)

52. During ROM boot, some clock frequencies are determined based on the XTALINFO[1:0] input and the frequency of XT1 other than 12/20/24/48 MHz may cause functional error.
However, because there is a possibility that the difference of the frequency is acceptable in some extent, please contact our representative if needed.

The requirements of XT1 are below to use USB Host or USB Device function.

- Frequency deviation： ±200 ppm or less
- Jitter: ±50 ps or less

XTALINFO[1:0] port should be set in accordance with the frequency of XT1.

Some products which don't have XTALINFO[1:0] port, select the appropriate products which set XTALINFO[1:0] internally in accordance with the frequency of XT1.
(Regarding the product name, please contact our representative).

10bit ADC Converter Characteristic

Table 28. 10BIT ADC CONVERTER CHARACTERISTIC
(T_A = 25°C, $V_{DD}1$ = 1.2 V, $AV_{DD}ADC$ = 3.0 V, FVIN = 1 kHz (Note 53))

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin Applied
ADC Power−supply Voltage	AVDH		2.7	−	3.6	V	$AV_{DD}ADC$
ADC GND Voltage	AVDL		0	−	−	V	$AV_{SS}ADC$
ADC Reference Voltage High	VRH		AVDH × 3/4	−	AVDH	V	VRH
ADC Reference Voltage Low	VRL		AVssADC	−	AVDH × 1/4	V	VRL
Decoupling Capacity	CREF		0.047	−	−	µF	VR
Analog Input Voltage	AN		VRL	−	VRH	V	AN[5:0]
ADC Resolution	BIT		−	−	10	Bit	AN[5:0]
Reference Resistance	RR	(Note 55)	7.3	9	10.7	kΩ	VRH, VRL
ADC Conversion Frequency (Note 60)	Fs		−	−	1000	KS/s	
ADC Operation Clock Frequency (Note 60)	Fc	(Note 56)	2	−	20	MHz	
		(Note 57)	2		5	MHz	
Number of ADC Conversion Clocks (Note 60)	Nc		12	−	−	1/Fc	
Number of ADC Sample Holding Clocks (Note 60)	Ns		2	−	−	1/Fc	
ADC Sample Holding Time (Sampling Time) (Note 60)	Tstc		1	−	−	µs	

Table 28. 10BIT ADC CONVERTER CHARACTERISTIC (continued)
(T_A = 25°C, $V_{DD}1$ = 1.2 V, $AV_{DD}ADC$ = 3.0 V, FVIN = 1 kHz (Note 53))

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin Applied
While it Stabilizes of Ladder (Resumption Time)	Tstr		−	−	(Note 56)		
0 Scale Offset Voltage (Transit Voltage from 0 to 1)	VZT	(Note 58)	Typ−20	VRL + (VRH−VRL)/ 1024	Typ +20	mV	AN[5:0]
Full−scale Offset Voltage (Transit Voltage from 1022 to 1023)	VFST	(Note 58)	Typ−20	VRH − (VRH−VRL)/ 1024	Typ +20	mV	AN[5:0]
Differential Linearity Error	DNL	(Note 59)	−1.5	−	+1.5	LSB	AN[5:0]
Linearity Error	INL	(Note 59)	−2.0	−	+2.0	LSB	AN[5:0]

*Each electrical specification is the results of simulation.

53. Each electrical characteristic is specified under the condition which VR terminal is connected with analog ground through 0.1 μF decoupling capacitor and the voltage is independently supplied to VRH and VRL.
54. A normal conversion result is not obtained immediately after the power supply turning on and immediately after the return from the state of the power down. The time to get a normal performance depends on the state of the terminal VR as shown in the following table.
For example, it takes about 2 ms until a normal conversion result can be obtained when VR terminal is connected with analog ground through 0.1 μF decoupling capacitor.

Terminal VR	T_{STR}
Decoupled	1.0 ms × CREF / 0.047 μF
Not Decoupled (Include no VR Terminal)	1 μs

55. Between VRH and VRL
56. The terminal VR is decoupled.
57. The terminal VR is not decoupled (include no VR terminal)
58. VZT, VFST depend on analog driver output impedance(Rimp) of AN[5:0]

Rimp(Ω)	VZT			VFST		
	Min	Typ	Max	Min	Typ	Max
1000	typ − 20	VRL+(VRH−VRL)/1024	typ + 20	typ − 20	VRH−(VRH−VRL)/1024	typ + 20
10000	typ − 32	VRL+(VRH−VRL)/1024	typ + 20	typ − 20	VRH−(VRH−VRL)/1024	typ + 25
100000	typ − 125	VRL+(VRH−VRL)/1024	typ + 20	typ − 35	VRH−(VRH−VRL)/1024	typ + 65

59. 1LSB = (VFST−VZT)/1022 , INLn = ((1LSB x n+VZT)−Vn)/1LSB , DNLn = (Vn+1−Vn)/1LSB−1
INL depends on analog driver output impedance(Rimp) of AN[5:0]

Rimp(Ω)	INL		
	Min	Typ	Max
1000	−2.0	−	2.0
10000	−3.0	−	3.0
100000	−12.0	−	12.0

60. Tstc(ADC sample holding time) must satisfy following formula, too.
Tstc > tA (Tstc = (1/Fc) × Ns)
- Fc: Frequency of reference clock of ADC(AD_CLK).
Refer to ADC specifications for the method of generating AD_CLK.
- Ns: fADCSMPL + 2.5.
fADCSMPL can be set by the register. Refer to ADC specifications.
- tA: Time decided by output impedance (Rimp) of analog input driver of AN[5:0] (value of tA)
  - In case of VR terminal is decoupled

Rimp	tA
1	117
3.3	118
10	118
33	119
100	124
330	141
1000	199
3300	433
10000	1150
33000	3600
100000	10785

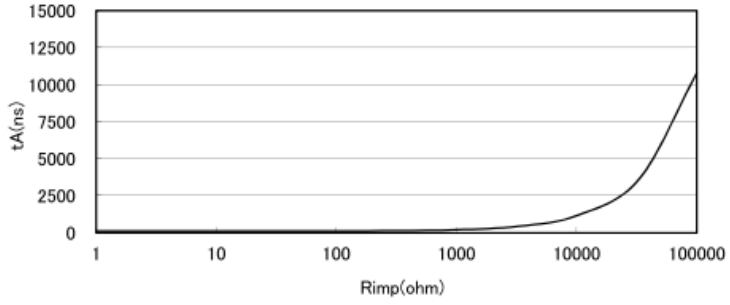


Figure 8.

– In case of VR terminal is not decoupled(include the products w/o VR terminal)

Rimp	tA
1	332
3.3	335
10	332
33	335
100	336
330	346
1000	380
3300	540
10000	1183
33000	3600
100000	10622

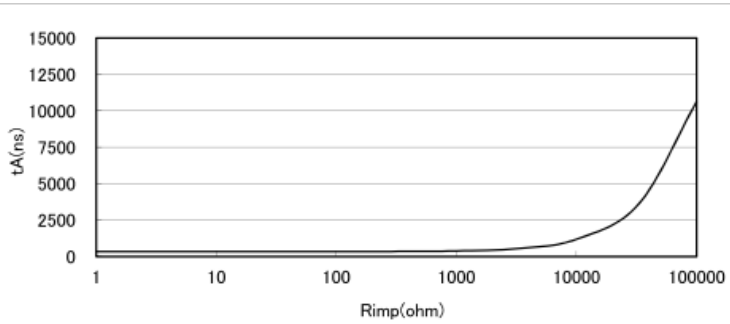


Figure 9.

- $F_C = F_S \times (N_S + N_C)$

USB2.0 PHY Characteristics

Table 29. USB2.0 PHY CHARACTERISTICS

(T_A = 25°C, V_{DD}1 = 1.2 V, AV_{DD}USBPHY1 = DV_{DD}USBPHY1 = 1.2 V, AV_{DD}USBPHY2 = 3.3 V)

Item	Symbol	Condition	Min	Max	Unit
INPUT LEVELS FOR FULL−SPEED:					
High−level Input Voltage (Drive)	V_{IH}		2.0		V
High−level Input Voltage (Floating)	V_{IHZ}		2.7	3.6	
Low−level Input Voltage	V_{IL}			0.8	V
Differential Input Sensitivity	V_{DI}	|(D+) − (D−)|	0.2		V
Differential Common Mode Range	V_{CM}	Includes V_{DI} range Figure 10	0.8	2.5	V
OUTPUT LEVELS FOR FULL−SPEED:					
High−level Output Voltage	V_{OH}	R_L of 14.25 kΩ to V_{SS}	2.8	3.6	V
Low−level Output Voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output Signal Crossover Point Voltage	V_{CRS}	Figure 10	1.3	2.0	V

Table 29. USB2.0 PHY CHARACTERISTICS (continued)
(T_A = 25°C, $V_{DD}1$ = 1.2 V, AV_{DD}USBPHY1 = DV_{DD}USBPHY1 = 1.2 V, AV_{DD}USBPHY2 = 3.3 V)

Item	Symbol	Condition	Min	Max	Unit
INPUT CAPACITANCE FOR FULL−SPEED:					
Downstream Facing Port (beginning shared with Upstream Facing Port at Device mode, so the less value is selected as the maximum spec)	C_{IND} (V_{INUB})			100	pF
Transceiver Edge Rate Control Capacitance	C_{EDGE}			75	pF
TERMINATION IN FULL−SPEED:					
Bus Pull−Up Resistor on Upstream Port (Idle Bus) (This is Used only for the Device Mode (RPUENXEN = '0' Setting))	R_{PUI}		0.9	1.575	kΩ
Bus Pull−Up Resistor on Upstream Port (Upstream Port Receiving) (This is Used Only for the Device Mode (RPUENXEN = '0' Setting))	R_{PUA}		1.425	3.090	kΩ
Input Impedance Exclusive of pullup/pulldown	Z_{INP}		300		kΩ
Termination Voltage on Upstream Port Pull−Up	V_{TERM}		3.0	3.6	V
DRIVER CHARACTERISTICS IN FULL−SPEED:					
Rise Time (10% − 90%)	T_{FR}		4	20	ns
Fall Time(10% − 90%)	T_{FF}		4	20	ns
Difference Rise and Fall Time Matching	T_{FRFM}		90	111.11	%
CLOCK TIMING IN FULL−SPEED(INTERNAL SIGNAL FSSEL='0'):					
Full−speed Data Rate for hubs and Devices which are High−speed Capable	$T_{FDRATHS}$		11.994	12.006	Mb/s
FULL−SPEED DATA TIMINGS(INTERNAL SIGNAL FSSEL='0'):					
Source Jitter Total (Including Frequency Tolerance): To Next Transition For Paired Transitions	 T_{DJ1} T_{DJ2}		 −3.5 −4	 3.5 4	 ns ns
Source Jitter for Differential Transition to SE0 Transition	T_{FDEOP}		−2	5	ns
Receiver Jitter: To Next Transitions For Paired Transitions	 T_{JR1} T_{JR2}		 −18.5 −9	 18.5 9	 ns ns
Source SE0 Interval of EOP	T_{FEOPT}		160	175	ns
Receiver SE0 Interval of EOP	T_{FEOPR}		82		ns
Width of SE0 Interval During Differential Transition	T_{FST}			14	ns
INPUT LEVELS FOR HIGH−SPEED:					
High−speed Squelch Detection Threshold (Differential Signal)	V_{HSSQ}		100	200	mV
High−speed Disconnect Detection Threshold (Differential Signal)	V_{HSDSC}		525	625	mV
High−speed Data Signaling Common Mode Voltage Range	V_{HSCM}		−50	500	mV
High−speed Differential Input Signaling Level (This Spec is Based on 'Template 6')	Figure 11				
OUTPUT LEVELS FOR HIGH−SPEED:					
High−speed Idle State	V_{HSOI}		−10.0	10	mV
High−speed Data Signaling High	V_{HSOH}		360	440	mV
High−speed Data Signaling Low	V_{HSOL}		−10.0	10	mV
Chirp J Level (Different Signal)	V_{CHIRPJ}		700	1100	mV
Chirp K Level (Different Signal)	V_{CHIRPK}		−900	−500	mV

Table 29. USB2.0 PHY CHARACTERISTICS (continued)
(T_A = 25°C, $V_{DD}1$ = 1.2 V, AV_{DD}USBPHY1 = DV_{DD}USBPHY1 = 1.2 V, AV_{DD}USBPHY2 = 3.3 V)

Item	Symbol	Condition	Min	Max	Unit
TERMINATION IN HIGH−SPEED:					
Termination Voltage in High−speed	V_{HSTERM}		−10.0	10	mV
DRIVER CHARACTERISTICS IN HIGH−SPEED:					
Rise Time(10% − 90%)	V_{HSR}		500		ps
Fall Time(10% − 90%)	V_{HSF}		500		ps
Driver Waveform Requirement	Complying with USB2.0 Specification (section 7.1.2)				
Driver Output Resistance (which also serves as high−speed termination)	Z_{HSDRV}		40.5	49.5	Ω
CLOCK TIMING IN HIGH−SPEED:					
High−Speed Data Rate	T_{HSDRAT}		479.76	480.24	Mb/s
HIGH−SPEED DATA TIMINGS:					
Data Source Jitter	Complying with USB2.0 Specification (section 7.1.2)				
Receiver Jitter Tolerance					
INPUT LEVELS FOR LOW−SPEED:SAME AS FULL−SPEED					
OUTPUT LEVELS FOR LOW−SPEED: SAME AS FULL−SPEED					
INPUT CAPACITANCE FOR LOW−SPEED: SAME AS FULL−SPEED					
TERMINATIONS IN LOW−SPEED: SAME AS FULL−SPEED					
DRIVER CHARACTERISTICS IN LOW−SPEED:					
Rise Time (10% − 90%)	T_{LR}		75	300	ns
Fall Time (10% − 90%)	T_{LF}		75	300	ns
Difference Rise and Fall Time Matching	T_{LRFM}		80	125	%
TERMINATIONS USED AS HOST SIDE (INTERNAL SIGNAL RPDPEN = 1, RPDMEN = 1):					
Bus Pull−down Resistor on Downstream Facing Port	R_{PD}		14.25	24.80	kΩ

*Each electrical specification is the results of simulation.

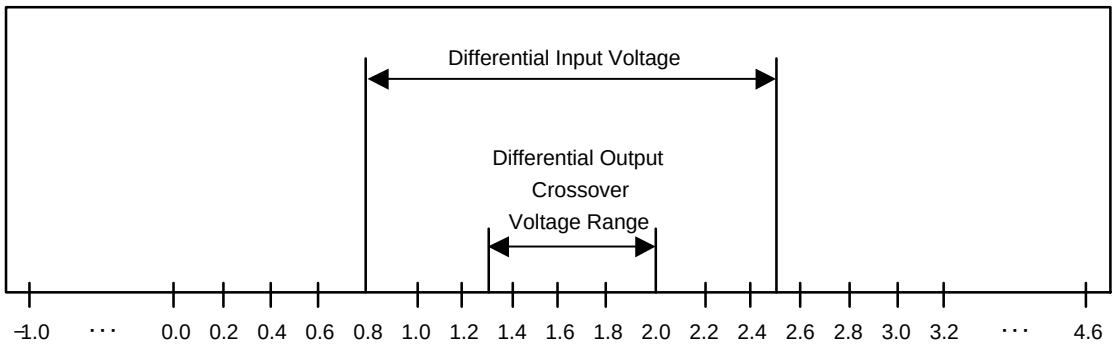


Figure 10. Differential Input Sensitivity Range for Full−speed

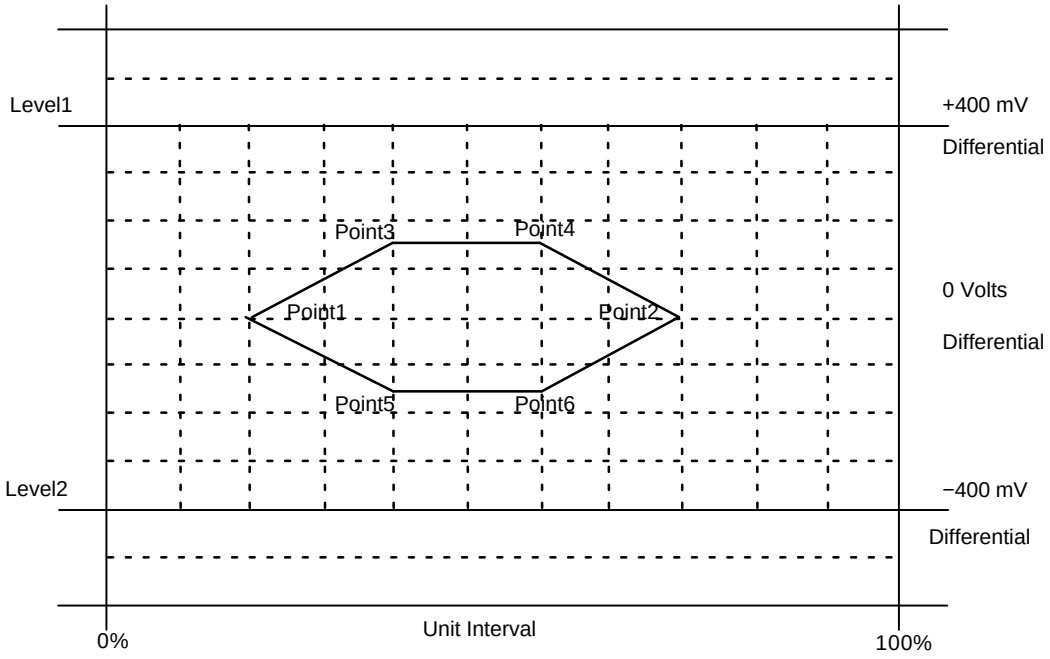


Figure 11. Differential Input Sensitivity Range for High−speed

AC Characteristics

Reset

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$ = 1.7 to 1.95 V or 2.7 V to 3.6 V
  External load 15 pF to 40 pF

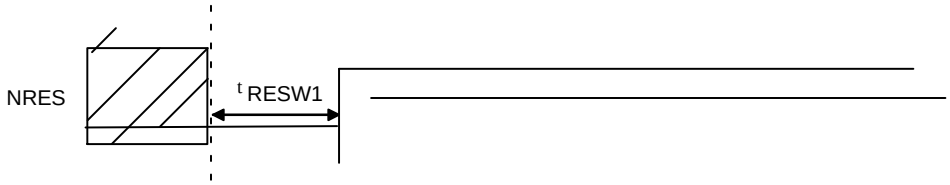


Figure 12. AC Characteristic − Reset

Table 30.

Item	Symbol	Condition	Min	Typ	Max	Unit
Resetting active period	tRESW1	Time after Vdd* reaches to recommended operating voltage	10	−	−	μs

*Refer to the interrupt controller (INTC) specification ProgrammersModel_INTC us for more detail in case of using noise filter, etc.

External Interrupt

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$, $V_{DD}SD1$, $V_{DD}SD2$, $V_{DD}QSPI$ = 1.7 to 1.95 V or 2.7 V to 3.6 V
  External load 15 pF to 40 pF

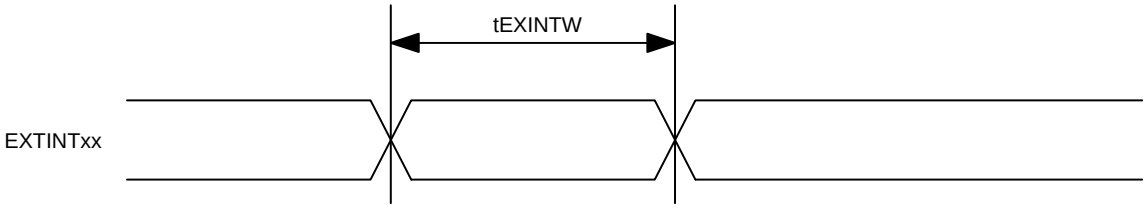


Figure 13. AC Characteristic − External Interrupt

Table 31.

Item	Symbol	Condition	Min	Typ	Max	Unit
Pulse width of External Interrupt	tEXINTW	Set of Interruption Factor not Use Noise Filter Function	2	−	−	T

61. T: BASICCLK clock rate (frequency = Farm)

I²C

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$ = 1.7 V to 1.95 V or
  2.7 V to 3.6 V
  External load 15 pF to 40 pF

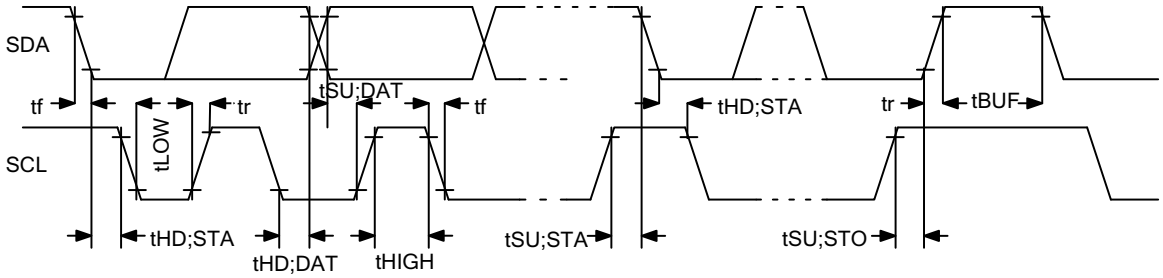


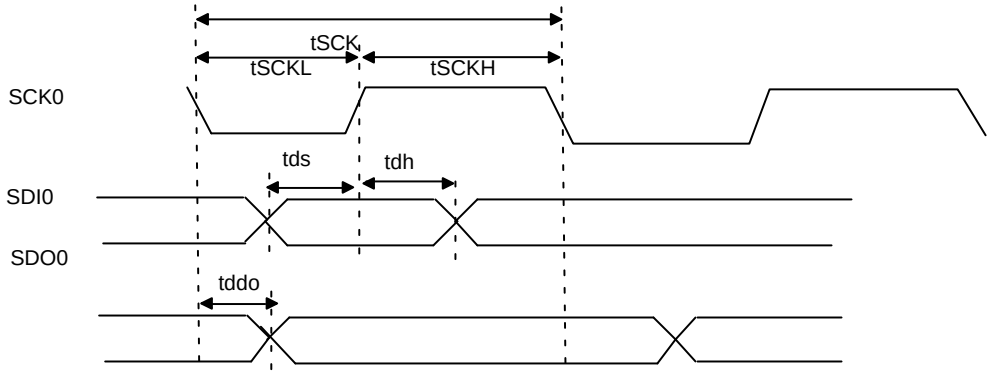
Figure 14. AC Characteristics − I²C

Table 32.

Item	Symbol	Standard Mode		Full Mode		Unit
		Min	Max	Min	Max	
SCL Frequency	fSCL	0	100	0	400	kHz
Holding Time START (Repetition) Condition (After this Period, the First Clock Pulse is Generated)	tHD; STA	4.0	–	0.6	–	µs
Low Period of SCL	tLOW	4.7	–	1.3	–	µs
High Period of SCL	tHIGH	4.0	–	0.6	–	µs
Setup Time of Repetition START Condition	tSU; STA	4.7	–	0.6	–	µs
Data Holding Time: (for Master in Accordance with CBUS)	tHD; DAT	5.0	3.45	0	0.9	µs
Data Setup Time	tSU; DAT	250	–	100	–	ns
Rise Time SDA and SCL	Tr	–	1000	–	300	ns
Fall Time SDA and SCL	Tf	–	300	–	300	ns
Setup Time of STOP Condition	tSU; STO	4.0	–	0.6	–	µs
Time of Bus Release between STOP and START Condition	tBUF	4.7	–	1.3	–	µs

SPI Interface

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$ = 1.7 V to 1.95 V or
  2.7 V to 3.6 V
  External load 15 pF to 40 pF



62. Polarity of SCK is changed, SCK of figure is inversed.

Figure 15. AC Characteristics − SPI Interface

Table 33.

Item	Symbol	Condition	Min	Max	Unit
SCLK Rate	tSCK	8		−	T
SCLK LOW Time	tSCKL	4		−	T
SCLK HIGH Time	tSCKH	4		−	T
Data Setup Time	tds	2		−	T
Data Hold Time	tdh	2		−	T
Data Delay Time	tddo	−		2	T

63. T : APB CLK rate (frequency = Fapb).

Serial Flash Interface

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, V_{DD}QSPI = 1.7 V to 1.95 V
  or 2.7 V to 3.6 V
  External load 10 to 30 pF

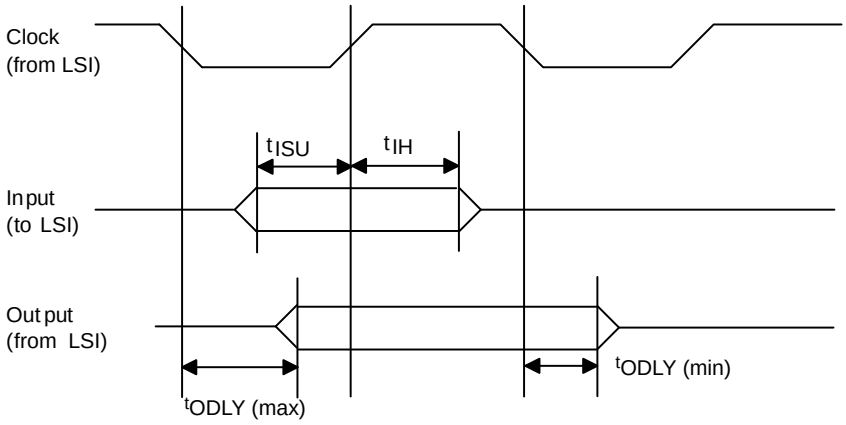


Figure 16. AC Characteristics − Serial Flash Interface

- [applied pin]
  - Clock: SCK1
  - Output: SDI1, SDO1, SWP1, SHOLD1, QSCS output
  - Input: SDI1, SDO1, SWP1, SHOLD1 input

Table 34.

I/O voltage (VddQSPI)		2.7 V to 3.6 V				1.7 V to 1.95 V		
External Load		10 pF to 30 pF				10 pF to 30 pF		
I/O Drivability		8 mA		6 mA		10 mA		
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit
SFIFSEL2 = 0 (Note 64)								
Clock Frequency	f_{clk}	−	41	−	40	−	40	MHz
Input Set−up Time	t_{ISU}	3.4	−	4.3	−	4.5	−	ns
Input Hold−up Time	t_{IH}	7.5	−	7.1	−	6.9	−	ns
Output Delay Time	t_{ODLY}	0.3	5.1	1.2	5.2	0.6	5.4	ns
SFIFSEL2 = 1 (Note 64)								
Clock frequency	f_{clk}	−	42	−	40	−	40	MHz
Input set−up time	t_{ISU}	4.5	−	5.4	−	5.3	−	ns
Input hold−up time	t_{IH}	3.3	−	2.9	−	3.7	−	ns
Output Delay time	t_{ODLY}	0.3	5.1	1.2	5.2	0.6	5.4	ns

64. SFIFSEL2 is the value of S−Flash I/F select register (SFIFSEL) bit2 SFIFSEL2 described in the SystemController ProgrammersModel_SystemController.

XMC External Memory Bus Timing

- [condition]
  $V_{DD}1$ = 0.93 to 1.27 V, $V_{DD}2$ = 2.7 V to 3.6 V
  External load 15 pF to 40 pF

External Memory Bus Read

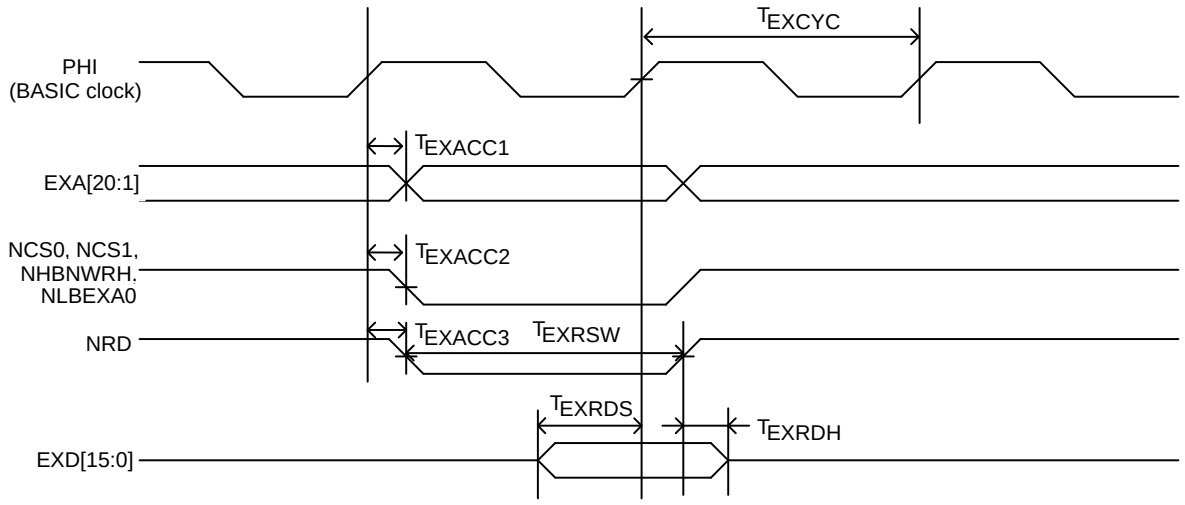


Figure 17. AC Characteristics − External Memory Bus Read Timing

External Memory Bus Write

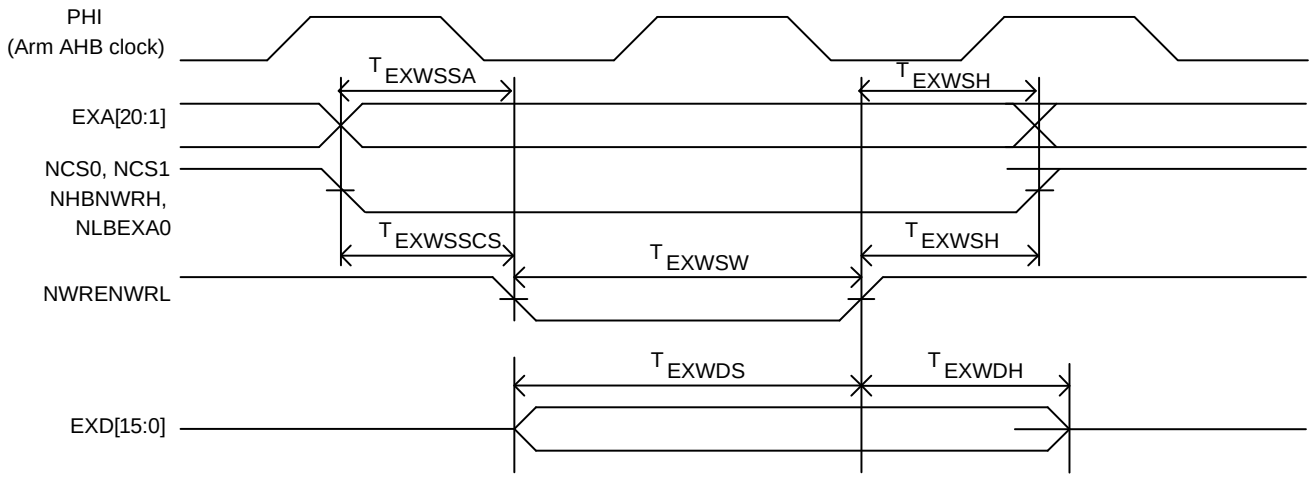


Figure 18. AC Characteristics − External Memory Bus Write Timing

Table 35.

Item	Symbol	Min	Typ	Max	Unit
CPUclock Cycle Time	T_{EXCYC}	–	1T	–	ns
Read Data Access Time	T_{EXACC1}	–	–	13	ns
	T_{EXACC2}	–	–	Tacs + 13	ns
	T_{EXACC3}	–	–	Tacs + Tcos + 12	ns
Read Data Setup Time	T_{EXRDS}	20	–	–	ns
Read Data Hold Time	T_{EXRDH}	0	–	–	ns
Read Strobe Pulse Width	T_{EXRSW}	Tpgwt +1 T_{sub} −12	–	–	ns
Write Strobe Pulse Width	T_{EXWSW} (Note 65)	Tpgwt + 1 T_{sub}−5	–	–	ns
Write Address Setup Time	T_{EXWSSA}	Tacs+Tcos + 0.5 T_{sub}−10	–	–	ns
Write Strobe Setup Time	$T_{EXWSSCS}$	Tcos +0.5 T_{sub} −5	–	–	ns
Write Strobe Hold Time	T_{EXWSH}	Tcoh + 0.5 T_{sub}−5	–	–	ns
Write Data Setup Time	T_{EXWDS} (Note 65)	Tcos+ Tpgwt +1 T_{sub} −10	–	–	ns
Write Data Hold Time	T_{EXWDH}	Tcoh + 0.5 T_{sub}−10	–	Tcoh + 0.5 T_{sub}	ns

65. T: BASIC clock rate (frequency = Farm)

Regarding Tacs, Tcos, Tpgwt, Tcoh, refer to the external memory controller (XMC) specification Programmers Model_XMC.

Even when Tpgwt (programmable wait register) = 1, equivalent to Tpgwt = 0.

SDRAM Interface

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$ = 1.7 V to 1.95 V or
  2.7 V to 3.6 V
  External load 5 to 15 pF

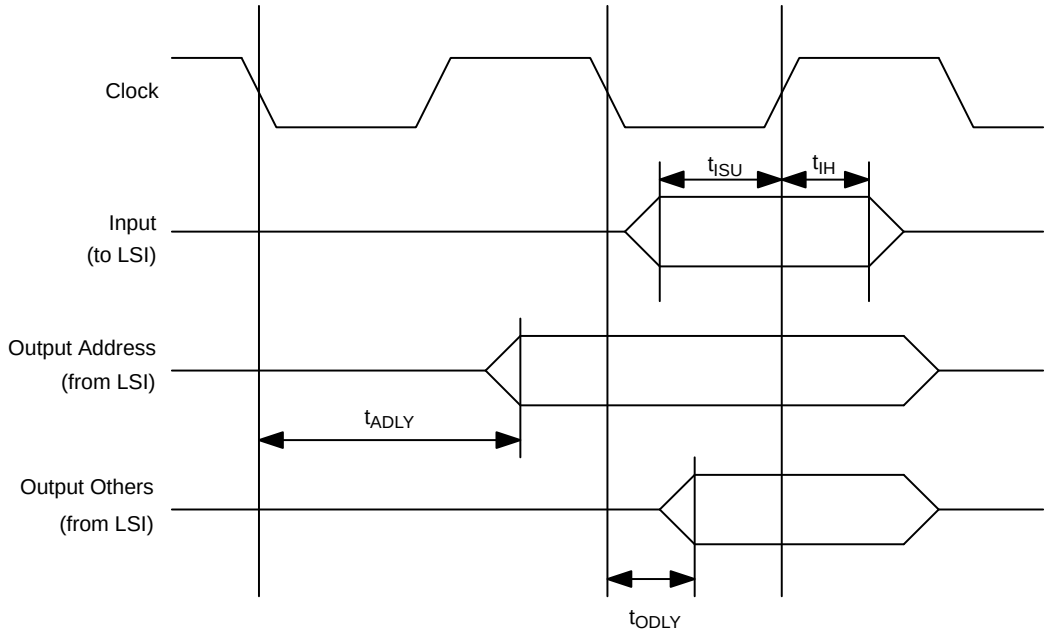


Figure 19. AC Characteristics − SDRAM Interface

- [applied pin]
  - Clock : SDRCLK
  - Output : SDRCKE, SDRCS, SDRWE, SDRCAS, SDRRAS, SDRDQM[1:0], SDRADDR[10:0], SDRBA[1:0], SDRDATA[15:0] output
  - Input : SDRDATA[15:0] input

Table 36.

I/O Voltage ($V_{DD}2$)		2.7 V to 3.6 V		1.7 V to 1.95 V		
External Load		5 pF to 15 pF				
I/O Drivability		4 mA		8 mA		
Item	Symbol	Min	Max	Min	Max	Unit
Clock frequency	f_{clk}	–	65	–	54	MHz
Input set−up time	t_{ISU}	8.3	–	9.9	–	ns
Input hold−up time	t_{IH}	−1.9	–	−2.7	–	ns
Address Delay time	t_{ADLY}	1.0	21.7	0.7	27.3	ns
Output Delay time	t_{ODLY}	−2.9	3.2	−3.3	4.9	ns

66. Address becomes valid 1 cycle before the timing when CS becomes active. Address is stable while CS is active.

Memory Stick Interface

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}SD1$ = 1.7 V to 1.95 V
  or 2.7 V to 3.6 V
  External load 10 pF to 40 pF

Serial Clock Timing

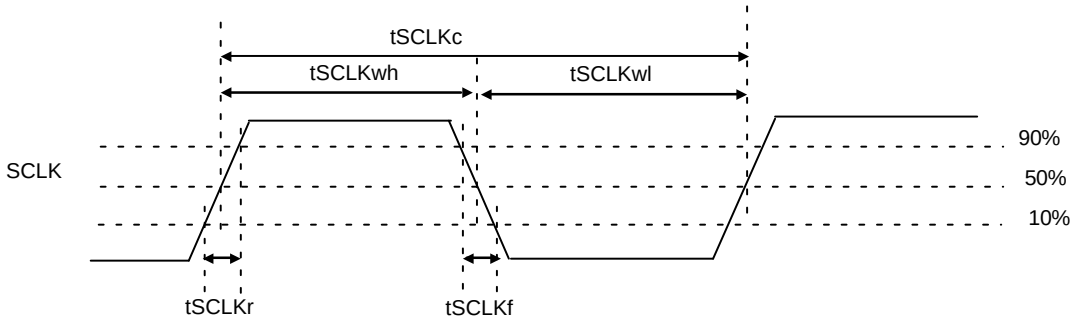


Figure 20. Serial Clock Timing

Table 37.

Item	Symbol	min	max	unit
Clock Period	tSCLKc	50	−	ns
Clock High Level Width	tSCLKwh	15	−	ns
Clock Low Level Width	tSCLKwl	15	−	ns
Clock Rise Time	tSCLKr	−	10	ns
Clock Fall Time	tSCLKf	−	10	ns

Parallel Clock Timing

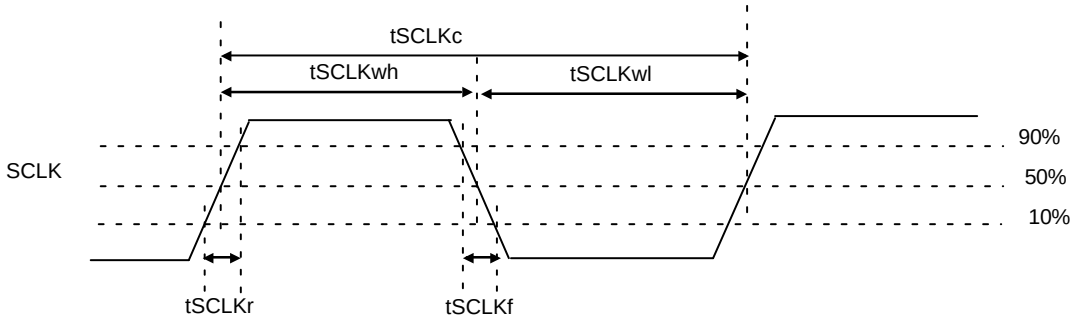


Figure 21. Parallel Clock Timing

Table 38.

Item	Symbol	min	max	unit
Clock Period	tSCLKc	25	−	ns
Clock High Level Width	tSCLKwh	5	−	ns
Clock Low Level Width	tSCLKwl	5	−	ns
Clock Rise Time	tSCLKr	−	10	ns
Clock Fall Time	tSCLKf	−	10	ns

Serial Interface

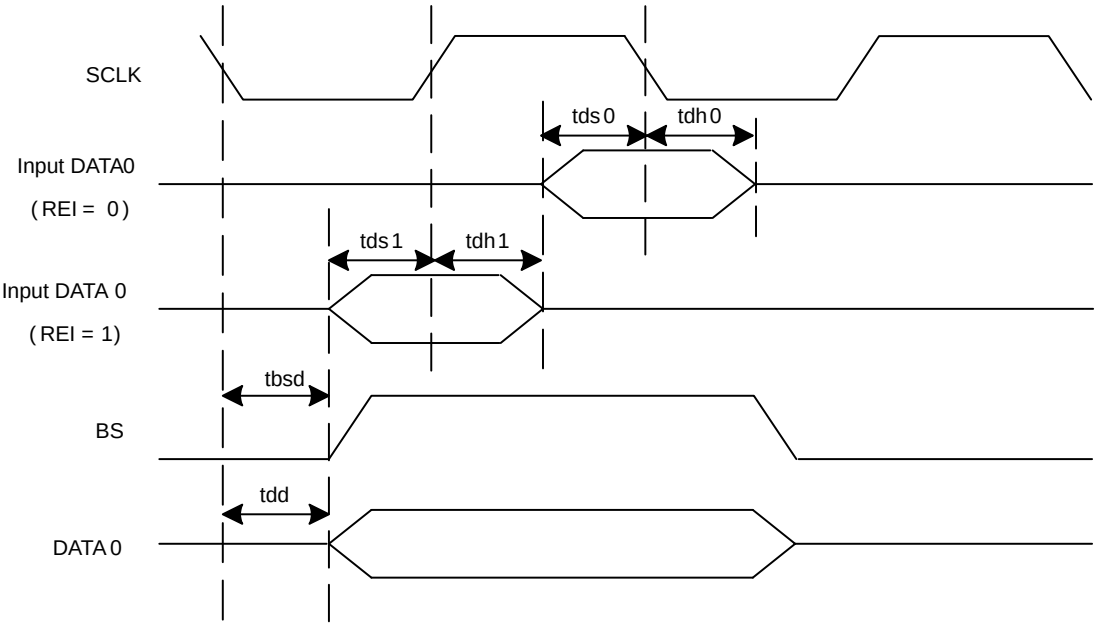


Figure 22. Serial Interface

Table 39.

I/O Voltage		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**				
External Load		**10 pF to 40 pF**		**10 pF to 30 pF**				
I/O Drivability		**8 mA**		**10 mA**		**8 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input setup time (REI=0)	tds0	9.0	−	9.3	−	9.3	−	ns
Input hold time (REI=0)	tdh0	−0.2	−	−0.2	−	−0.4	−	ns
Input setup time (REI=1)	tds1	1.7	−	1.4	−	1.4	−	ns
Input hold time (REI=1)	tdh1	7.0	−	7.1	−	7.2	−	ns
BS Output delay time	tbsd	1.7	5.1	1.7	5.2	2.2	5.3	ns
DATA Output delay time	tdd	1.7	5.1	1.7	5.2	2.2	5.3	ns

Parallel Interface

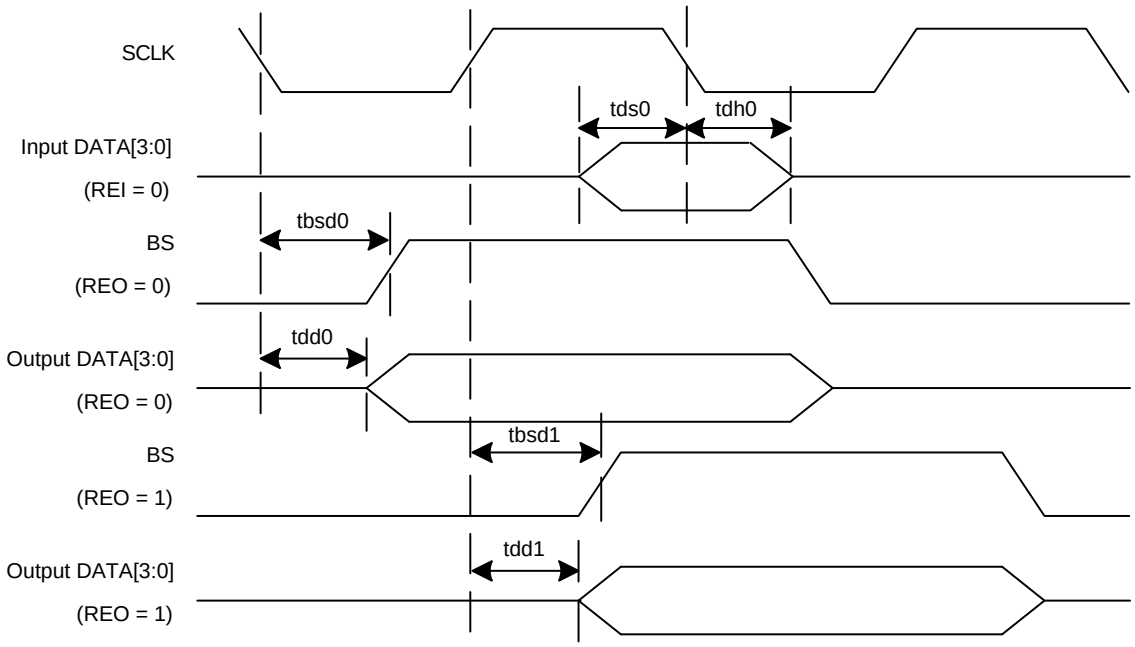


Figure 23. Parallel Interface

Table 40.

I/O Voltage		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**				
External Load		**10 pF to 40 pF**		**10 pF to 30 pF**				
I/O Drivability		**8 mA**		**10 mA**		**8 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input setup time (REI=0)	tds0	9.3	−	9.7	−	9.7	−	ns
Input hold time (REI=0)	tdh0	−0.1	−	−0.4	−	−0.4	−	ns
BS Output delay time (REO=0)	tbsd0	1.2	16.4	1.2	16.5	1.2	16.6	ns
DATA Output delay time (REO=0)	tdd0	1.2	16.4	1.2	16.5	1.2	16.6	ns
BS Output delay time (REO=1)	tbsd1	2.1	4.2	2.1	4.3	2.6	4.4	ns
DATA Output delay time (REO=1)	tdd1	2.1	4.2	2.1	4.3	2.6	4.4	ns

PCM Timing

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$ = 1.7 V to 1.95 V or
  2.7 V to 3.6 V
  External load 5 pF to 15 pF

Master mode

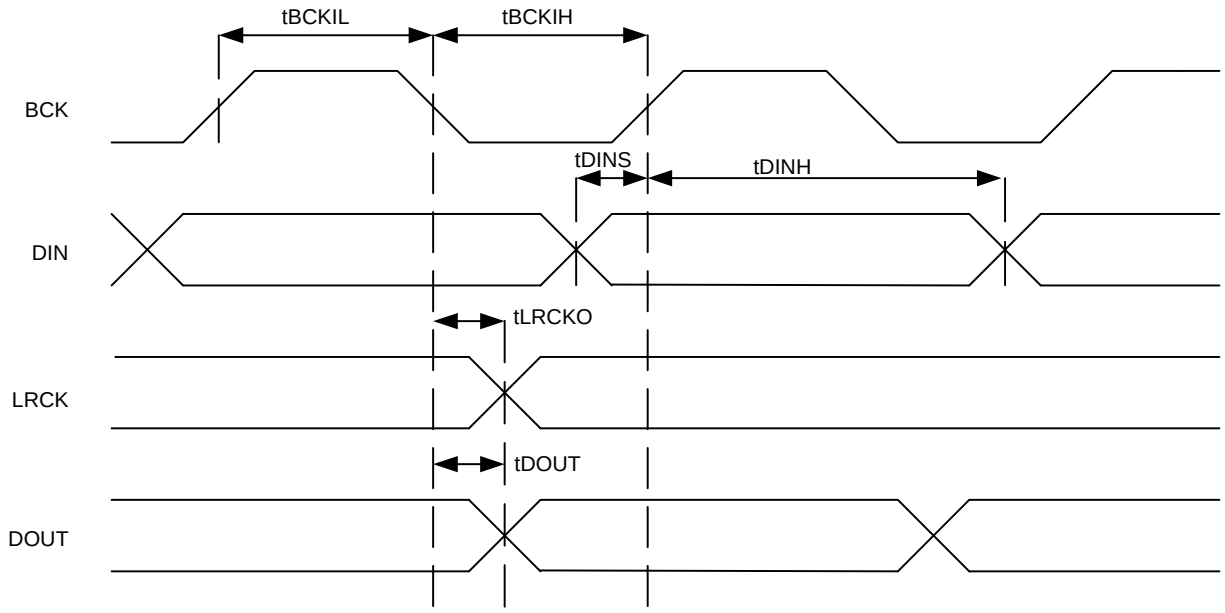


Figure 24. Master Mode

- [Applied pin]
  - Clock : BCK0, BCK1
  - Output : LRCK0, LRCK1, DOUT0, DOUT1 output
  - Input : DIN0, DIN1 input

Table 41.

I/O Voltage ($V_{DD}2$)		1.7 V to 1.95 V / 2.7 V to 3.6 V						
External Load		5 pF to 15 pF						
I/O Drivability		4 mA		2 mA		1 mA		
Item	Symbol	Min	Max	Min	Max	Min	Mix	Unit
BCKI Low Period	tBCKIL	38	−	38	−	38	−	ns
BCKI High Period	tBCKIH	38	−	38	−	38	−	ns
DIN setup Time	tDINS	8	−	8	−	8	−	ns
DIN Hold Time	tDINH	8	−	8	−	8	−	ns
LRCK Delay Time	tLRCKO	−10	10	−10	10	−10	10	ns
DOUT Delay Time	tDOUT	−10	10	−10	10	−10	10	ns

Slave Mode

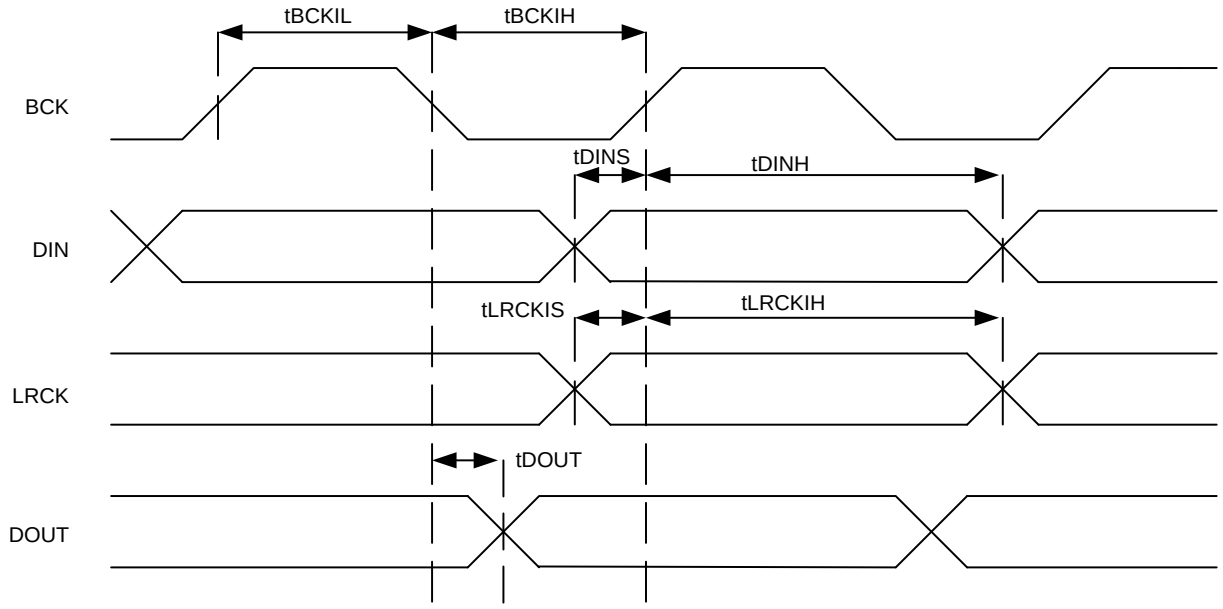


Figure 25. Slave Mode

- [Applied pin]
  - Clock : BCK0, BCK1
  - Output : DOUT0, DOUT1 output
  - Input : LRCK0, LRCK1, DIN0, DIN1 input

Table 42.

I/O Voltage ($V_{DD}2$)		**1.7 V to 1.95 V / 2.7 V to 3.6 V**						
External		**5 pF to 15 pF**						
I/O Drivability		**4 mA**		**2 mA**		**1 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Mix**	**Unit**
BCKI Low Period	tBCKIL	30	−	30	−	30	−	ns
BCKI High Period	tBCKIH	30	−	30	−	30	−	ns
DIN Setup Time	tDINS	8	−	8	−	8	−	ns
DIN Hold Time	tDINH	8	−	8	−	8	−	ns
LRCK Setup Time	tLRCKIS	8	−	8	−	8	−	ns
LRCK Hold Time	tLRCKIH	8	−	8	−	8	−	ns
I/O VOLTAGE($V_{DD}2$) = 1.7 V TO 1.95 V								
DOUT Delay Time	tDOUT	−10	12.1	−10	14.6	−10	19.7	ns
I/O VOLTAGE($V_{DD}2$) = 2.7 V TO 3.6 V								
DOUT Delay Time	tDOUT	−10	10	−10	11.2	−10	14.7	ns

SD Card Interface Timing

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}SD0$, $V_{DD}SD1$,
  $V_{DD}SD2$ = 1.7 V to 1.95 V or 2.7 V to 3.6 V
  External load 10 to 40 pF

Normal(Default) Mode

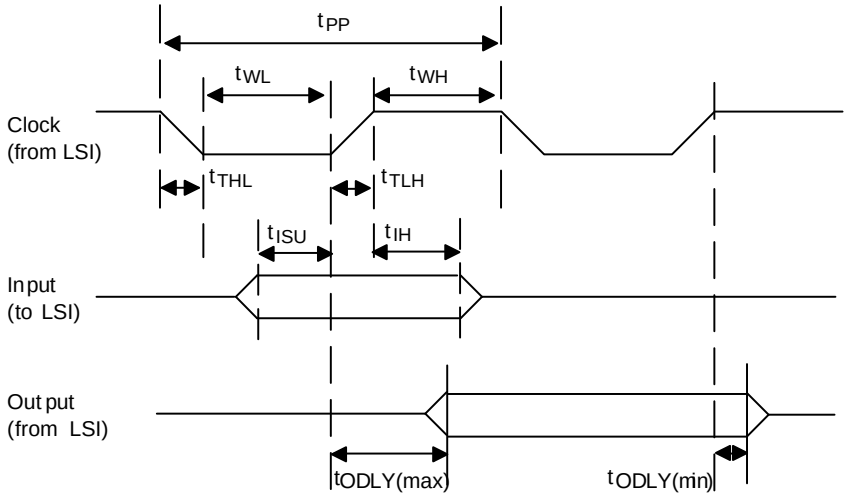


Figure 26. Normal (Default) Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 43.

I/O Voltage ($V_{DD}SD0$, $V_{DD}SD1$, $V_{DD}SD2$)		**2.7 V to 3.6 V**		
External Load		**10 pF to 40 pF**		
I/O Drivability		**8 mA**		
Item	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	25	MHz
Clock Low Time	t_{WL}	10	–	ns
Clock High Time	t_{WH}	10	–	ns
Clock Rise Time	t_{TLH}	–	10	ns
Clock Fall Time	t_{THL}	–	10	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	5.9	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	0	–	ns
Output Delay Time During Data Transfer Mode (from LSI to SD)	t_{ODLY}	5.1	27.8	ns

High−Speed Mode

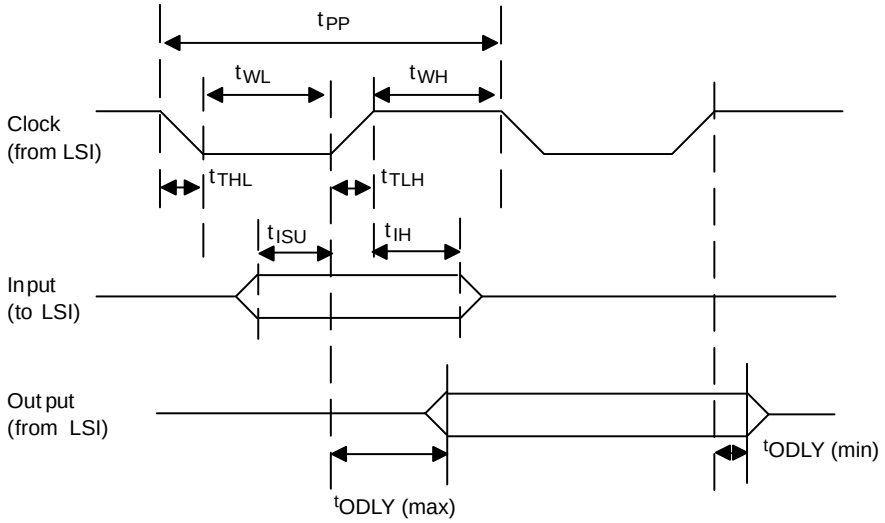


Figure 27. High−Speed Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 44.

I/O Voltage (V_{DD}SD0, V_{DD}SD1, V_{DD}SD2)		**2.7 V to 3.6 V**		
External Load		**10 pF to 40 pF**		
I/O Drivability		**8 mA**		
Item	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	45	MHz
Clock Low Time	t_{WL}	7	–	ns
Clock High Time	t_{WH}	7	–	ns
Clock Rise Time	t_{TLH}	–	3	ns
Clock Fall Time	t_{THL}	–	3	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	5.9	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	2.1	–	ns
Output Delay Time (from LSI to SD)	t_{ODLY}	2.1	15.9	ns

SDR25 Mode

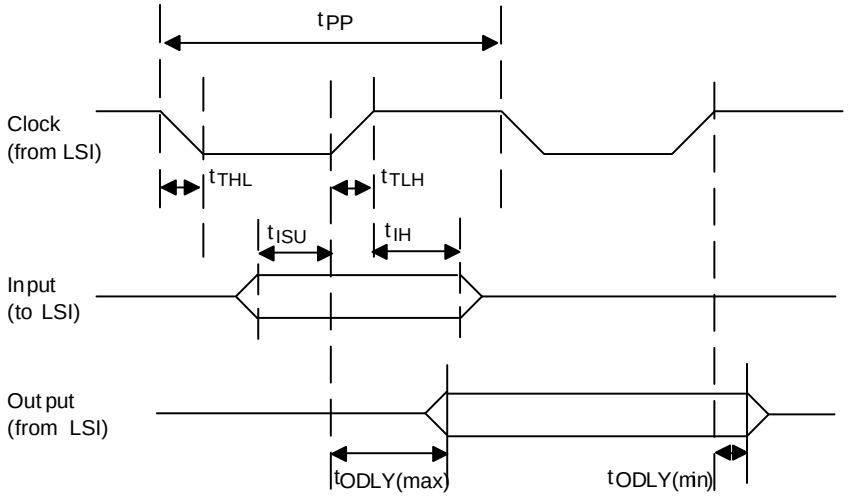


Figure 28. SDR25 Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 45.

I/O Voltage (V_{DD}SD0, V_{DD}SD1, V_{DD}SD2)		**1.7 V to 1.95 V**						
External Load		**10 pF to 30 pF**				**10 pF to 23 pF**		
I/O Drivability		**10 mA**		**8 mA**		**6 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Mix**	**Unit**
Clock Frequency	f_{PP}	0	47	0	47	0	44	MHz
Clock Rise Time	t_{TLH}	–	2.9	–	2.9	–	2.9	ns
Clock Fall Time	t_{THL}	–	2.9	–	2.9	–	2.9	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	6.7	–	6.9	–	8.2	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	0.9	–	0.9	–	0.4	–	ns
Output Delay Time (from LSI to SD)	t_{ODLY}	0.9	11.4	0.9	12.6	0.9	16.2	ns

SDR50 Mode

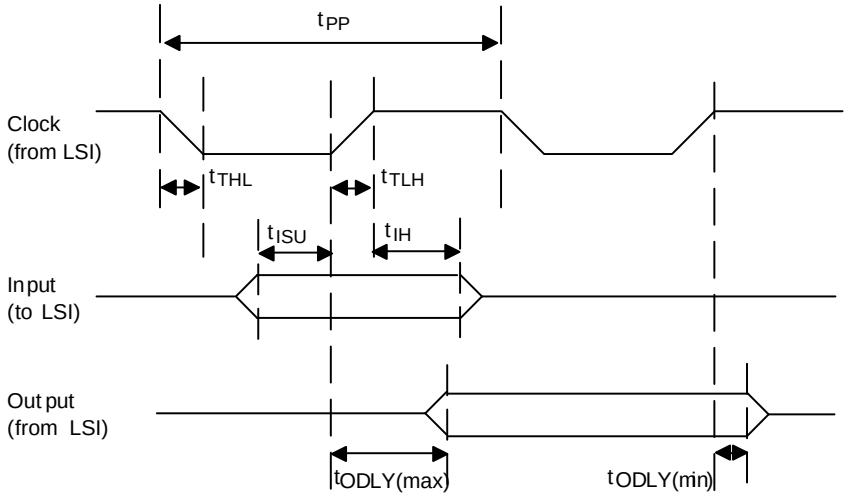


Figure 29. SDR50 Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 46.

I/O Voltage (V_{DD}SD0, V_{DD}SD1, V_{DD}SD2)		**1.7 V to 1.95 V**						
External Load		**10 pF to 30 pF**				**10 pF to 23 pF**		
I/O Drivability		**10 mA**		**8 mA**		**6 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Mix**	**Unit**
Clock Frequency	f_{PP}	0	68	0	63	0	52	MHz
Clock Rise time	t_{TLH}	–	2.9	–	2.9	–	2.9	ns
Clock Fall Time	t_{THL}	–	2.9	–	2.9	–	2.9	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	6.6	–	6.7	–	8.1	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	0.9	–	0.9	–	0.4	–	ns
Output Delay Time (from LSI to SD)	t_{ODLY}	0.9	11.2	0.9	12.4	0.9	16.1	ns

DDR50 Mode

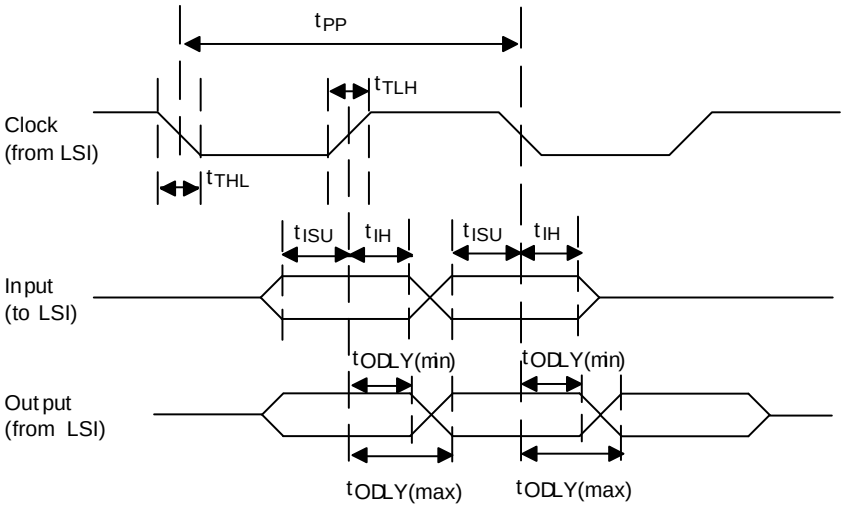


Figure 30. DDR50 Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 47.

I/O Voltage (V_{DD}SD0, V_{DD}SD1, V_{DD}SD2)		**1.7 V to 1.95 V**						
External Load		**10 pF to 30 pF**				**10 pF to 23 pF**		
I/O Drivability		**10 mA**		**8 mA**		**6 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Mix**	**Unit**
Clock Frequency	f_{PP}	0	31	0	29	0	25	MHz
Clock Rise Time	t_{TLH}	–	2.9	–	2.9	–	2.9	ns
Clock Fall Time	t_{THL}	–	2.9	–	2.9	–	2.9	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	7.1	–	7.4	–	9.1	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	1.4	–	1.4	–	1.1	–	ns
Output Delay Time (from LSI to SD)	t_{ODLY}	0.9	11.8	0.9	13.2	0.9	16.6	ns

eMMC Interface Timing

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}SD0$, $V_{DD}SD1$,
  $V_{DD}SD2$ = 1.7 V to 1.95 V or 2.7 V to 3.6 V
  External load 10 to 40pF

Normal(Default) Mode

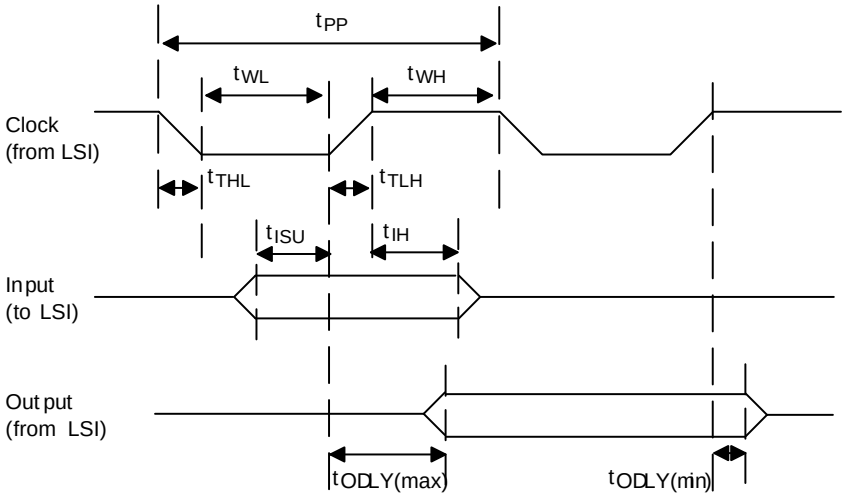


Figure 31. Normal (Default) Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 48.

I/O Voltage ($V_{DD}SD0$, $V_{DD}SD1$, $V_{DD}SD2$)		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**						
External Load		**10 pF to 40 pF**		**10 pF to 30 pF**				**10 pF to 23 pF**		
I/O Drivability		**8 mA**		**10 mA**		**8 mA**		**6 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	26	0	26	0	26	0	26	MHz
Clock Low Time	t_{WL}	10	–	10	–	10	–	10	–	ns
Clock High Time	t_{WH}	10	–	10	–	10	–	10	–	ns
Clock Rise Time	t_{TLH}	–	3	–	3	–	3	–	3	ns
Clock Fall Time	t_{THL}	–	3	–	3	–	3	–	3	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	6.9	–	8.3	–	8.7	–	10.3	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	0.7	–	0	–	0	–	0	–	ns
Output Delay Time (from LSI to SD)	t_{ODLY}	3.1	20.1	3.1	20.1	3.1	20.9	3.1	23.2	ns

High−Speed SDR Mode

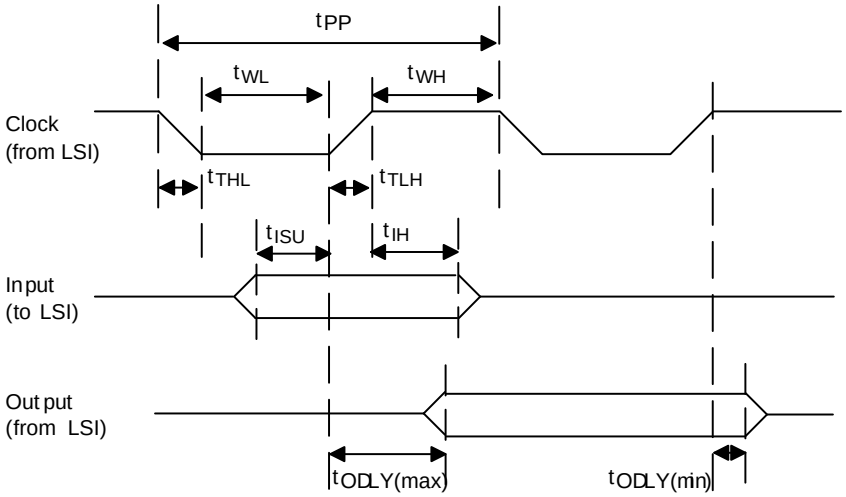


Figure 32. High−Speed SDR Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 49.

I/O Voltage (V_{DD}SD0, V_{DD}SD1, V_{DD}SD2)		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**						
External Load		**10 pF to 40 pF**		**10 pF to 30 pF**				**10 pF to 23 pF**		
I/O Drivability		**8 mA**		**10 mA**		**8 mA**		**6 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	43	0	43	0	43	0	37	MHz
Clock Low Time	t_{WL}	7	–	7	–	7	–	7	–	ns
Clock High Time	t_{WH}	7	–	7	–	7	–	7	–	ns
Clock Rise Time	t_{TLH}	–	3	–	3	–	3	–	3	ns
Clock Fall Time	t_{THL}	–	3	–	3	–	3	–	3	ns
Input Set−up Time (from SD to LSI)	t_{ISU}	5.5	–	6.2	–	6.7	–	8.6	–	ns
Input Hold−up Time (from SD to LSI)	t_{IH}	2.1	–	1.2	–	1.1	–	0	–	ns
Output Delay Time (from LSI to SD)	t_{ODLY}	3.1	19.7	3.1	19.9	3.1	20.2	3.1	23.0	ns

High−Speed DDR Mode

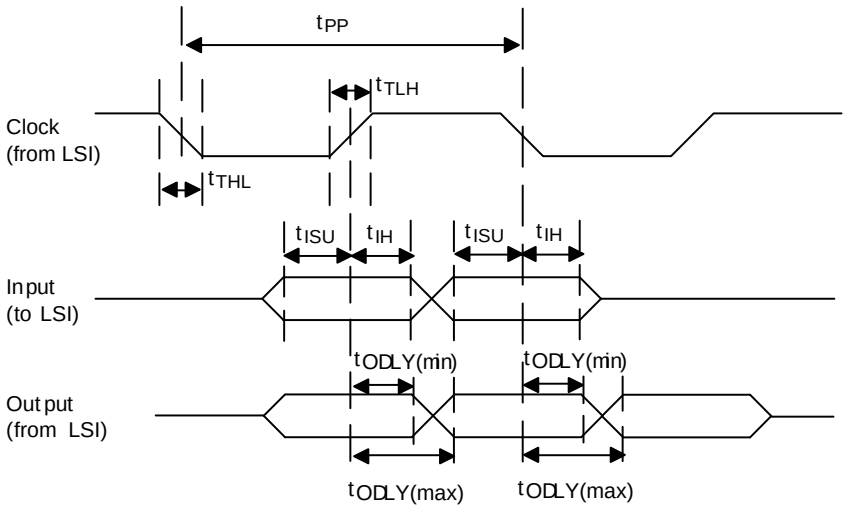


Figure 33. High−Speed DDR Mode

- [Applied pin]
  - Clock : SDCLK0, SDCLK1, SDCLK2
  - Output : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] output
  - Input : SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0] input

Table 50.

I/O Voltage (V_{DD}SD0, V_{DD}SD1, V_{DD}SD2)		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**						
External Load		**10 pF to 40 pF**		**10 pF to 30 pF**				**10 pF to 23 pF**		
I/O Drivability		**8 mA**		**10 mA**		**8 mA**		**6 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	24	0	24	0	23	0	20	MHz
Clock rise time	t_{TLH}	–	3	–	3	–	3	–	3	ns
Clock fall time	t_{THL}	–	3	–	3	–	3	–	3	ns
INPUT CMD										
Input set−up time (from SD to LSI)	t_{ISU}	7.0	–	7.4	–	7.7	–	10.2	–	ns
Input hold−up time (from SD to LSI)	t_{IH}	0.7	–	0.6	–	0.8	–	0	–	ns
OUTPUT CMD										
Output Delay time (from LSI to SD)	t_{ODLY}	3.1	20.5	3.1	20.5	3.1	21.1	3.1	24.1	ns
INPUT DAT										
Input set−up time (from SD to LSI)	t_{ISU}	7.1	–	7.4	–	7.7	–	10.7	–	ns
Input hold−up time (from SD to LSI)	t_{IH}	1.3	–	1.4	–	1.4	–	0	–	ns
OUTPUT DAT										
Output Delay time (from LSI to SD)	t_{ODLY}	2.6	17.8	2.6	17.6	2.6	18.5	2.6	22.2	ns

Digital Mic Timing

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, $V_{DD}2$, V_{DD}QSPI= 1.7 V to 1.95 V or 2.7 V to 3.6 V
  External load 15 pF to 40 pF

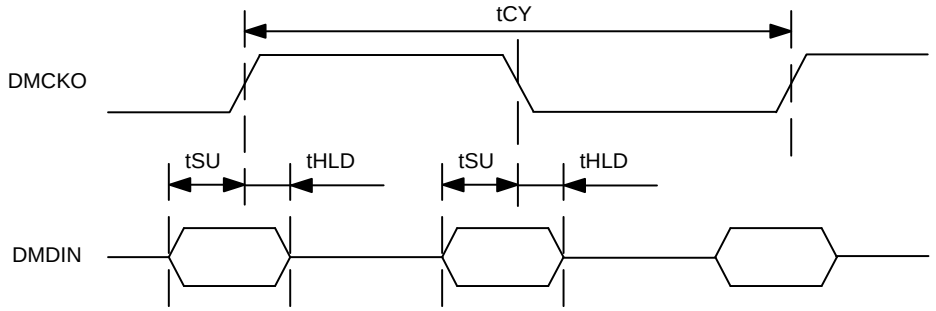


Figure 34. Digital Mic Timing

- [applied pin]
  - Clock : DMCKO0, DMCKO1
  - Input : DMDIN0, DMDIN1

Table 51.

Item	Symbol	Min	Typ	Max	Unit
Period of clock cycle (Note 67)	tCY	−		3.25	MHz
Clock duty		60 : 40		40:60	
Data setup time	tSU	40		−	ns
Data hold time	tHLD	0		−	ns

67. Internal clock and register setting.

UART Timing

- [condition]
  $V_{DD}1$ = 0.93 V to 1.27 V, V_{DD}SD2= 1.7 V to 1.95 V or 2.7 V to 3.6 V
  External load 10 pF to 30 Pf (V_{DD}SD2 = 1.7 V to 1.95 V), 10 pF to 40 pF (V_{DD}SD2 = 2.7 V to 3.6 V)

CTS Timing

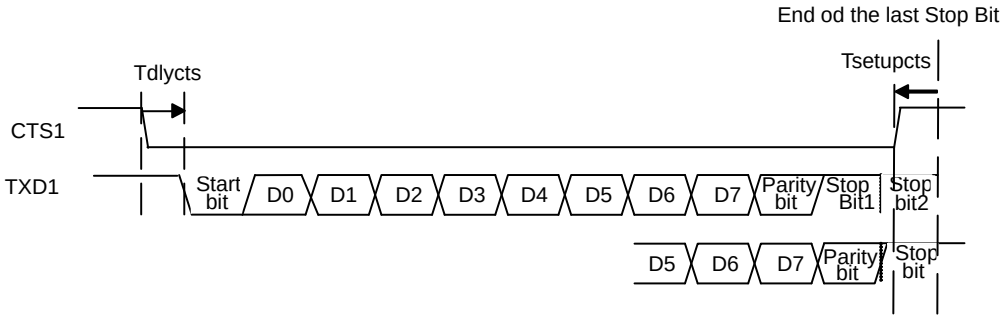


Figure 35. CTS Timing

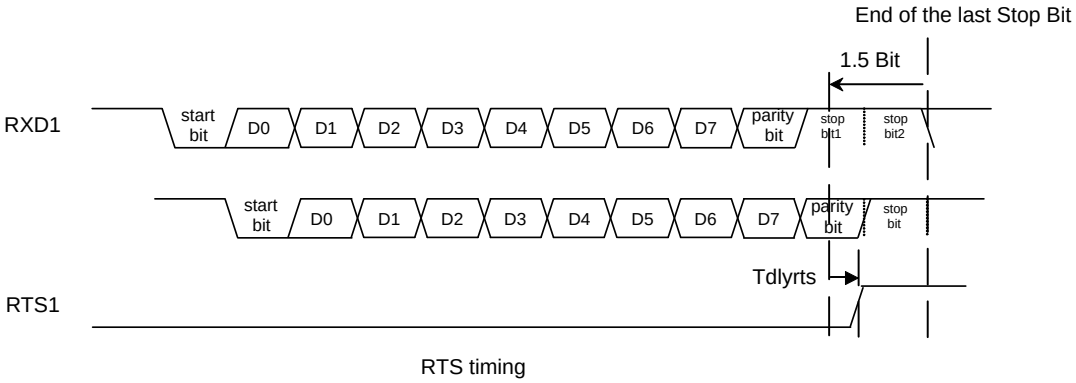
- [applied pin]
  - Input : CTS1
  - Output : TXD1

Table 52.

Item	Condition	Symbol	min	max	unit
Delay Time	Completing preparation to transmit the current TXD data by setting registers at CTS1 = high From the negative edge	Tdlycts	−	6 T + 20	ns
CTS Setup Time (not to transmit the next TXD data)	From end of the last StopBit	Tsetupcts	3 T + 20	−	ns

68. T: UART functional clock rate
69. In using hardware flow control by CTS/RTS, if the CTS setup time above is NOT met, the next TXD data will be transmitted at the time of having prepared it regardless of the CTS level.

RTS Timing



RTS timing

Figure 36. RTS Timing

- [applied pin]
  - Input : RXD1
  - Output : RTS1

Table 53.

Item	Condition	Symbol	min	max	unit
Delay Time	Receiving the current RXD data with 15 data existing in Reception FIFO or Receiving the current RXD data without using Reception FIFO From 1.5 Bit before end of the last StopBit	Tdlyrts	−	4 T + 20	ns

70. T: UART functional clock rate

APPLICATION

XTAL

For Oscillation

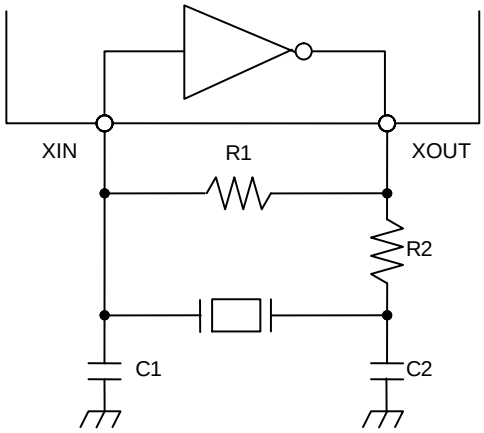


Figure 37. For Oscillation

Table 54.

Symbol	Value		
	XT1 XIN1/XOUT1		XTRTC XIN32K/XOUT32K
	20 MHz	48 MHz	32.768 KHz
R1	1 MΩ	1 MΩ	10 MΩ
R2	0 Ω	0 Ω	0 Ω
C1	3 pF	3 pF	10 pF
C2	3 pF	3 pF	10 pF

71. Optimize the circuit constant for each product when you use this oscillation cell and ask to the manufacturer of the crystal oscillator to investigate (matching investigation) because the best circuit constant changes depending on the specification of the crystal oscillator used and the ambient surrounding (parasitic capacitance etc. of an external substrate).
72. The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.
73. The following may be needed as the anti−noise measures of oscillation circuit.
    - Be adjacent as much as possible, and shorten wiring between elements such as this LSI and the crystal oscillator.
    - GND of the oscillation circuit close to GND (VSS) of this LSI as much as possible.
    - Do not bring the wiring pattern of the large current drive close around the oscillation circuit.
    - Take wide pattern to avoid the effect of interference of other signals.

For Input from External Clock Source (XT1)

Do as follows when use the external clock signal that is generated outside of LSI by the oscillation module, etc. The specification about XTRTC is not available.

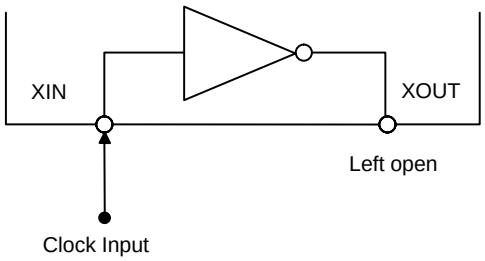


Figure 38. For Input from External Clock Source (XT1)

- Input the signal of full amplitude to XIN (external clock input)

Table 55. (FOR YOUR REFERENCE)

Item	Symbol	Min	Max	Unit
H Level Input Voltage (Note 74)	V_{IH}	$V_{DD}XT1 \times 0.7$	$V_{DD}XT1 + 0.3$	V
L Level Input Voltage (Note 74)	V_{IL}	−0.3	$V_{DD}XT1 \times 0.3$	V
Hysteresis (Note 74)	V_{HYS}	$V_{DD}XT1 \times 0.1$	$V_{DD}XT1 \times 0.4$	V

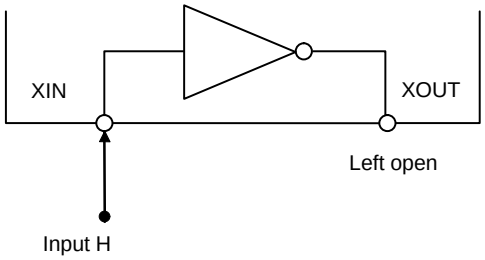
74. No VIH/VIL available to input cell of xtal oscillator.

The schmitt input of xtal oscillator is compliant with (JEDEC Standard JESD8−12A.01 [Normal Range]).

- There is a possibility of influencing the signal quality when there is a long wire pattern on a circuit board of XOUT (The terminal opens). Therefore, recommend to cut the wire pattern on a circuit board or no wire pattern on it.
- The xtal oscillator is supposed to be used with quartz resonator or ceramic resonator, we have no plan to evaluate this LSI in case of external input to xtal oscillator.

XTAL not Used

Do as follows when not use the oscillation cell.



75. Supply the voltage of recommended operating range of $V_{DD}XT1/V_{SS}XT1$ (XIN1/XOUT1) even though XT1 is not used.
76. Supply the voltage of recommended operating range of $V_{DD}RTC/V_{SS}RTC$ (XIN32K/XOUT32K), or recommended operating range of Vdd1 even though XTRTC is not used.

Figure 39. XTAL not Used

PLL1 (System)

The figure below shows the PLL1 circuit. Place the decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

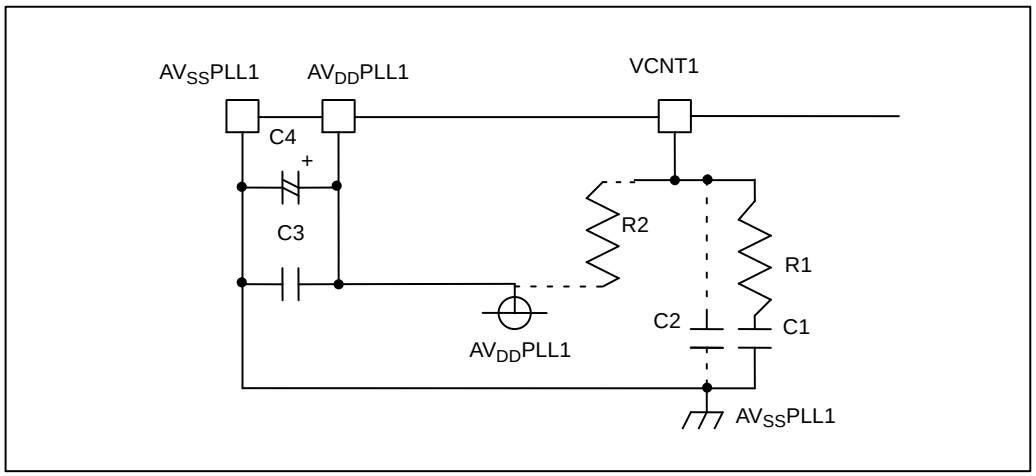


Figure 40. PLL1 (System)

Table 56. PLL1 (SYSTEM)

Symbol	Value1 (Note 78)	Value2 (Note 79)	Serial Number or Accuracy
R1	100 Ω	100 Ω	±5%
R2	*M Ω	*M Ω	±5%
C1	4.7 μF	0.1 μF	Capacitor: ±10% Temperature: ±15% (–20°C to +65°C)
C2	0.047 μF	0.001 μF	
C3	0.1 μF	0.1 μF	
C4	33 μF	33 μF	16CV33BS

77. C4: refers to the part of mounting on the catalog of our company (CV−B S Series).
78. appropriate value for Fref ≥ 32.768 kHz.
79. appropriate value for Fref ≥ 1 MHz.
80. Use R2 basically by unmounting.
    The characteristic of PLL might be improved by mounting R2. Prepare the wire pattern.
81. The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.
82. Connect with decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

PLL2(Audio)

The figure below shows the PLL2 circuit. Place the decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

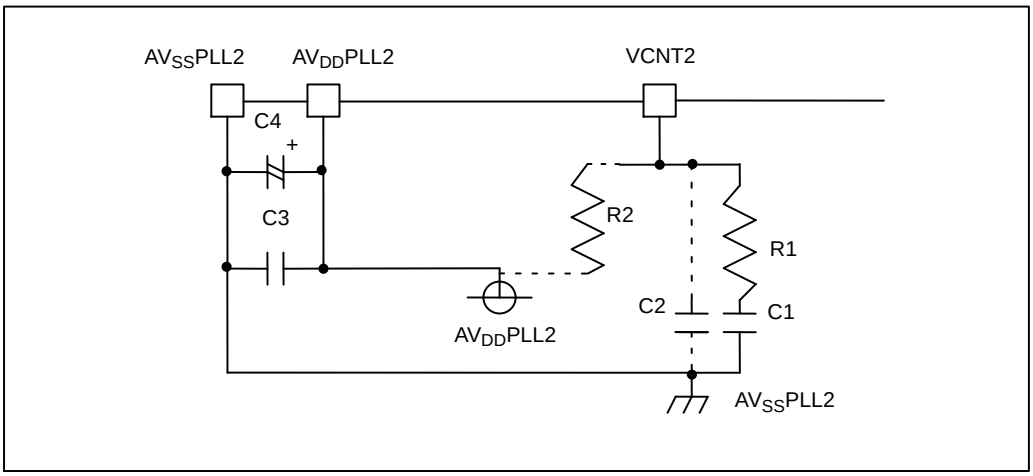


Figure 41. PLL2 (Audio)

Table 57. PLL2 (AUDIO)

Symbol	Value1 (Note 84)	Value2 (Note 85)	Serial Number or Accuracy
R1	120 Ω	560 Ω	±5%
R2	*M Ω	*M Ω	±5%
C1	4.7 μF	0.33 μF	Capacitor : ±10% Temperature : ±15% (–20°C to +65°C)
C2	0.047 μF	0.015 μF	
C3	0.1 μF	0.1 μF	
C4	33 μF	33 μF	16CV33BS

83. C4 : refers to the part of mounting on the catalog of our company (CV−B S Series).
84. appropriate value for Fre ≥ 6.4 kHz
85. appropriate value for Fref ≥ 38.4 kHz
86. Use R2 basically by unmounting.
    The characteristic of PLL might be improved by mounting R2. Prepare the wire pattern.
87. The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.
88. Connect with decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

PLL3 (Audio)

The figure below shows the PLL3 circuit. Place the decoupling capacitor in the terminal neighborhood on the board, and keep low noise by apart from other power supply lines.

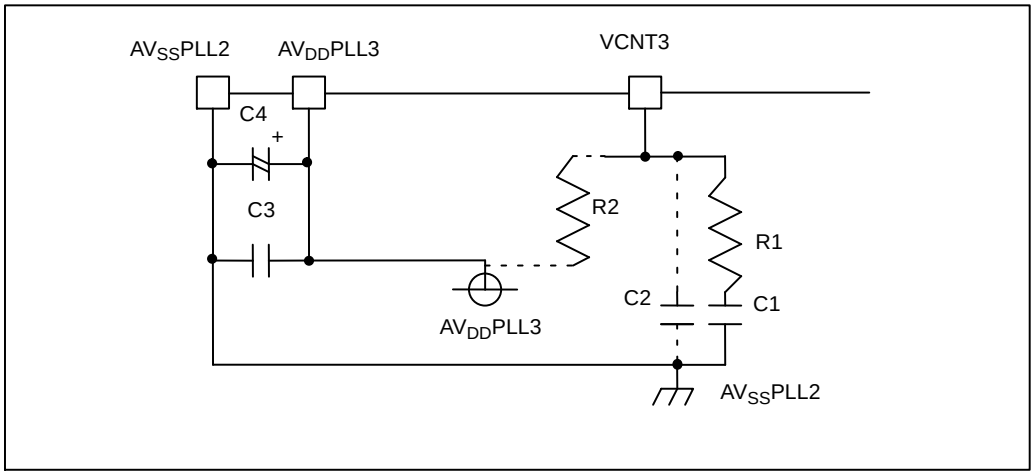


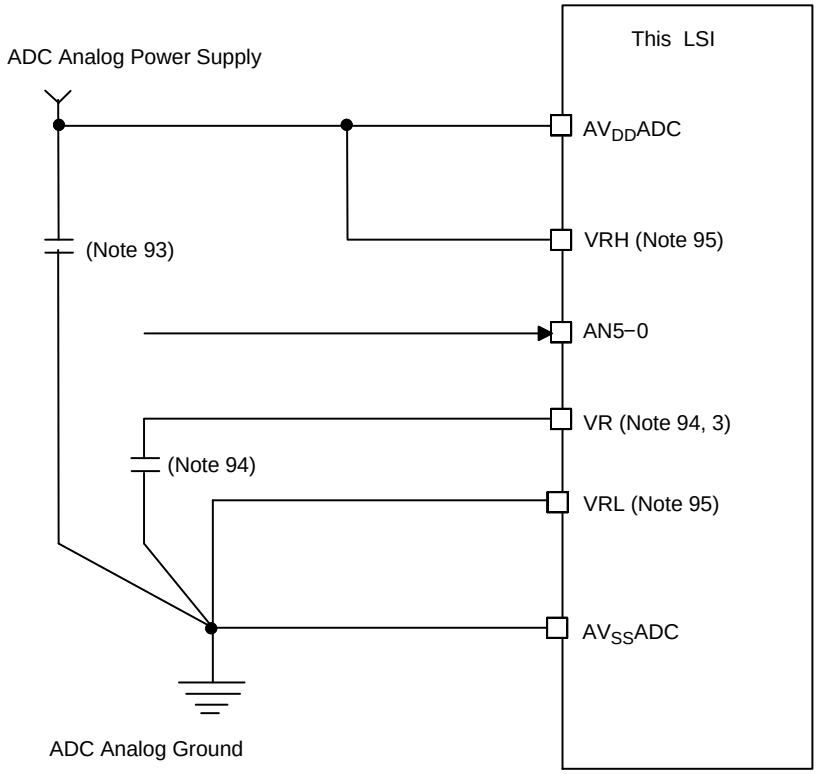
Figure 42. PLL3 (Audio)

Table 58. PLL3 (AUDIO)

Symbol	Value	Serial Number or Accuracy
R1	120 Ω	±5%
R2	*M Ω	±5%
C1	4.7 μF	Capacitor : ±10% Temperature : ±15% (−20°C to +65°C)
C2	0.047 μF	
C3	0.1 μF	
C4	33 μF	16CV33BS

89. C4 : refers to the part of mounting on the catalog of our company (CV−B S Series).
90. Use R2 basically by unmounting.
    The characteristic of PLL might be improved by mounting R2.
    Place the wire pattern.
91. The values of parts are for reference. There is a possibility that the adjustment is needed according to the situation of the set.
92. Connect with decoupling capacitor in the terminal neighborhood on the board,
    and keep low noise by apart from other power supply lines.

10Bit AD Converter



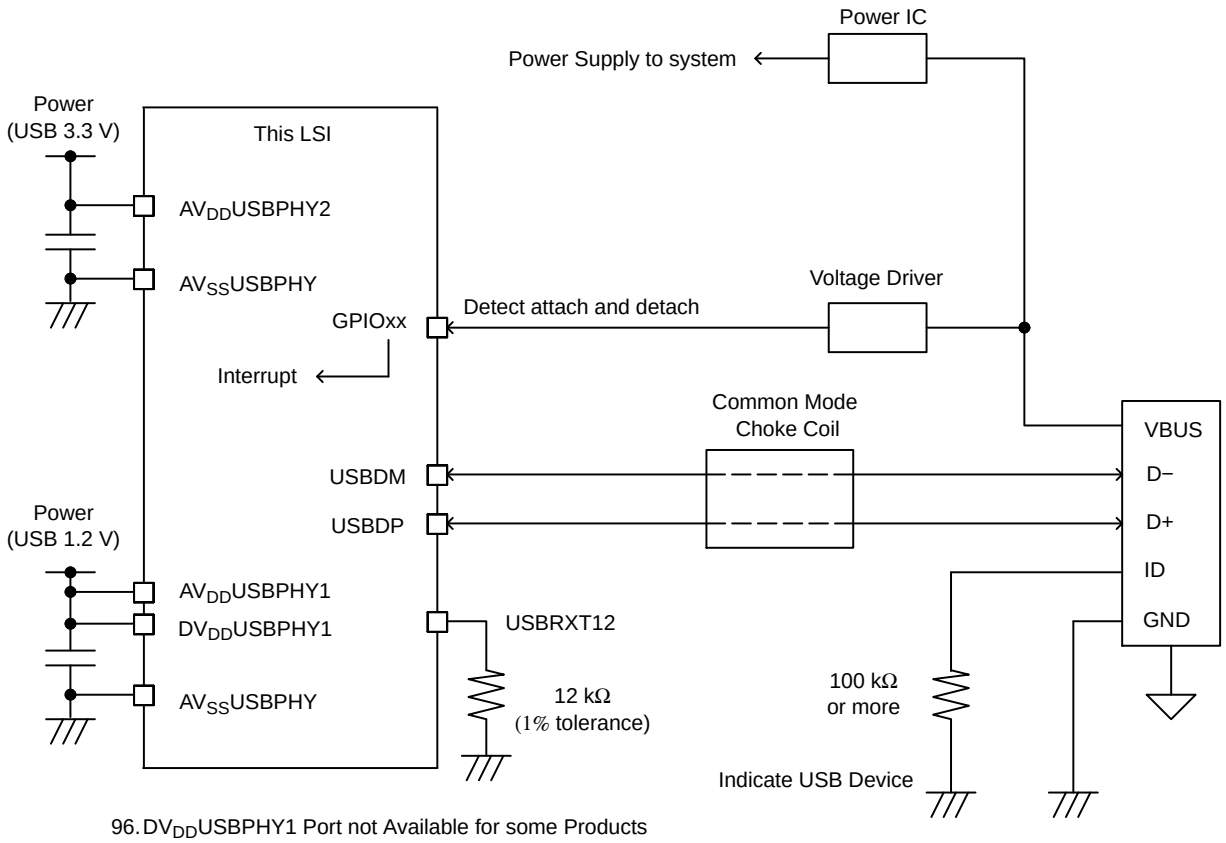
93. It is important to get the correct ADC conversion result that the wiring resistance is accurate. Pay attention to keeping low noise.
    It is recommended that the ceramic capacitor of the high frequency type to be used as a decoupling capacitor between AV_{DD}ADC and AV_{SS}ADC.
    Place the capacitor close to the terminal of LSI as much as possible so that the wiring length may be short as much as possible.
94. When the terminal VR is prepared (Package Code = “RA”, etc), the ADC conversion speed (operation clock frequency) is different depending on the value of the capacitor used. Confirm specs of ADC.
95. VRH and AVddADC, VRL and AVssADC are connected in the package (Package Code = “TA”, “XA”, “XB”, “XC”, “XD”, etc). VR terminal is open in the package.

Figure 43. 10Bit AD Converter

USB2.0 PHY

Refer to the LC823450−USB20PCB design guideline.

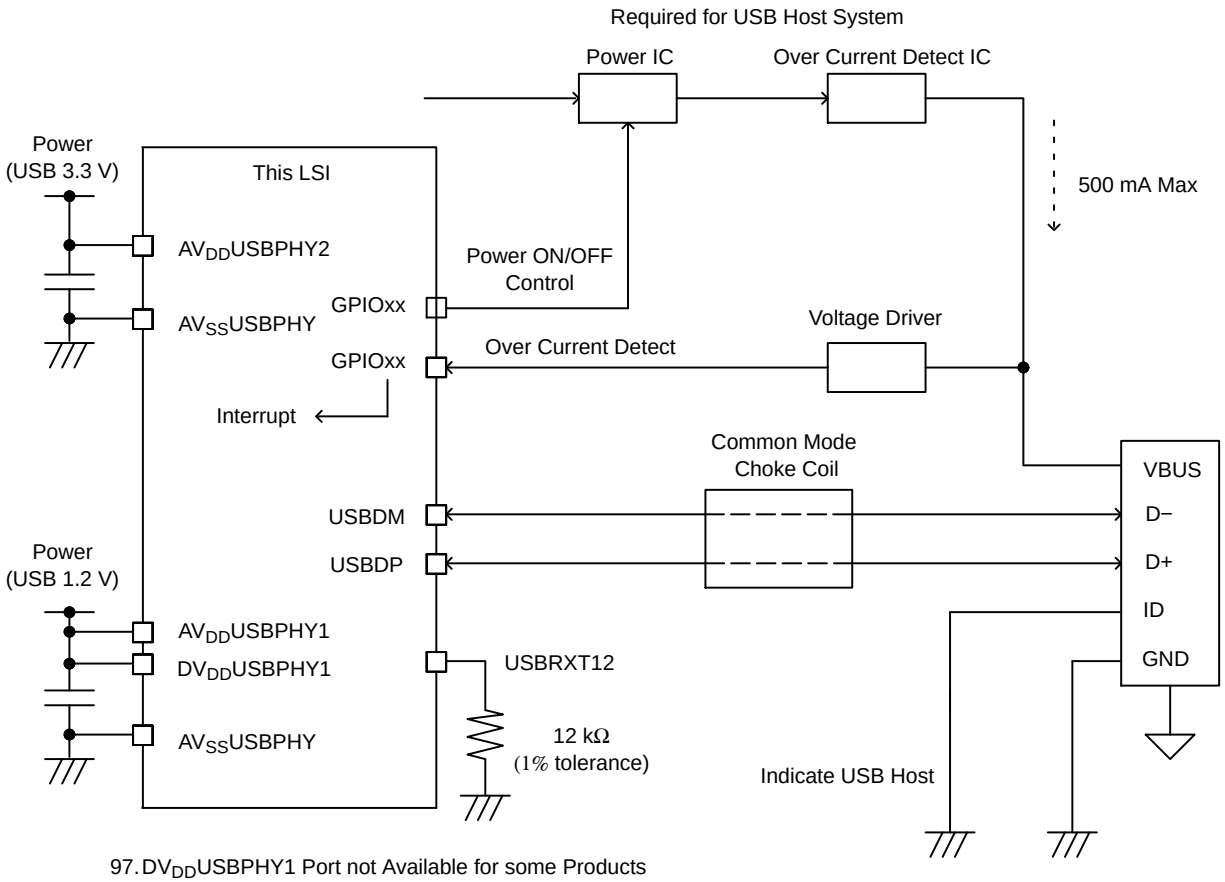
USB Device



96. DV_{DD}USBPHY1 Port not Available for some Products

Figure 44. USB Device

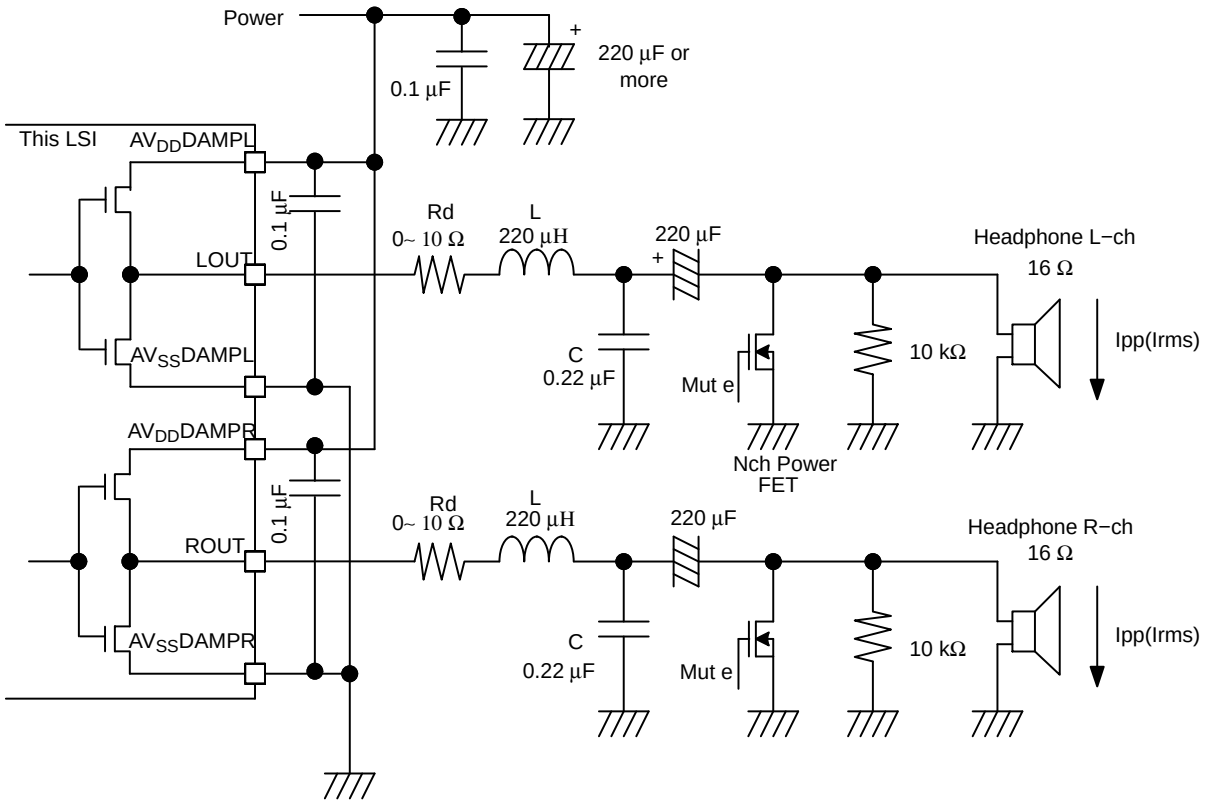
USB Host



97. DV_{DD}USBPHY1 Port not Available for some Products

Figure 45. USB Host

Class−D AMP



98. Add the bypass condenser (0.1 µF) between AV_{DD}DAMPL and AV_{SS}DAMPL, AV_{DD}DAMPR and AV_{SS}DAMPR as close as possible to terminals.
99. Add the large electrolyte capacitor (220 µF or more recommended) to AV_{DD}DAMPL, AV_{DD}DAMPR terminal to reject the noise and reduce the pumping phenomenon of Class−D AMP.
100. Check the voltage level of AV_{DD}DAMPL, AV_{DD}DAMPR and make sure not to exceed 1.65 V (recommended operating voltage) by using playback of 20 Hz, 0db (full scale) sin wave.
101. The combination of L = 47 µH and C = 1 µF is acceptable.
102. Large volume of damping resister, Rd causes the drop of output voltage. Besides, Rd has a strong relationship between L and C, and, the “Q” value depending on Rd, L and C determines the frequency characteristics. Therefore the resister value should be decided depending on your real system. Please note that the peripheral constants should be considered including the DC resistance component.
103. When Class−D Amp terminal is used as GPO (General Purpose Output), it is not necessary to add LC filter circuit because of avoidance of overvoltage supply though AVddDAMPL and AVddDAMPR can supply up to 1.95 V.

Figure 46. Class−D AMP

Output Power Calculation

[condition]

- The DC resistance element of the coil, capacitor is small
- Maximum output amplitude = 90% (Theoretical Value of Delta−sigma Circuit) to power supply of PWM
- Class−D AMP power supply (Av_{DD}DAMPL, AV_{DD}DAMPR) = 1.2 V
- Class−D AMP Turning on resistance of internal transistor(Ron) = 2 Ω
- Headphone load resistance(RL) = 15 Ω
- Series resistance(Rd) = 0 Ω

Assume the current that flows to the headphone to be Ipp:

Ipp = (1200 / 2) × 0.9 / (15 + 2) = 31.7 (mA)

Irms = Ipp / SQRT(2) = 22.4 (mA)

Prms = Irms ^ 2 × 15 = 7.53 (mW)

Power Supply

Class−D AMP power supply to (AV_{DD}DAMPL, AV_{DD}DAMPR) must use a transient response and good power supply. When the power supply where the transient response is bad is used and the capacity of the capacitor is small, a peculiar pumping phenomenon to Class−D AMP is generated. The power supply voltage must not exceed the recommended operating range when the pumping phenomenon occurs.

Class−D AMP output is PWM. The power supply noise affects the output of Class−D AMP.

Power sources which have large internal impedance such as dry cell should not be directly connected to power supply of Class−D AMP, and those which have large switching noise such as switching regulator are not suitable and need to be taken care of.

Digital Mic

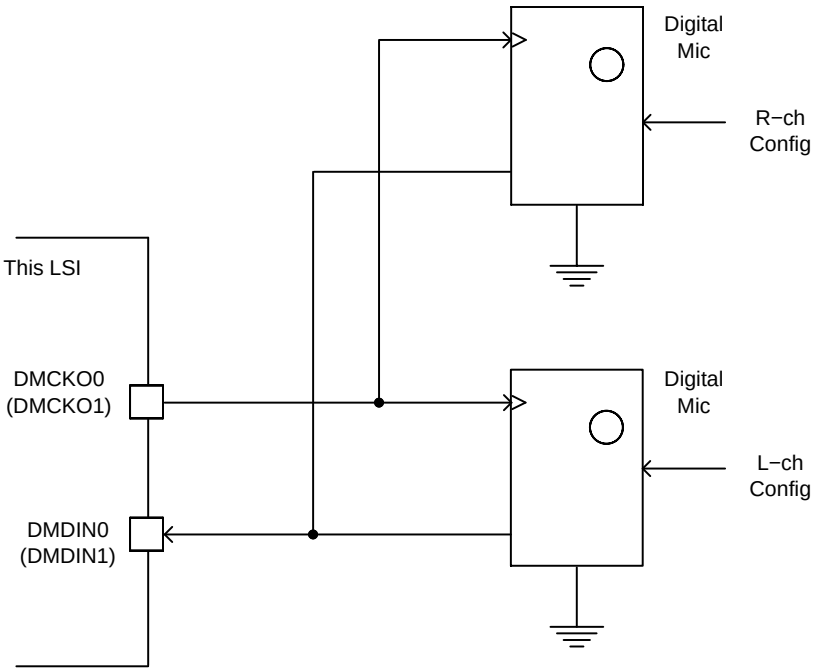


Figure 47. Digital Mic

I²C

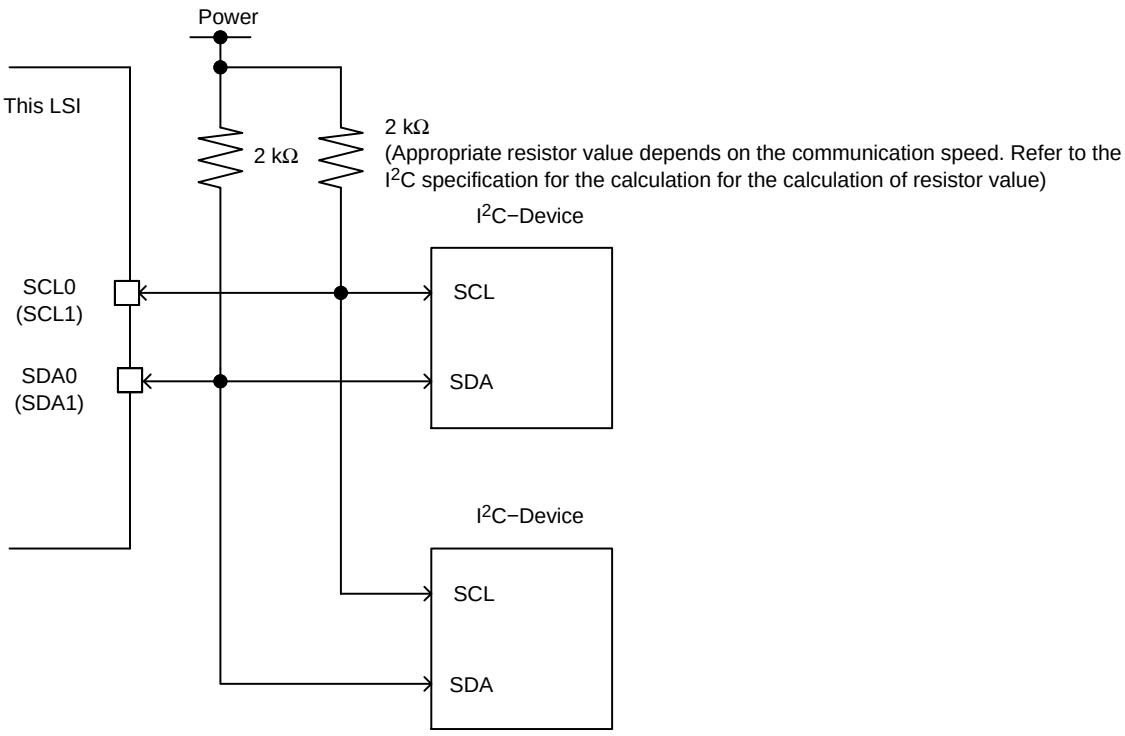
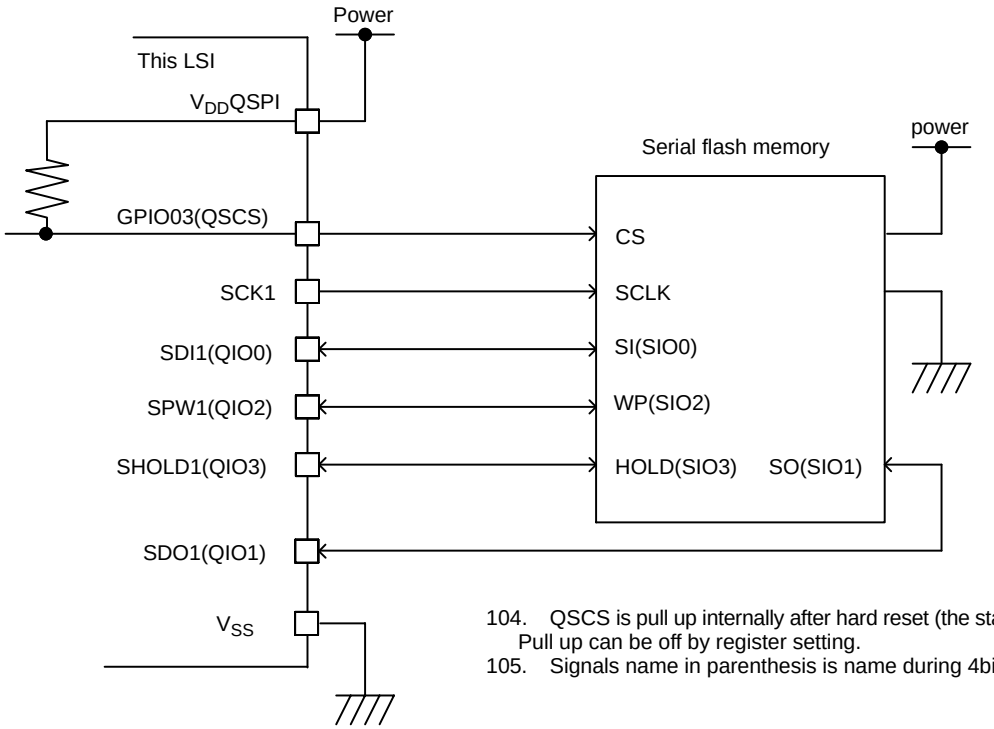


Figure 48. I²C

S−Flash I/F



104. QSCS is pull up internally after hard reset (the state of figure). Pull up can be off by register setting.
105. Signals name in parenthesis is name during 4bit mode.

Figure 49. S−Flash I/F

RTC (General RTC)

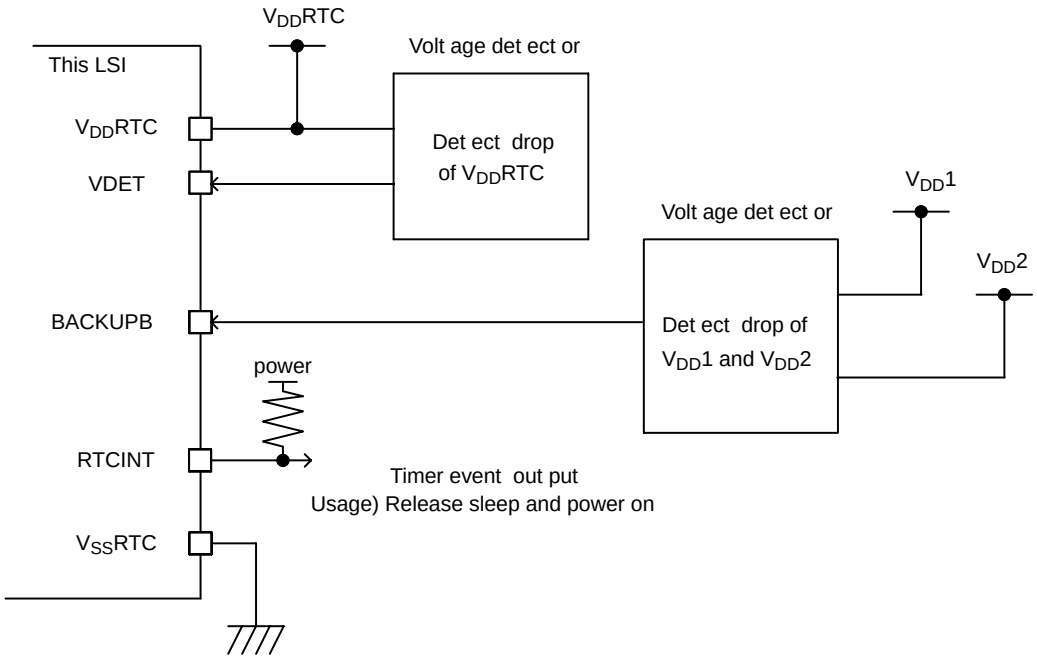


Figure 50. RTC (General RTC)

RTC (KeyInt RTC)

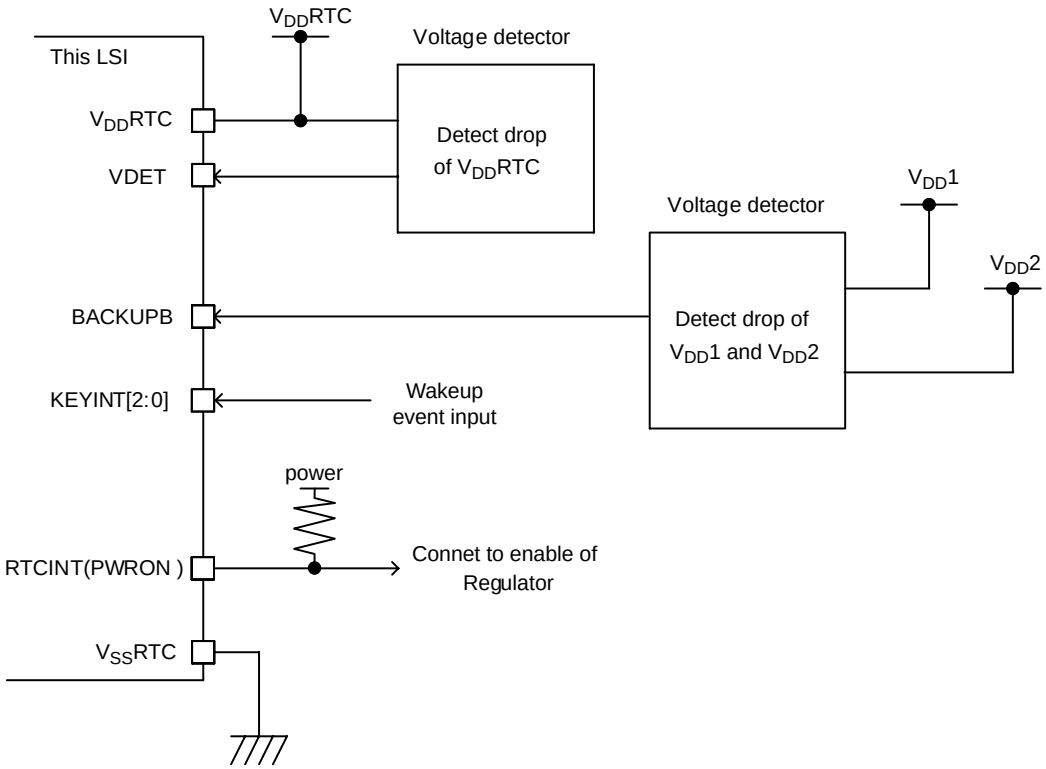
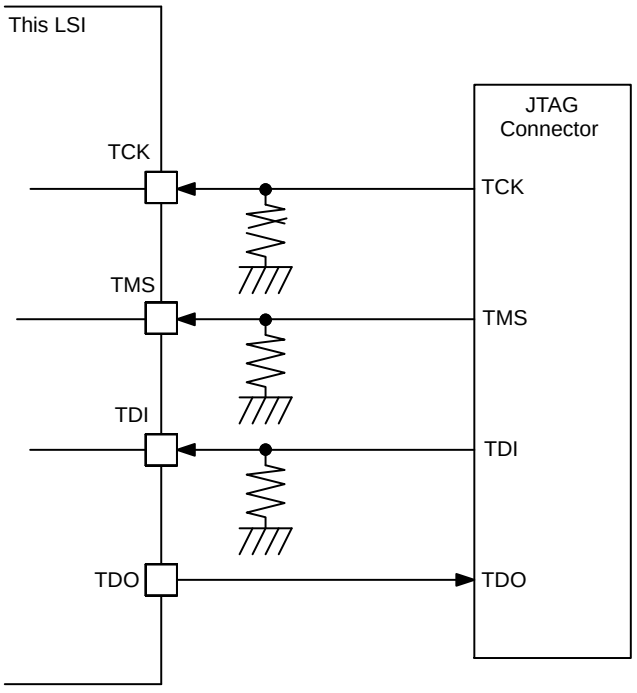


Figure 51. RTC (KeyInt RTC)

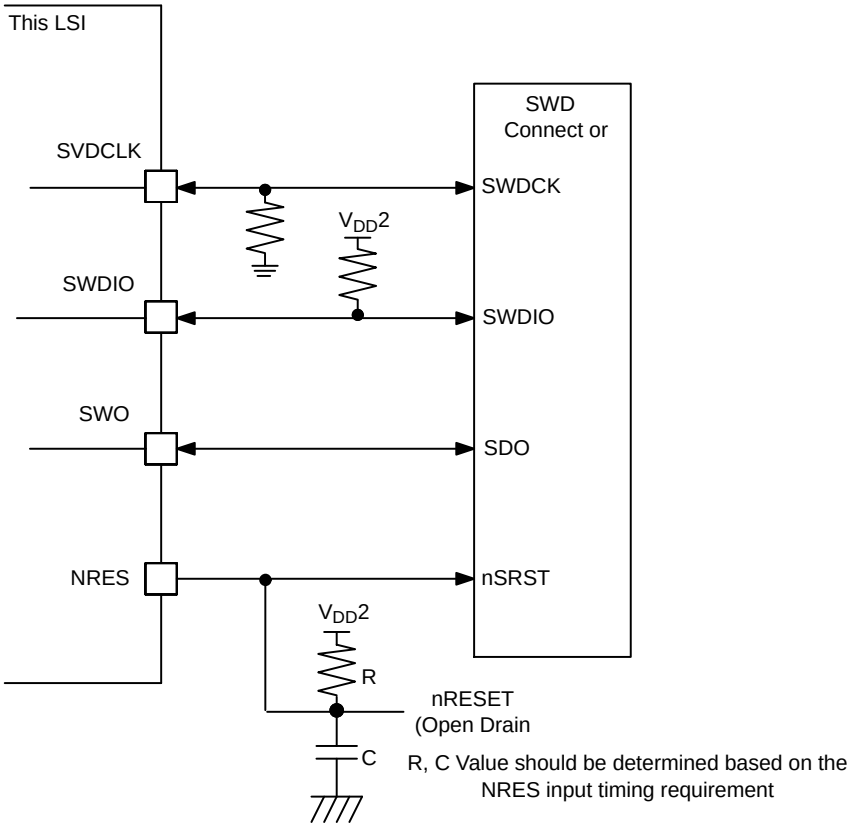
JTAG



106. LPDSP32 reset is available by reset command using debugger through JTAG. The connection of reset signal between JTAG and LSI is not
mandatory.
107. Internal pull down resistor can be used if the pull down resistors are enabled before the reset release of LPDSP32.
108. JTAG signals should be pull up or down for avoiding being left open if JTAG function is not used and JTAG signals are in input state.
109. Regarding JTAG signal connection, refer to the reference circuit from ICE tool vendor also.

Figure 52. JTAG

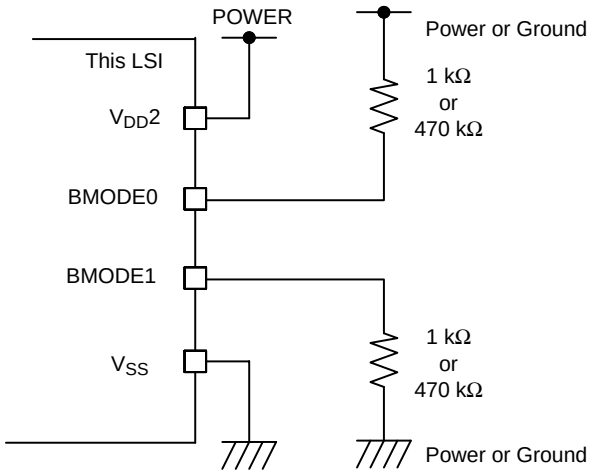
SWD



110. Pull up and pull down can be implemented by usgin internal registor.
111. Regarding SWD conneter signal, refer to the document about ICE tool

Figure 53. SWD

BMODE[1:0]



112. Don’t put capacitance on BMODE pin Don’t use long pattern on board. Otherwise these factors cause wrong BMODE level decision.

Figure 54. BMODE[1:0]

APPLICATION DIAGRAM

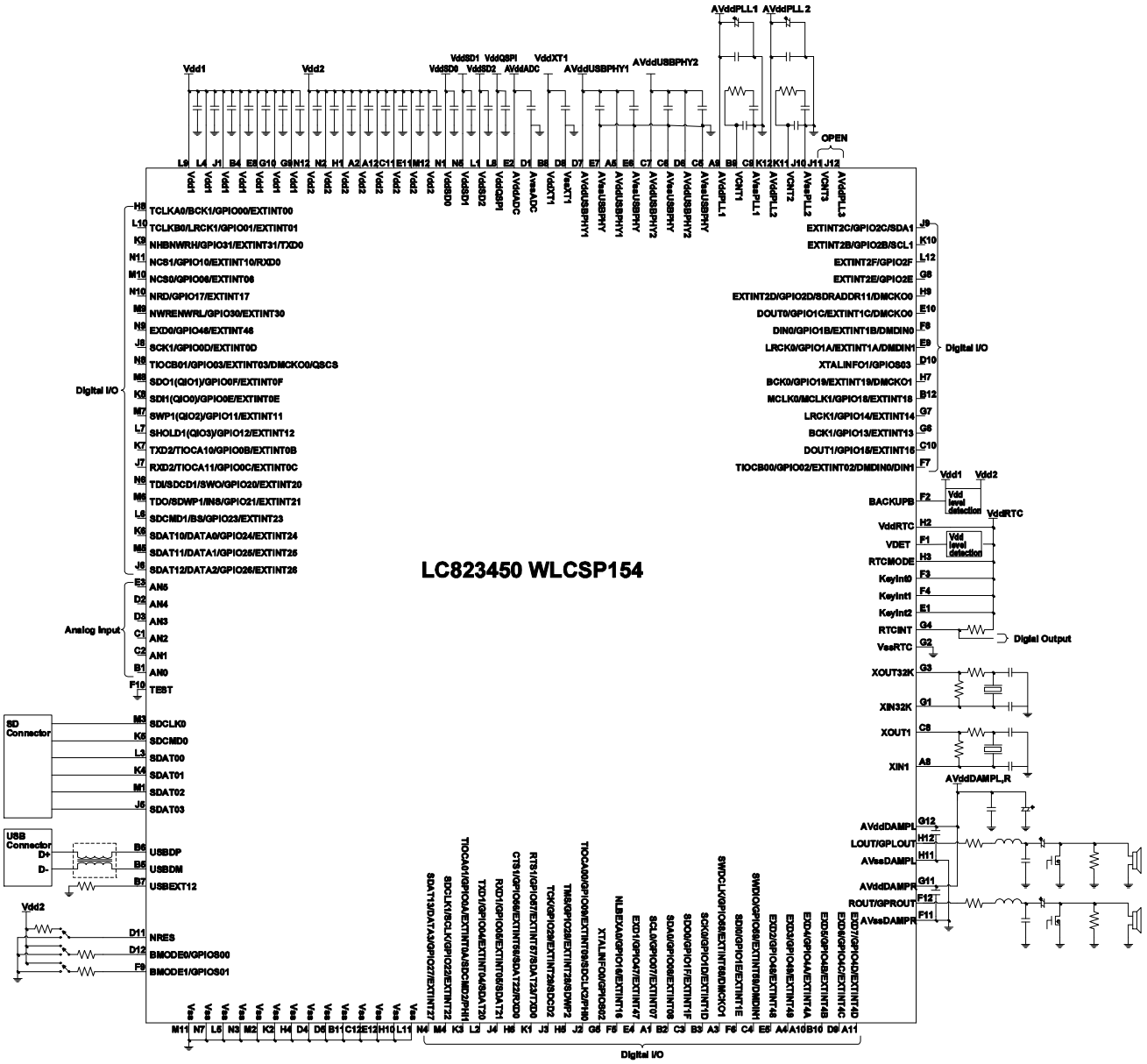


Figure 55. Application Diagram

INTERNAL POWER DOMAIN CONTROL

This LSI has eight power isolated region of internal core for leakage current reduction, these can be power supply OFF separately. Power isolated region ISOLATED−X (X means one of the eight region ISOLATED A to I. ISOLATED F doesn't exist) described in Figure 37. Power ON / OFF for each power domain is controlled by the appropriate bit of System Controller of power control register (LSISTBY). However, to control the power control register (LSISTBY), also control ISOLATION control register (ISOCNT) as necessary. Please refer to the ProgrammersModel_SystemController for details.

Each power isolation region and its contents, the flag of the corresponding power control register (LSISTBY) and power control register (LSISTBY) is as follows.

Table 59.

Name	Content	LSISTBY	ISOCNT
ISOLATED−A	Audio Block	Bit0 STBYA	Bit0 ISOCNTA
ISOLATED−B	Internal SRAM(seg 3/4/5)	Bit0 STBYB	Bit0 ISOCNTB
ISOLATED−C	Internal SRAM(seg 6/7/8)	Bit0 STBYC	Bit0 ISOCNTC
ISOLATED−D	Internal SRAM(seg 9) 220KB LPDSP32 ROM	Bit0 STBYD	Bit0 ISOCNTD
ISOLATED−E	USB 2.0 Holt Controller SRAM for USB	Bit0 STBYE	Bit0 ISOCNTE
ISOLATED−G	Cache for S−Flash I/F	Bit0 STBYG	Bit0 ISOCNTG
ISOLATED−H	SD Card I/F Memory Stick I/F	Bit0 STBYH	Bit0 ISOCNTH
ISOLATED−I	Internal ROM 256KB	Bit0 STBYI	Bit0 ISOCNTI

POWER SUPPLY SEQUENCE

Background

The basic sequence of power on/off of power supply is the following order.
(Simultaneous power on/off is acceptable)

- Power on Vdd*(Internal) → Vdd*(IO) → Vsig(Signal)
- Power off Vsig(Signal) → Vdd*(IO) → Vdd*(Internal)

Power on of Vdd*(IO) while Vdd *(Internal) are power off might generate the glitch on IO signals and flow of through current.
To avoid it, the sequence mentioned above is recommended as the basic sequence.

Recommendation

Following sequence is recommended (Simultaneous power on/off is acceptable).

- Power on 1 → 2 → Vsig(signal)
- Power off Vsig(signal) → 2 → 1

NOTE: The sequence of 1(Internal) → 2(IO) causes LSI hard reset and prevent from making IO glitch 3(RTC) has dedicated power supply and sequence which is described on the following section.

Power Supply Group

1. Internal core, analog power supply (1V power supply)
   Vdd1, VddXT1, AVddPLL1, AVddPLL2, AVddUSBPHY1, DVddUSBPHY1
2. External IO power supply (3V power supply)
   Vdd2, VddSD0, VddSD1, VddSD2, VddQSPI AVddUSBPHY2, AVddADC, AVddPLL3 AVddDAMPL, AVddDAMPR
3. RTC power supply
   VddRTC

(Dedicated power supply and sequence is dedicated power on/off sequence is described in the following sections)

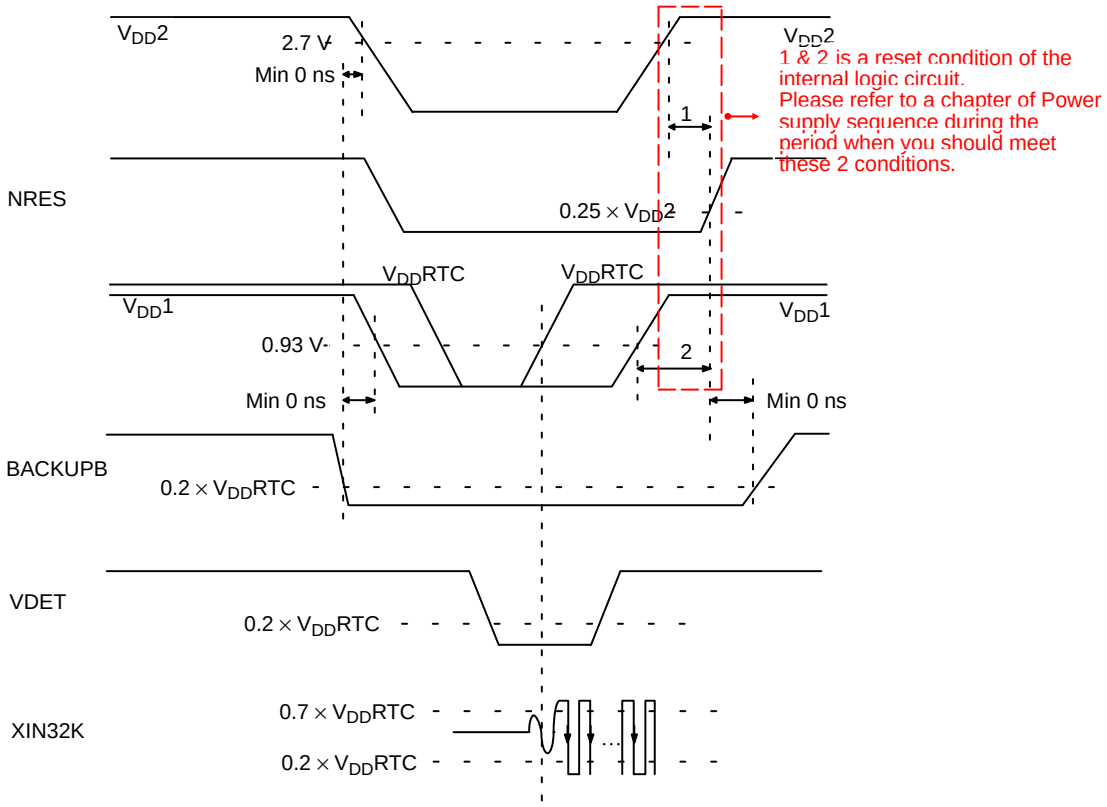
RTC Terminal Control Sequence

A power supply sequence and other terminal control sequence of RTC are described as follows.

General RTC Mode (RTCMODE = 1)

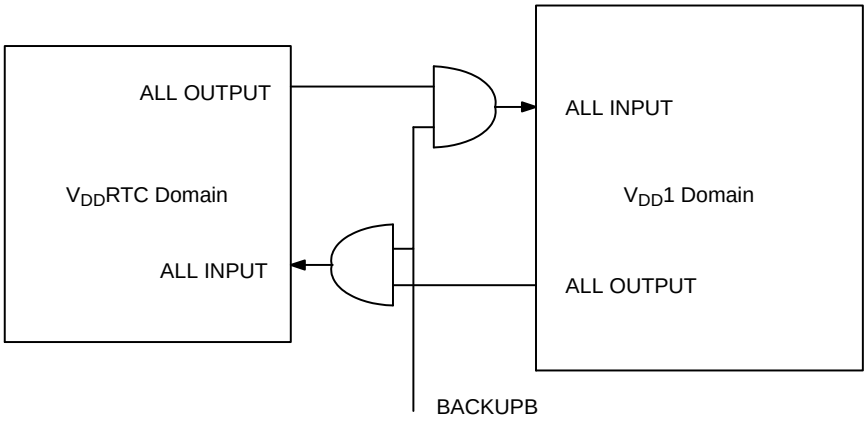
When only RTC operates, it is necessary to detect the drop of the voltage of Vdd1 and Vdd2 power supply, and set BACKUPB to Low which isolates VddRTC Domain from Vdd1 Domain.

Moreover, it is necessary to detect the drop of the voltage of VddRTC power supply, and set VDET to Low. (The RTC operation stops).



113. Internal control logic for isolation.

Figure 56.



114. $V_{DD}1$ can be shut down while BACKUPB = Low

Figure 57.

KeyInt RTC Mode (RTCMODE = 0)

By the master command from Cortex−M3, internal sequencer of RTC controls BACKUPB signal for isolation and power off. KEYINT input or internal RTCINT signal can generate power on sequence. Power off sequence using BACKUPB is also available for activation of power off by external source.

It is necessary to detect the drop of the voltage of V_{DD}RTC power supply, and set VDET to Low. (The RTC operation stops).

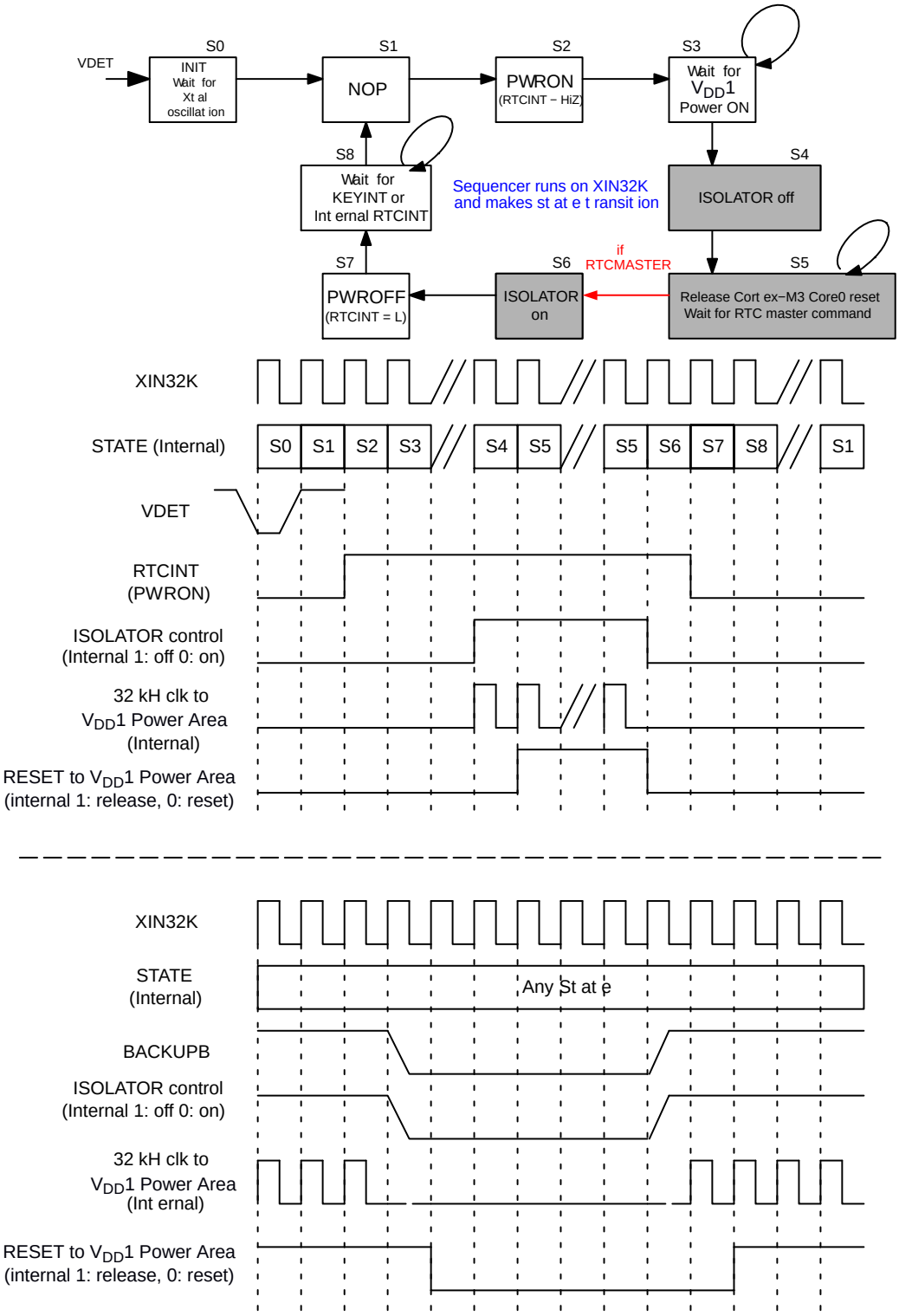


Figure 58.

THE GUIDANCE OF POWER SUPPLY CONTROL (RECOMMENDATION)

Power supply control should keep at least one of the guidances below, and make sure no problem for mass production based on customer side evaluations.

The Guidence in Terms of Power on Wave Form

Power on wave form should keep the guidance below.

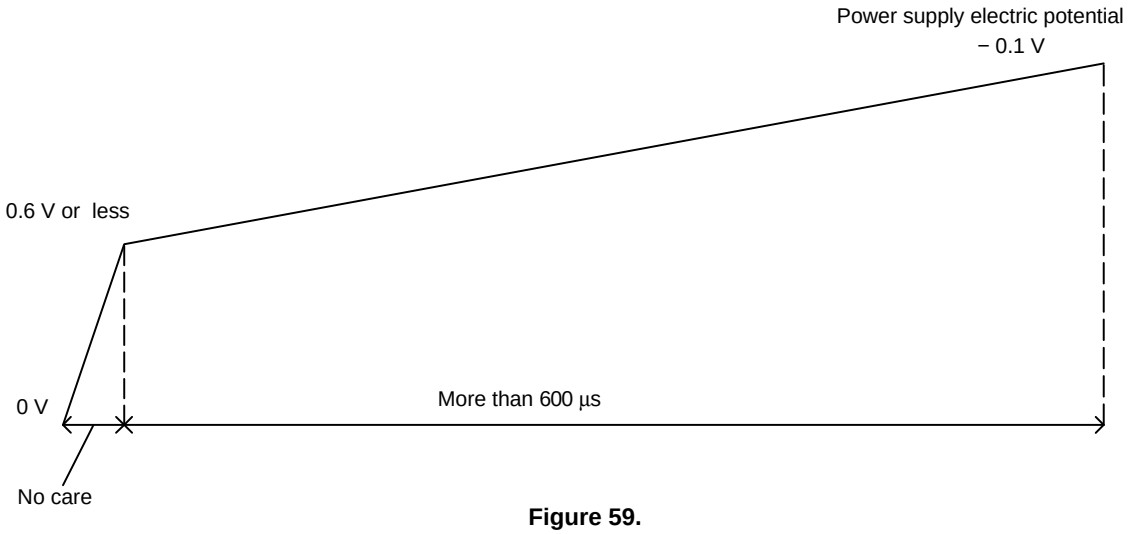


Figure 59.

When the voltage suddenly stands up at the time of power supply injection, please make the voltage to arrive at it less than 0.6 V. Please spend time beyond 600 μs and increase the voltage from the voltage which rose momentarily to the power supply electric potential – 0.1 V. When the voltage does not suddenly rise and stands up to power supply electric potential linearly, please spend time beyond 600 μs and increase the voltage from 0 V to the power supply electric potential.

The Guidence in Terms of the Placement of Bypass Condenser

Place bypass condenser 0.1 μF or more at the nearest point of each power supply pin, and place power circuit at the nearest point of power supply pin.

Parasitic inductance L1 and L2 should be equal to or below the value described in the table below. In addition, as for the value of L1 of the WLP package, it becomes the value that added 4nH to value of L1 of the table.

The inductance can be calculated from the width:W[mm], thickness: H[mm] and length: L[mm] of wiring on board, and affect layour of this LSI and bypass condenser.

Refer to “The formula to calculate parasitic inductance” to calculate indactance.

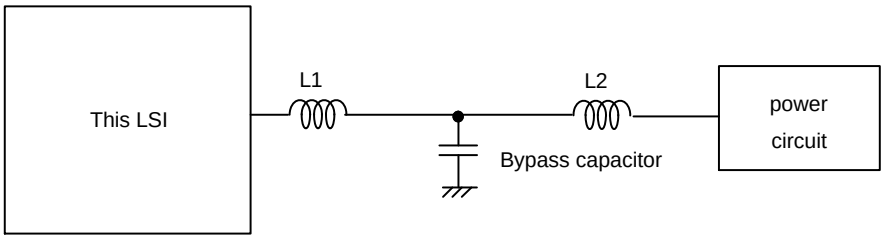


Figure 60.

Table 60.

FBGA (Ball)	TQFP (Pin No)	WLP (Ball)	PIN NAME	L1 (FBGA/TQFP/WLP) [nH]	L2 (FBGA/TQFP, WLP) [nH]	Bypass Capacitor (FBGA/TQFP, WLP) [μF]	Power Supply Range
D2	69	A2	Vdd2 B4	− / 4/ 8	160 / 50	- / 0.1	under 2 V case
				− /1.5 / 5.5	160 / 50	− / 0.1	equal 2 V or more case
F2	75	A5	AVddUSBPHY1	− / 4 / 8	160 / 80	− / 0.1	−
M2	91	A9	AVddPLL1	− / 4 / 8	160 / 80	− / 0.1	−
R13	120	K12	AVddPLL2	− / 4 / 8	160 / 80	− / 0.1	−
−	−	J12	AVddPLL3	− / 6 / 10	- / 80	− / 0.1	−
R7	113	G11	AVddDAMPR	− / 8 / 12	160 / 160	− / 0.1	−
R8	114	G12	AVddDAMPL	− / 8 / 12	160 / 160	− / 0.1	−
P15	2	N12	Vdd2 B1	40 / 8 / 12	160 / 160	0.01 / 0.01	under 2 V case
				40 / 6 / 10	160 / 80	0.01 / 0.1	equal 2 V or more case
R14	127	M12	Vdd2 P8	− / 8 / 12	160 / 160	0.01 / 0.01	under 2 V case
				− / 6 / 10	160 / 80	0.01 / 0.1	equal 2 V or more case
P4	95	A12	Vdd2 P6	− / 16 / 20	160 / 160	0.01 / 0.01	under 2 V case
				− / 6 / 10	160 / 160	0.01 / 0.01	equal 2 V or more case
P5	99	C11	Vdd2 P6	− / 16 / 20	160 / 160	0.01 / 0.01	under 2 V case
				− / 6 / 10	160 / 160	0.01 / 0.01	equal 2 V or more case
P8	108	E11	Vdd2 P6	40 / 16 / 20	160 / 160	0.01 / 0.01	under 2 V case
				40 / 6 / 10	160 / 160	0.01 / 0.01	equal 2 V or more case
H2	80	D6	AVddUSBPHY2	12 / 12 / 16	160 / 160	0.01 / 0.01	−
J2	83	C7	AVddUSBPHY2	12 / 12 / 16	160 / 160	0.01 / 0.01	−
D14	28	N2	Vdd2 B2	− / 16 / 20	160 / 160	− / 0.01	under 2 V case
				− / 6 / 10	160 / 160	− / 0.01	equal 2 V or more case
C9	49	H1	Vdd2 B3	16 / 16 / 20	160 / 160	0.01 / 0.01	under 2 V case
				16 / 16 / 20	160 / 160	0.01 / 0.01	equal 2 V or more case
C12	31	N1	VddSD0	32 / 32 / 36	160 / 160	0.01 / 0.01	−
D8	50	H2	VddRTC	− / 16 / 20	160 / 160	− / 0.01	−
A6	57	E2	AVddADC	− / 32 / 36	160 / 160	− / 0.01	−
L13	5	L9	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
G14	9	L8	VddQSPI	40 / 40 / 44	160 / 160	0.01 / 0.01	−
F14	20	N5	VddSD1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
E13	26	L4	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
D12	40	L1	VddSD2	40 / 40 / 44	160 / 160	0.01 / 0.01	−
A9	47	J1	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
E3	74	B4	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
H3	84	D7	AVddUSBPHY1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
K2	86	B8	VddXT1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
L4	90	E8	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
P9	110	G10	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
P11	121	G9	Vdd1	40 / 40 / 44	160 / 160	0.01 / 0.01	−
L15	−	−	Vdd2 B1	− / − / -	160 / −	− / −	under 2 V case
				− / − / −	160 / −	− / −	equal 2 V or more case
J13	−	−	Vdd2 B1	40 / − / −	160 / −	0.01 / −	under 2 V case
				40 / − / −	160 / −	0.01 / −	equal 2 V or more case
B16	−	−	Vdd2 B2	- / − / −	160 / −	− / −	under 2 V case
				- / − / −	160 / −	− / −	equal 2 V or more case
B2	−	−	Vdd2 B4	- / − / −	160 / −	− / −	under 2 V case
				- / − / −	160 / −	− / −	equal 2 V or more case
F3	−	−	Vdd2 B4	40 / − / −	160 / −	0.01 / −	under 2 V case
				40 / − / −	160 / −	0.01 / −	equal 2 V or more case

Table 60. (continued)

FBGA (Ball)	TQFP (Pin No)	WLP (Ball)	PIN NAME	L1 (FBGA/TQFP/WLP) [nH]	L2 (FBGA/TQFP, WLP) [nH]	Bypass Capacitor (FBGA/TQFP, WLP) [μF]	Power Supply Range
E2	–	–	DVddUSBPHY1	40 / – / –	160 / -	0.01 / –	
K3	–	–	DVddUSBPHY1	40 / – / –	160 / –	0.01 / –	
P1	–	–	Vdd2 B6	40 / – / –	160 / –	0.01 / –	under 2 V case
				40 / – / –	160 / –	0.01 / –	equal 2 V or more case
P10	–	–	Vdd1	40 / – / –	160 / –	0.01 / –	–
N12	–	–	Vdd2 B8	40 / – / –	160 / –	0.01 / –	under 2 V case
				40 / – / –	160 / –	0.01 / –	equal 2V or more case

The formula to calculate parasitic inductance (for your reference):

$$0.0002L\left[\ln\left(\frac{2L}{W+H}\right)+0.2235\left(\frac{W+H}{L}\right)+0.5\right]\mu H \quad \text{(eq. 1)}$$

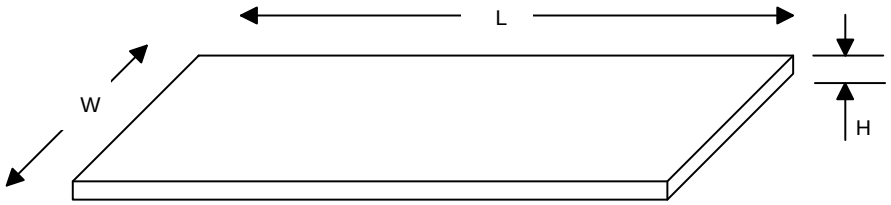


Figure 61.

Rush Current

This LSI has the circuits to protect from electrostatic discharge. The rush current flows in accordance with the steepness of rising curve of power supply.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)†
LC823450TA−2H	TQFP128 14x14 / TQFP128L (Pb−Free / Halogen Free)	450 / Tray JEDEC
LC823450XATBG	WLCSP154, 5.52x5.33 (Pb−Free / Halogen Free)	1000 / Tape & Reel
LC823450XBTBG	WLCSP154, 5.52x5.33 (Pb−Free / Halogen Free)	1000 / Tape & Reel
LC823450XCTBG	WLCSP154, 5.52x5.33 (Pb−Free / Halogen Free)	1000 / Tape & Reel
LC823450XDTBG	WLCSP154, 5.52x5.33 (Pb−Free / Halogen Free)	1000 / Tape & Reel
LC823450RAH−2H	LFBGA240 (Pb−Free / Halogen Free)	840 / Tray JEDEC
LC823450RBH−2H	LFBGA240 (Pb−Free / Halogen Free)	840 / Tray JEDEC

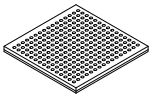
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

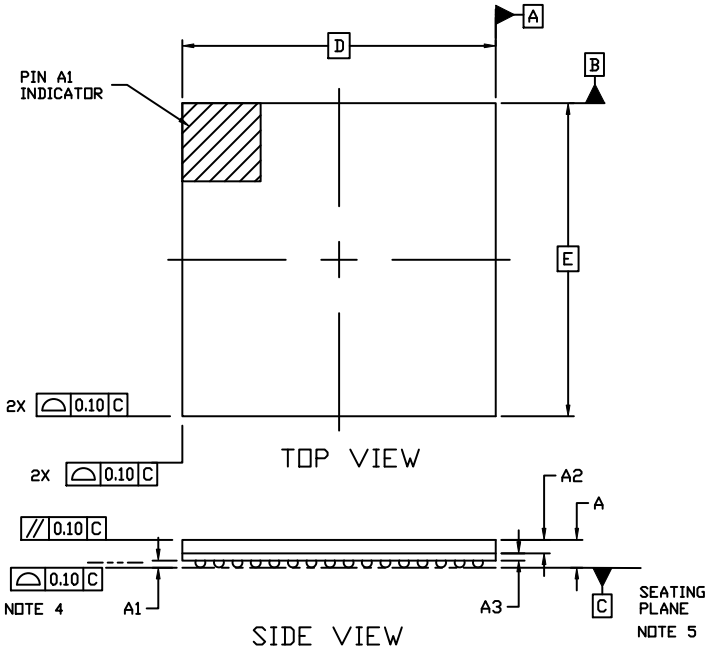
ON Semiconductor®

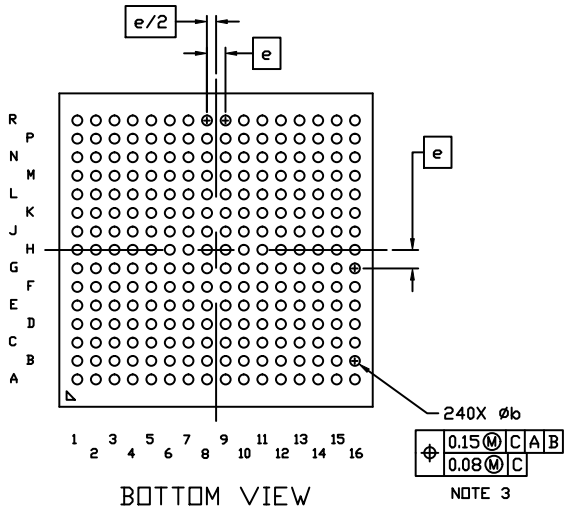
LFBGA240, 11x11
CASE 566EY
ISSUE A

DATE 05 FEB 2020



SCALE 1:1

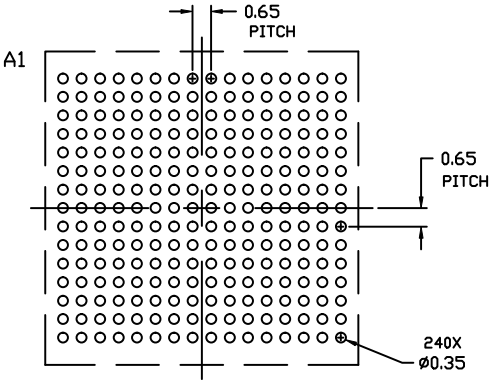




NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.31
A1	0.20	0.30
A2	0.70 REF	
A3	0.26 REF	
b	0.30	0.40
D	11.00 BSC	
E	11.00 BSC	
e	0.65 BSC	



RECOMMENDED
MOUNTING FOOTPRINT

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

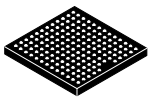
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package
CC = Country of Origin

GENERIC MARKING DIAGRAM*

DOCUMENT NUMBER:	**98AON92743F**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**LFBGA240, 11X11**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

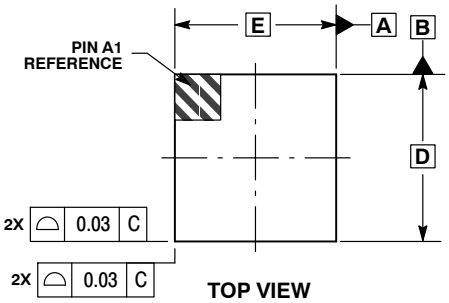
ON Semiconductor®

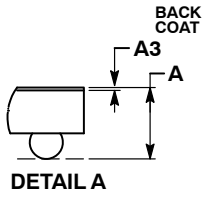


SCALE 2:1

WLCSP154, 5.52x5.33
CASE 567LD
ISSUE A

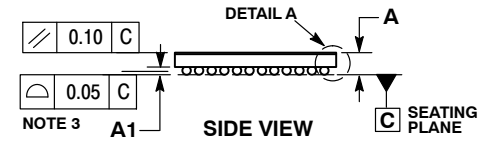
DATE 28 OCT 2015

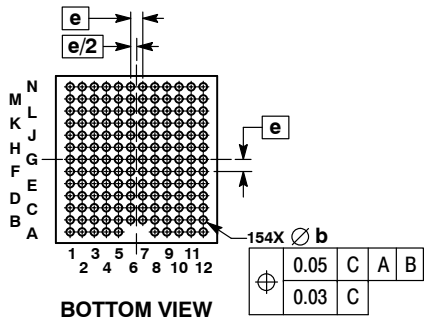




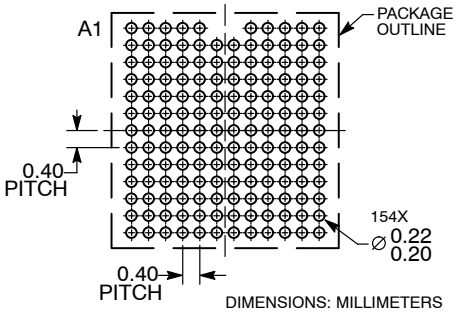
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.73
A1	0.18	0.24
A3	0.04 REF	
b	0.23	0.29
D	5.52 BSC	
E	5.33 BSC	
e	0.40 BSC	





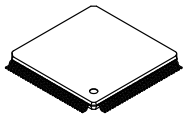
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

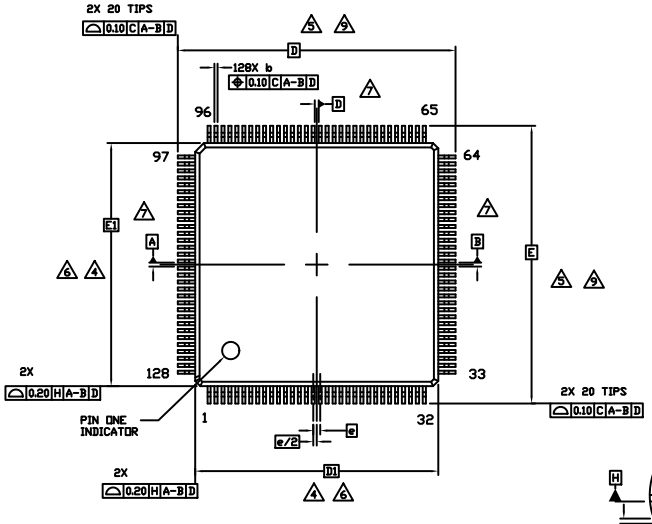
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

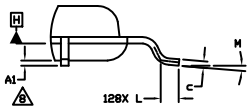
DOCUMENT NUMBER:	**98AON93273F**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**WLCSP154, 5.52X5.33**		**PAGE 1 OF 1**

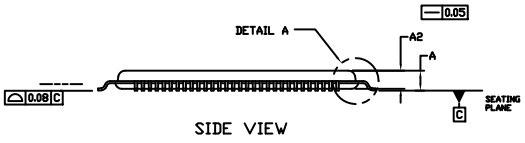


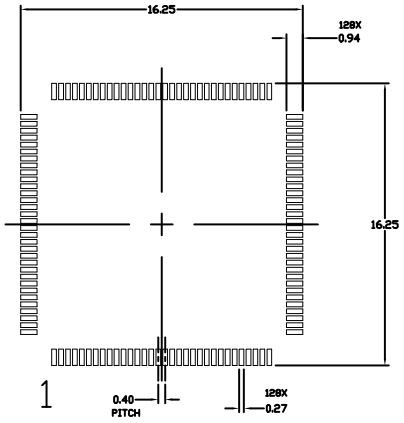
TQFP128 14x14 / TQFP128L
CASE 932BA
ISSUE A

DATE 30 APR 2015





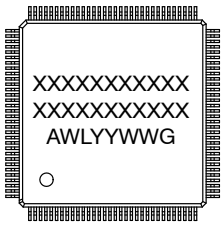




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DIMENSIONS D1 AND E1 TO BE DETERMINED AT DATUM PLANE H.
7. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
9. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.20
A1	0.05	0.15
A2	1.00 REF	
b	0.13	0.23
c	0.09	0.20
D	16.00 BSC	
D1	14.00 BSC	
E	16.00 BSC	
E1	14.00 BSC	
e	0.40 BSC	
L	0.45	0.75
M	0°	7°

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TQFP128 14X14 / TQFP128L**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

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