

MC74VHC1GT125

Noninverting Buffer / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHC1GT125 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC1GT125 requires the 3-state control input (\overline{OE}) to be set High to place the output into the high impedance state.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT125 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT125 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: $t_{PD} = 3.5$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62; Equivalent Gates = 16

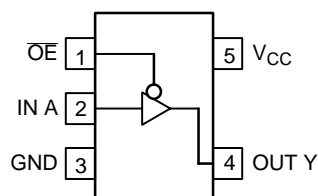


Figure 1. Pinout (Top View)

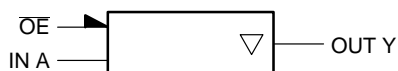


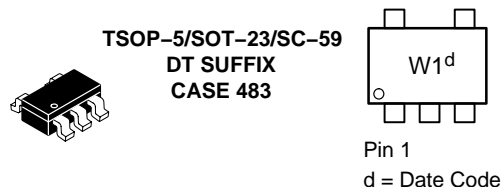
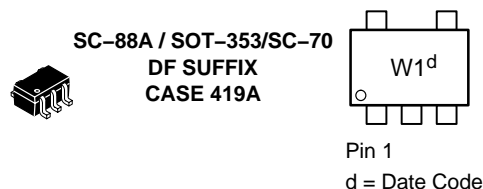
Figure 2. Logic Symbol



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



PIN ASSIGNMENT

Pin	Function
1	\overline{OE}
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	\overline{OE} Input	Y Output
L	L	L
H	L	H
X	H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1GT125

MAXIMUM RATINGS (Note 1)

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	V _{CC} = 0 High or Low State -0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	V _{OUT} < GND; V _{OUT} > V _{CC}	mA
I _{OUT}	DC Output Current, per Pin	+25	mA
I _{CC}	DC Supply Current, V _{CC} and GND	+50	mA
P _D	Power Dissipation in Still Air	SC-88A, TSOP-5	mW
θ _{JA}	Thermal Resistance	SC-88A, TSOP-5	°C/W
T _L	Lead Temperature, 1 mm from Case for 10 s	260	°C
T _J	Junction Temperature Under Bias	+150	°C
T _{stg}	Storage Temperature	-65 to +150	°C
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A
I _{Latch-Up}	Latch-Up Performance	Above V _{CC} and Below GND at 125°C (Note 5)	±500

- Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
- Tested to EIA/JESD22-A114-A
- Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	3.0	5.5	V
V _{IN}	DC Input Voltage	0.0	5.5	V
V _{OUT}	DC Output Voltage	0.0	V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 5.0 V ± 0.5 V	0	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

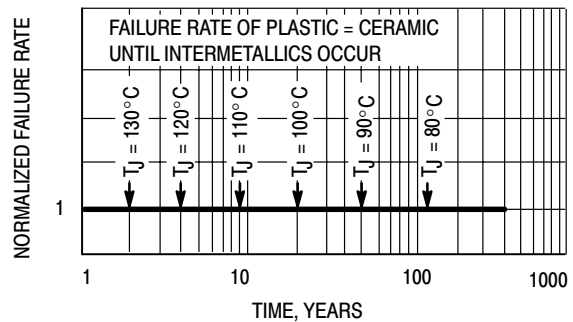


Figure 3. Failure Rate vs. Time Junction Temperature

MC74VHC1GT125

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0	1.4			1.4		1.4		V
			4.5	2.0			2.0		2.0		
			5.5	2.0			2.0		2.0		
V _{IL}	Maximum Low-Level Input Voltage		3.0			0.53		0.53		0.53	V
			4.5			0.8		0.8		0.8	
			5.5			0.8		0.8		0.8	
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = - 50 μA	3.0	2.9	3.0		2.9		2.9		V
			4.5	4.4	4.5		4.4		4.4		
		V _{IN} = V _{IH} or V _{IL} I _{OH} = - 4 mA I _{OH} = - 8 mA	3.0	2.58			2.48		2.34		
			4.5	3.94			3.80		3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	3.0		0.0	0.1		0.1		0.1	V
			4.5		0.0	0.1		0.1		0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0			0.36		0.44		0.52	
			4.5			0.36		0.44		0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.10		± 1.0		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μA
I _{CC(T)}	Quiescent Supply Current	Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			± 0.25		± 2.5		± 2.5	μA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y (Figures 3. and 5.)	V _{CC} = 3.3 ± 0.3 V C _L = 15pF C _L = 50pF		5.6	8.0	1.0	9.5		12.0	ns
				8.1	11.5	1.0	13.0		16.0	
		V _{CC} = 5.0 ± 0.5 V C _L = 15pF C _L = 50pF		3.8	5.5	1.0	6.5		8.5	
				5.3	7.5	1.0	8.5		10.5	
t _{PZL} , t _{PZH}	Maximum Output Enable Time, OE to Y (Figures 4. and 5.)	V _{CC} = 3.3 ± 0.3 V C _L = 15pF R _L = R _I = 500 Ω C _L = 50pF		5.4	8.0	1.0	9.5		11.5	ns
				7.9	11.5	1.0	13.0		15.0	
		V _{CC} = 5.0 ± 0.5 V C _L = 15pF R _L = R _I = 500 Ω C _L = 50pF		3.6	5.1	1.0	6.0		7.5	
				5.1	7.1	1.0	8.0		9.5	
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time, OE to Y (Figures 4. and 5.)	V _{CC} = 3.3 ± 0.3 V C _L = 15pF R _L = R _I = 500 Ω C _L = 50pF		6.5	9.7	1.0	11.5		14.5	ns
				8.0	13.2	1.0	15.0		18.0	
		V _{CC} = 5.0 ± 0.5 V C _L = 15pF R _L = R _I = 500 Ω C _L = 50pF		4.8	6.8	1.0	8.0		10.0	
				7.0	8.8	1.0	10.0		12.0	
C _{in}	Maximum Input Capacitance			4	10		10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)			6						pF
C _{PD}	Power Dissipation Capacitance (Note 6)	Typical @ 25°C, V_{CC} = 5.0 V								pF
		14								

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC1GT125

SWITCHING WAVEFORMS

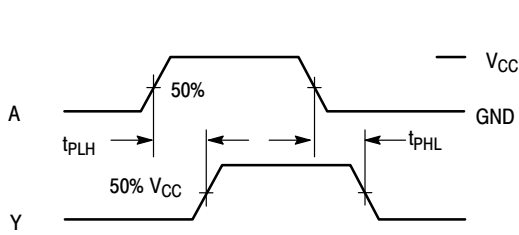


Figure 4. Switching Waveforms

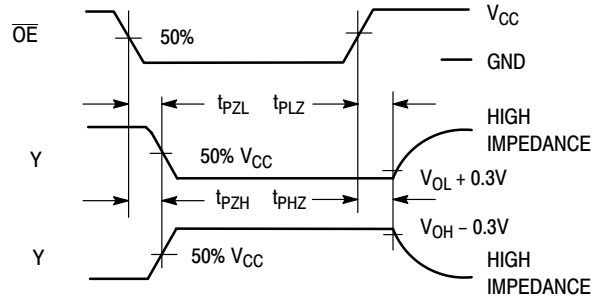
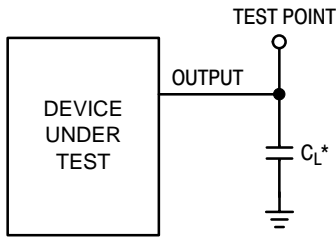
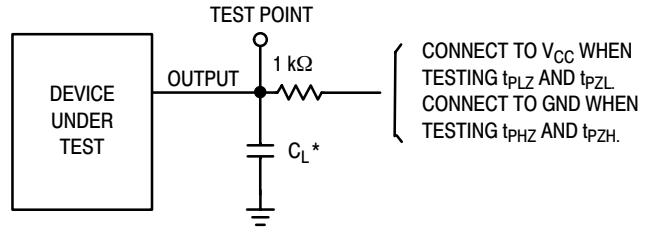


Figure 5.



*Includes all probe and jig capacitance

Figure 6. Test Circuit



*Includes all probe and jig capacitance

Figure 7. Test Circuit

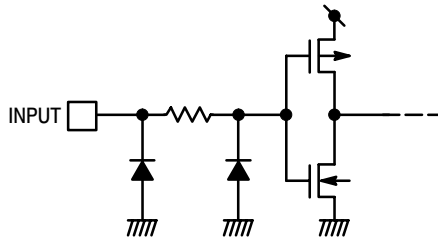


Figure 8. Input Equivalent Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/Common Name)	Tape and Reel Size†
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT125DF1	MC	74	VHC1G	T125	DF	1	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT125DF2	MC	74	VHC1G	T125	DF	2	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT125DT1	MC	74	VHC1G	T125	DT	1	TSOPS / SOT-23 / SC-59	178 mm (7") 3000 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74VHC1GT125



Figure 9. Tape Ends for Finished Goods

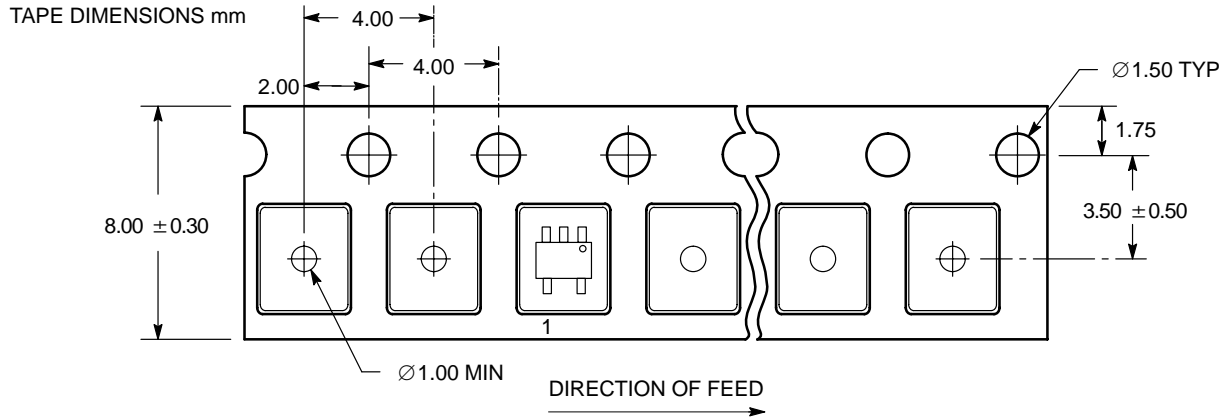


Figure 10. SC-70-5/SC-88A/SOT-353 DF1 Reel Configuration/Orientation

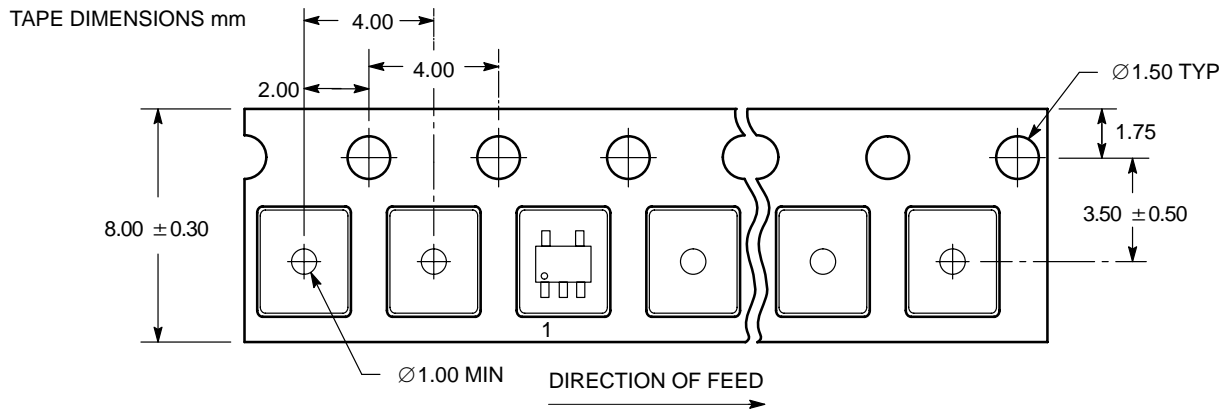


Figure 11. SC-70/SC-88A/SOT-353 DF2 and SOT23-5/TSOP-5/SC59-5 DT1 Reel Configuration/Orientation

MC74VHC1GT125

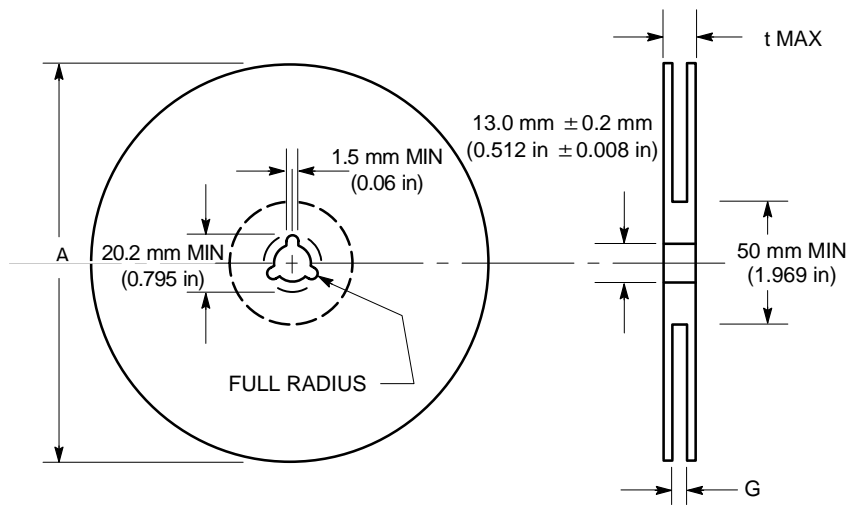


Figure 12. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	1, 2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

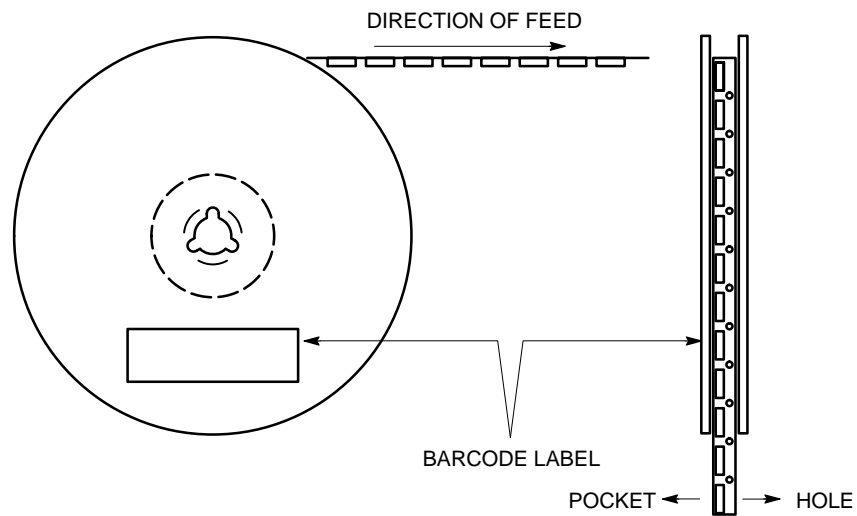
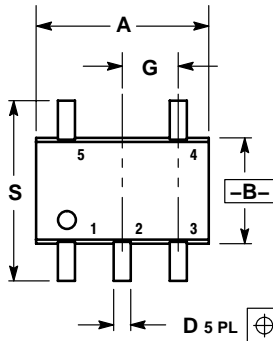


Figure 13. Reel Winding Direction

MC74VHC1GT125

PACKAGE DIMENSIONS

SC70-5/SC-88A/SOT-353
DF SUFFIX
5-LEAD PACKAGE
CASE 419A-02
ISSUE G

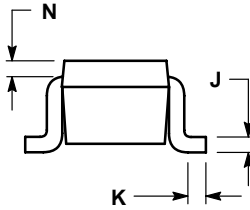


$\text{D } 5 \text{ PL } \text{ } \oplus \text{ } 0.2 \text{ (0.008) } \text{ } \text{M} \text{ } \text{B } \text{ } \text{M}$

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



SOLDERING FOOTPRINT*

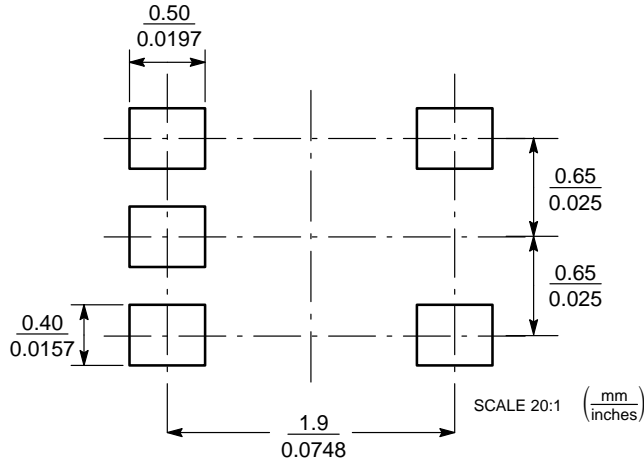


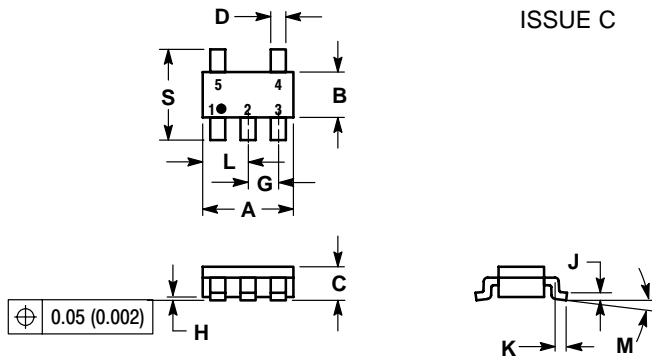
Figure 14. SC-88A/SC70-5/SOT-353

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC1GT125

PACKAGE DIMENSIONS

SOT23-5/TSOP-5/SC59-5
DT SUFFIX
5-LEAD PACKAGE
CASE 483-01
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*

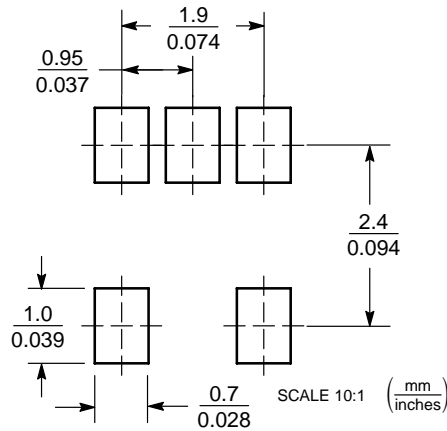



Figure 15. THIN SOT23-5/TSOP-5/SC59-5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.