

# NCV4274C

## Regulator, 400 mA, Low Dropout Voltage

### Description

The NCV4274C is a precision micro-power voltage regulator with an output current capability of 400 mA available in the DPAK, D2PAK and SOT-223 packages.

The output voltage is accurate within  $\pm 2.0\%$  with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 125  $\mu\text{A}$  with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

### Features

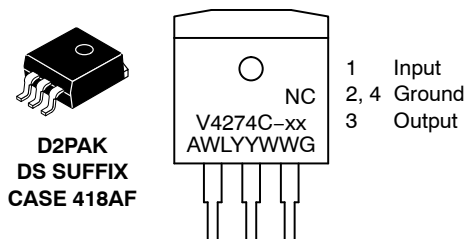
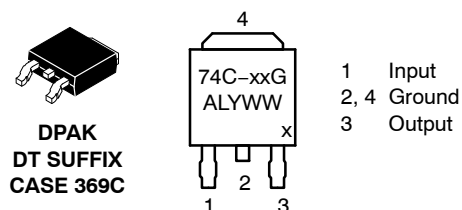
- 3.3 V, 5.0 V,  $\pm 2.0\%$  Output Options
- Low 125  $\mu\text{A}$  Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
  - -42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Very Low Dropout Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices



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### MARKING DIAGRAMS



xx = 33 (3.3 V)  
= 50 (5.0 V)  
A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

# NCV4274C

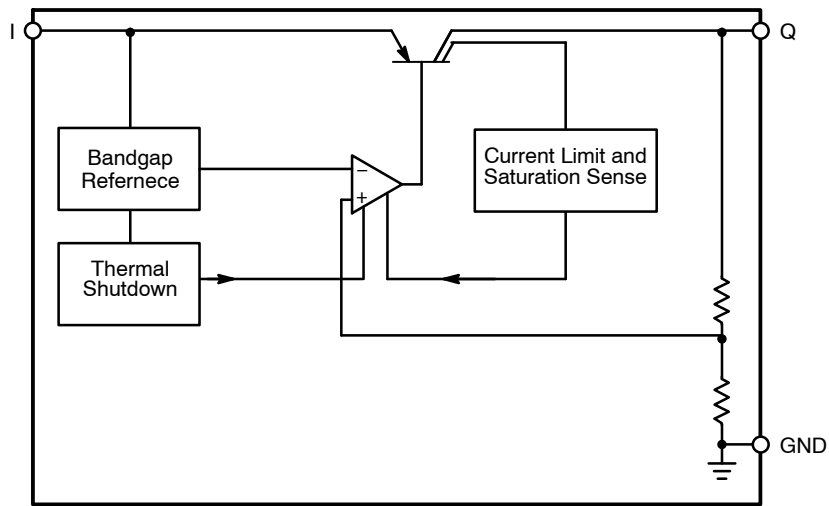


Figure 1. Block Diagram

## Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	Input; Bypass directly at the IC with a ceramic capacitor to GND.
2,4	GND	Ground
3	Q	Output; Bypass with a capacitor to GND.

## ABSOLUTE MAXIMUM RATINGS

Pin Symbol, Parameter	Symbol	Condition	Min	Max	Unit
I, Input-to-Regulator	Voltage	$V_I$	-42	45	V
	Current	$I_I$	Internally Limited	Internally Limited	
I, Input peak Transient Voltage to Regulator with Respect to GND (Note 1)	$V_I$			60	V
Q, Regulated Output	Voltage	$V_Q = V_I$	-1.0	40	V
	Current	$I_Q$	Internally Limited	Internally Limited	
GND, Ground Current	$I_{GND}$		-	100	mA
Junction Temperature	$T_J$		-40	150	°C
Storage Temperature	$T_{Stg}$		-50	150	°C
ESD Capability, Human Body Model (Note 2)	$ESD_{HB}$		4		kV
ESD Capability, Machine Model (Note 2)	$ESD_{MM}$		200		V
ESD Capability, Charged Device Model (Note 2)	$ESD_{CDM}$		1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C.
- This device series incorporates ESD protection and is tested by the following methods:  
 ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD MM tested per AEC-Q100-003 (EIA/JESD22-A115)  
 Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes  $<50\text{mm}^2$  due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2014.

# NCV4274C

## OPERATING RANGE

Parameter	Symbol	Condition	Min	Max	Unit
Input Voltage (5.0 V Version)	$V_I$		5.5	40	V
Input Voltage (3.3 V Version)	$V_I$		4.5	40	V
Junction Temperature	$T_J$		-40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## THERMAL RESISTANCE

Parameter		Symbol	Condition	Min	Max	Unit
Junction-to-Ambient	DPAK	$R_{thja}$		-	72.5 (Note 3)	°C/W
Junction-to-Ambient	D2PAK	$R_{thja}$		-	56.7 (Note 3)	°C/W
Junction-to-Case	DPAK	$R_{thjc}$		-	5.8	°C/W
Junction-to-Case	D2PAK	$R_{thjc}$		-	5.8	°C/W
Junction-to-Tab	SOT-223	$\Psi_{-JLX}$ , $\Psi_{LX}$		-	15.6 (Note 3)	°C/W
Junction-to-Ambient	SOT-223	$R_{\theta JA}$ , $\theta_{JA}$		-	87 (Note 3)	°C/W

3. 1 oz copper, 300 mm<sup>2</sup> copper area, single-sided FR4 PCB.

## MOISTURE SENSITIVITY LEVEL (Note 4)

Parameter	Symbol	Condition	Min	Max	Unit
Moisture Sensitivity Level	MSL	DPAK and D2PAK SOT-223	1 3	- -	

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCV4274C

## ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$ ;  $V_I = 13.5\text{ V}$  unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>REGULATOR</b>						
Output Voltage (5.0 V Version)	$V_Q$	$5\text{ mA} < I_Q < 400\text{ mA}$ $6\text{ V} < V_I < 28\text{ V}$	4.9	5.0	5.1	V
Output Voltage (5.0 V Version)	$V_Q$	$5\text{ mA} < I_Q < 200\text{ mA}$ $6\text{ V} < V_I < 40\text{ V}$	4.9	5.0	5.1	V
Output Voltage (3.3 V Version)	$V_Q$	$5\text{ mA} < I_Q < 400\text{ mA}$ $4.5\text{ V} < V_I < 28\text{ V}$	3.23	3.3	3.37	V
Output Voltage (3.3 V Version)	$V_Q$	$5\text{ mA} < I_Q < 200\text{ mA}$ $4.5\text{ V} < V_I < 40\text{ V}$	3.23	3.3	3.37	V
Current Limit (All Versions)	$I_Q$	$V_Q = 90\% V_{QTYP}$	400	600	–	mA
Quiescent Current	$I_q$	$I_Q = 1\text{ mA}$ $V_Q = 5.0\text{ V}$ $V_Q = 3.3\text{ V}$ $I_Q = 250\text{ mA}$ $V_Q = 5.0\text{ V}$ $V_Q = 3.3\text{ V}$ $I_Q = 400\text{ mA}$ $V_Q = 5.0\text{ V}$ $V_Q = 3.3\text{ V}$	–	125	250	$\mu\text{A}$ $\mu\text{A}$ mA mA mA mA
Dropout Voltage 5.0 V Version	$V_{DR}$	$I_Q = 250\text{ mA}$ , $V_{DR} = V_I - V_Q$ $V_I = 5.0\text{ V}$	–	250	500	mV
Load Regulation (3.3 V and 5 V Versions)	$\Delta V_Q$	$I_Q = 5\text{ mA to } 400\text{ mA}$	–	3	20	mV
Line Regulation (3.3 V and 5 V Versions)	$\Delta V_Q$	$\Delta V_I = 12\text{ V to } 32\text{ V}$ $I_Q = 5\text{ mA}$	–	4	25	mV
Power Supply Ripple Rejection	PSRR	$f_r = 100\text{ Hz}$ , $V_r = 0.5 V_{PP}$	–	60	–	dB
Thermal Shutdown Temperature*	$T_{SD}$	$I_Q = 5\text{ mA}$	150	–	210	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

\*Guaranteed by design, not tested in production

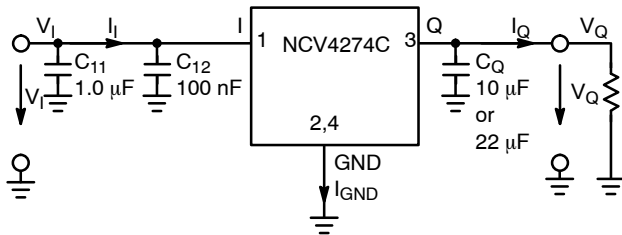


Figure 2. Measuring Circuit

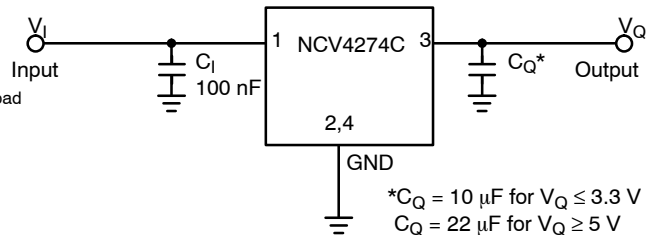


Figure 3. Application Circuit

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION

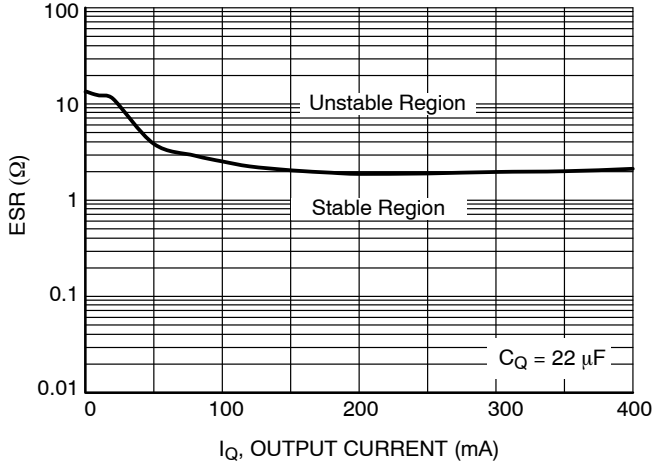


Figure 4. Output Stability with Output Capacitor ESR

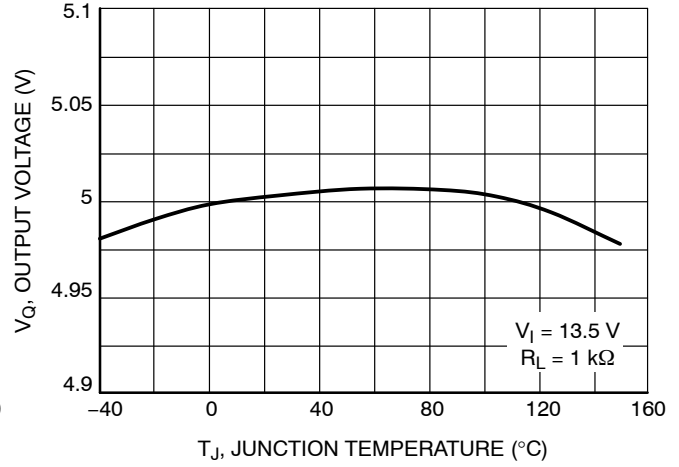


Figure 5. Output Voltage vs. Junction Temperature

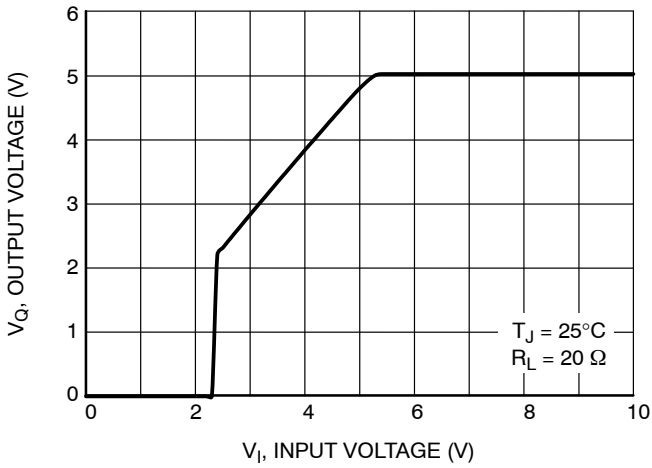


Figure 6. Output Voltage vs. Input Voltage

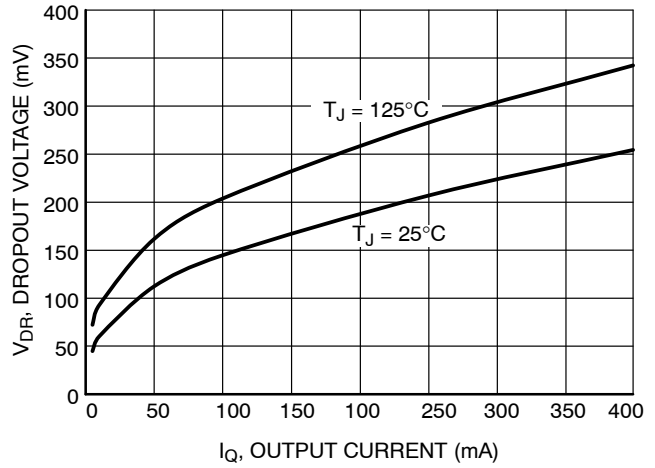


Figure 7. Dropout Voltage vs. Output Current

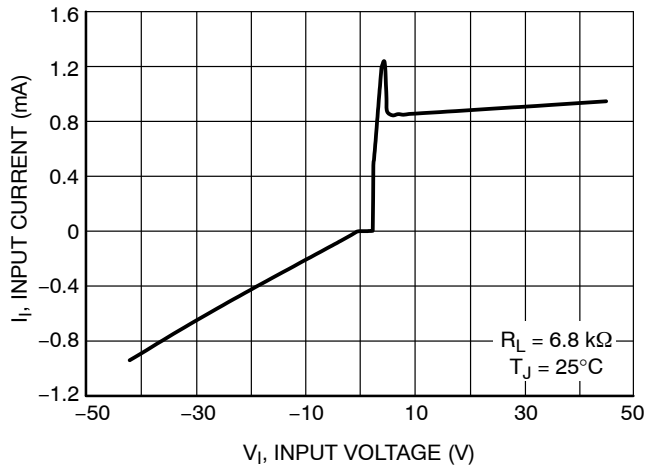


Figure 8. Input Current vs. Input Voltage

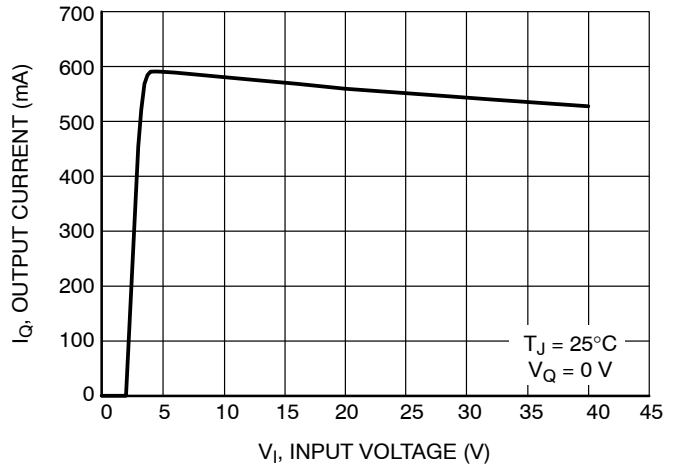


Figure 9. Maximum Output Current vs. Input Voltage

# NCV4274C

## TYPICAL CHARACTERISTIC CURVES – 5 V VERSION

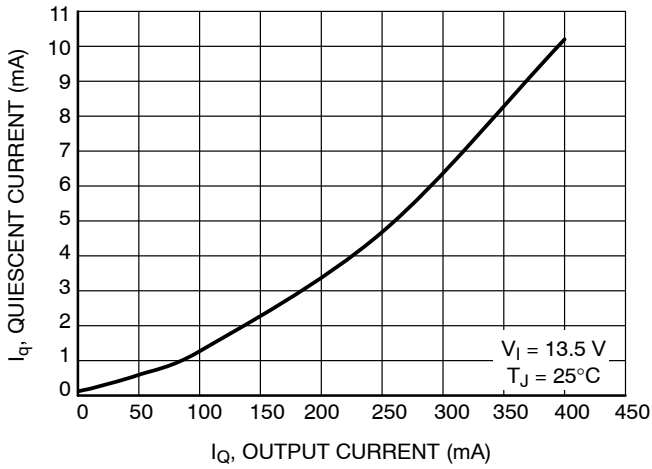


Figure 10. Quiescent Current vs. Output Current (High Load)

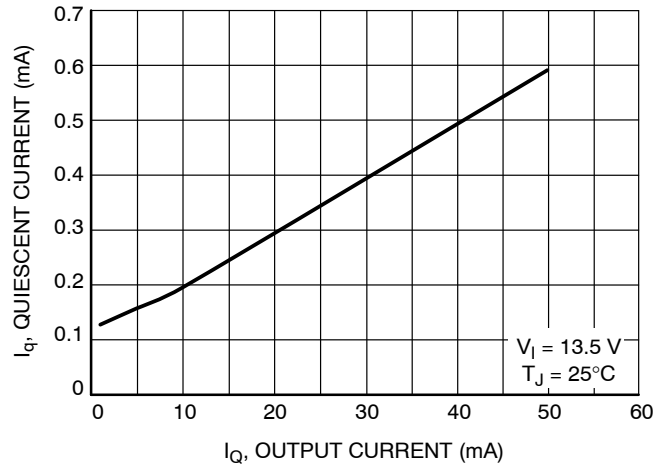


Figure 11. Quiescent Current vs. Output Current (Low Load)

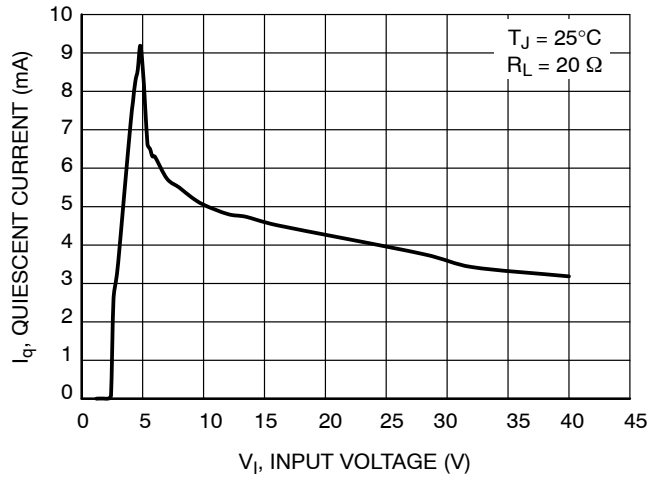


Figure 12. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION

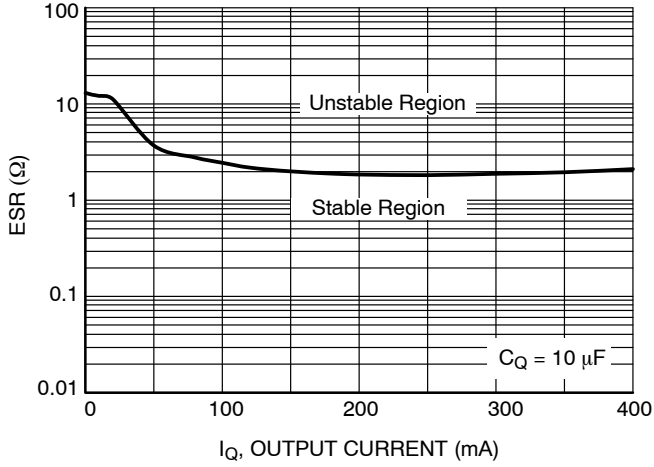


Figure 13. Output Stability with Output Capacitor ESR

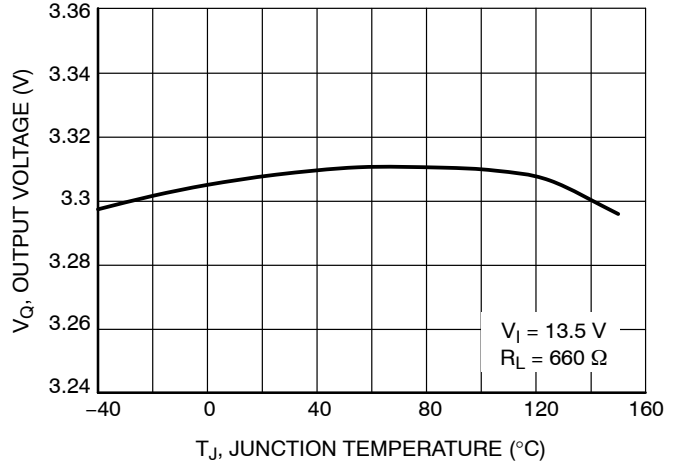


Figure 14. Output Voltage vs. Junction Temperature

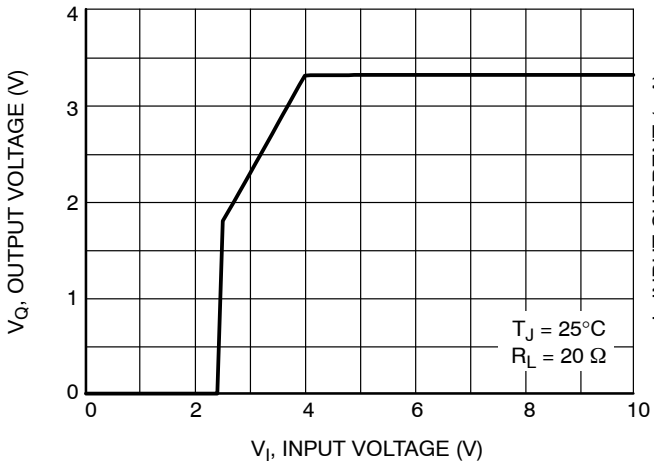


Figure 15. Output Voltage vs. Input Voltage

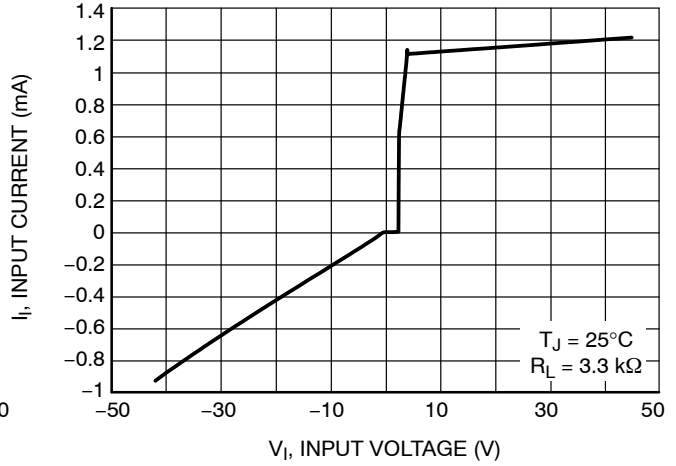


Figure 16. Input Current vs. Input Voltage

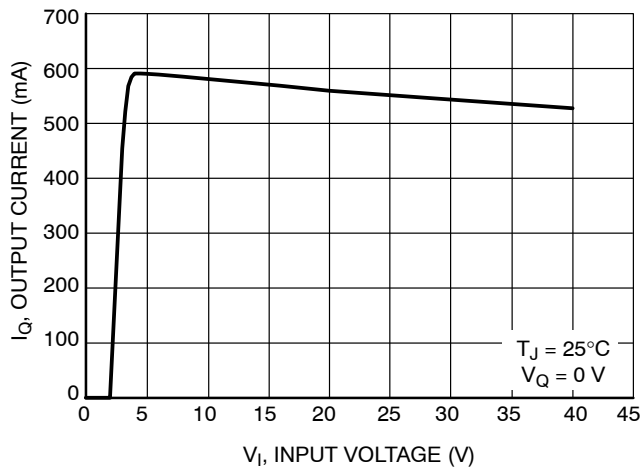


Figure 17. Maximum Output Current vs. Input Voltage

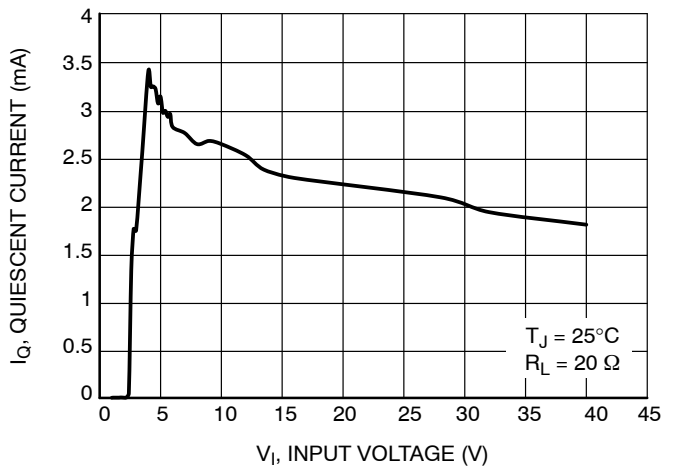


Figure 18. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION

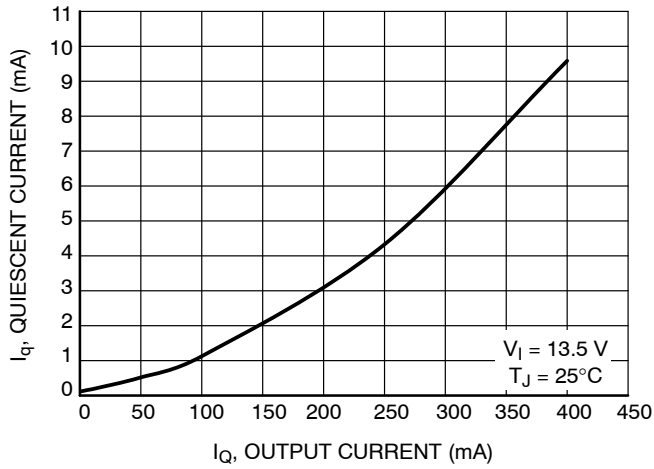


Figure 19. Quiescent Current vs. Output Current (High Load)

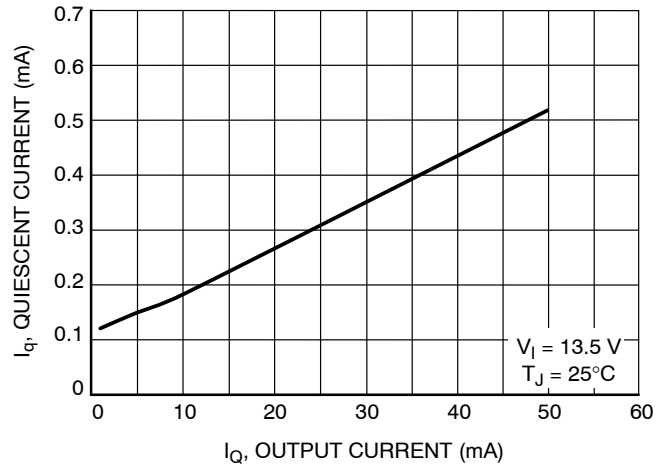


Figure 20. Quiescent Current vs. Output Current (Low Load)



APPLICATION DESCRIPTION

**Output Regulator**

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

**Stability Considerations**

The input capacitor C<sub>I1</sub> in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C<sub>I2</sub>.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information.

The value for the output capacitor C<sub>O</sub> shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Actual Stability Regions are shown in a graphs in the Typical Performance Characteristics section.

**Calculating Power Dissipation in a Single Output Linear Regulator**

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad (\text{eq. 1})$$

Where:

- V<sub>I(max)</sub> is the maximum input voltage,
- V<sub>Q(min)</sub> is the minimum output voltage,
- I<sub>Q(max)</sub> is the maximum output current for the application, and
- I<sub>q</sub> is the quiescent current the regulator consumes at I<sub>Q(max)</sub>.

Once the value of P<sub>D(max)</sub> is known, the maximum permissible value of R<sub>θJA</sub> can be calculated:

$$R_{\theta JA} = \frac{(150\text{ C} - T_A)}{P_D} \quad (\text{eq. 2})$$

The value of R<sub>θJA</sub> can then be compared with those in the package section of the data sheet. Those packages with R<sub>θJA</sub>’s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

**Heat Sinks**

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of R<sub>θJA</sub>:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (\text{eq. 3})$$

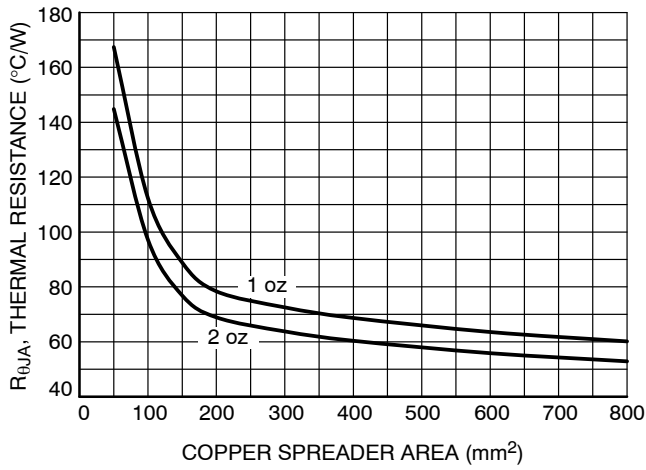
Where:

- R<sub>θJC</sub> = the junction–to–case thermal resistance,
- R<sub>θCS</sub> = the case–to–heat sink thermal resistance, and
- R<sub>θSA</sub> = the heat sink–to–ambient thermal resistance.

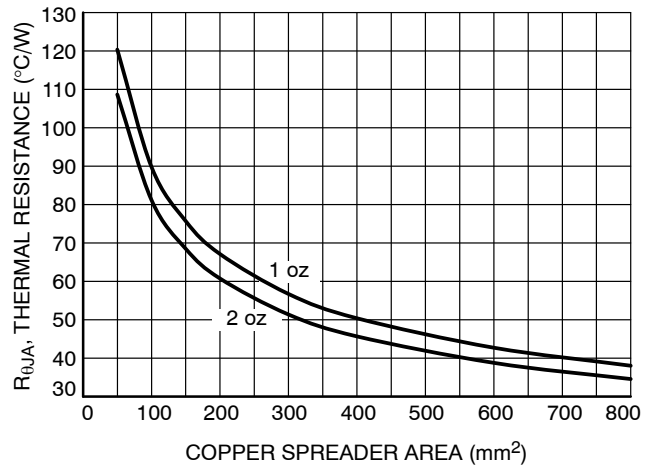
R<sub>θJC</sub> appears in the package section of the data sheet. Like R<sub>θJA</sub>, it too is a function of package type. R<sub>θCS</sub> and R<sub>θSA</sub> are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers.

Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the [ON Semiconductor Website](http://www.onsemi.com).

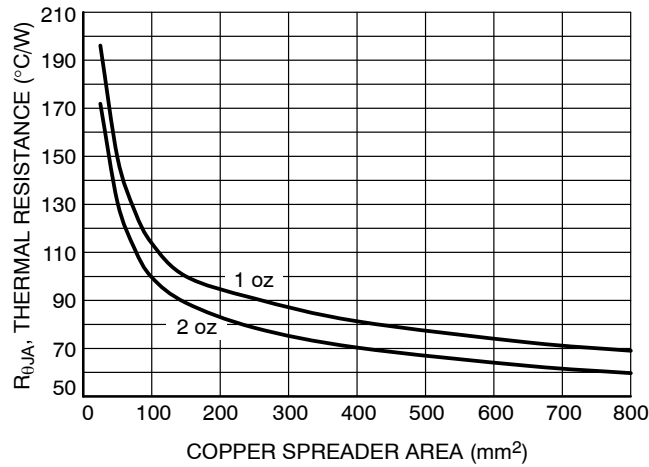
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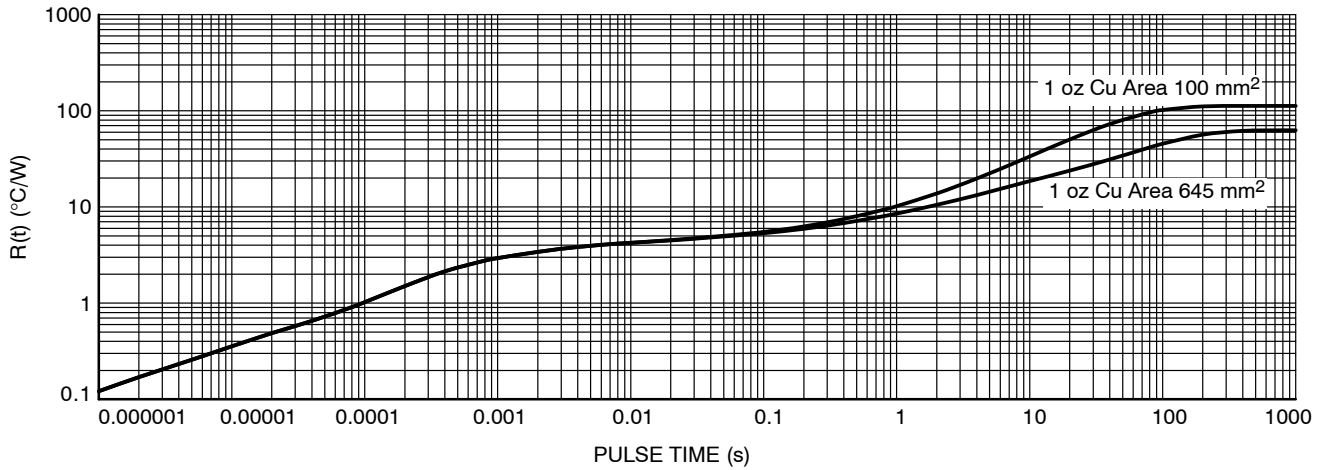
**Figure 21.  $R_{\theta JA}$  vs. Copper Spreader Area, DPAK 3-Lead**



**Figure 22.  $R_{\theta JA}$  vs. Copper Spreader Area, D<sup>2</sup>PAK 3-Lead**



**Figure 23.  $R_{\theta JA}$  vs. Copper Spreader Area, SOT 223-Lead**



**Figure 24. Single-Pulse Heating Curves, DPAK 3-Lead**

# NCV4274C

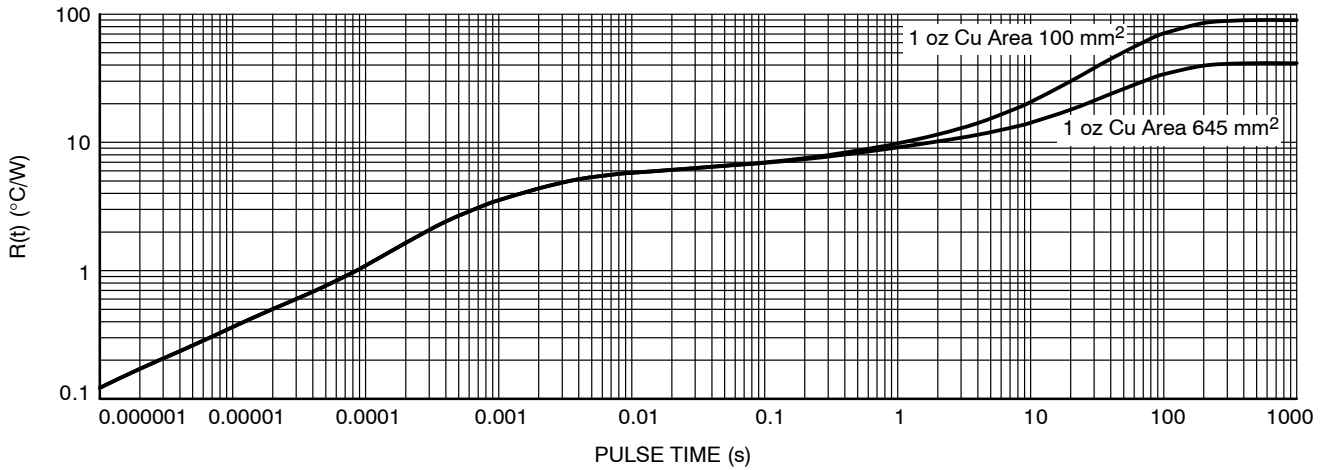


Figure 25. Single-Pulse Heating Curves, D<sup>2</sup>PAK 3-Lead

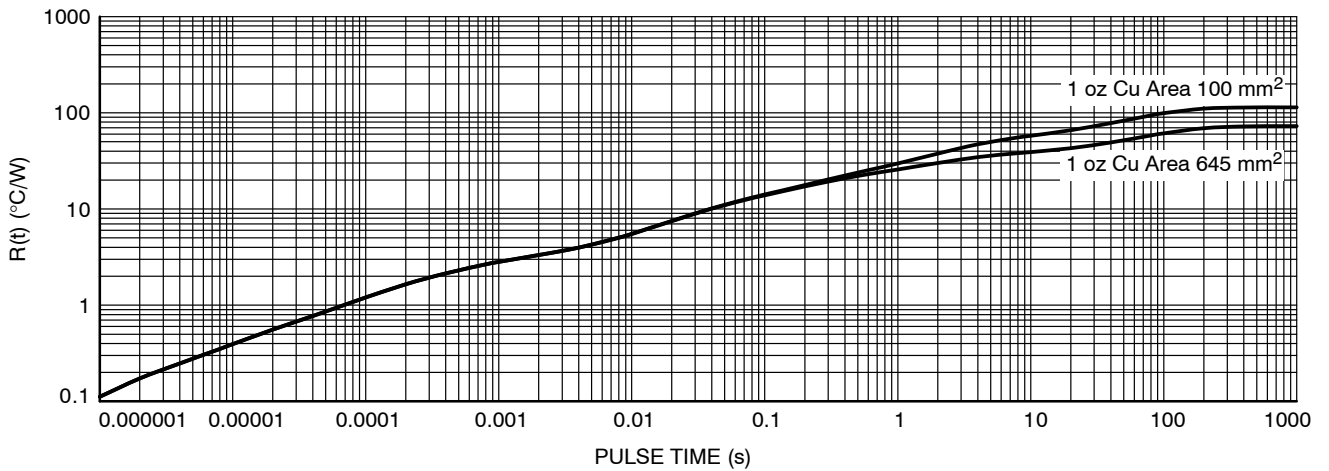


Figure 26. Single-Pulse Heating Curves, SOT 223-Lead

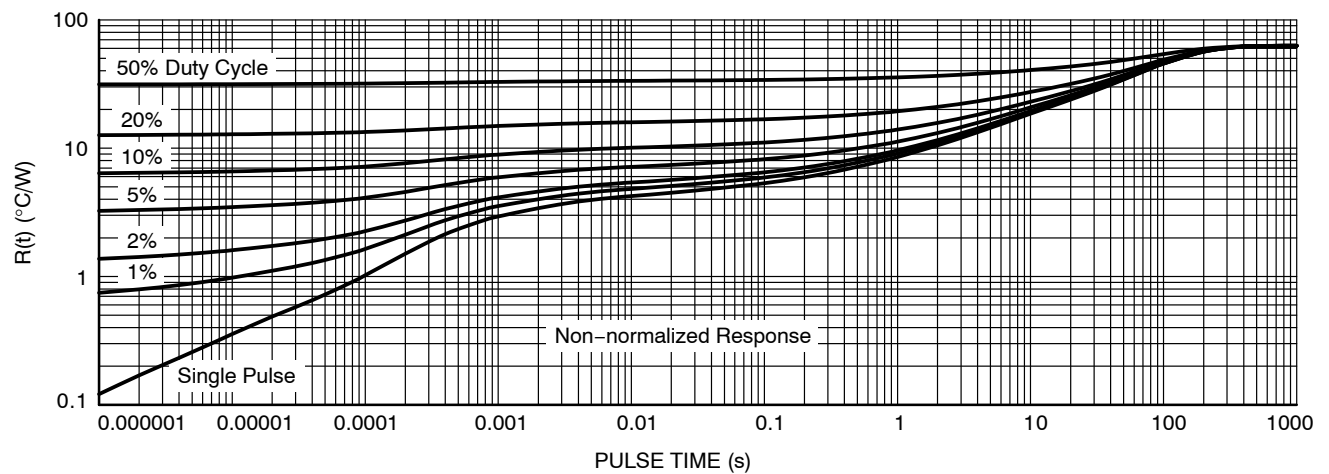


Figure 27. Duty Cycle for 1 inch<sup>2</sup> (645 mm<sup>2</sup>) Spreader Board, DPAK 3-Lead

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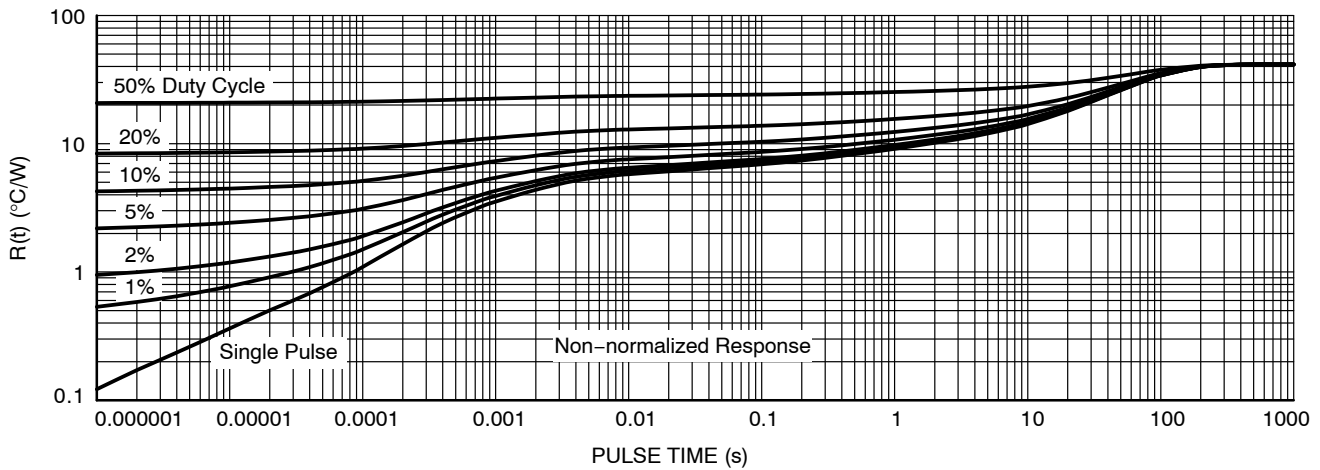


Figure 28. Duty Cycle for 1 inch<sup>2</sup> (645 mm<sup>2</sup>) Spreader Board, D<sup>2</sup>PAK 3-Lead

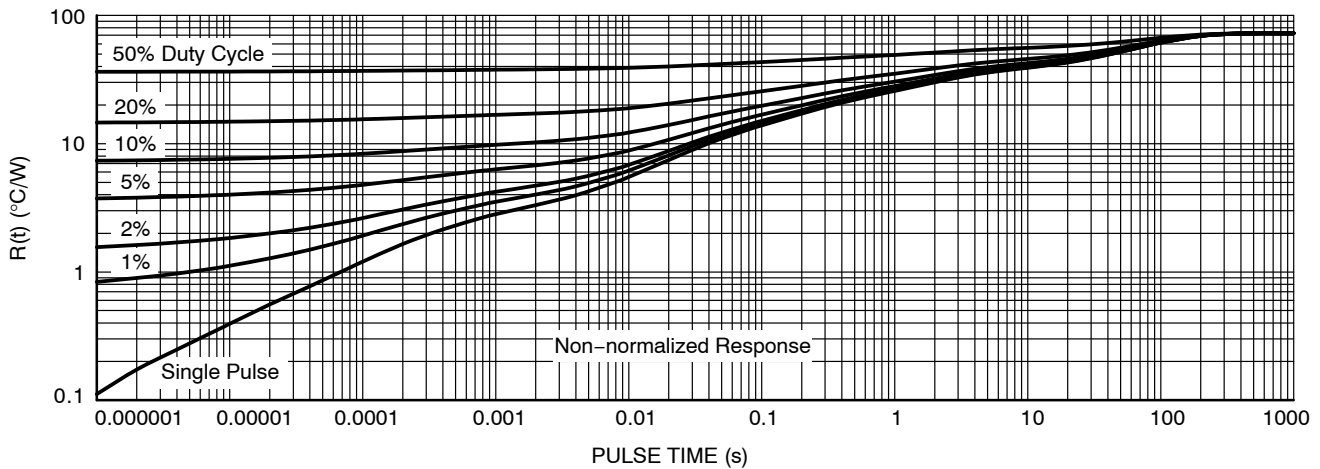


Figure 29. Duty Cycle for 1 inch<sup>2</sup> (645 mm<sup>2</sup>) Spreader Board, SOT 223-Lead

## ORDERING INFORMATION

Device*	Output Voltage Accuracy	Output Voltage	Package	Shipping†
NCV4274CDT33RKG	2%	3.3 V	DPAK (Pb-Free)	2500 / Tape & Reel
NCV4274CDS33R4G	2%	3.3 V	D2PAK (Pb-Free)	800 / Tape & Reel
NCV4274CDT50RKG	2%	5.0 V	DPAK (Pb-Free)	2500 / Tape & Reel
NCV4274CDS50R4G	2%	5.0 V	D2PAK (Pb-Free)	800 / Tape & Reel
NCV4274CST33T3G	2%	3.3 V	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV4274CST50T3G	2%	5.0 V	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

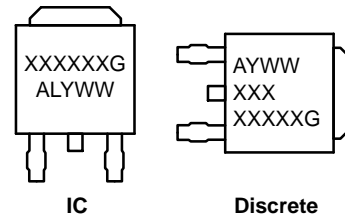


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

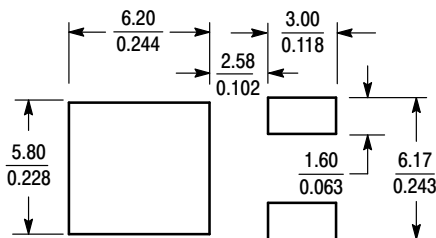


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*




SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>	<b>REF TO JEDEC TO-252</b>	
<b>DESCRIPTION:</b>	<b>DPAK SINGLE GAUGE SURFACE MOUNT</b>	<b>PAGE 1 OF 2</b>



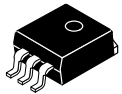
ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELLED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAM- BALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

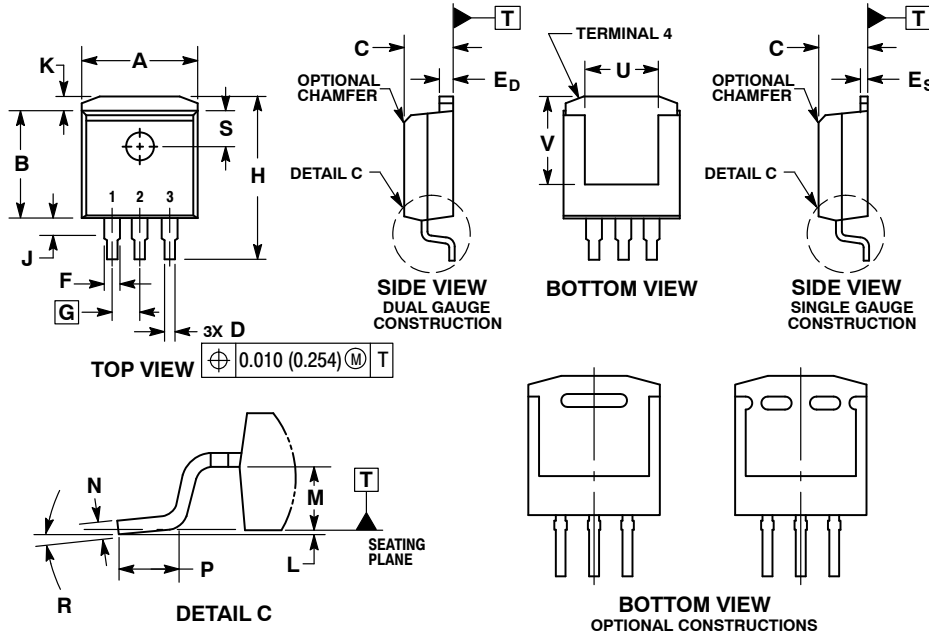
ON Semiconductor®



SCALE 1:1

D2PAK  
CASE 418AF  
ISSUE E

DATE 15 SEP 2015

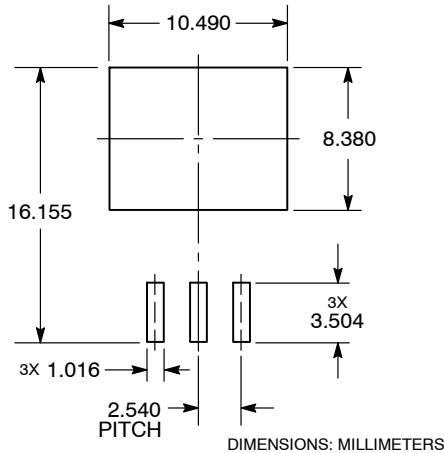


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

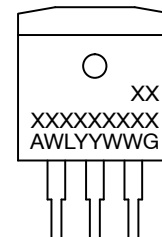
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E <sub>D</sub>	0.045	0.055	1.143	1.397
E <sub>S</sub>	0.018	0.026	0.457	0.660
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

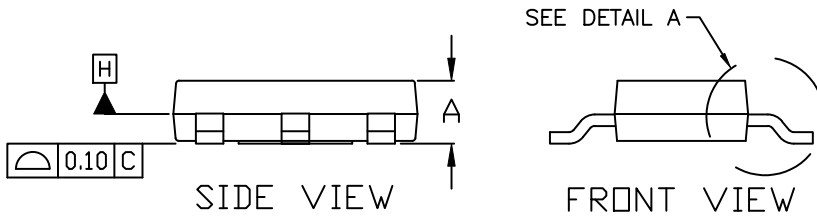
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

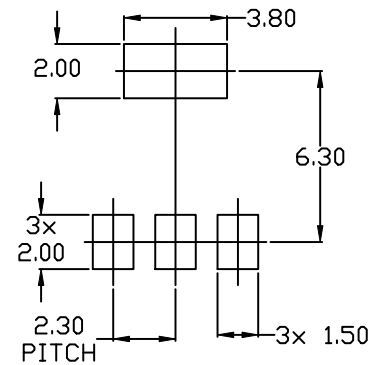
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***




- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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