

FEATURES:

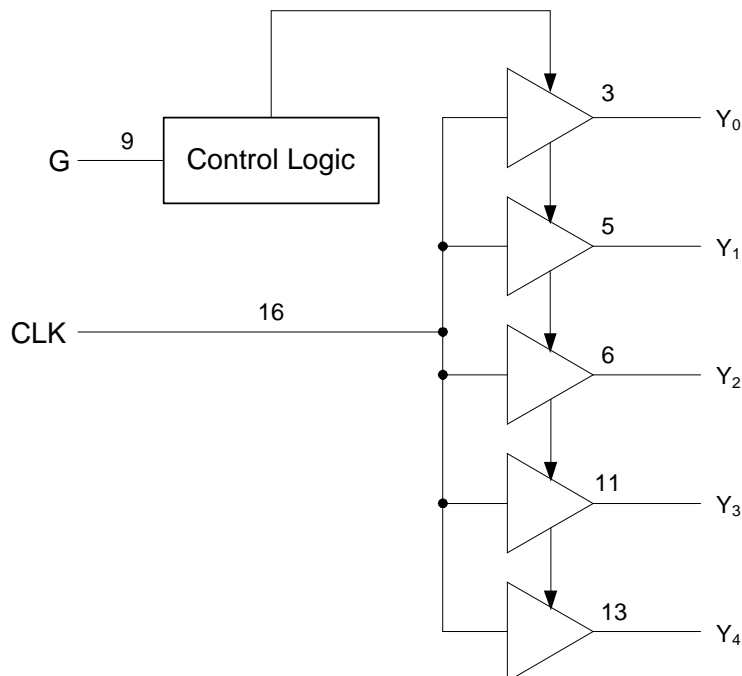
- High performance 1:5 clock driver for general purpose applications
- Operates up to 170MHz at $V_{DD} = 2.5V$
- Operates up to 200MHz at $V_{DD} = 3.3V$
- Pin-to-pin skew < 75ps at 3.3V operation
- V_{DD} range: 2.3V to 3.6V
- Output enable glitch suppression
- Available in TSSOP and VFQFPN packages

DESCRIPTION:

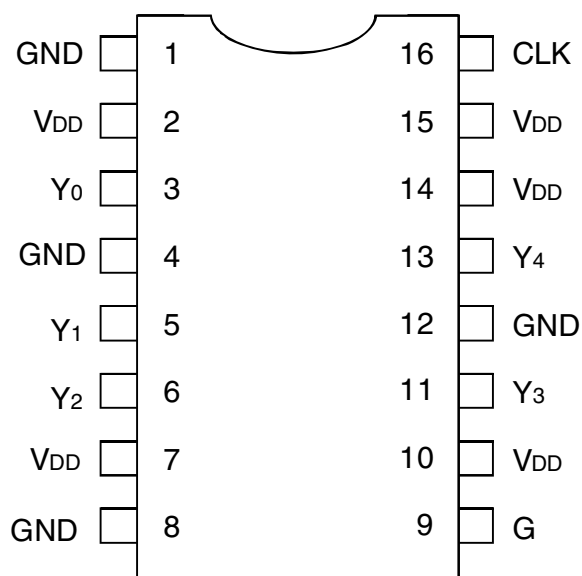
The IDT5V2305 is a high performance, low skew clock buffer that operates up to 200MHz. One bank of five outputs provides low skew copies of CLK. Through the use of control pin G, the outputs of bank Y(0:4) can be placed in a low state regardless of CLK input. The device operates in 2.5V and 3.3V environments. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The IDT5V2305 is characterized for operation from -40°C to +85°C.

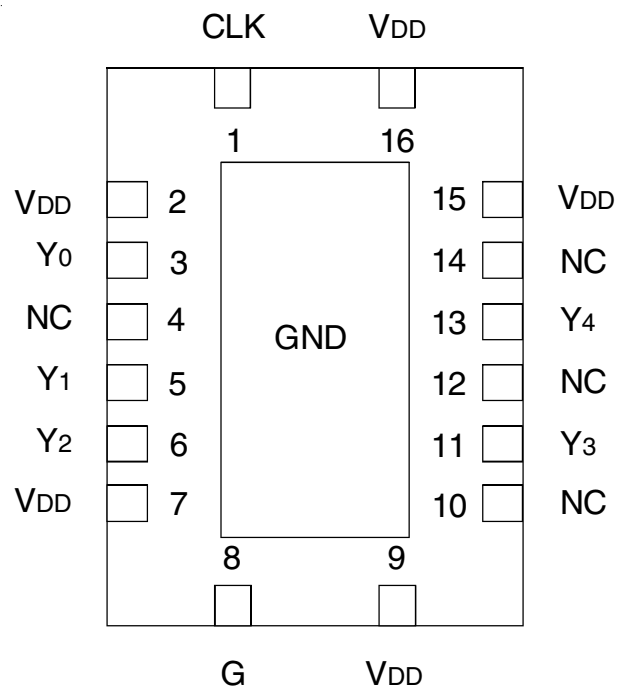
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW



VFQFPN
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|------------------|--|-------------------------------|------|
| V _{DD} | Power Supply Voltage | -0.5 to +4.6 | V |
| V _I | Input Voltage ⁽²⁾ | -0.5 to V _{DD} + 0.5 | V |
| V _O | Output Voltage ⁽²⁾ | -0.5 to V _{DD} + 0.5 | V |
| I _{IK} | Input Clamp Current V _I < 0 or V _I > V _{DD} | ±50 | mA |
| I _{OK} | Output Clamp Current V _O < 0 or V _O > V _{DD} | ±50 | mA |
| I _O | Continuous Total Output Current V _O < 0 to V _{DD} | ±50 | mA |
| T _{STG} | Storage Temperature | -65 to +150 | °C |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Not to exceed 4.6V.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------------|---|------|------|------|------|
| C _{IN} | Input Capacitance V _I = 0V or V _{DD} | — | 2.5 | — | pF |

FUNCTION TABLE⁽¹⁾

| Inputs | | Output |
|--------|-----|--------|
| G | CLK | Y(0:4) |
| L | X | L |
| H | H | H |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

PIN DESCRIPTION

| TERMINAL | | Description |
|-----------------|-----|--|
| Symbol | I/O | |
| G | I | Output Enable Control for Y(0:4) Outputs. This output enable is active HIGH. If this pin is Logic HIGH, the Y(0:4) clock outputs will follow the input clock (CLK). If this pin is logic LOW, the Y(0:4) outputs will drive low independent of the state of CLK. |
| Y(0:4) | O | Buffered Output Clocks |
| CLK | I | Input Reference Frequency |
| GND | | Ground |
| V _{DD} | PWR | DC Power Supply, 2.3V to 3.6V |

RECOMMENDED OPERATING RANGE

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--------------------------------|------|-----------------|------|
| V _{DD} | Internal Power Supply Voltage | 2.3 | 2.5 | | V |
| | | | 3.3 | 3.6 | |
| V _{IL} | Input Voltage LOW | V _{DD} = 3V to 3.6V | | 0.8 | V |
| | | V _{DD} = 2.3V to 2.7V | | 0.7 | |
| V _{IH} | Input Voltage HIGH | V _{DD} = 3V to 3.6V | 2 | | V |
| | | V _{DD} = 2.3V to 2.7V | 1.7 | | |
| V _I | Input Voltage | 0 | | V _{DD} | V |
| I _{OH} | Output Current HIGH | V _{DD} = 3V to 3.6V | | -12 | mA |
| | | V _{DD} = 2.3V to 2.7V | | -6 | |
| I _{OL} | Output Current LOW | V _{DD} = 3V to 3.6V | | 12 | mA |
| | | V _{DD} = 2.3V to 2.7V | | 6 | |
| T _A | Ambient Operating Temperature | -40 | | +85 | °C |

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max | Unit |
|-----------------|--------------------------------------|--|------|------|------|------|
| V _{IK} | Input Voltage | V _{DD} = 3V, I _{IN} = -18mA | | | -1.2 | V |
| I _{IN} | Input Current | V _I = 0V or V _{DD} | | | ±5 | μA |
| I _{DD} | Static Device Current ⁽¹⁾ | CLK = 0V or V _{DD} , I _O = 0mA, V _{DD} = 3.3V | | | 25 | μA |

NOTE:

1. For I_{DD} over frequency, see TEST CIRCUIT AND WAVEFORMS.

DC ELECTRICAL CHARACTERISTICS - V_{DD} = 3.3V ± 0.3V

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max | Unit |
|-----------------|---------------------------|--------------------------------|--------------------------|-----------------------|---------------------|------|------|
| V _{OH} | HIGH level Output Voltage | V _{DD} = Min. to Max. | I _{OH} = -100μA | V _{DD} - 0.2 | | | V |
| | | V _{DD} = 3V | I _{OH} = -12mA | 2.1 | | | |
| | | | I _{OH} = -6mA | 2.4 | | | |
| V _{OL} | LOW level Output Voltage | V _{DD} = Min. to Max. | I _{OH} = 100μA | | | 0.2 | V |
| | | V _{DD} = 3V | I _{OH} = 12mA | | | 0.8 | |
| | | | I _{OH} = 6mA | | | 0.55 | |
| I _{OH} | HIGH level Output Current | V _{DD} = 3V | V _O = 1V | -28 | | | mA |
| | | V _{DD} = 3.3V | V _O = 1.65V | | -36 | | |
| | | | V _O = 3.135V | | | -14 | |
| I _{OL} | LOW level Output Current | V _{DD} = 3V | V _O = 1.95V | 28 | | | mA |
| | | V _{DD} = 3.3V | V _O = 1.65V | | 36 | | |
| | | | V _O = 0.4V | | | 14 | |

NOTE:

1. All typical values are at respective nominal V_{DD}.

DC ELECTRICAL CHARACTERISTICS - $V_{DD} = 2.5V \pm 0.2V$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max | Unit |
|-----------------|---------------------------|--------------------------------|--------------------------|-----------------------|---------------------|------|------|
| V _{OH} | HIGH level Output Voltage | V _{DD} = Min. to Max. | I _{OH} = -100μA | V _{DD} - 0.2 | | | V |
| | | V _{DD} = 2.3V | I _{OH} = -6mA | 1.8 | | | |
| V _{OL} | LOW level Output Voltage | V _{DD} = Min. to Max. | I _{OH} = 100μA | | | 0.2 | V |
| | | V _{DD} = 2.3V | I _{OH} = 6mA | | | 0.55 | |
| I _{OH} | HIGH level Output Current | V _{DD} = 2.3V | V _O = 1V | -17 | | | mA |
| | | V _{DD} = 2.5V | V _O = 1.25V | | -25 | | |
| | | V _{DD} = 2.7V | V _O = 2.375V | | | -10 | |
| I _{OL} | LOW level Output Current | V _{DD} = 2.3V | V _O = 1.2V | 17 | | | mA |
| | | V _{DD} = 2.5V | V _O = 1.25V | | 25 | | |
| | | V _{DD} = 2.7V | V _O = 0.3V | | | 10 | |

NOTE:

1. All typical values are at respective nominal V_{DD}.

TIMING REQUIREMENTS OVER RECOMMENDED RANGE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max | Unit |
|------------------|-----------------|--------------------------------|------|------|-----|------|
| f _{CLK} | Clock Frequency | V _{DD} = 3V to 3.6V | 0 | | 200 | MHz |
| | | V _{DD} = 2.3V to 2.7V | 0 | | 170 | |

SWITCHING CHARACTERISTICS OVER OPERATING RANGE -

$$V_{DD} = 3.3V \pm 0.3V^{(1)}$$

| Symbol | Parameter | Test Conditions | Min. | Typ. ⁽¹⁾ | Max | Unit |
|--------------------------------------|-----------------------|---|------|---------------------|-----|------|
| t _{PLH} t _{PHL} | CLK to Yx | f = 0MHz to 200MHz, C _L = 25pF | 1.3 | | 2.6 | ns |
| t _{sk(o)} ⁽²⁾ | Output Skew, Yx to Yx | | | | 75 | ps |
| t _{sk(p)} | Pulse Skew | | | | 200 | ps |
| t _{sk(pp)} | Part-to-Part Skew | | | | 500 | ps |
| t _r | Rise Time | V _O = 0.4V to 2V ⁽³⁾ | 1.0 | | 2.3 | V/ns |
| t _f | Fall Time | V _O = 2V to 0.4V ⁽³⁾ | 1.0 | | 2.3 | V/ns |
| t _{SU} | G before CLK↓ | V _(THRESHOLD) = V _{DD} /2 | 0.1 | | | ns |
| t _H | G after CLK↓ | | 0.4 | | | |

NOTES:

1. All typical values are at respective nominal V_{DD}.
2. This specification is only valid for equal loading of all outputs.
3. Measured at 100MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE -

$$V_{DD} = 2.5V \pm 0.2V^{(1)}$$

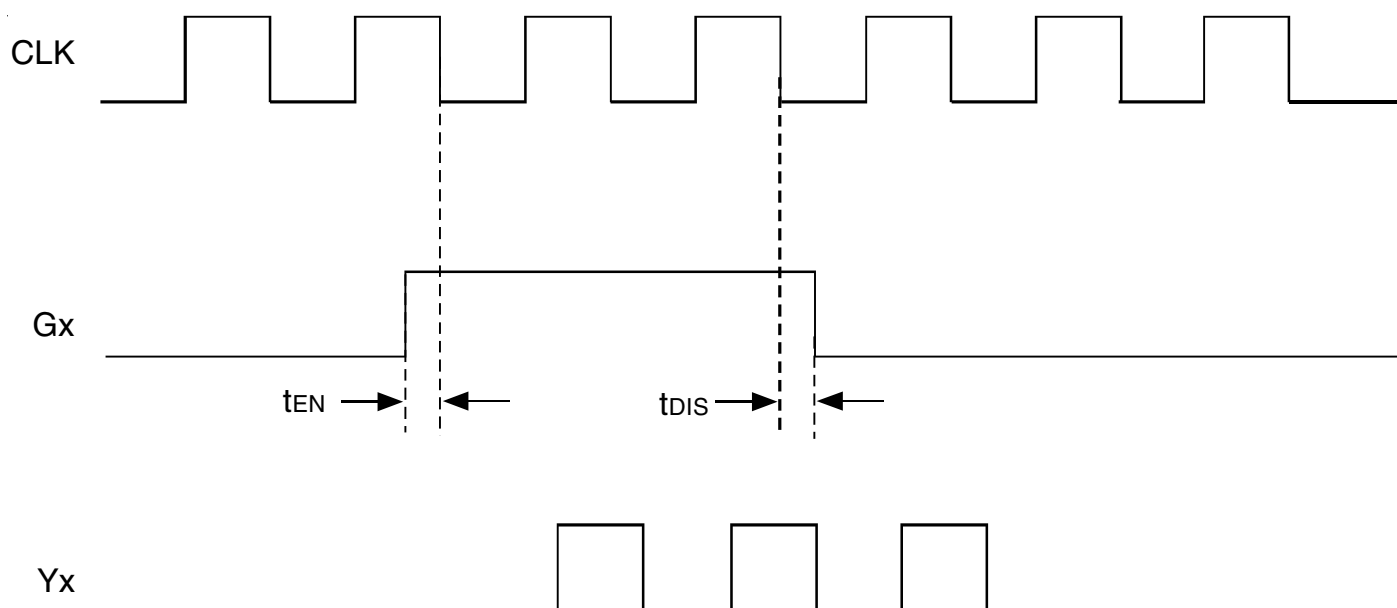
| Symbol | Parameter | Test Conditions | Min. | Typ. ⁽¹⁾ | Max | Unit |
|--------------------------------------|-----------------------|---|------|---------------------|-------|------|
| t _{PLH} t _{PHL} | CLK to Yx | f = 0MHz to 170MHz, C _L = 25pF | 1.5 | | 3 | ns |
| t _{sk(o)} ⁽²⁾ | Output Skew, Yx to Yx | | | | 100 | ps |
| t _{sk(p)} | Pulse Skew | | | | 350 | ps |
| t _{sk(pp)} | Part-to-Part Skew | | | | 600 | ps |
| t _r | Rise Time | V _O = 0.4V to 1.7V ⁽³⁾ | 0.4 | | 1.625 | V/ns |
| t _f | Fall Time | V _O = 1.7V to 0.4V ⁽³⁾ | 0.4 | | 1.625 | V/ns |
| t _{SU} | G before CLK↓ | V _(THRESHOLD) = V _{DD} /2 | 0.1 | | | ns |
| t _H | G after CLK↓ | | 0.4 | | | |

NOTES:

1. All typical values are at respective nominal V_{DD}.
2. This specification is only valid for equal loading of all outputs.
3. Measured at 100MHz.

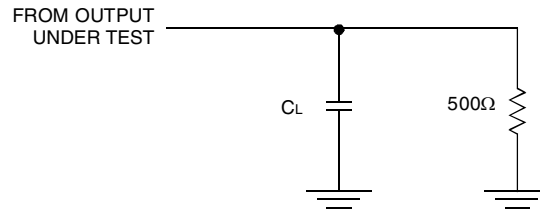
OUTPUT ENABLE GLITCH SUPPRESSION CIRCUIT

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer will be enabled on the next full period of the input clock (negative edge triggered by the input clock). The G input must be stable one t_{EN} - time prior to the falling edge of the CLK for predictable operation.



G (t_{EN} , t_{DIS}) Relative to CLK↓

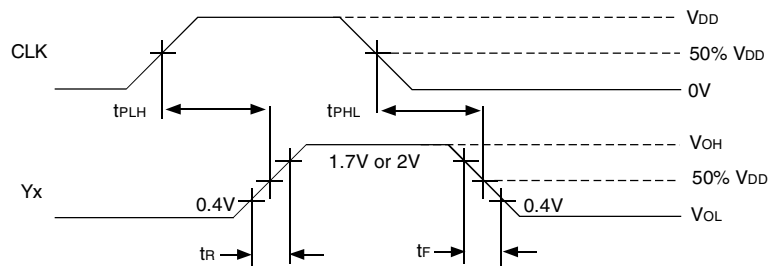
TEST CIRCUITS AND WAVEFORMS



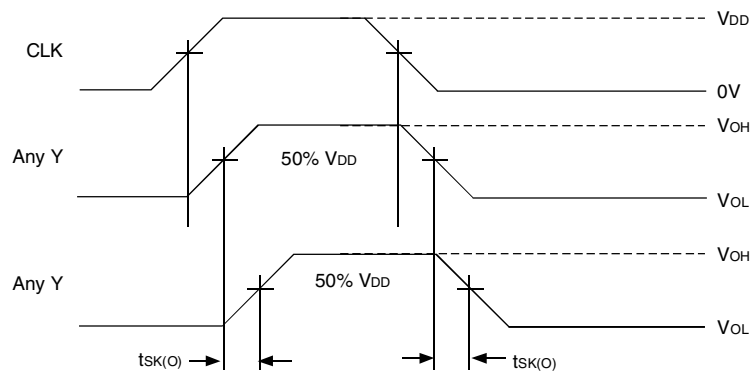
NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 200MHz; $Z_o = 50\Omega$; $t_r < 1.2ns$; $t_f < 1.2ns$.

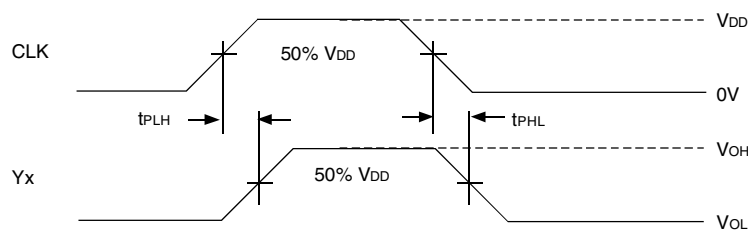
Test Load Circuit



Voltage Waveforms Propagation Delay Times



Output Skew

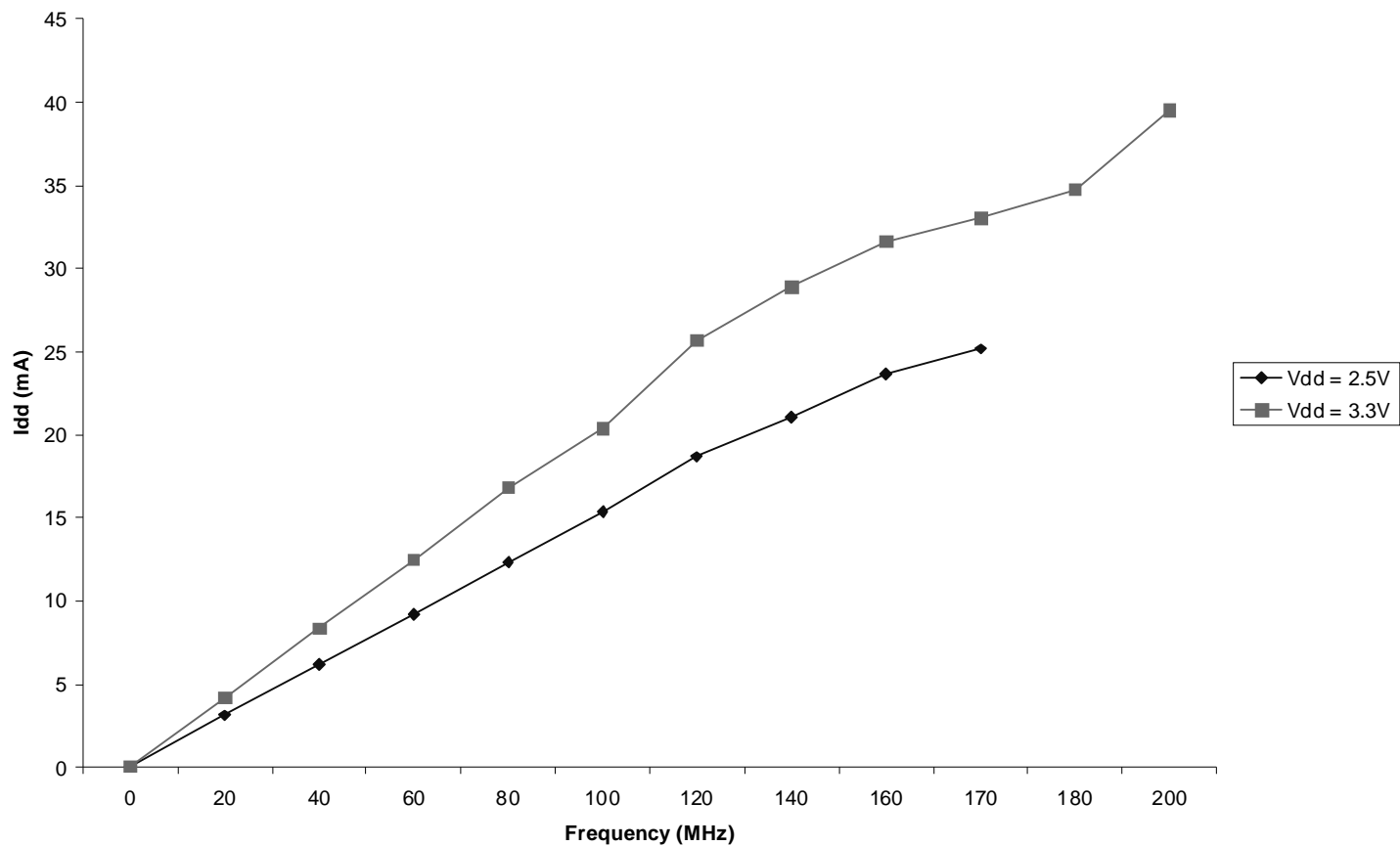


$$t_{SK(P)} = | t_{PLH} - t_{PHL} |$$

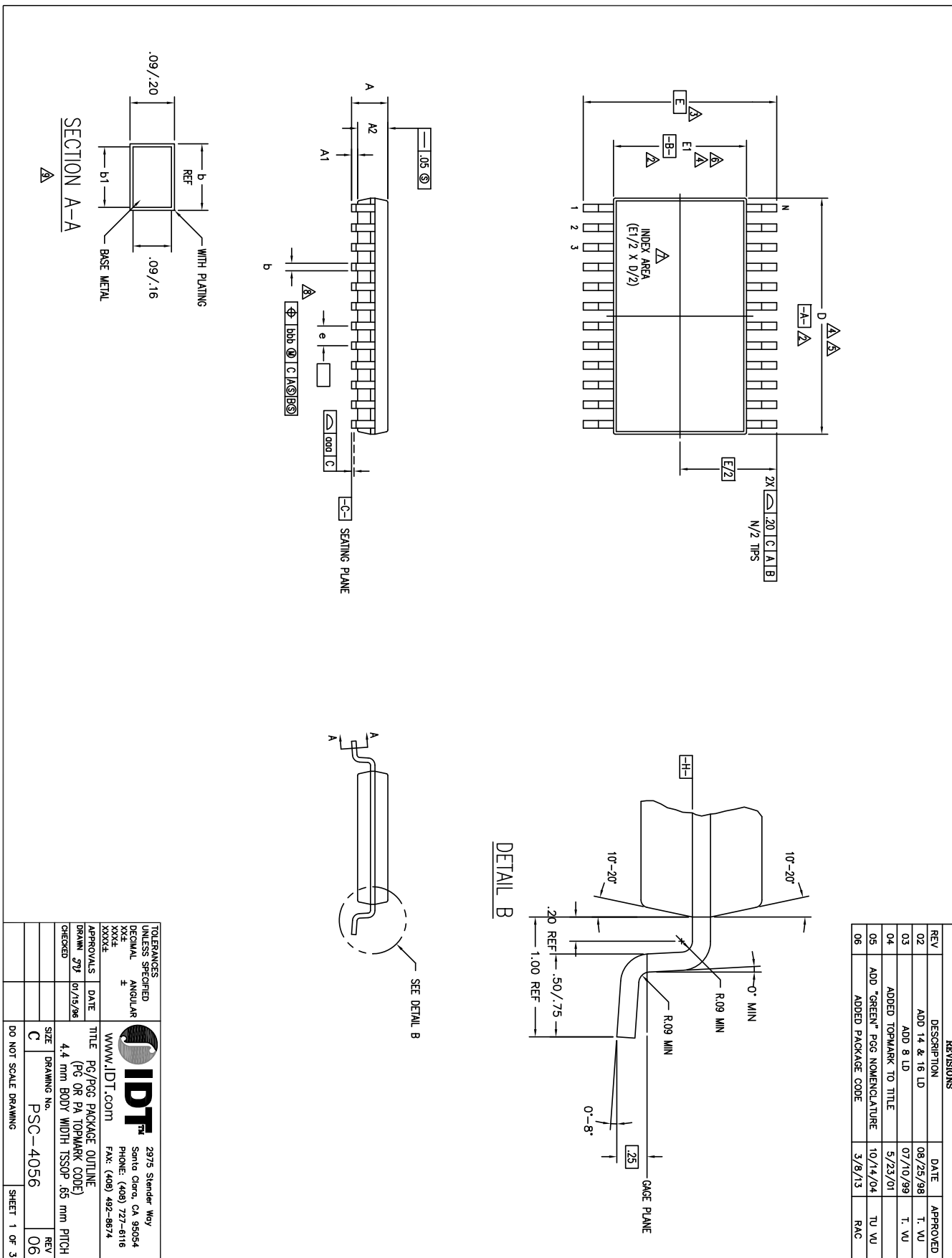
Pulse Skew

TEST CIRCUITS AND WAVEFORMS (cont.)

I_{dd} vs Frequency











PACKAGE DRAWINGS AND DIMENSIONS - 16TSSOP



PACKAGE DRAWINGS AND DIMENSIONS - 16TSSOP (cont.)

| SYMBOL | PG/PGG16 | | | NOTE |
|--------|-----------------|------|------|------|
| | JEDEC VARIATION | | | |
| | AB | | | |
| | MIN | NOM | MAX | |
| A | — | — | 1.20 | |
| A1 | .05 | — | .15 | |
| A2 | .80 | 1.00 | 1.05 | |
| D | 4.90 | 5.00 | 5.10 | 4,5 |
| E | 6.40 BSC | | | 3 |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 |
| e | .65 BSC | | | |
| b | .19 | — | .30 | |
| b1 | .19 | .22 | .25 | |
| aaa | — | — | .10 | |
| bbb | — | — | .10 | |
| N | 16 | | | |

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
-  DATUMS $\boxed{-A-}$ AND $\boxed{-B-}$ TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$
-  DIMENSION E TO BE DETERMINED AT SEATING PLANE $\boxed{-C-}$
-  DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$
-  DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
-  DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
-  DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
-  LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
-  THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

ORDERING INFORMATION

| Part/Order Number | Shipping Packaging | Package | Temperature |
|-------------------|--------------------|---------------|---------------|
| 5V2305PGGI | Tubes | 16-pin TSSOP | -40° to +85°C |
| 5V2305PGGI8 | Tape and Reel | 16-pin TSSOP | -40° to +85°C |
| 5V2305NRGI | Tubes | 16-pin VFQFPN | -40° to +85°C |
| 5V2305NRGI8 | Tape and Reel | 16-pin VFQFPN | -40° to +85°C |

"G" suffix to the part number denotes Pb-free configuration, RoHS compliant.

REVISION HISTORY

August 11, 2014 Pg. 5; Changed Rise/Fall Time minimum specs in 3.3V Switching Characteristics table from 0.7V/ns to 1.0V/ns
September 25, 2014 Added 16TSSOP landing pattern and 16VFQFPN/TSSOP package drawings

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.