ADVANCED MEMORY BUFFER FOR FULLY BUFFERED DIMM MODULES

IDTAMB0480 PRODUCT BRIEF

FEATURES:

- **Advanced Memory Buffer for Fully buffered DIMMs**
- **3.2 and 4 Gbit/s serial speeds (DDR2-533 and 667 DRAM)**
- **Support for up to eight DIMMs per channel**
- **Repeater Mode for extending FB-DIMM links**
- **Northbound and Southbound single lane fail over and channel error detection**
- **Voltage and Timing margin high-speed I/O test capability**
- **Fully Supports the FB-DIMM configuration register set**
- **Test features supported include:**
  - **Integrated thermal sensor and status indicator**
  - **Supports MEMBIST, IBIST and Virtual Host mode**
  - **Transparent mode and direct access mode for DRAM testing**
- **Complies with JEDEC Architecture and Protocol Specification**
- **Available in 655 ball FCBGA package**

EXPANDED FEATURES:

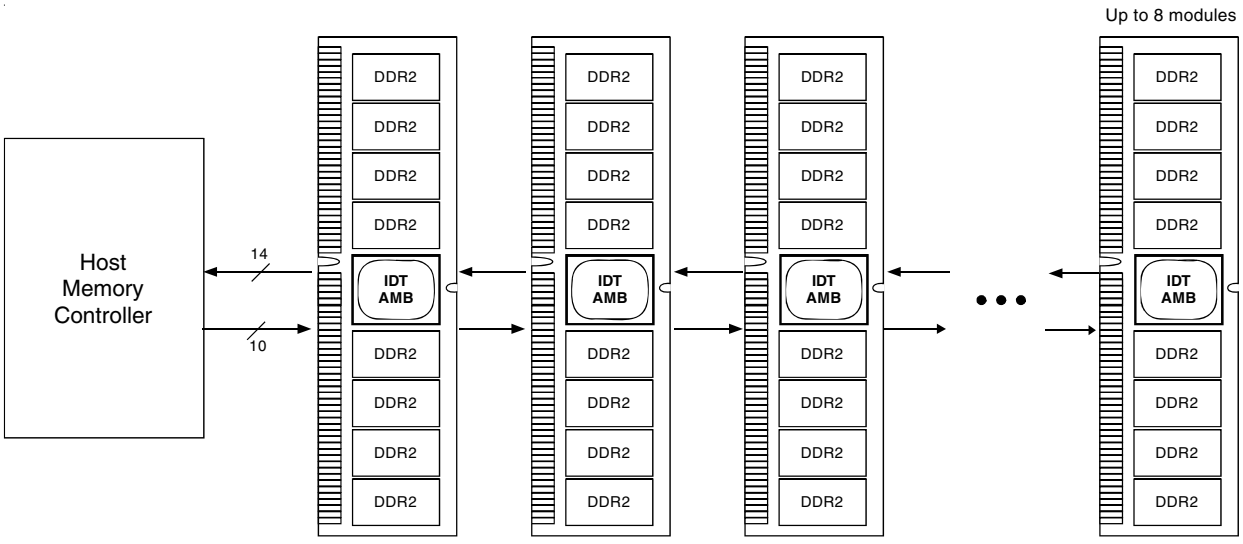
- **Wide range DDR Timing Control**
- **Superfine adjustment for DDR timing**
- **Wide range of DDR slew rate control**
- **Slew rate controllable independent of output impedance**
- **High speed SMBus in test mode**
- **IBIST IDT PRBS Generator**

DESCRIPTION:

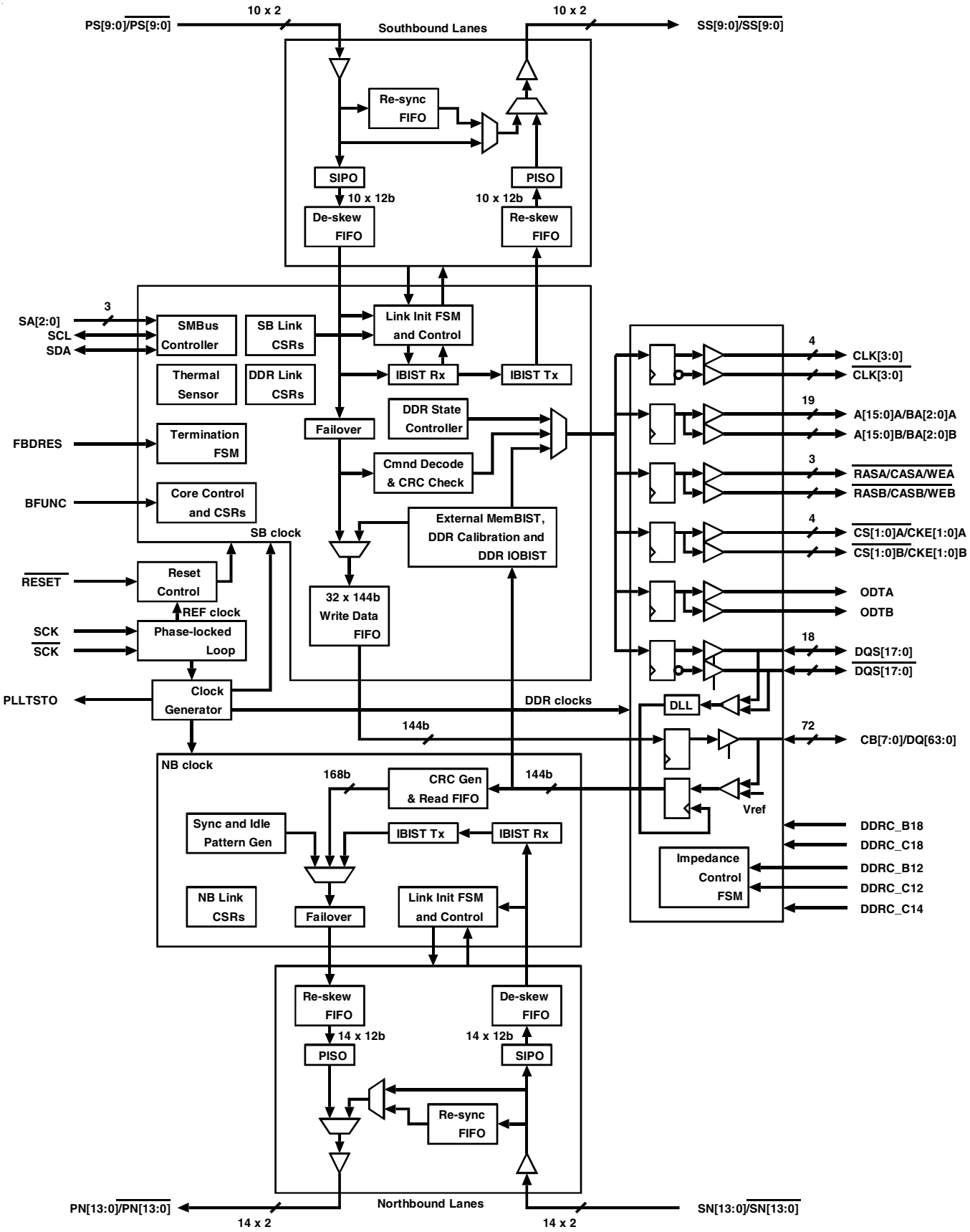
The fully buffered dual in-line memory module (FB-DIMM) is the next generation memory architecture to meet the growing memory requirement of servers and workstations. The IDT Advanced Memory Buffer (AMB) chip is the essential building block located on each FB-DIMM. The IDT AMB receives commands and data from the host controller to control and write/read data to/from the DRAMs on the DIMM. Commands and write data are sent southbound from the host controller to AMBs in a daisy chain fashion and interpreted by the target AMB. Status and read data are sent northbound from AMBs to the host controller also in a daisy chain fashion, passing through non-target AMBs. This unique channel structure alleviates buffer loading issues common in registered DIMM technology, enabling designers to use a large number of DIMMs within a single system.

IDTAMB0480 complies with the latest JEDEC defined FB-DIMM Architecture and Protocol Specification and supports DDR2-533 and DDR2-667 DRAM. It also enables serial data transfer at 3.2 and 4.0Gbps. The IDTAMB0480 supports servers, workstations, storage devices and communication applications that support the next generation FB-DIMM architecture.

FDB MEMORY CHANNEL



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			VSS	DQ26	DQ12	VDD	DQS 10	DQ13	VDD	$\overline{\text{DQS1}}$	DQ10	VDD	TEST LO	VDD	VDD
B		VDD	DQS3	$\overline{\text{DQS3}}$	VSS	DQ14	$\overline{\text{DQS 10}}$	VSS	DQ11	DQS1	VSS	DDRC _B12	TEST LO	VDD	VSS
C	VSS	DQS2	DQ18	VSS	DQ4	$\overline{\text{DQS9}}$	VSS	DQ15	DQ9	VSS	DQ8	DDRC _C12	VSS	DDRC _C14	DQS 17
D	DQ19	$\overline{\text{DQS2}}$	VSS	DQ16	DQ24	VSS	DQS9	DQ7	VSS	DQ3	DQS0	VSS	$\overline{\text{DQS8}}$	DQS8	VDD
E	DQ21	VSS	DQ17	DQ29	VSS	DQ25	DQ6	VSS	DQ5	DQ1	VSS	DQ0	CB1	VSS	CB2
F	VSS	DQ20	DQ23	VSS	DQ31	DQ27	VSS	TEST LO	TEST	VSS	$\overline{\text{DQS0}}$	DQ2	VDD	CB0	CB3
G	$\overline{\text{DQS 11}}$	DQS 11	NC	NC	NC	VSS	DQS 12	$\overline{\text{DQS 12}}$	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	VSS	NC	NC	NC	DQ28	DQ30	VSS	NC	NC	NC	VSS	VDD	VSS	VDD
J	VSS	CLK2	NC	NC	NC	BA1A	VSS	CKE 1A	NC	NC	NC	VDD	VSS	VDD	VSS
K	$\overline{\text{CLK2}}$	CLK0	NC	NC	NC	VSS	$\overline{\text{WEA}}$	$\overline{\text{RASA}}$	NC	NC	NC	VSS	VCC	VSS	VCC
L	$\overline{\text{CLK0}}$	VSS	NC	NC	NC	A0A	CKE 0A	VSS	NC	NC	NC	VCC	VSS	VCC	VSS
M	ODT 0A	RFU	NC	NC	NC	$\overline{\text{CASA}}$	VSS	BA2A	NC	NC	NC	VSS	VCC	VSS	VCC
N	$\overline{\text{CS1A}}$	$\overline{\text{CS0A}}$	NC	NC	NC	VSS	BA0A	A10A	NC	NC	NC	VCC	VSS	VCC	VSS
P	A6A	VSS	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	VSS	VCC	VSS	VCC
R	VSS	A8A	NC	NC	NC	A11A	VSS	A5A	NC	NC	NC	VCC	VSS	VCC	VSS
T	A4A	A13A	NC	NC	NC	VSS	A9A	A7A	NC	NC	NC	VSS	VCC	VSS	VCC
U	PN0	$\overline{\text{PN0}}$	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	VCC FBD	VSS	VSS
V	PN1	$\overline{\text{PN1}}$	VSS	SN0	$\overline{\text{SN0}}$	VCC FBD	VSS	VCC FBD	VSS	RFU(1)	RFU(1)	VCC FBD	VSS	VSS	VSS
W	PN2	$\overline{\text{PN2}}$	VSS	SN1	$\overline{\text{SN1}}$	$\overline{\text{SN3}}$	$\overline{\text{SN4}}$	$\overline{\text{SN5}}$	$\overline{\text{SN13}}$	$\overline{\text{SN12}}$	$\overline{\text{SN6}}$	$\overline{\text{SN7}}$	$\overline{\text{SN8}}$	$\overline{\text{SN9}}$	$\overline{\text{SN10}}$
Y	PN3	$\overline{\text{PN3}}$	VSS	SN2	$\overline{\text{SN2}}$	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	VSS	PN4	$\overline{\text{PN4}}$	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB		VSS	$\overline{\text{RESET}}$	$\overline{\text{PN5}}$	$\overline{\text{PN13}}$	RFU(1)	$\overline{\text{PN12}}$	$\overline{\text{PN6}}$	$\overline{\text{PN7}}$	$\overline{\text{PN8}}$	$\overline{\text{PN9}}$	VSS APLL	VCC APLL	$\overline{\text{PN10}}$	$\overline{\text{PN11}}$
AC			VSS	PN5	PN13	RFU(1)	PN12	PN6	PN7	PN8	PN9	FBD RES	PLL TSTO	PN10	PN11

FCBGA
TOP VIEW, LEFT SIDE

NOTE:
1. These pin positions are reserved for forward clocks to be used in future implementations.

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	VDD	TEST	VDD	DQ52	DQS15	VDD	DQ49	$\overline{DQS6}$	VDD	DQ48	DQ38	VDD		
B	VDD	TEST LO	DDRC_B18	VSS	$\overline{DQS15}$	DQ53	VSS	DQS6	DQ50	VSS	$\overline{DQS13}$	DQS13	VSS	
C	$\overline{DQS17}$	VSS	DDRC_C18	DQ54	VSS	DQ55	DQ51	VSS	DQS7	DQ56	VSS	DQ46	$\overline{DQS14}$	VDD
D	CB6	CB7	VSS	DQS16	DQ63	VSS	DQ59	$\overline{DQS7}$	VSS	DQ36	DQ44	VSS	DQS14	DQ47
E	VSS	CB5	$\overline{DQS16}$	VSS	DQ61	DQ57	VSS	DQ58	DQ39	VSS	DQ33	DQ45	VSS	DQ41
F	CB4	VDD	DQ62	DQ60	VSS	TEST	TEST	VSS	DQ37	DQ35	VSS	$\overline{DQS5}$	DQ43	VSS
G	TEST LO	RFU	RFU	NC	NC	NC	DQS4	$\overline{DQS4}$	VSS	NC	NC	NC	DQS5	DQ40
H	VSS	VDD	VSS	NC	NC	NC	VSS	DQ34	DQ32	NC	NC	NC	VSS	DQ42
J	VDD	VSS	VDD	NC	NC	NC	$\overline{RASB}$	VSS	RFU	NC	NC	NC	$\overline{CLK3}$	VSS
K	VSS	VCC	VSS	NC	NC	NC	ODT 0B	$\overline{CS1B}$	VSS	NC	NC	NC	$\overline{CLK1}$	CLK3
L	VCC	VSS	VCC	NC	NC	NC	VSS	$\overline{CASB}$	$\overline{WEB}$	NC	NC	NC	VSS	CLK1
M	VSS	VCC	VSS	NC	NC	NC	$\overline{CS0B}$	VSS	BA1B	NC	NC	NC	CKE0B	VSS
N	VCC	VSS	VCC	NC	NC	NC	A0B	A2B	VSS	NC	NC	NC	BA0B	BA2B
P	VSS	VCC	VSS	NC	NC	NC	VSS	A4B	A1B	NC	NC	NC	VSS	CKE1B
R	VCC	VSS	VCC	NC	NC	NC	A6B	VSS	A10B	NC	NC	NC	A3B	VSS
T	VSS	VCC	VSS	NC	NC	NC	A11B	A9B	VSS	NC	NC	NC	A7B	A5B
U	VSS	Vcc FBD	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	$\overline{PS8}$	PS8
V	Vcc FBD	VSS	Vcc FBD	VSS	Vcc FBD	RFU(1)	RFU(1)	VSS	A13B	A12B	SA2	SA1	$\overline{PS7}$	PS7
W	VSS	$\overline{SS0}$	$\overline{SS1}$	$\overline{SS2}$	$\overline{SS3}$	$\overline{SS4}$	$\overline{SS9}$	$\overline{SS5}$	$\overline{SS6}$	$\overline{SS7}$	$\overline{SS8}$	VSS	$\overline{PS6}$	PS6
Y	VSS	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	VSS	$\overline{PS5}$	PS5
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	$\overline{PS9}$	PS9	VSS
AB	VSS	$\overline{SN11}$	VSS	SCK	TESTLO_AB20	$\overline{PS0}$	$\overline{PS1}$	$\overline{PS2}$	$\overline{PS3}$	$\overline{PS4}$	RFU(1)	VDD SPD	VSS	
AC	RFU	SN11	VSS	$\overline{SCK}$	TESTLO_AC20	PS0	PS1	PS2	PS3	PS4	RFU(1)	VSS		

FCBGA
TOP VIEW, RIGHT SIDE

NOTE:
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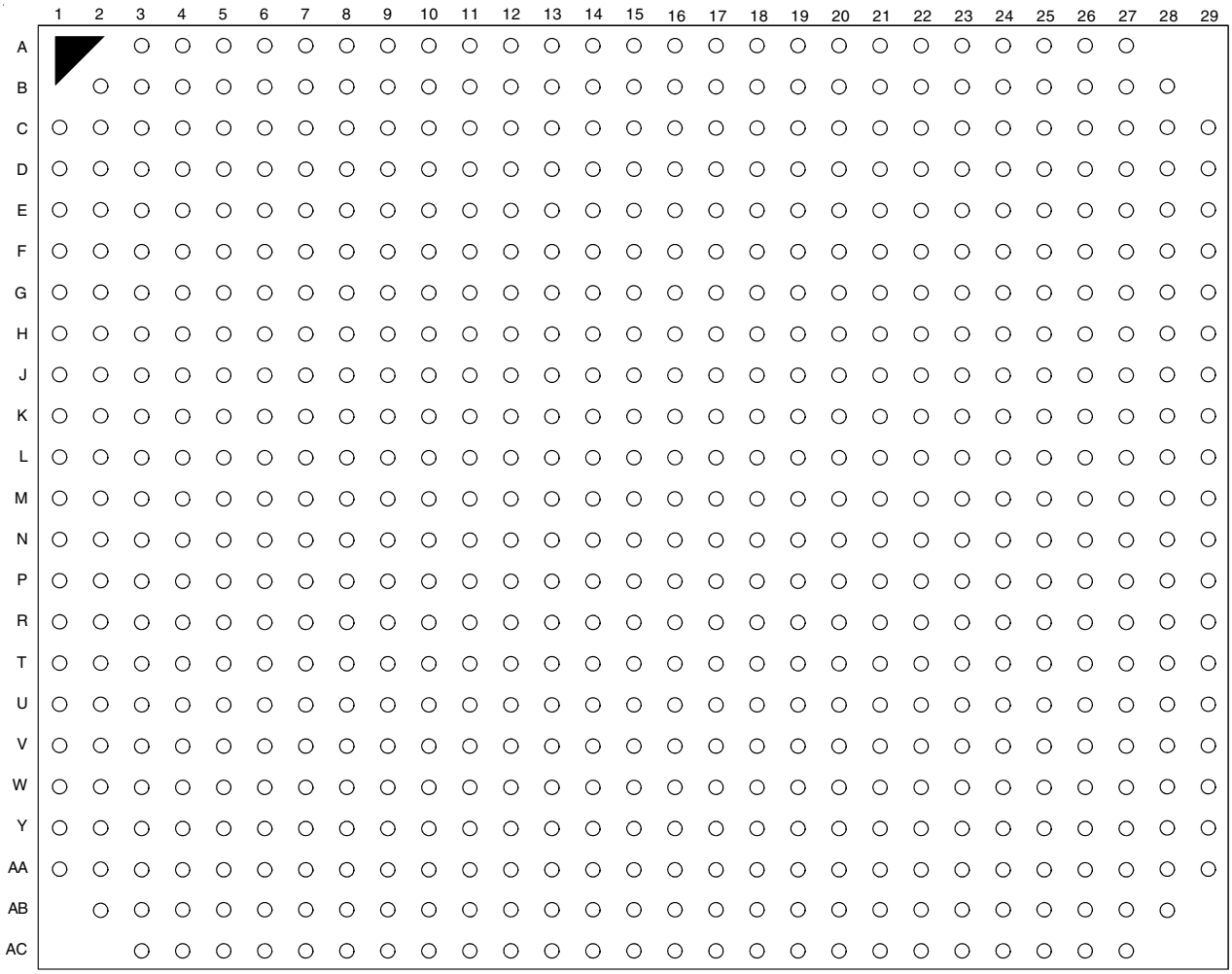
655 BALL BGA PACKAGE ATTRIBUTES



ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER

Ball No.	Signal
A3	VSS
A4	DQ26
A5	DQ12
A6	VDD
A7	DQS10
A8	DQ13
A9	VDD
A10	$\overline{DQS}$1
A11	DQ10
A12	VDD
A13	TESTLO
A14	VDD
A15	VDD
A16	VDD
A17	TEST
A18	VDD
A19	DQ52
A20	DQS15
A21	VDD
A22	DQ49
A23	$\overline{DQS}$6
A24	VDD
A25	DQ48
A26	DQ38
A27	VDD
B2	VDD
B3	DQS3
B4	$\overline{DQS}$3
B5	VSS
B6	DQ14
B7	$\overline{DQS}$10
B8	VSS
B9	DQ11
B10	DQS1
B11	VSS
B12	DDRC_B12
B13	TESTLO
B14	VDD
B15	VSS
B16	VDD
B17	TESTLO
B 18	DDRC_B18
B19	VSS
B20	$\overline{DQS}$15
B21	DQ53
B22	VSS
B23	DQS6
B24	DQ50
B25	VSS

Ball No.	Signal
B26	$\overline{DQS}$13
B27	DQS13
B28	VSS
C1	VSS
C2	DQS2
C3	DQ18
C4	VSS
C5	DQ4
C6	$\overline{DQS}$9
C7	VSS
C8	DQ15
C9	DQ9
C10	VSS
C11	DQ8
C12	DDRC_C12
C13	VSS
C14	DDRC_C14
C15	DQS17
C16	$\overline{DQS}$17
C17	VSS
C18	DDRC_C18
C19	DQ54
C20	VSS
C21	DQ55
C22	DQ51
C23	VSS
C24	DQS7
C25	DQ56
C26	VSS
C27	DQ46
C28	$\overline{DQS}$14
C29	VDD
D1	DQ19
D2	$\overline{DQS}$2
D3	VSS
D4	DQ16
D5	DQ24
D6	VSS
D7	DQS9
D8	DQ7
D9	VSS
D10	DQ3
D11	DQS0
D12	VSS
D13	$\overline{DQS}$8
D14	DQS8
D15	VDD
D16	CB6
D17	CB7

Ball No.	Signal
D18	VSS
D19	DQS16
D20	DQ63
D21	VSS
D22	DQ59
D23	$\overline{DQS}$7
D24	VSS
D25	DQ36
D26	DQ44
D27	VSS
D28	DQS14
D29	DQ47
E1	DQ21
E2	VSS
E3	DQ17
E4	DQ29
E5	VSS
E6	DQ25
E7	DQ6
E8	VSS
E9	DQ5
E10	DQ1
E11	VSS
E12	DQ0
E13	CB1
E14	VSS
E15	CB2
E16	VSS
E17	CB5
E18	$\overline{DQS}$16
E19	VSS
E20	DQ61
E21	DQ57
E22	VSS
E23	DQ58
E24	DQ39
E25	VSS
E26	DQ33
E27	DQ45
E28	VSS
E29	DQ41
F1	VSS
F2	DQ20
F3	DQ23
F4	VSS
F5	DQ31
F6	DQ27
F7	VSS
F8	TESTLO

Ball No.	Signal
F9	TEST
F10	VSS
F11	$\overline{DQS}$0
F12	DQ2
F13	VDD
F14	CB0
F15	CB3
F16	CB4
F17	VDD
F18	DQ62
F19	DQ60
F20	VSS
F21	TEST
F22	TEST
F23	VSS
F24	DQ37
F25	DQ35
F26	VSS
F27	$\overline{DQS}$5
F28	DQ43
F29	VSS
G1	$\overline{DQS}$11
G2	DQS11
G3	NC
G4	NC
G5	NC
G6	VSS
G7	DQS12
G8	$\overline{DQS}$12
G9	NC
G10	NC
G11	NC
G12	BFUNC
G13	RFU
G14	RFU
G15	RFU
G16	TESTLO
G17	RFU
G18	RFU
G19	NC
G20	NC
G21	NC
G22	DQS4
G23	$\overline{DQS}$4
G24	VSS
G25	NC
G26	NC
G27	NC
G28	DQS5

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER (CONT.)

Ball No.	Signal
G29	DQ40
H1	DQ22
H2	VSS
H3	NC
H4	NC
H5	NC
H6	DQ28
H7	DQ30
H8	VSS
H9	NC
H10	NC
H11	NC
H12	VSS
H13	VDD
H14	VSS
H15	VDD
H16	VSS
H17	VDD
H18	VSS
H19	NC
H20	NC
H21	NC
H22	VSS
H23	DQ34
H24	DQ32
H25	NC
H26	NC
H27	NC
H28	VSS
H29	DQ42
J1	VSS
J2	CLK2
J3	NC
J4	NC
J5	NC
J6	BA1A
J7	VSS
J8	CKE1A
J9	NC
J10	NC
J11	NC
J12	VDD
J13	VSS
J14	VDD
J15	VSS
J16	VDD
J17	VSS
J18	VDD
J19	NC

Ball No.	Signal
J20	NC
J21	NC
J22	$\overline{\text{RASB}}$
J23	VSS
J24	RFU
J25	NC
J26	NC
J27	NC
J28	$\overline{\text{CLK}}$3
J29	VSS
K1	$\overline{\text{CLK}}$2
K2	CLK0
K3	NC
K4	NC
K5	NC
K6	VSS
K7	$\overline{\text{WEA}}$
K8	$\overline{\text{RASA}}$
K9	NC
K10	NC
K11	NC
K12	VSS
K13	VCC
K14	VSS
K15	VCC
K16	VSS
K17	VCC
K18	VSS
K19	NC
K20	NC
K21	NC
K22	ODT0B
K23	$\overline{\text{CS}}$1B
K24	VSS
K25	NC
K26	NC
K27	NC
K28	$\overline{\text{CLK}}$1
K29	CLK3
L1	$\overline{\text{CLK}}$0
L2	VSS
L3	NC
L4	NC
L5	NC
L6	A0A
L7	CKE0A
L8	VSS
L9	NC
L10	NC

Ball No.	Signal
L11	NC
L12	VCC
L13	VSS
L14	VCC
L15	VSS
L16	VCC
L17	VSS
L18	VCC
L19	NC
L20	NC
L21	NC
L22	VSS
L23	$\overline{\text{CASB}}$
L24	$\overline{\text{WEB}}$
L25	NC
L26	NC
L27	NC
L28	VSS
L29	CLK1
M1	ODT0A
M2	RFU
M3	NC
M4	NC
M5	NC
M6	$\overline{\text{CASA}}$
M7	VSS
M8	BA2A
M9	NC
M10	NC
M11	NC
M12	VSS
M13	VCC
M14	VSS
M15	VCC
M16	VSS
M17	VCC
M18	VSS
M19	NC
M20	NC
M21	NC
M22	$\overline{\text{CS}}$0B
M23	VSS
M24	BA1B
M25	NC
M26	NC
M27	NC
M28	CKE0B
M29	VSS
N1	$\overline{\text{CS}}$1A

Ball No.	Signal
N2	$\overline{\text{CS}}$0A
N3	NC
N4	NC
N5	NC
N6	VSS
N7	BA0A
N8	A10A
N9	NC
N10	NC
N11	NC
N12	VCC
N13	VSS
N14	VCC
N15	VSS
N16	VCC
N17	VSS
N18	VCC
N19	NC
N20	NC
N21	NC
N22	A0B
N23	A2B
N24	VSS
N25	NC
N26	NC
N27	NC
N28	BA0B
N29	BA2B
P1	A6A
P2	VSS
P3	NC
P4	NC
P5	NC
P6	A2A
P7	A1A
P8	A3A
P9	NC
P10	NC
P11	NC
P12	VSS
P13	VCC
P14	VSS
P15	VCC
P16	VSS
P17	VCC
P18	VSS
P19	NC
P20	NC
P21	NC

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER (CONT.)

Ball No.	Signal
P22	Vss
P23	A4B
P24	A1B
P25	NC
P26	NC
P27	NC
P28	Vss
P29	CKE1B
R1	Vss
R2	A8A
R3	NC
R4	NC
R5	NC
R6	A11A
R7	Vss
R8	A5A
R9	NC
R10	NC
R11	NC
R12	Vcc
R13	Vss
R14	Vcc
R15	Vss
R16	Vcc
R17	Vss
R18	Vcc
R19	NC
R20	NC
R21	NC
R22	A6B
R23	Vss
R24	A10B
R25	NC
R26	NC
R27	NC
R28	A3B
R29	Vss
T1	A4A
T2	A13A
T3	NC
T4	NC
T5	NC
T6	Vss
T7	A9A
T8	A7A
T9	NC
T10	NC
T11	NC

Ball No.	Signal
T12	Vss
T13	Vcc
T14	Vss
T15	Vcc
T16	Vss
T17	Vcc
T18	Vss
T19	NC
T20	NC
T21	NC
T22	A11B
T23	A9B
T24	Vss
T25	NC
T26	NC
T27	NC
T28	A7B
T29	A5B
U1	PN0
U2	$\overline{\text{PN0}}$
U3	NC
U4	NC
U5	NC
U6	A15A
U7	A14A
U8	A12A
U9	NC
U10	NC
U11	NC
U12	RFU
U13	VccFBD
U14	Vss
U15	Vss
U16	Vss
U17	VccFBD
U18	RFU
U19	NC
U20	NC
U21	NC
U22	A8B
U23	A15B
U24	A14B
U25	SA0
U26	SCL
U27	SDA
U28	PS8
U29	PS8
V1	PN1

Ball No.	Signal
V2	$\overline{\text{PN1}}$
V3	Vss
V4	SN0
V5	$\overline{\text{SN0}}$
V6	VccFBD
V7	Vss
V8	VccFBD
V9	Vss
V10	RFU(1)
V11	RFU(1)
V12	VccFBD
V13	Vss
V14	Vss
V15	Vss
V16	VccFBD
V17	Vss
V18	VccFBD
V19	Vss
V20	VccFBD
V21	RFU(1)
V22	RFU(1)
V23	Vss
V24	A13B
V25	A12B
V26	SA2
V27	SA1
V28	$\overline{\text{PS7}}$
V29	PS7
W1	PN2
W2	$\overline{\text{PS2}}$
W3	Vss
W4	SN1
W5	$\overline{\text{SN1}}$
W6	$\overline{\text{SN3}}$
W7	$\overline{\text{SN4}}$
W8	$\overline{\text{SN5}}$
W9	$\overline{\text{SN13}}$
W10	$\overline{\text{SN12}}$
W11	$\overline{\text{SN6}}$
W12	$\overline{\text{SN7}}$
W13	$\overline{\text{SN8}}$
W14	$\overline{\text{SN9}}$
W15	$\overline{\text{SN10}}$
W16	Vss
W17	$\overline{\text{SS0}}$
W18	$\overline{\text{SS1}}$
W19	$\overline{\text{SS2}}$
W20	$\overline{\text{SS3}}$

Ball No.	Signal
W21	$\overline{\text{SS4}}$
W22	$\overline{\text{SS9}}$
W23	$\overline{\text{SS5}}$
W24	$\overline{\text{SS6}}$
W25	$\overline{\text{SS7}}$
W26	$\overline{\text{SS8}}$
W27	Vss
W28	$\overline{\text{PS6}}$
W29	PS6
Y1	PN3
Y2	$\overline{\text{PN3}}$
Y3	Vss
Y4	SN2
Y5	$\overline{\text{SN2}}$
Y6	SN3
Y7	SN4
Y8	SN5
Y9	SN13
Y10	SN12
Y11	SN6
Y12	SN7
Y13	SN8
Y14	SN9
Y15	SN10
Y16	Vss
Y17	SS0
Y18	SS1
Y19	SS2
Y20	SS3
Y21	SS4
Y22	SS9
Y23	SS5
Y24	SS6
Y25	SS7
Y26	SS8
Y27	Vss
Y28	$\overline{\text{PS5}}$
Y29	PS5
AA1	Vss
AA2	PN4
AA3	$\overline{\text{PN4}}$
AA4	Vss
AA5	Vss
AA6	Vss
AA7	Vss
AA8	Vss
AA9	Vss
AA10	Vss

NOTE:
1. These pin positions are reserved for forward clocks to be used in future implementations.

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER (CONT.)

Ball No.	Signal
AA11	V_{SS}
AA12	V_{SS}
AA13	V_{SS}
AA14	V_{SS}
AA15	V_{SS}
AA16	V_{SS}
AA17	V_{SS}
AA18	V_{SS}
AA19	V_{SS}
AA20	V_{SS}
AA21	V_{SS}
AA22	V_{SS}
AA23	V_{SS}
AA24	V_{SS}
AA25	V_{SS}
AA26	V_{SS}
AA27	$\overline{PS}9$
AA28	PS9
AA29	V_{SS}
AB2	V_{SS}
AB3	$\overline{RESET}$
AB4	$\overline{PN}5$
AB5	$\overline{PN}13$
AB6	RFU(1)
AB7	$\overline{PN}12$
AB8	$\overline{PN}6$
AB9	$\overline{PN}7$
AB10	$\overline{PN}8$
AB11	$\overline{PN}9$
AB12	V_{SSA}PLL
AB13	V_{CCA}PLL
AB14	$\overline{PN}10$
AB15	$\overline{PN}11$
AB16	V_{SS}
AB17	$\overline{PN}11$
AB18	V_{SS}
AB19	SCK
AB20	TESTLO_AB20
AB21	$\overline{PS}0$
AB22	$\overline{PS}1$
AB23	$\overline{PS}2$
AB24	$\overline{PS}3$
AB25	$\overline{PS}4$
AB26	RFU(1)
AB27	V_{DD}SPD
AB28	V_{SS}
AC3	V_{SS}
AC4	PN5

Ball No.	Signal
AC5	PN13
AC6	RFU(1)
AC7	PN12
AC8	PN6
AC9	PN7
AC10	PN8
AC11	PN9
AC12	FBDRES
AC13	PLLTSTO
AC14	PN10
AC15	PN11
AC16	RFU
AC17	SN11
AC18	V_{SS}
AC19	$\overline{SCK}$
AC20	TESTLO_AC20
AC21	PS0
AC22	PS1
AC23	PS2
AC24	PS3
AC25	PS4
AC26	RFU(1)
AC27	V_{SS}

NOTE:
1. These pin positions are reserved for forward clocks to be used in future implementations.

PIN DESCRIPTION

Signal	Type	Description
Channel Interface		
PN[13:0]	O	Northbound Output Data: High speed serial signal. Read path from AMB toward host on primary side of the DIMM connector.
$\overline{\text{PN}}$[13:0]	O	Northbound Output Data Complement
SN[13:0]	I	Northbound Input Data: High speed serial signal. Read path from the previous AMB toward this AMB on secondary side of the DIMM connector.
$\overline{\text{SN}}$[13:0]	I	Northbound Input Data Complement
PS[9:0]	I	Southbound Input Data: High speed serial signal. Write path from host toward AMB on primary side of the DIMM connector.
$\overline{\text{PS}}$[9:0]	I	Southbound Input Data Complement
SS[9:0]	O	Southbound Output Data: High speed serial signal. Write path from this AMB toward next AMB on secondary side of the DIMM connector. These output buffers are disabled for the last AMB on the channel.
$\overline{\text{SS}}$[9:0]	O	Southbound Output Data Complement
FBDRES	A	External 100Ω precision resistor connected to V_{CC}. On-die termination calibrated against this resistor.
DRAM Interface		
CB[7:0]	I/O	Check bits
DQ[63:0]	I/O	Data
DQS[17:0]	I/O	Data Strobe: DDR2 data and check-bit strobe.
$\overline{\text{DQS}}$[17:0]	I/O	Data Strobe Complement: DDR2 data and check-bit strobe complements.
A0A-A15A, A0B-A15B	O	Address: Used for providing multiplexed row and column address to SDRAM.
BA0A-BA2A, BA0B-BA2B	O	Bank Active: Used to select the bank within a rank.
$\overline{\text{RASA}}$, $\overline{\text{RASB}}$	O	Row Address Strobe: Used with $\overline{\text{CS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ to specify the SDRAM command.
$\overline{\text{CASA}}$, $\overline{\text{CASB}}$	O	Column Address Strobe: Used with $\overline{\text{CS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ to specify the SDRAM command.
$\overline{\text{WEA}}$, $\overline{\text{WEB}}$	O	Write Enable: Used with $\overline{\text{CS}}$, $\overline{\text{CAS}}$, and $\overline{\text{RAS}}$ to specify the SDRAM command.
$\overline{\text{CS}}$0A-$\overline{\text{CS}}$1A, $\overline{\text{CS}}$0B-$\overline{\text{CS}}$1B	O	Chip Select: Used with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ to specify the SDRAM command. These signals are used for selecting one of two SDRAM ranks. $\overline{\text{CS0}}$ is used to select the first rank and $\overline{\text{CS1}}$ is used to select the second rank.
CKE0A-CKE1A, CKE0B-CKE1B	O	Clock Enable: DIMM command register enable.
ODT0A, ODT0B	O	DIMM On-Die-Termination: Dynamic ODT enables for each DIMM on the channel.
CLK[3:0]	O	Clock: Clocks to DRAMs. CLK0 and CLK1 are always used. CLK2 and CLK3 are used when the AMB is configured for dual rank DIMMs.
$\overline{\text{CLK}}$[3:0]	O	Clock Complement: Clocks to DRAMs.
DDR Compensation		
DDRC_C14	A	DDR Compensation Common: Common return (ground) pin for DDRC_B18 and DDRC_C18
DDRC_B18	A	DDR Compensation Ball Resistor (825Ω) connected to Compensation Common above
DDRC_C18	A	DDR Compensation Ball Resistor (121Ω) connected to Compensation Common above
DDRC_B12	A	DDR Compensation Ball Resistor (82Ω) connected to V_{SS}
DDRC_C12	A	DDR Compensation Ball Resistor (82Ω) connected to V_{DD}

PIN DESCRIPTION (CONT.)

Signal	Type	Description
Clocking		
SCK	I	AMB Clock: This is one of the two differential reference clock inputs to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
$\overline{SCK}$	I	AMB Clock Complement: This is the other differential reference clock input to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
PLLTSTO	O	PLL Clock Observability Output: This pin can be used to observe VCO, reference clock, core clock, etc. For system debug and design characterization.
V_{CC}A PLL	A	V_{CC}: PLL Analog Voltage for the core PLL
V_{SS}A PLL	A	V_{SS}: PLL Analog Voltage for the core PLL
System Management		
SCL	I/O	SMBus Clock
SDA	I/O	SMBus Address/Data
SA[2:0]		DIMM Select ID
Reset		
$\overline{RESET}$		Power Good Reset
Miscellaneous Test		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to V_{CC}FBD, the other resistor is connected to V_{SS}.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to V_{CC}FBD, the other resistor is connected to V_{SS}.
Power Supplies		
V_{CC} (24 pins)	A	1.5V nominal supply for core I/O
V_{CC}FBD (8 pins)	A	1.5V nominal supply for FBD high speed I/O
V_{DD} (24 pins)	A	1.8V nominal supply for DDR I/O
V_{SS} (156 pins)	A	Ground
V_{DD}SPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	Buffer Function Bit: When BFUNC = 0, AMB is used as a regular buffer on FBDIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	Reserved for Future Use. Must be floated on DIMM. RFU pins denoted by “a” are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	NC	No Connect pins

ELECTRICAL, POWER, AND THERMAL

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
V_{DD}	Supply voltage DRAM Interface	-0.5	+2.3	V
V_{IN} (DDR2). V_{OUT} (DDR2)	Voltage on any DDR2 interface pin relative to Vss(2)	0.5	+2.3	V
I_{INK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{DD})		+30	mA
I_{OUTK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{DD})		+30	mA
I_{OUT}	Continous Output Current (V_{OUT} = 0 to V_{DD})		+30	mA
N/A	Continuous current through each V_{DD} or GND		+100	mA
V_{CC}	Supply voltage for Core and High Speed Interface	-0.3	+1.75	V
T_J	Junction Temperature		+125	° C
T_{STG}	Storage Temperature Range	–55	+100	° C

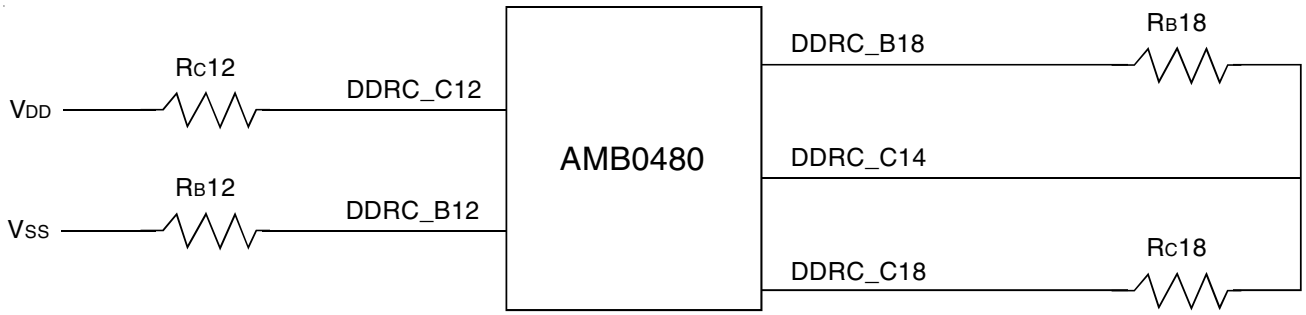
NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 2.3V maximum.

ADVANCED MEMORY BUFFER NORMAL MODE DC ELECTRICAL PARAMETERS

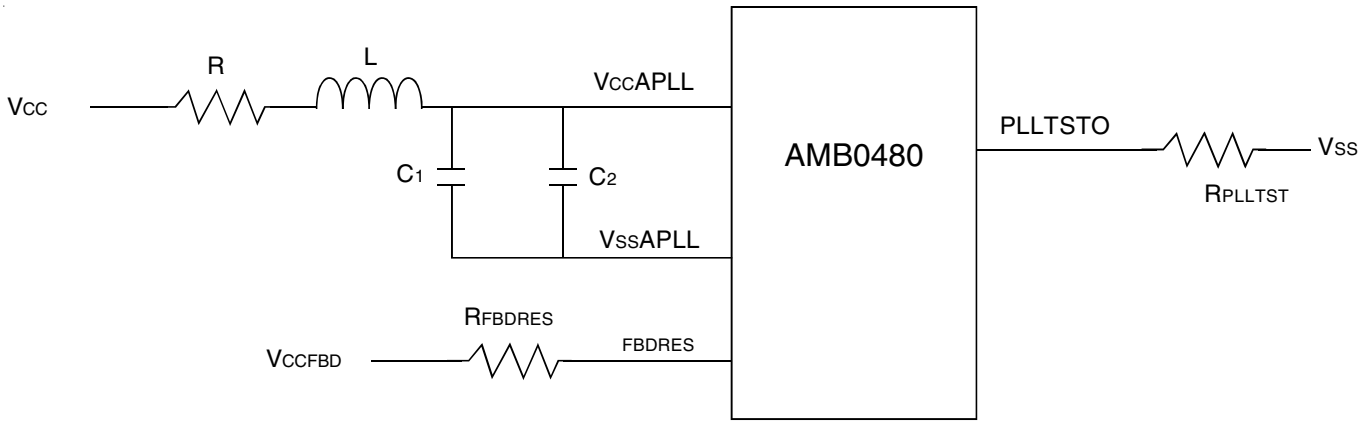
Parameter	Min	Typ	Max	Unit
V_{CC} link / core(1,2,3,4)	1.425	1.5	1.59	V
V_{DD}	1.7	1.8	1.9	V
V_{DDSPD}	3.0	3.3	3.6	V

NOTES:
1. AMB 1.5V voltage regulation as measured at the package Balls.
2. DC defined as 0 KHz to 30 KHz.
3. DC + AC specified as 1.5V +6%, -5% 30KHz to 1 MHz.
4. There is also a +7%, -5% tolerance allowed for current load steps associated with initialization/error-recovery state transitions, such as into and out of EI, IBIST, and MEMBIST. For these transitions, a temporary voltage overshoot is expected and acceptable as long as it is within +7% (step transition for 20µs and maximum duty cycle of 10^{-6} %). Transitions between Active and Idle states are not included in this +7%, -5% tolerance.

DDR BIAS



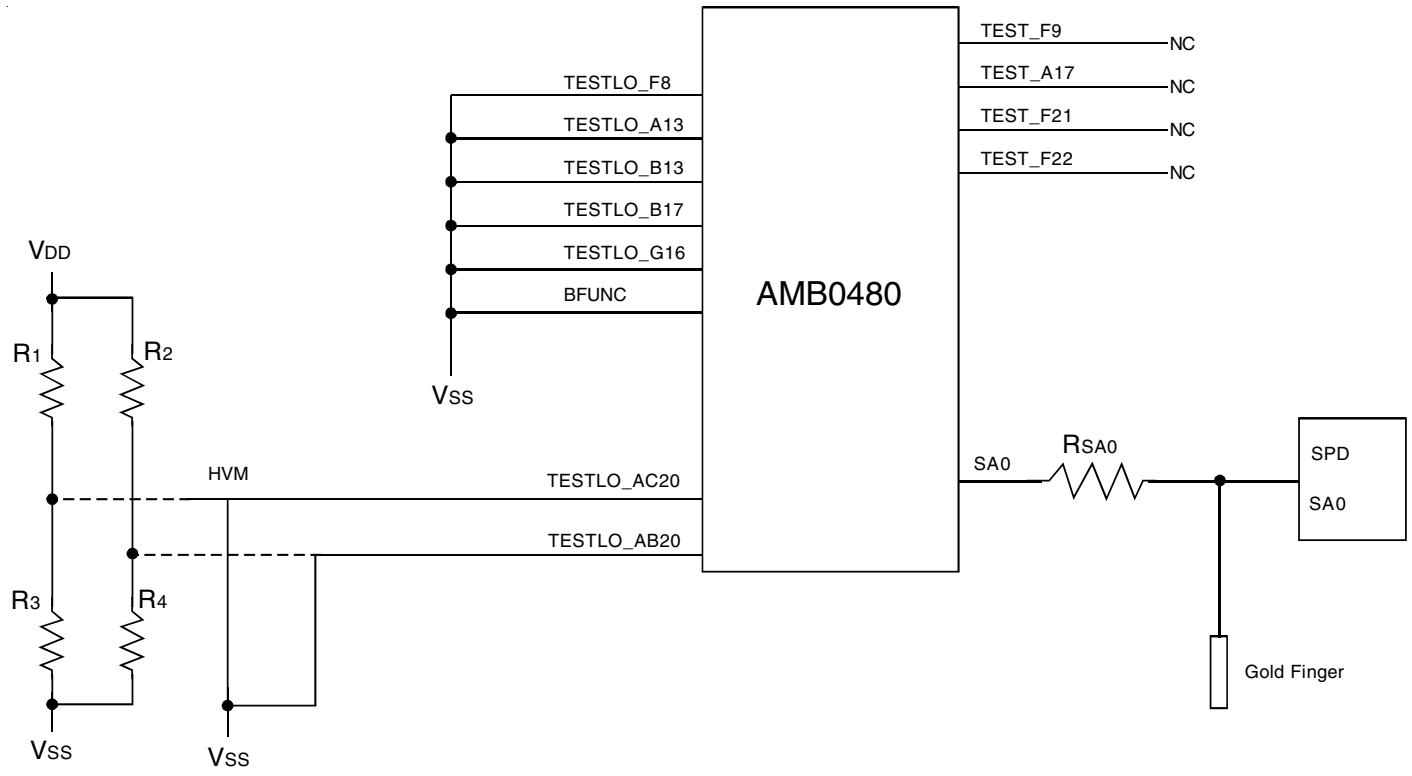
PLL AND CHANNEL BIAS



NOTES:

1. Refer to JEDEC PC2-4200/5300/6400 DDR2 FULLY BUFFERED DIMM DESIGN SPECIFICATIONS, rev 2.0.
2. The resistor R must be 0Ω and the inductor L needs to be replaced with a 0Ω resistor. The resistor R_{FBDRES} = 100Ω and Resistor R_{PLLTST} = 51Ω.
3. It is not recommended to use a serpentine copper trace in place of the resistor R. This resistor value needs to be AMB manufacturer defined and not set to a single fixed value. Some raw cards have implemented the resistor with a serpentine copper trace on the DIMM PCB, while others use a discrete resistor. The limitation of using the copper trace has been discussed in JEDEC, highlighting that the resistor implemented as a serpentine copper trace is not a generic solution. The raw card artwork now allows the option of bypassing any serpentine trace with a 0Ω resistor to V_{CC}.

MISCELLANEOUS BIAS

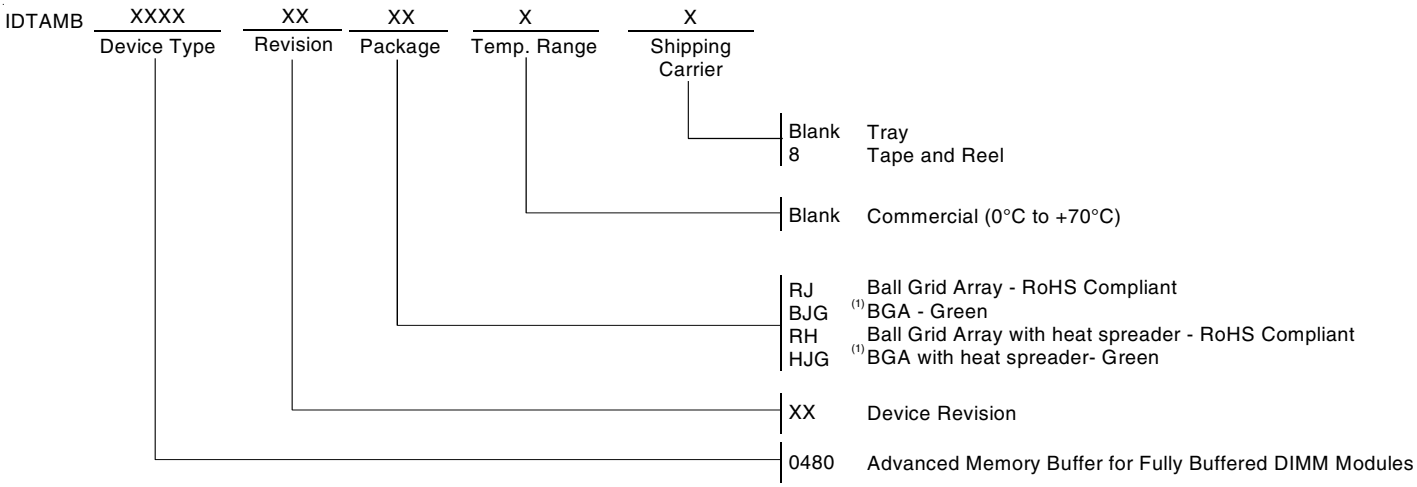


NOTES:
1. Refer to JEDEC PC2-4200/5300/6400 DDR2 FULLY BUFFERED DIMM DESIGN SPECIFICATIONS, rev 2.0.
2. Component values for the AMB0480 are summarized in the BIAS COMPONENT table.

BIAS COMPONENTS - RECOMMENDED VALUES AMB0480

Schematic Diagram	Reference	Value	Description
DDR Bias	RC_{12}	82Ω	The impedance of the pull up (PRU) and pull down (PRD) on the AMB DDR Outputs is relatedto RB_{12} & RC_{12} as follows: $RC_{12} = RB_{12} = 5.3125 * \text{Desired Output Impedance}$ A resistor value of 82Ω results in an impedance at a JEDEC nominal value of 15Ω. The user can adjust these value to optimize the DDR output impedance for a DIMM raw card configuration.
	RB_{12}	82Ω	
	RB_{18}	825Ω	
	RC_{18}	121Ω	
PLL and Channel	R	0Ω	Resistor R must be 0Ω
	L	0Ω	Inductor L needs to be replaced with a 0Ω resistor
	C_1	10µF	
	C_2	10µF	
	RPLLTSTO	51Ω	
	R_{FBDRES}	100Ω	
Miscellaneous	R_1	Not loaded	
	R_2	Not loaded	
	R_3	0Ω	
	R_4	0Ω	
	RSA0	825Ω	

ORDERING INFORMATION



NOTE:
1. Contact factory for availability.

Device Revision		**Status**
A5	AMB revision A1.5	Active

Other Ordering Information

AMB0480xxRJ8	AMB in bare die packaged in tape/reel
AMB0480xxRJ	AMB in bare die packaged in tray
AMB0480xxRH8	AMB with heatspreader packaged in tape/reel
AMB0480xxRH	AMB with heatspreader packaged in tray

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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