

**FEATURES:**

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Pin compatible with the 74F245, 74FCT245, and 74FCT245T
- Low power CMOS proprietary technology
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- 25Ω resistors for low noise
- TTL-compatible control inputs
- Available in QSOP and TSSOP packages

**APPLICATIONS:**

- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Power conservation
- Capacitance reduction and isolation
- Logic replacement (data processing)
- Clock gating
- Bus switching and isolation

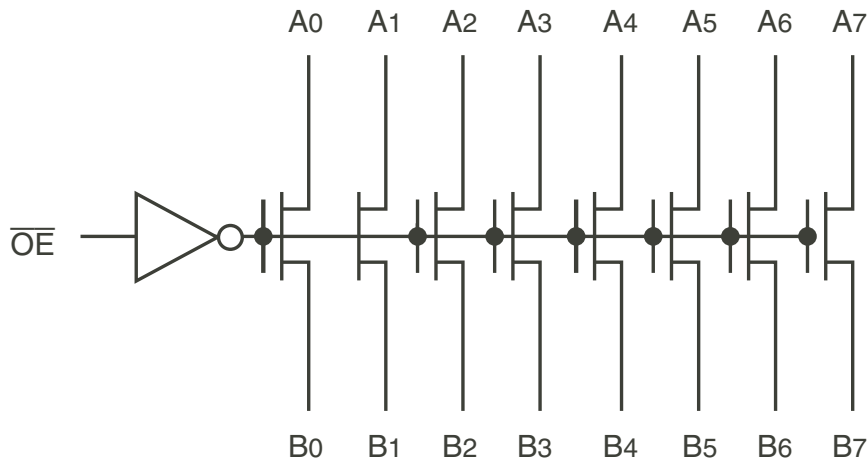
**DESCRIPTION:**

The QS32245 provides a set of eight high-speed CMOS TTL-compatible bus switches in a pinout compatible with 74FCT245, 74F245, 74ALS/AS/LS245 8-bit transceivers. The Output Enable ( $\overline{OE}$ ) signal turns the switches on similar to the  $\overline{OE}$  signal of the 74'245. The QS32245 has 25Ω series resistors to reduce ground bounce noise.

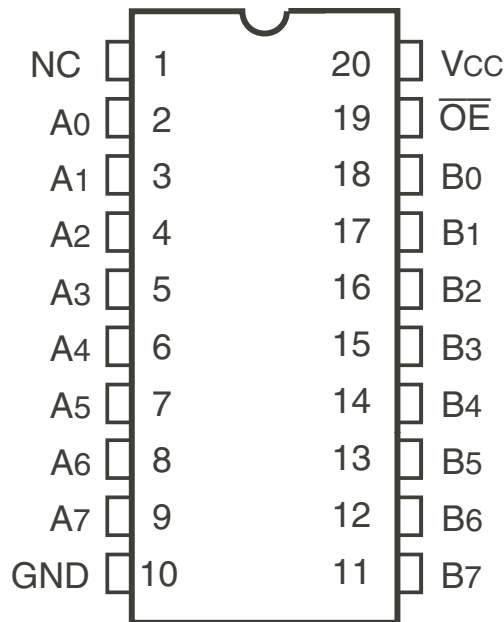
QuickSwitch devices provide an order of magnitude faster speed than conventional logic devices.

The QS32245 is characterized for operation at -40°C to +85°C.

**FUNCTIONAL BLOCK DIAGRAM**



PIN CONFIGURATION



TOP VIEW

| Package Type | Package Code | Order Code |
|--------------|--------------|------------|
| TSSOP        | PGG20        | PAG        |
| QSOP         | PCG20        | QG         |

ABSOLUTE MAXIMUM RATINGS(1)

| Symbol               | Description                           | Max         | Unit |
|----------------------|---------------------------------------|-------------|------|
| VTERM <sup>(2)</sup> | Supply Voltage to Ground              | -0.5 to +7  | V    |
| VTERM <sup>(3)</sup> | DC Switch Voltage Vs                  | -0.5 to +7  | V    |
| VTERM <sup>(3)</sup> | DC Input Voltage VIN                  | -0.5 to +7  | V    |
| VAC                  | AC Input Voltage (pulse width ≤ 20ns) | -3          | V    |
| IOUT                 | DC Output Current                     | 120         | mA   |
| P <sub>MAX</sub>     | Maximum Power Dissipation (TA = 85°C) | 0.5         | W    |
| TSTG                 | Storage Temperature                   | -65 to +150 | °C   |

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, VIN = 0V, VOUT = 0V)

| Pins                              | Typ. | Max. <sup>(1)</sup> | Unit |
|-----------------------------------|------|---------------------|------|
| Control Pins                      | 3    | 5                   | pF   |
| Quickswitch Channels (Switch OFF) | 5    | 7                   | pF   |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names       | Description   |
|-----------------|---------------|
| $\overline{OE}$ | Output Enable |
| An              | Data I/Os     |
| Bn              | Data I/Os     |

FUNCTION TABLE(1)

| $\overline{OE}$ | Outputs      |
|-----------------|--------------|
| H               | Disconnected |
| L               | An = Bn      |

NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

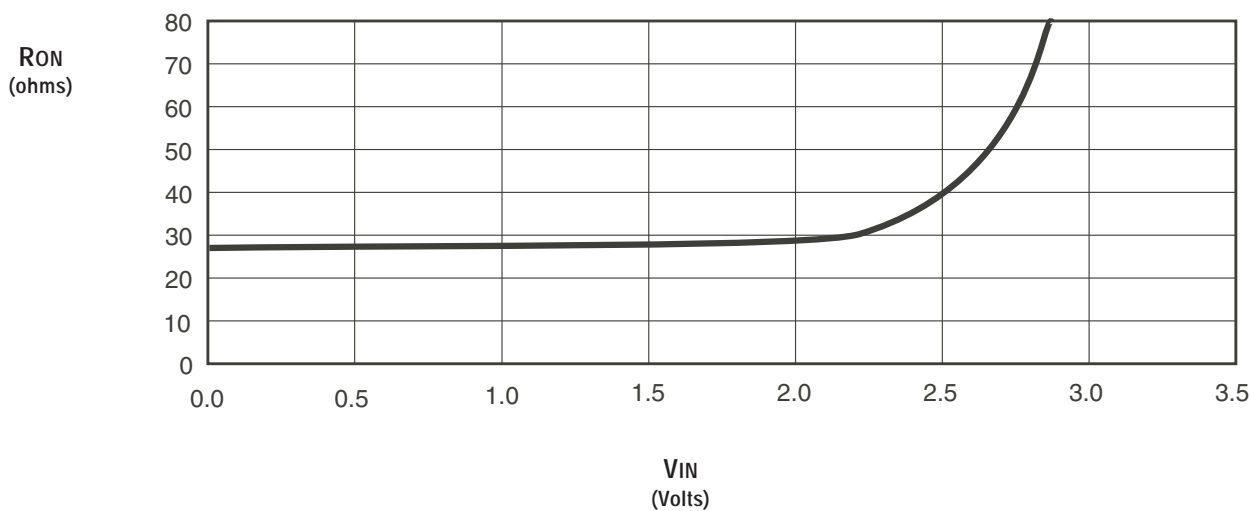
Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

| Symbol         | Parameter   | Test Conditions  | Min. | Typ. <sup>(1)</sup> | Max.    | Unit          |
|----------------|---|--|------|---------------------|---------|---------------|
| $V_{IH}$       | Input HIGH Level                                      | Guaranteed Logic HIGH for Control Pins                             | 2    | —                   | —       | V             |
| $V_{IL}$       | Input LOW Level                                       | Guaranteed Logic LOW for Control Pins                              | —    | —                   | 0.8     | V             |
| $I_{IN}$       | Input Leakage Current (Control Inputs) <sup>(2)</sup> | $0\text{V} \leq V_{IN} \leq V_{CC}$                                | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZ}$       | Off-State Output Current (Hi-Z)                       | $0\text{V} \leq V_{OUT} \leq V_{CC}$ , Switches OFF                | —    | $\pm 0.001$         | $\pm 1$ | $\mu\text{A}$ |
| $R_{ON}^{(3)}$ | Switch ON Resistance                                  | $V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$   | 18   | 23                  | 35      | $\Omega$      |
|                |   | $V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$ | 18   | 25                  | 40      |               |
| $V_P$          | Pass Voltage <sup>(2)</sup>                           | $V_{IN} = V_{CC} = 5\text{V}, I_{OUT} = -5\mu\text{A}$             | 3.7  | 4                   | 4.2     | V             |

**NOTES:**

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .
2. Pass Voltage is guaranteed but not production tested.
3.  $R_{OUT}$  changed on March 8, 2002. See rear page for more information.

### TYPICAL ON RESISTANCE VS $V_{IN}$ AT $V_{CC} = 5\text{V}$



## POWER SUPPLY CHARACTERISTICS

| Symbol           | Parameter  | Test Conditions <sup>(1)</sup>   | Max. | Unit   |
|------------------|--|--|------|--------|
| I <sub>CCQ</sub> | Quiescent Power Supply Current                             | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0               | 3    | μA     |
| ΔI <sub>CC</sub> | Power Supply Current per Control Input HIGH <sup>(2)</sup> | V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f = 0                                  | 1.5  | mA     |
| I <sub>CCD</sub> | Dynamic Power Supply Current per MHz <sup>(3)</sup>        | V <sub>CC</sub> = Max., A and B pins open<br>Control Inputs Toggling at 50% Duty Cycle | 0.25 | mA/MHz |

**NOTES:**

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TLL driven input (V<sub>IN</sub> = 3.4V, control inputs only). A and B pins do not contribute to ΔI<sub>CC</sub>.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 5%;

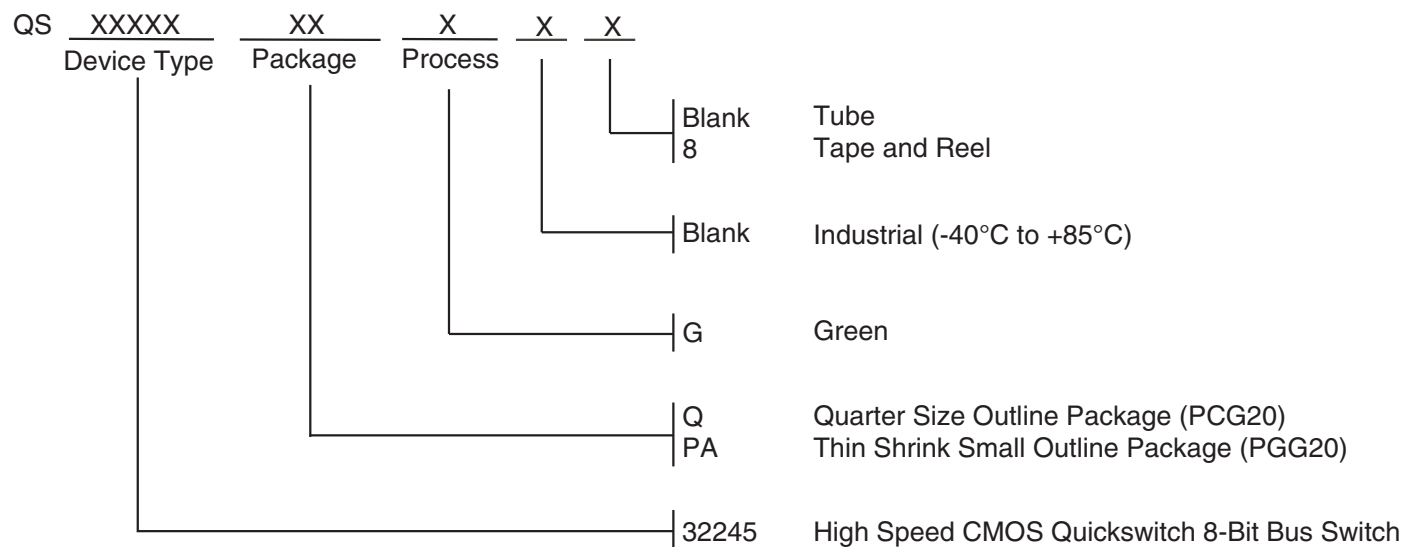
C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

| Symbol           | Parameter                               | Min. <sup>(1)</sup> | Typ. | Max. | Unit |
|------------------|---|---------------------|------|------|------|
| t <sub>PLH</sub> | Data Propagation Delay <sup>(2,3)</sup> | —                   | —    | 1.25 | ns   |
| t <sub>PHL</sub> | An to/from Bn                           | —                   | —    | —    | —    |
| t <sub>PZL</sub> | Switch Turn-on Delay                    | 0.5                 | —    | 6.6  | ns   |
| t <sub>PZH</sub> | $\overline{OE}$ to An/Bn                | —                   | —    | —    | —    |
| t <sub>PLZ</sub> | Switch Turn-off Delay <sup>(2)</sup>    | 0.5                 | —    | 4.5  | ns   |
| t <sub>PHZ</sub> | $\overline{OE}$ to An/Bn                | —                   | —    | —    | —    |

**NOTES:**

- Minimums are guaranteed but not production tested.
- This parameter is guaranteed but not production tested.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 1.25ns for C<sub>L</sub> = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION



## Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
|            | QS32245PAG        | PGG20     | TSSOP     | I           |
|            | QS32245PAG8       | PGG20     | TSSOP     | I           |
|            | QS32245QG         | PCG20     | QSOP      | I           |
|            | QS32245QG8        | PCG20     | QSOP      | I           |

## Datasheet Document History

|            |        |   |
|------------|--------|---|
| 02/09/2011 | Pg. 5  | Updated the ordering information by removing the "IDT" notation, non RoHS part and by adding Tape and Reel information.   |
| 06/03/2019 | Pg.2,5 | Added table under pin configuration diagram with detailed package information and orderable part information table. Updated the ordering information diagram in clearer detail. |

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(Rev.1.0 Mar 2020)

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