8-Channel, High Throughput, 24-Bit Σ-Δ ADC

AD7738

FEATURES

High Resolution ADC
- 24 Bits No Missing Codes
- ±0.0015% Nonlinearity

Optimized for Fast Channel Switching
- 18-Bits p-p Resolution (21 Bits Effective) at 500 Hz
- 16-Bits p-p Resolution (19 Bits Effective) at 8.5 kHz
- 15-Bits p-p Resolution (18 Bits Effective) at 15 kHz
- On-Chip Per Channel System Calibration

Configurable Inputs
- 8 Single-Ended or 4 Fully Differential

Input Ranges
- +625 mV, +1.25 V, +2.5 V, ±625 mV, ±1.25 V, ±2.5 V

3-Wire Serial Interface
- SPI™, QSPI™, MICROWIRE™ and DSP Compatible
- Schmitt Trigger on Logic Inputs

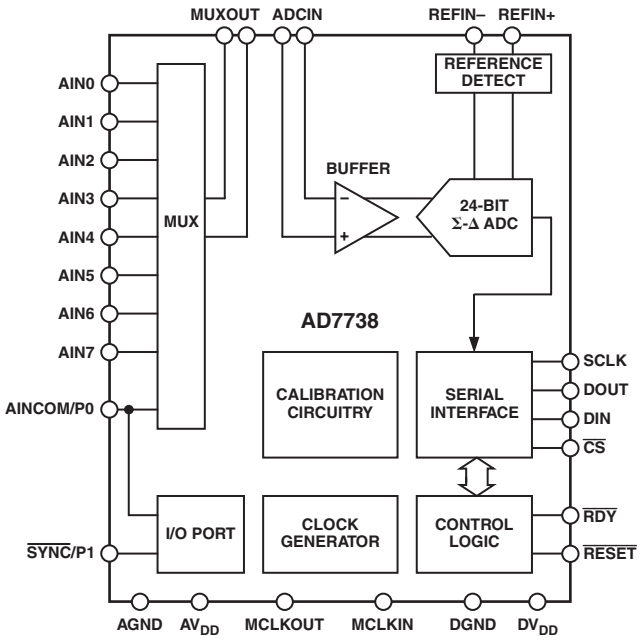
Single-Supply Operation
- 5 V Analog Supply
- 3 V or 5 V Digital Supply

Package: 28-Lead TSSOP

APPLICATIONS

PLCs/DCS
Multiplexing Applications
Process Control
Industrial Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7738 is a high precision, high throughput analog front end. True 16-bit p-p resolution is achievable with a total conversion time of 117 µs (8.5 kHz channel switching), making it ideally suitable for high resolution multiplexing applications.

The part can be configured via a simple digital interface, which allows users to balance the noise performance against data throughput up to a 15.4 kHz.

The analog front end features eight single-ended or four fully differential input channels with unipolar or bipolar 625 mV, 1.25 V, and 2.5 V input ranges and accepts a common-mode input voltage from 200 mV above AGND to AV_{DD} – 300 mV. The multiplexer output is pinned out externally, allowing the user to implement programmable gain or signal conditioning before applying the input to the ADC.

The differential reference input features "No-Reference" detect capability. The ADC also supports per channel system calibration options.

The digital serial interface can be configured for 3-wire operation and is compatible with microcontrollers and digital signal processors. All interface inputs are Schmitt triggered.

The part is specified for operation over the extended industrial temperature range of –40°C to +105°C.

Other parts in the AD7738 family are the AD7734 and the AD7732.

The AD7734 analog front end features four single-ended input channels with unipolar or true bipolar input ranges to ±10 V while operating from a single 5 V analog supply. The AD7734 accepts an analog input overvoltage to ±16.5 V while not degrading the performance of the adjacent channels.

The AD7732 is similar to AD7734, but its analog front end features two fully differential input channels.

REV. 0

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AD7738–SPECIFICATIONS (–40°C to +105°C, AV_{DD} = 5 V ± 5%, DV_{DD} = 2.7 V to 3.6 V or 5 V ± 5%, REFIN(+) = 2.5 V, REFIN(–) = 0 V, AINCOM = 2.5 V, MUXOUT(+) = ADCIN(+), MUXOUT(–) = ADCIN(–), Internal Buffer ON, AIN Range = ±1.25 V, f_{MCLK} = 6.144 MHz; unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
ADC PERFORMANCE— CHOPPING ENABLED					
Conversion Time Rate	372		12190	Hz	Configure via Conversion Time Register
No Missing Codes[1]	24			Bits	FW ≥ 6 (Conversion Time ≥ 165 µs) See Typical Performance Characteristics
Output Noise		See Table I			
Resolution		See Tables II and III			
Integral Nonlinearity (INL)			±0.0015	% of FSR	AIN Range = ±2.5 V
		±0.0015		% of FSR	AIN Range = ±1.25 V
Offset Error (Unipolar, Bipolar)[2]		±10		µV	Before Calibration
Offset Drift vs. Temperature[1]			±280	nV/°C	
Gain Error[2]			±0.2	%	Before Calibration
Gain Drift vs. Temperature[1]			±2.5	ppm of FS/°C	
Positive Full-Scale Error[2]			±0.2	% of FSR	Before Calibration
Positive Full-Scale Drift vs. Temperature[1]			±2.5	ppm of FS/°C	
Bipolar Negative Full-Scale Error[3]		±0.0030		% of FSR	After Calibration[3]
Common-Mode Rejection	80	100		dB	At DC, AIN = 1 V
Power Supply Rejection	70	80		dB	At DC, AIN = 1 V
ADC PERFORMANCE— CHOPPING DISABLED					
Conversion Time Rate	737		15437	Hz	Configure via Conversion Time Register
No Missing Codes[1]	24			Bits	FW ≥ 8 (Conversion Time ≥ 117 µs) See Typical Perfomance Charateristics
Output Noise		See Table IV			
Resolution		See Tables V and VI			
Integral Nonlinearity (INL)		±0.0015		% of FSR	
Offset Error (Unipolar, Bipolar)[4]		±1		mV	Before Calibration
Offset Drift vs. Temperature		±1.5		µV/°C	
Gain Error[2]		±0.2		%	Before Calibration
Gain Drift vs. Temperature		±2.5		ppm of FS/°C	
Positive Full-Scale Error[2]		±0.2		% of FSR	Before Calibration
Positive Full-Scale Drift vs. Temperature		±2.5		ppm of FS/°C	
Bipolar Negative Full-Scale Error[3]		±0.0030		% of FSR	After Calibration[3]
Common-Mode Rejection		75		dB	At DC, AIN = 1 V
Power Supply Rejection		65		dB	At DC, AIN = 1 V
ANALOG INPUTS					
Analog Input Voltage Ranges[1, 5]					
±2.5 V Range	–2.9	±2.5	+2.9	V	
+2.5 V Range	0	0 to 2.5	2.9	V	
±1.25 V Range	–1.45	±1.25	+1.45	V	
+1.25 V Range	0	0 to 1.25	1.45	V	
±0.625 V Range	–725	±625	+725	mV	
+0.625 V Range	0	0 to 625	725	mV	
AIN, AINCOM Common-Mode Voltage[1]	0.2		AV_{DD} – 0.3	V	
AIN, AINCOM Input Current[6]			200	nA	Only One Channel, Chop Disabled
AIN to MUXOUT On Resistance[1]		200		Ω	
REFERENCE INPUT					
REFIN(+) to REFIN(–) Voltage[1, 7]	2.475	2.5	2.525	V	
NOREF Trigger Voltage		0.5		V	NOREF Bit in Channel Status Register
REFIN(+), REFIN(–) Common-Mode Voltage[1]	0		AV_{DD}	V	
Reference Input Current[8]			400	µA	
SYSTEM CALIBRATION[1, 9]					
Full Scale Calibration Limit			+1.05 × FS	V	
Zero Scale Calibration Limit	–1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
LOGIC INPUTS					
SCLK, DIN, $\overline{CS}$, and $\overline{RESET}$ Inputs					
Input Current			±1	μA	
Input Current $\overline{CS}$			±10	μA	$\overline{CS}$ = AV_{DD}
			–40	μA	Internal Pull-Up Resistor
Input Capacitance		4		pF	
V_{T+}[1]	1.4		2	V	DV_{DD} = 5 V
V_{T-}[1]	0.8		1.4	V	DV_{DD} = 5 V
$V_{T+} – V_{T-}$[1]	0.3		0.85	V	DV_{DD} = 5 V
V_{T+}[1]	0.95		2	V	DV_{DD} = 3 V
V_{T-}[1]	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} – V_{T-}$[1]	0.3		0.85	V	DV_{DD} = 3 V
MCLK IN Only					
Input Current			±10	μA	
Input Capacitance		4		pF	
V_{INL} Input Low Voltage			0.8	V	DV_{DD} = 5 V
V_{INH} Input High Voltage	3.5			V	DV_{DD} = 5 V
V_{INL} Input Low Voltage			0.4	V	DV_{DD} = 3 V
V_{INH} Input High Voltage	2.5			V	DV_{DD} = 3 V
LOGIC OUTPUTS					
MCLKOUT[10], DOUT, $\overline{RDY}$					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 800 μA, DV_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 μA, DV_{DD} = 5 V
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 100 μA, DV_{DD} = 3 V
V_{OH} Output High Voltage	DV_{DD} – 0.6			V	I_{SOURCE} = 100 μA, DV_{DD} = 3 V
Floating State Leakage Current			±1	μA	
Floating State Leakage Capacitance		3		pF	
P1 INPUT					Levels Referenced to Analog Supplies
Input Current			±10	μA	
V_{INL} Input Low Voltage			0.8	V	AV_{DD} = 5 V
V_{INH} Input High Voltage	3.5			V	AV_{DD} = 5 V
P0, P1 OUTPUT					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 8 mA, T_{MAX} = 70°C, AV_{DD} = 5 V
			0.4	V	I_{SINK} = 5 mA, T_{MAX} = 85°C, AV_{DD} = 5 V
			0.4	V	I_{SINK} = 2.5 mA, T_{MAX} = 105°C, AV_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 μA, AV_{DD} = 5 V
POWER REQUIREMENTS					
AV_{DD} – AGND Voltage	4.75		5.25	V	
DV_{DD} – DGND Voltage	4.75		5.25	V	
	2.70		3.60	V	
AV_{DD} Current (Normal Mode)		13.6	16	mA	AV_{DD} = 5 V
AV_{DD} Current (Internal Buffer Off)		8.5		mA	AV_{DD} = 5 V
DV_{DD} Current (Normal Mode)[11]		2.7	3	mA	DV_{DD} = 5 V
DV_{DD} Current (Normal Mode)[11]		1.0	1.5	mA	DV_{DD} = 3 V
AV_{DD} + DV_{DD} Current (Standby Mode)[12]		80		μA	AV_{DD} = DV_{DD} = 5 V
Power Dissipation (Normal Mode)[11]		85	100	mW	
Power Dissipation (Standby Mode)[12]		500		μW	AV_{DD} = DV_{DD} = 5 V

NOTES

[1]Specifications are not production tested, but guaranteed by design and/or characterization data at initial product release.

[2]Specifications before calibration. Channel System Calibration reduces these errors to the order of the noise.

[3]Applies after the Zero Scale and Full-Scale calibration. The Negative Full Scale error represents the remaining error after removing the offset and gain error.

[4]Specifications before calibration. ADC Zero Scale Self-Calibration or Channel Zero Scale System Calibration reduces this error to the order of the noise.

[5]The output data span corresponds to the Nominal (Typical) Input Voltage Range. Correct operation of the ADC is guaranteed within the specified min/max. Outside the Nominal Input Voltage Range, the OVR bit in the Channel Status register is set and the Channel Data register value depends on CLAMP bit in the Mode register. See the register description and circuit description for more details.

[6]If chopping is enabled or when switching between channels, there will be a dynamic current charging the capacitance of the multiplexer, capacitance of the pins, and any additional capacitance connected to the MUXOUT. See the circuit description for more details.

[7]For specified performance. Part is functional with Lower V_{REF}

[8]Dynamic current charging the sigma-delta modulator input switching capacitor.

[9]Outside the specified calibration range, calibration is possible but the performance may degrade.

[10]These logic output levels apply to the MCLK OUT output when it is loaded with a single CMOS load.

[11]With external MCLK, MCLKOUT disabled (CLKDIS bit set in the Mode register).

[12]External MCLKIN = 0 V or DV_{DD}, Digital Inputs = 0 V or DV_{DD}, P0 and P1 = 0 V or AV_{DD}.

Specifications are subject to change without notice.

TIMING SPECIFICATIONS[1, 2, 3]

(AV_{DD} = 5 V ± 5%; DV_{DD} = 2.7 V to 3.6 V or 5 V ± 5%; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
MASTER CLOCK RANGE	1		6.144	MHz	
t_1	50			ns	$\overline{SYNC}$ Pulsewidth
t_2	500			ns	$\overline{RESET}$ Pulsewidth
READ OPERATION					
t_4	0			ns	$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time
t_5[4]					SCLK Falling Edge to Data Valid Delay
	0		60	ns	DV_{DD} of 4.75 V to 5.25 V
	0		80	ns	DV_{DD} of 2.7 V to 3.3 V
t_{5A}[4, 5]					$\overline{CS}$ Falling Edge to Data Valid Delay
	0		60	ns	DV_{DD} of 4.75 V to 5.25 V
	0		80	ns	DV_{DD} of 2.7 V to 3.3 V
t_6	50			ns	SCLK High Pulsewidth
t_7	50			ns	SCLK Low Pulsewidth
t_8	0			ns	$\overline{CS}$ Rising Edge after SCLK Rising Edge Hold Time
t_9[6]	10		80	ns	Bus Relinquish Time after SCLK Rising Edge
WRITE OPERATION					
t_{11}	0			ns	$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup
t_{12}	30			ns	Data Valid to SCLK Rising Edge Setup Time
t_{13}	25			ns	Data Valid after SCLK Rising Edge Hold Time
t_{14}	50			ns	SCLK High Pulsewidth
t_{15}	50			ns	SCLK Low Pulsewidth
t_{16}	0			ns	$\overline{CS}$ Rising Edge after SCLK Rising Edge Hold Time

NOTES

[1]Sample tested during initial release to ensure compliance.

[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[3]See Figures 1 and 2.

[4]These numbers are measured with the load circuit of Figure 3 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[5]This specification is relevant only if CS goes low while SCLK is low.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications are subject to change without notice.

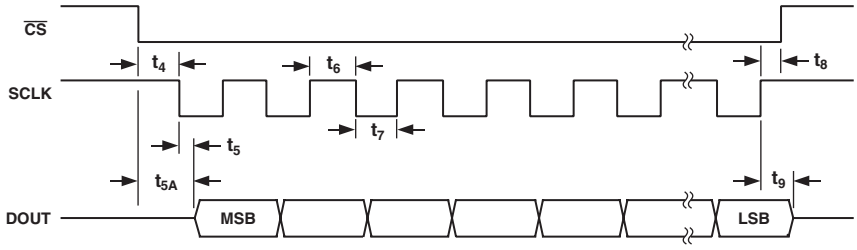


Figure 1. Read Cycle Timing Diagram

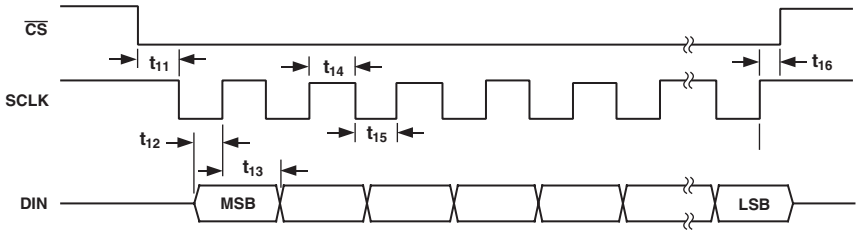


Figure 2. Write Cycle Timing Diagram

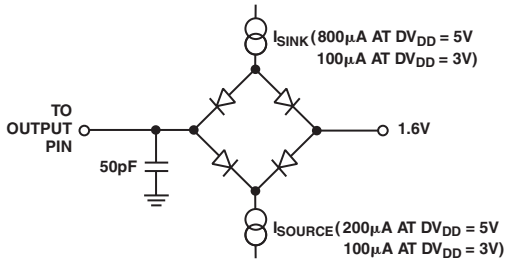


Figure 3. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted.)

AV_{DD} to AGND, DV_{DD} to DGND	–0.3 V to +7 V
AGND to DGND	–0.3 V to +0.3 V
AV_{DD} to DV_{DD}	–5 V to +5 V
AIN, AINCOM to AGND	–0.3 V to AV_{DD} + 0.3 V
REFIN(+), REFIN(–) to AGND	–0.3 V to AV_{DD} + 0.3 V
MUXOUT(+) to AGND	–0.3 V to AV_{DD} + 0.3 V
MUXOUT(–) to AGND	–0.3 V to AV_{DD} + 0.3 V
ADCIN(+), ADCIN(–) to AGND	–0.3 V to AV_{DD} + 0.3 V
P1 Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	–0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	660 mW
θ_{JA} Thermal Impedance	97.9°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD7738BRU	–40°C to +105°C	TSSOP 28	RU-28

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7738 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

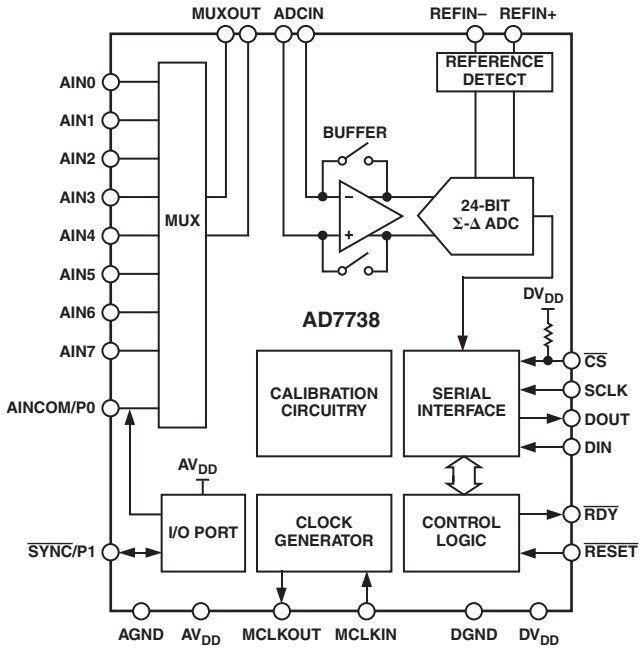
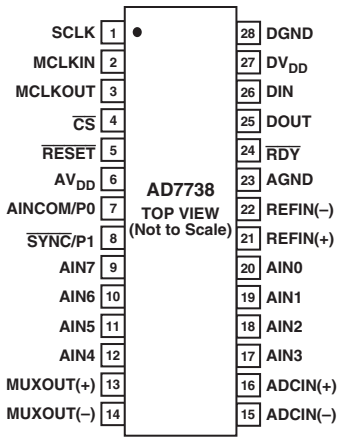


Figure 4. Block Diagram

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock. Schmitt-Triggered Logic Input. An external serial clock is applied to this input to transfer serial data to or from the AD7738.
2	MCLKIN	Master Clock Signal for the ADC. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLKIN and MCLKOUT pins. Alternatively, the MCLKIN pin can be driven with a CMOS compatible clock and MCLKOUT left unconnected.
3	MCLKOUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLKIN and MCLKOUT. If an external clock is applied to the MCLKIN, MCLKOUT provides an inverted clock signal or can be switched off to lower the device power consumption. MCLKOUT is capable of driving one CMOS load.
4	$\overline{CS}$	Chip Select. Active low Schmitt triggered logic input with an internal pull-up resistor. With this input hardwired low, the AD7738 can operate in its 3-wire interface mode using SCLK, DIN, and DOUT. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus. It can also be used as an 8-bit frame synchronization signal.
5	$\overline{RESET}$	Schmitt-Triggered Logic Input. Active low input that resets the control logic, interface logic, digital filter, analog modulator, and all on-chip registers of the part to power-on status. Effectively, everything on the part except the clock oscillator is reset when the $\overline{RESET}$ pin is exercised.
6	AV_{DD}	Analog Positive Supply Voltage. 5 V to AGND nominal.
7	AINCOM/P0	Analog Inputs Common Terminal/Digital Output. The pin is determined by the P0 Dir bit; the digital value can be written as the P0 bit in the I/O Port register. The digital voltage is referenced to analog supplies. When configured as an input (P0 Dir bit set to 1), the single-ended Analog Inputs 0 to 7 can be referenced to this pin's voltage level.
8	$\overline{SYNC}$/P1	$\overline{SYNC}$/Digital Input/Digital Output. The pin direction is determined by the P1 Dir bit; the digital value can be read/written as the P1 bit in the I/O Port register. When the SYNC Enable bit in the I/O Port register is set to 1, the $\overline{SYNC}$/P1 pin can be used to synchronize the AD7738 modulator and digital filter with other devices in the system. The digital voltage is referenced to the analog supplies. When configured as an input, the pin should be tied high or low.
9–12, 17–20	AIN0–AIN7	Analog Inputs
13	MUXOUT(+)	Analog Multiplexer Positive Output
14	MUXOUT(–)	Analog Multiplexer Negative Output

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Mnemonic	Pin Description
15	ADCIN(–)	ADC Negative Input. In normal circuit configuration, this pin should be connected to the MUXOUT– pin.
16	ADCIN(+)	ADC Positive Input. In normal circuit configuration, this pin should be connected to the MUXOUT+ pin.
21	REFIN(+)	Positive Terminal of the Differential Reference Input. REFIN+ voltage potential can lie any where between AV_{DD} and AGND. In normal circuit configuration, this pin should be connected to a 2.5 V reference voltage.
22	REFIN(–)	Negative Terminal of the Differential Reference Input. REFIN– voltage potential can lie any where between AV_{DD} and AGND. In normal circuit configuration, this pin should be connected to a 0 V reference voltage.
23	AGND	Ground Reference Point for Analog Circuitry
24	$\overline{RDY}$	Logic Output. Used as a status output in both conversion mode and calibration mode. In conversion mode, a falling edge on this output indicates that either any channel or all channels have unread data available—according to the RDY function bit in the I/O Port register. In calibration mode, a falling edge on this output indicates that calibration is complete. See more details in Digital Interface Description section later in this data sheet.
25	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from any AD7738 register depending on the address bits of the Communications register.
26	DIN	Serial Data Input (Schmitt triggered) with serial data being written to the input shift register on the part. Data from this input shift register is transferred to any AD7738 register depending on the address bits of the Communications register.
27	DV_{DD}	Digital Supply Voltage, 3 V or 5 V Nominal
28	DGND	Ground Reference Point for Digital Circuitry

OUTPUT NOISE AND RESOLUTION SPECIFICATION

The AD7738 can be operated with chopping enabled or disabled, allowing the ADC to be programmed either to optimize the throughput rate and channel switching time or to optimize offset drift performance. Noise tables for these two primary modes of operation are outlined below for a selection of output rates and settling times.

CHOPPING ENABLED

The first mode, in which the AD7738 is configured with chopping enabled (CHOP = 1), provides very low noise numbers with lower output rates. Tables I to III show the –3 dB frequencies and typical performance versus channel conversion time or equivalent output data rate, respectively. Table I shows the typical output rms noise. Table II shows the typical effective resolution based on the rms noise. Table III shows the typical output peak-to-peak resolution, representing values for which there will be no code flicker within a six-sigma limit. The peak-to-peak resolutions are not calculated based on rms noise, but on peak-to-peak noise.

These typical numbers are generated from 4096 data samples acquired in Continuous Conversion mode with an analog input voltage set to 0 V and MCLK = 6.144 MHz. The Conversion Time is selected via the Channel Conversion Time register.

Table I. Typical Output RMS Noise in μV vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (μs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range	
					±2.5 V, +2.5 V	±1.25 V, +1.25 V, ±625 mV, +625 mV
127	FFh	2686	372	194	1.8	1.1
46	AEh	999	1001	521	3.0	1.8
17	91h	395	2534	1317	5.1	3.0
8	88h	207	4826	2510	8.1	4.5
4	84h	124	8074	4198	9.3	5.3
2	82h	82	12166	6326	17.0	10.6

Table II. Typical Effective Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (μs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±625 mV	+625 mV
127	FFh	2686	372	194	21.4	20.4	21.1	20.1	20.1	19.1
46	AEh	999	1001	521	20.6	19.6	20.4	19.4	19.4	18.4
17	91h	395	2534	1317	19.9	18.9	19.6	18.6	18.6	17.6
8	88h	207	4826	2510	19.2	18.2	19.0	18.0	18.0	17.0
4	84h	124	8074	4198	19.0	18.0	18.8	17.8	17.8	16.8
2	82h	82	12166	6326	18.1	17.1	17.8	16.8	16.8	15.8

Table III. Typical Peak-to-Peak Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled

FW	Conversion Time Register	Conversion Time (μs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±625 mV	+625 mV
127	FFh	2686	372	194	18.4	17.4	18.2	17.2	17.2	16.2
46	AEh	999	1001	521	17.8	16.8	17.5	16.5	16.5	15.5
17	91h	395	2534	1317	16.8	15.8	16.7	15.7	15.7	14.7
8	88h	207	4826	2510	16.5	15.5	16.2	15.2	15.2	14.2
4	84h	124	8074	4198	16.0	15.0	16.0	15.0	15.0	14.0
2	82h	82	12166	6326	15.0	14.0	15.0	14.0	14.0	13.0

CHOPPING DISABLED

The second mode, in which the AD7738 is configured with chopping disabled (CHOP = 0), provides faster conversion time while still maintaining high resolution. Tables IV to VI show the –3 dB frequencies and typical performance versus channel conversion time or equivalent output data rate, respectively. Table IV shows the typical output rms noise. Table V shows the typical effective resolution based on the rms noise. Table VI shows the typical output peak-to-peak resolution, representing values for which there will be no code flicker within a six-sigma limit. The peak-to-peak resolutions are not calculated based on rms noise, but on peak-to-peak noise.

These typical numbers are generated from 4096 data samples acquired in Continuous Conversion mode with an analog input voltage set to 0 V and MCLK = 6.144 MHz. The Conversion Time is selected via the Channel Conversion Time register.

Table IV. Typical Output RMS Noise in μV vs. Conversion Time and Input Range with Chopping Disabled

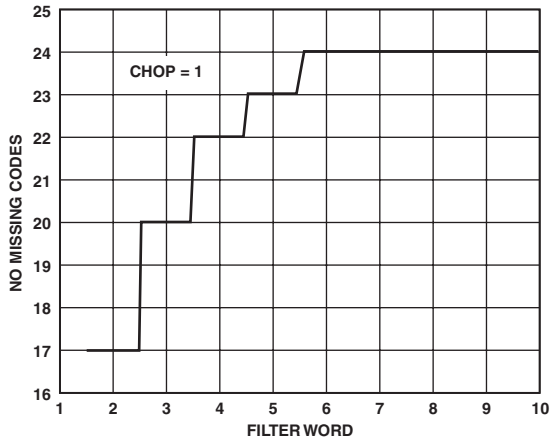
FW	Conversion Time Register	Conversion Time (μs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range	
					±2.5 V, +2.5 V	±1.25 V, +1.25 V, ±625 mV, +625 mV
127	7Fh	1357	737	671	2.7	1.5
92	5Ch	992	1008	917	3.0	1.8
35	23h	398	2511	2285	5.1	3.0
16	10h	200	4991	2510	7.5	4.5
9	9h	127	7847	7141	10.2	5.9
8	8h	117	8545	7776	11.4	6.5
3	3h	65	15398	14013	15.5	10.3

Table V. Typical RMS Resolution in Bits vs. Conversion Time and Input Range with Chopping Disabled

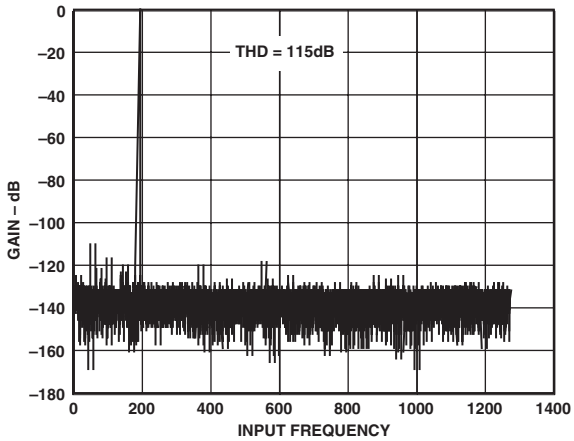
FW	Conversion Time Register	Conversion Time (μs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±625 mV	+625 mV
127	7Fh	1357	737	671	20.8	19.8	20.6	19.6	19.6	18.6
92	5Ch	992	1008	917	20.6	19.6	20.4	19.4	19.4	18.4
35	23h	398	2511	2285	19.9	18.9	19.6	18.6	18.6	17.6
16	10h	200	4991	2510	19.3	18.3	19.0	18.0	18.0	17.0
9	9h	127	7847	7141	18.9	17.9	18.7	17.7	17.7	16.7
8	8h	117	8545	7776	18.7	17.7	18.5	17.5	17.5	16.5
3	3h	65	15398	14013	18.0	16.7	17.8	17.1	17.1	16.1

Table VI. Typical Peak-to-Peak Resolution in Bits vs. Conversion Time and Input Range with Chopping Disabled

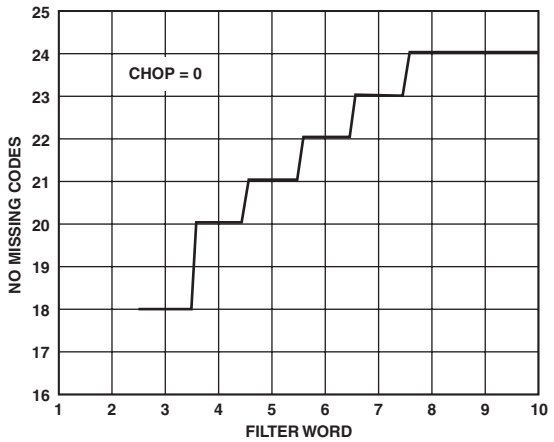
FW	Conversion Time Register	Conversion Time (μs)	Output Data Rate (Hz)	–3 dB Frequency (Hz)	Input Range					
					±2.5 V	+2.5 V	±1.25 V	+1.25 V	±625 mV	+625 mV
127	7Fh	1357	737	671	17.9	16.9	17.8	16.8	16.8	15.8
92	5Ch	992	1008	917	17.8	16.8	17.4	16.4	16.4	15.4
35	23h	398	2511	2285	17.0	16.0	16.8	15.8	15.8	14.8
16	10h	200	4991	2510	16.3	15.3	16.2	15.2	15.2	14.2
9	9h	127	7847	7141	16.1	15.1	15.9	14.9	14.9	13.9
8	8h	117	8545	7776	16.0	15.0	15.7	14.7	14.7	13.7
3	3h	65	15398	14013	15.0	14.0	14.8	13.8	13.8	12.8



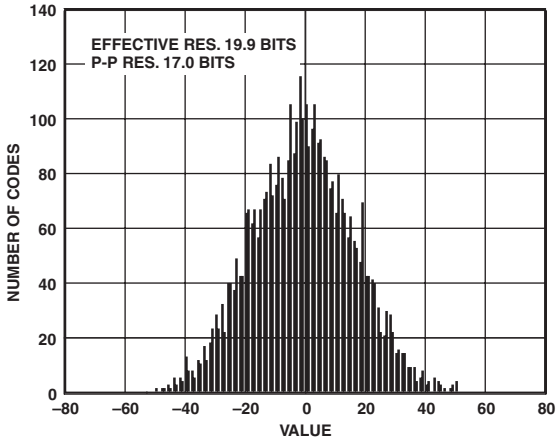
TPC 1. No Missing Codes Performance, Chopping Enabled



TPC 3. Typical FFT Plot; Input Sinewave 183 Hz, 1.2 V Peak, Range ±1.25 V, Conversion Time 394 μs, Chopping Enabled



TPC 2. No Missing Codes Performance, Chopping Disabled



TPC 4. Typical Histogram; Analog Inputs Shorted; Range ±2.5 V, Conversion Time 394 μs; Chopping Enabled

Table VII. Register Summary

Register	Addr hex	Dir	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Default Value							
Communications	00	W	0	R/$\overline{W}$	6-Bit Register Address					
I/O Port	01	R/W	P0	P1	P0 DIR	P1 DIR	RDY FN	0	0	SYNC
			P0 Pin	P1 Pin	1	1	0	0	0	0
Revision	02	R	Chip Revision Code				Chip Generic Code			
			x	x	x	x	0	0	0	1
Test	03	R/W	24 Bits Manufacturing Test Register							
ADC Status	04	R	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
			0	0	0	0	0	0	0	0
Checksum	05	R/W	16-Bit Checksum Register							
ADC ZS Calibration	06	R/W	24-Bit ADC Zero-Scale Calibration Register							
			800000h							
ADC FS	07	R/W	24-Bit ADC Full-Scale Register							
			800000h							
Channel Data[1]	08-0F	R	16-/24-Bit Data Registers							
			8000h							
Channel ZS Calibration[1]	10–17	R/W	24-Bit Channel Zero-Scale Calibration Registers							
			800000h							
Channel FS Calibration[1]	18–1F	R/W	24-Bits Channel Full-Scale Calibration Registers							
			200000h							
Channel Status[1]	20–27	R	CH2	CH1	CH0	0/P0	RDY/P1	NOREF	SIGN	OVR
			Channel Number			0	0	0	0	0
Channel Setup[1]	28–2F	R/W	BUF OFF	COM1	COM0	Stat. Opt.	ENABLE	RNG2	RNG1	RNG0
			0	0	0	0	0	0	0	0
Channel Conv. Time[1]	30–37	R/W	CHOP	FW (7-Bit Filter Word)						
			1	11h						
Mode[2]	38–3F	R/W	MD2	MD1	MD0	CLKDIS	DUMP	Cont. RD	24/16 Bits	CLAMP
			0	0	0	0	0	0	0	0

NOTES
[1]The three LSBs of the register address, i.e., Bit 2, Bit 1, and Bit 0 in the Communication register, specify the channel number of the register being accessed.
[2]There is only one Mode register, although the Mode register can be accessed in one of eight address locations The address used to write the Mode register specifies the ADC channel on which the mode will be applied. Address 38h only must be used for reading from the Mode register.

Table VIII. Operational Mode Summary

MD2	MD1	MD0	Mode
0	0	0	Idle Mode
0	0	1	Continuous Conversion Mode
0	1	0	Single Conversion Mode
0	1	1	Power-Down (Standby) Mode
1	0	0	ADC Zero-Scale Self Calibration
1	0	1	For Future Use
1	1	0	Channel Zero-Scale System Calibration
1	1	1	Channel Full-Scale System Calibration

Table IX. Input Range Summary

RNG2	RNG1	RNG0	Nominal Input Voltage Range
1	0	0	±2.5 V
1	0	1	0 V to +2.5 V
0	0	0	±1.25 V
0	0	1	0 V to +1.25 V
0	1	0	±0.625 V
0	1	1	0 V to +0.625 V

REGISTER DESCRIPTION

The AD7738 is configurable through a series of registers. Some of them configure and control general AD7738 features, others are specific to each channel. The register data widths vary from 8 bits to 24 bits. All registers are accessed through the Communication register, i.e., any communication to the AD7738 must start with a write to the Communication register, specifying which register will be subsequently read or written.

Communications Register

8 Bits, Write-Only Register, Address 00h

All communications to the part must start with a write operation to the Communications register. The data written to the Communications register determines whether the subsequent operation will be a read or write and to which register this operation will be directly placed. The digital interface defaults to expect write operation to the Communication register after power on, after reset, or after the subsequent read or write operation to the selected register is complete. If the interface sequence is lost, the part can be reset by writing at least 32 serial clock cycles with DIN high and $\overline{CS}$ low (Note that all of the parts including modulator, filter, interface and all registers are reset in this case). Remember to keep DIN low while reading 32 or more bits either in Continuous Read mode or with the DUMP bit and "24/16" bit in the Mode register set.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	0	R/$\overline{W}$	6-Bit Register Address					

Bit	Mnemonic	Description
7	0	This bit must be zero for proper operation.
6	R/$\overline{W}$	A zero in this bit indicates that the next operation will be a write to a specified register. A one in this bit indicates that the next operation will be a read from a specified register.
5–0	Address	Address specifying to which register the read or write operation will be directed. For channel specific registers the three LSBs, i.e., Bit 2, Bit 1, and Bit 0, specify the channel number. When the subsequent operation writes to the Mode register, then the three LSBs specify the channel selected for operation determined by the Mode register value. See Table X. (The analog input's configuration depends on the COM1, COM0 bits in the Channel Setup register.)

Table X.

Bit 2	Bit 1	Bit 0	Channel	Single Input	Differential Input
0	0	0	0	AIN0	AIN0–AIN1
0	0	1	1	AIN1	AIN2–AIN3
0	1	0	2	AIN2	AIN4–AIN5
0	1	1	3	AIN3	AIN6–AIN7
1	0	0	4	AIN4	AIN0–AIN1
1	0	1	5	AIN5	AIN2–AIN3
1	1	0	6	AIN6	AIN4–AIN5
1	1	1	7	AIN7	AIN6–AIN7

I/O Port Register

8 Bits, Read/Write Register, Address 01h, Default Value 30h + Digital Input Value × 40h

The bits in this register are used to configure and access the digital I/O pin on the AD7738.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	P0	P1	P0 DIR	P1 DIR	RDY FN	0	0	SYNC
Default	P0 Pin	P1 Pin	1	1	0	0	0	0

Bit	Mnemonic	Description
7	P0	When the AINCOM/P0 pin is configured as a digital output, the P0 bit determines the pin's output level.
6	P1	When the P1 pin is configured as an output, the P1 bit determines the pin's output level. When the P1 pin is configured as an input, the P1 bit reflects the current input level on the pin.
5	P0 DIR	When set to 1, the AINCOM/P0 pin is configured as an analog input. When set to 0, the AINCOM/P0 pin is configured as a digital output.
4	P1 DIR	This bit determines whether P1 pin is configured as an input or an output. When set to 1, the P1 pin will be a digital input; when reset to 0, the pin will be a digital output.
3	RDY FN	This bit is used to control the function of the $\overline{\text{RDY}}$ pin on the AD7738. When this bit is reset to 0 the $\overline{\text{RDY}}$ pin goes low when any channel has unread data. When this bit is set to 1, the $\overline{\text{RDY}}$ pin will only go low if all enabled channels have unread data.
2, 1	0	These bits must be zero for proper operation.
0	SYNC	This bit enables the $\overline{\text{SYNC}}$ pin function. By default, this bit is 0 and $\overline{\text{SYNC}}$/P1 can be used as a digital I/O pin. When the SYNC EN bit is set to 1, the $\overline{\text{SYNC}}$ pin can be used to synchronize the AD7738 modulator and digital filter with other devices in the system.

Revision Register

8 Bits, Read-Only Register, Address 02h, Default Value 01h + Chip Revision × 10h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	Chip Revision Code				Chip Generic Code			
Default	x	x	x	x	0	0	0	1

Bit	Mnemonic	Description
7–4	Chip Revision Code	4-Bit Factory Chip Revision Code
3–0	Chip Generic Code	On the AD7738, these bits will read back as 01h.

Test Register

24 Bits, Read/Write Register, Address 03h

This register is used for testing the part in the manufacturing process. The user must not change the default configuration of this register.

ADC Status Register

8 Bits, Read-Only Register, Address 04h, Default Value 00h

In conversion modes, the register bits reflect the individual channel status. When a conversion is complete, the corresponding Channel Data register is updated and the corresponding RDY bit is set to 1. When the Channel Data register is read, the corresponding bit is reset to 0. The bit is also reset to 0 when no read operation has taken place and the result of the next conversion is being updated to the Channel Data register. Writing to the Mode register resets all the bits to 0.

In calibration modes, all the register bits are reset to 0 while a calibration is in progress and all the bits are set to 1 when the calibration is complete.

The $\overline{\text{RDY}}$ pin output is related to the content of ADC Status register as defined by the RDY Function bit in the I/O Port register.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
Default	0	0	0	0	0	0	0	0

The RDY0 bit corresponds to Channel 0, RDY1 bit to Channel 1, and so on.

Checksum Register
16 Bits, Read/Write Register, Address 05h
This register is described in the "AD7732/34/38 Checksum Register" Technical Note.

ADC Zero Scale Calibration Register
24 Bits, Read/Write Register, Address 06h, Default Value 800000h
The register holds the ADC Zero-Scale Calibration coefficient. The value in this register is used in conjunction with the value in the ADC Full-Scale Calibration register and corresponding Channel Zero-Scale and Channel Full-Scale Calibration registers to scale digitally all channels' conversion results. The value in this register is updated automatically following the execution of an ADC Zero-Scale ADC Self-Calibration. Writing to this register is possible in the Idle Mode only. See the calibration description for more details.

ADC Full-Scale Register
24 Bits, Read/Write Register, Address 07h, Default Value 800000h
The register holds the ADC Full-Scale coefficient. The user is advised not to change the default configuration of this register.

Channel Data Registers
16/24 Bits, Read-Only Registers, Address 08h–0Fh, Default Width 16 Bits, Default Value 8000h
These registers contain the most up-to-date conversion results corresponding to each analog input channel. The 16- or 24-bit data width can be configured by setting the "16/24" bit in the Mode register. The relevant RDY bit in the Channel Status register goes high when the result is updated. The RDY bit will return low once the Data register reading has begun. The $\overline{\text{RDY}}$ pin can be configured to indicate when any channel has unread data or waits until all enabled channels have unread data. If any Channel Data Register read operation is in progress when the new result is updated, then no update of the Data register occurs. This is to avoid getting corrupted data. Reading the Status registers can be associated with reading the Data registers in the Dump mode. Reading the Status registers is always associated with reading the Data registers in the Continuous Read mode. See the digital interface description for more details.

Channel Zero-Scale Calibration Registers
24 Bits, Read/Write Registers, Address 10h–17h, Default Value 800000h
These registers hold the particular channel Zero-Scale Calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding Channel Full-Scale Calibration register, the ADC Zero-Scale Calibration register, and ADC Full-Scale Calibration register to scale digitally the particular channel conversion results. The value in this register is updated automatically following the execution of a Channel Zero-Scale System Calibration.

The format of the Channel Zero-Scale Calibration register is a sign bit and 22 bits unsigned value.

Writing this register is possible in the Idle Mode only. See the calibration description for more details.

Channel Full-Scale Calibration Registers
24 Bits, Read/Write Registers, Address 18h–1Fh, Default Value 200000h
These registers hold the particular channel Full-Scale Calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding Channel Zero-Scale Calibration register, the ADC Zero-Scale Calibration register, and ADC Full Scale Calibration register to scale digitally the particular channel conversion results. The value in this register is updated automatically following the execution of a Channel Full-Scale System Calibration. Writing this register is possible in the Idle mode only. See the calibration description for more details.

Channel Status Registers

8 Bits, Read-Only Register, Address 20h–27h, Default Value 20h × Channel Number

These registers contain individual channel status information and some general AD7738 status information. Reading the Status registers can be associated with reading the Data registers in the Dump mode. Reading the Status registers is always associated with reading the Data registers in the Continuous Read mode. See the Digital Interface Description section for more details.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CH2	CH1	CH0	0/P0	RDY/P1	NOREF	SIGN	OVR
Default	Channel Number			0	0	0	0	0

Bit	Mnemonic	Description
7–5	CH2–CH0	These bits reflect the channel number. This can be used for current channel identification and easier operation in the Dump mode and Continuous Read mode.
4	0/P0	When the Status Option bit in the corresponding Channel Setup register is reset to 0, this bit is read as a zero. When the Status Option bit in set to 1, this bit reflects the state of the P0 output pin.
3	RDY/P1	When the Status Option bit in the corresponding Channel Setup register is reset to 0, this bit reflects the selected channel RDY bit in the ADC Status register. When the Status Option bit is set to 1, this bit reflects the state of the P1 pin whether it is configured as an input or output.
2	NOREF	This bit indicates the reference input status. If the voltage between the REFIN+ and REFIN– pins is less than the NOREF trigger voltage, then the NOREF bit goes to a 1.
1	SIGN	The voltage polarity at the analog input. Will be 0 for a positive voltage; will be 1 for a negative voltage.
0	OVR	This bit reflects either overrange or underrange on an analog input. The bit is set to 1 when the analog input voltage goes over or under the Nominal Voltage Range. See the Analog Inputs Extended Voltage Range section.

Channel Setup Registers

8 Bits, Read/Write Register, Address 28h–2Fh, Default Value 00h

These registers are used to configure the selected channel, its input voltage range, and set up the corresponding Channel Status register.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	BUF OFF	COM1	COM0	Stat. Opt.	ENABLE	RNG2	RNG1	RNG0
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7	BUF OFF	Buffer Off. If reset to 0, then internal buffer is enabled. Only operation with internal buffer enabled is recommended.
6, 5	COM1, COM0	Analog Input Configuration. See Table XI.
4	Stat. Opt.	Status Option. When this bit is set to 1, the P1 bit in the Status Channel register will reflect the state of the P1 pin. When this bit is reset to 0, the P1 bit in the Status Channel register bit will reflect the channel corresponding RDY bit in the ADC Status register.
3	ENABLE	Channel Enable. Set this bit to 1 to enable the channel in the Continuous Conversion mode. A single conversion will take place regardless of this bit value.
2–0	RNG2–0	The Channel Input Voltage Range. See Table XII.

Table XI.

Channel	COM1 0	COM0 0	COM1 1	COM0 1
0	AIN0–AINCOM		AIN0–AIN1	
1	AIN1–AINCOM		AIN2–AIN3	
2	AIN2–AINCOM		AIN4–AIN5	
3	AIN3–AINCOM		AIN6–AIN7	
4	AIN4–AINCOM		AIN0–AIN1	
5	AIN5–AINCOM		AIN2–AIN3	
6	AIN6–AINCOM		AIN4–AIN5	
7	AIN7–AINCOM		AIN6–AIN7	

Table XII.

RNG2	RNG1	RNG0	Nominal Input Voltage Range
1	0	0	±2.5 V
1	0	1	0 V to +2.5 V
0	0	0	±1.25 V
0	0	1	0 V to +1.25 V
0	1	0	±0.625 V
0	1	1	0 V to +0.625 V

Channel Conversion Time Registers

8 Bits, Read/Write Register, Address 30h–37h, Default Value 91h

The Conversion Time registers enable or disable chopping and configure the digital filter for a particular channel.

This register value affects the conversion time, frequency response, and noise performance of the ADC.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CHOP	FW (7-Bit Filter Word)						
Default	1	11h						

Bit	Mnemonic	Description
7	CHOP	Chop Enable Bit. Set to 1 to apply chopping mode for a particular channel.
6–0	FW	CHOP = 1, Single Conversion or Continuous Conversion with one channel enabled. Conversion Time (μs) = (FW × 128 + 248)/MCLK Frequency (MHz), the FW in range of 2 to 127. CHOP = 1, Continuous Conversion with two or more channels enabled. Conversion Time (μs) = (FW × 128 + 249)/MCLK Frequency (MHz), the FW in range of 2 to 127. CHOP = 0, Single Conversion or Continuous Conversion with one channel enabled. Conversion Time (μs) = (FW × 64 + 206)/MCLK Frequency (MHz), the FW in range of 3 to 127. CHOP = 0, Single Conversion or Continuous Conversion with two or more channels enabled. Conversion Time (μs) = (FW × 64 + 207)/MCLK Frequency (MHz), the FW in range of 3 to 127.

Mode Register

8 Bits Read/Write Register, Address 38h–3Fh, Default Value 00h

The Mode register configures the part and determines the part's operating mode. Writing to the Mode register will clear the ADC Status register, set the $\overline{RDY}$ pin to logic high level, exit all current operations, and start the mode specified by the Mode bits.

The AD7738 contains only one Mode register. The three LSBs of the address used for writing to the Mode register specify the channel selected for operation determined by the MD2 to MD0 bits. The address 38h only must be used for reading from the Mode register.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	MD2	MD1	MD0	CLKDIS	DUMP	CONT RD	24/16 BIT	CLAMP
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7–5	MD2–MD0	Mode Bits. These three bits determine the AD7738 operation mode. Writing a new value to the Mode bits will exit the part from the mode in which it has been operating and place it in the new requested mode immediately. The function of the Mode bits is described in more detail below.
4	CLKDIS	Master Clock Output Disable. When this bit is set to 1 the master clock is disabled from appearing at the MCLKOUT pin and the MCLKOUT pin is in a high impedance state. This allows turning off the MCLKOUT as a power saving feature. When using an external clock on MCLKIN, the AD7738 continues to have internal clocks and will convert normally regardless of CLKDIS bit state. When using a crystal oscillator or ceramic resonator across the MCLKIN and MCLKOUT pins, the AD7738 clock is stopped and no conversions can take place when the CLKDIS bit is active. The AD7738 digital interface can still be accessed using the SCLK pin.
3	DUMP	DUMP Mode. When this bit is reset to 0, the Channel Status register and Channel Data register will be addressed and read separately. When the DUMP bit is set to 1, the Channel Status register will be followed immediately by a read of the Channel Data register regardless of whether the Status or Data register has been addressed through the Communication register. The Continuous Read mode will always be a "Dump Mode" reading of the Channel Status and Data register regardless of the Dump Bit value. See the Digital Interface Description section for more details.
2	CONT RD	When this bit is set to 1, the AD7738 will operate in the Continuous Read mode. See the Digital Interface Description section for more details.
1	24/16 BIT	The Channel Data Register Data Width Selection Bit. When set to 1, the Channel Data registers will be 24 bits wide. When set to 0, then the Channel Data registers will be 16 bits wide.
0	CLAMP	This bit determines the Channel Data register's value when the analog input voltage is outside the nominal input voltage range. When the CLAMP bit is set to 1, the Channel Data register will be digitally clamped either to all zeros or all ones when the analog input voltage goes outside the nominal input voltage range. When the CLAMP bit is reset to 0, the Data registers reflect the analog input voltage even outside the nominal voltage range. See the Analog Inputs Extended Voltage Range section.

MD2	MD1	MD0	Mode	Address Used for Mode Register Write Specify
0	0	0	Idle Mode	
0	0	1	Continuous Conversion Mode	The First Channel to Start Converting
0	1	0	Single Conversion Mode	Channel to Convert
0	1	1	Power Down (Standby) Mode	
1	0	0	ADC Zero-Scale Self Calibration	Channel Conversion Time Used for the ADC Self-Calibration
1	0	1	For Future Use	
1	1	0	Channel Zero-Scale System Calibration	Channel to Calibrate
1	1	1	Channel Full-Scale System Calibration	Channel to Calibrate

MD2	MD1	MD0	Operating Mode
0	0	0	Idle Mode The default mode after Power-On or Reset. The AD7738 returns to this mode automatically after any calibration or after a single conversion.
0	0	1	Continuous Conversion Mode The AD7738 performs a conversion on the specified channel. After the conversion is complete, the relevant Channel Data register and Channel Status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7738 continues converting on the next enabled channel. The AD7738 will cycle through all enabled channels until put into another mode or reset. The cycle period will be the sum of all enabled channels' conversion times, set by corresponding Channel Conversion Time registers.
0	1	0	Single Conversion Mode The AD7738 performs a conversion on the specified channel. After the conversion is complete, the relevant Channel Data register and Channel Status register are updated, the relevant RDY bit in the ADC status register is set, the $\overline{\text{RDY}}$ pin goes low, the MD2, MD1, and MD0 bits are reset, and AD7738 returns to the Idle mode. Requesting a single conversion ignores the Channel Setup registers' Enable bits and a conversion will be performed even if that channel is disabled.
0	1	1	Power-Down (Standby) Mode The ADC and the analog front end (internal buffer) go into the power-down mode. The AD7738 digital interface can still be accessed. The CLKDIS bit works separately, the MCLKOUT mode is not affected by Power-Down (Standby) mode.
1	0	0	ADC Zero-Scale Self-Calibration Mode A zero-scale self-calibration is performed on internally shorted ADC inputs. After the calibration is complete, the contents of the ADC Zero-Scale Calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{\text{RDY}}$ pin goes low, the MD2, MD1, and MD0 bits are reset, and the AD7738 returns to the Idle mode.
1	0	1	For Future Use
1	1	0	Channel Zero-Scale System Calibration Mode A zero-scale system calibration is performed on the selected channel. An external system zero-scale voltage should be provided at the AD7738 analog input and this voltage should remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding Channel Zero Scale Calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{\text{RDY}}$ pin goes low, the MD2, MD1, and MD0 bits are reset, and AD7738 returns to the Idle mode.
1	1	1	Channel Full-Scale System Calibration Mode A full-scale system calibration is performed on the selected channel. An external system full-scale voltage should be provided at the AD7738 analog input and this voltage should remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding Channel Full-Scale Calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{\text{RDY}}$ pin goes low, the MD2, MD1, and MD0 bits are reset, and AD7738 returns to the Idle mode.

DIGITAL INTERFACE DESCRIPTION

Hardware

The AD7738 serial interface can be connected to the host device via the serial interface in several different ways.

The $\overline{CS}$ pin can be used to select the AD7738 as one of several circuits connected to the host serial interface. When the $\overline{CS}$ is high, the AD7738 ignores the SCLK and DIN signals and the DOUT pin goes to the high impedance state. When the $\overline{CS}$ signal is not used, connect the $\overline{CS}$ pin to DGND.

The $\overline{RDY}$ pin can be either polled for high to low transition or can drive the host device interrupt input to indicate that the AD7738 has finished the selected operation and/or new data from the AD7738 are available. The host system can also wait a designated time after a given command is written to the device before reading. Alternatively, the AD7738 status can be polled. When the $\overline{RDY}$ pin is not used in the system, it should be left as an open circuit. (Note that the $\overline{RDY}$ pin is always an active digital output, i.e., never goes into a high impedance state).

The $\overline{RESET}$ pin can be used to reset the AD7738. When not used, connect this pin to DV_{DD}.

The AD7738 interface can be reduced to just two wires connecting DIN and DOUT pins to a single bidirectional data line. The second signal in this 2-wire configuration is the SCLK signal. The host system should change the data line direction with reference to the AD7738 timing specification (see the Bus Relinquish Time in the Timing Characteristics). The AD7738 cannot operate in the Continuous Read mode in 2-wire serial interface configuration.

All the digital interface inputs are Schmitt-Triggered. Therefore, the AD7738 interface features higher noise immunity and the AD7738 can be easily isolated from the host system via optocouplers.

Figure 5 outlines some of the possible host device interfaces: (a) SPI without using the $\overline{CS}$ signal, (b) DSP interface, and (c) 2-wire configuration.

Reset

The AD7738 can be reset by the $\overline{RESET}$ pin or by writing a reset sequence to the AD7738 serial interface. The reset sequence is N × "0" + 32 × "1", which could be the data sequence 00h + FFh + FFh + FFh + FFh in a byte oriented interface. The AD7738 also features a power-on reset with a trip point of 2 V and goes to the defined default state after power on.

It is the system designer's responsibility to prevent an unwanted write operation to the AD7738. The unwanted write operation could happen when a spurious clock appears on the SCLK while the $\overline{CS}$ pin is low. It should be noted that on system power-on, if the AD7738 interface signals are floating or undefined, the part can be inadvertently configured into an unknown state. This could be easily overcome by initiating either a HW reset event or a 32 ones reset sequence as the first step in the system configuration.

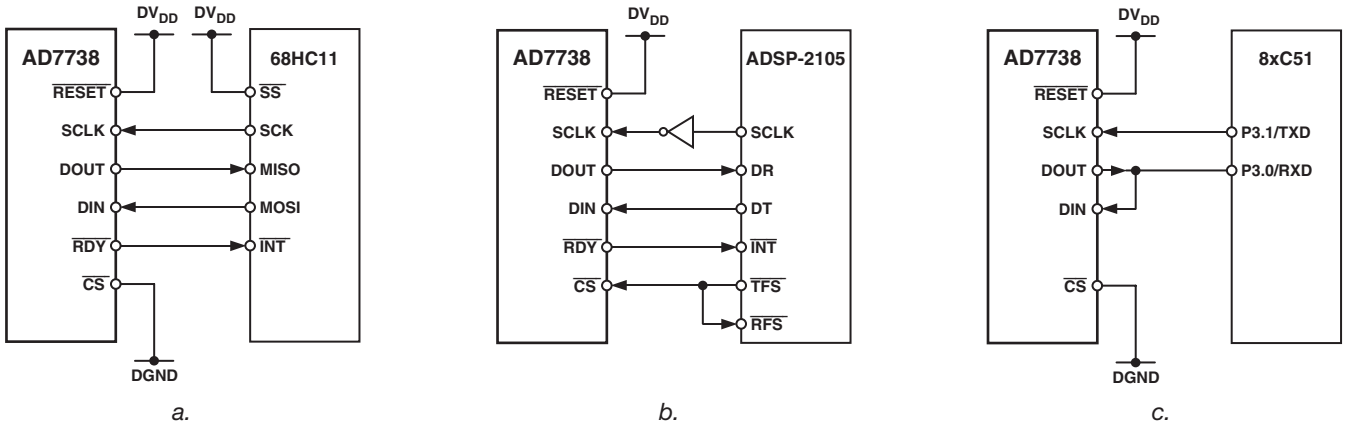


Figure 5. AD7738 to Host Device Possible Interface

Access the AD7738 Registers

All communications to the part start with a write operation to the Communications register followed by either reading or writing the addressed register.

In a simultaneous read-write interface (such as SPI), write "0" to the AD7738 while reading data.

Figure 6 shows the AD7738 interface read sequence for the ADC Status register.

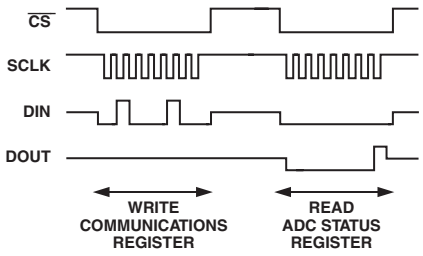


Figure 6. The Serial Interface Signals—Register Access

Single Conversion and Reading Data

When the Mode register is being written, the ADC Status Byte is cleared and the $\overline{RDY}$ pin goes high regardless of its previous state. When the single conversion command is written to the Mode register, the ADC starts the conversion on the channel selected by the address of the Mode register. After the conversion is completed, the Data register is updated, the Mode register is changed to Idle mode, the relevant RDY bit is set, and the $\overline{RDY}$ pin goes low. The RDY bit is reset and the $\overline{RDY}$ pin returns high when the relevant Channel Data register is being read.

Figure 7 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{RDY}$ pin low, and reading the Channel 0 Data register.

Dump Mode

When the DUMP bit in the Mode register is set to 1, the Channel Status register will be read immediately by a read of the Channel Data register regardless of whether the Status or the Data register has been addressed through the Communication register. The DIN pin should not be high while reading 24-bit data in Dump mode. Otherwise the AD7738 will be reset.

Figure 8 shows the digital interface signals executing a single conversion on Channel 0, waiting for for the $\overline{RDY}$ pin low, and reading the Channel 0 Status register and Data register in the Dump mode.

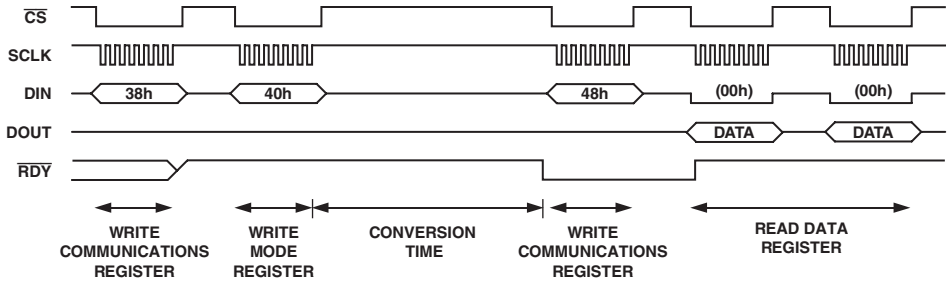


Figure 7. Serial Interface Signals—Single Conversion Command and 16-Bit Data Reading

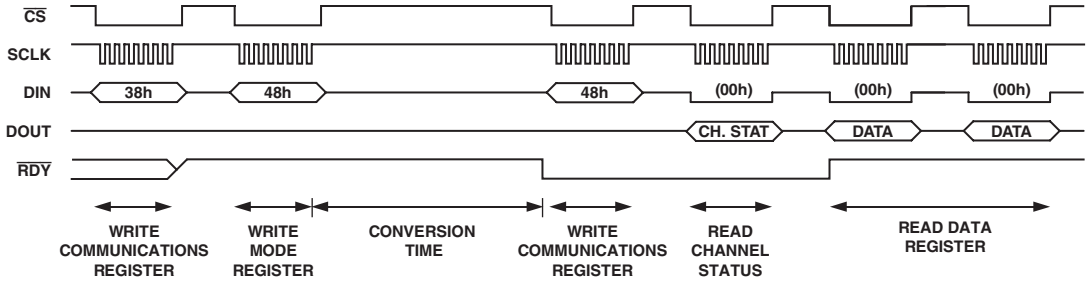


Figure 8. Serial Interface Signals—Single Conversion Command, 16-Bit Data Reading, Dump Mode

Continuous Conversion Mode

When the Mode register is being written, the ADC Status Byte is cleared and the $\overline{RDY}$ pin goes high regardless of its previous state. When the continuous conversion command is written to the Mode register, the ADC starts conversion on the channel selected by the address of the Mode register.

After the conversion is complete, the relevant Channel Data register and Channel Status register are updated, the relevant RDY bit in the ADC Status register is set, and the AD7738 continues converting on the next enabled channel. The AD7738 will cycle through all enabled channels until put into another mode or reset. The cycle period will be the sum of all enabled channels' conversion times, set by corresponding Channel Conversion Time registers.

The RDY bit is reset when the relevant Channel Data register is being read. The behavior of the $\overline{RDY}$ pin depends on the RDYFN bit in the I/O Port register. When RDYFN bit is 0, the $\overline{RDY}$ pin goes low when any channel has unread data. When this bit is set to 1 the $\overline{RDY}$ pin will only go low if all enabled channels have unread data.

If an ADC conversion result has not been read before a new ADC conversion is completed, then the new result will overwrite the previous one. The relevant RDY bit goes low and the $\overline{RDY}$ pin goes high for at least 163 MCLK cycles (~26.5 μs), indicating when the Data register is updated and the previous conversion data is lost.

If the Data register is being read as an ADC conversion completes, then the Data Register will not be updated with the new result (to avoid data corruption) and the new conversion data is lost.

Figure 9 shows the digital interface signals sequence for the Continuous Conversion mode with Channels 0 and 1 enabled and the RDYFN bit set to 0. The $\overline{RDY}$ pin goes low and the Data Register is read after each conversion. Figure 10 shows a similar sequence, but with the RDYFN bit set to 1. The $\overline{RDY}$ pin goes low and the Data register is read after all conversions are completed. Figure 11 shows the $\overline{RDY}$ pin when no data are read from the AD7738.

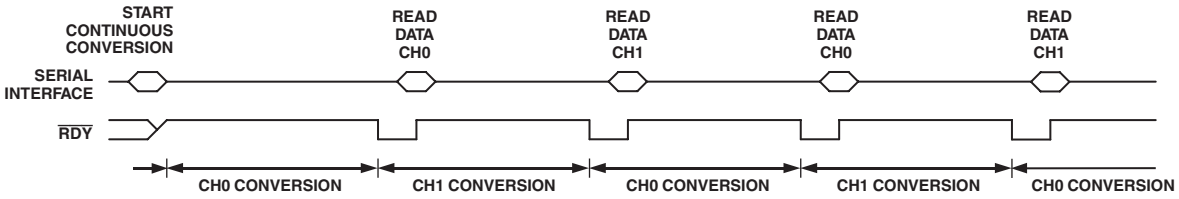


Figure 9. Continuous Conversion, CH0 and CH1, RDYFN = 0

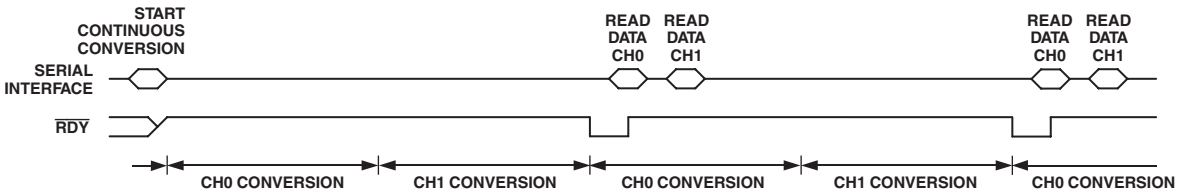


Figure 10. Continuous Conversion, CH0 and CH1, RDYFN = 1

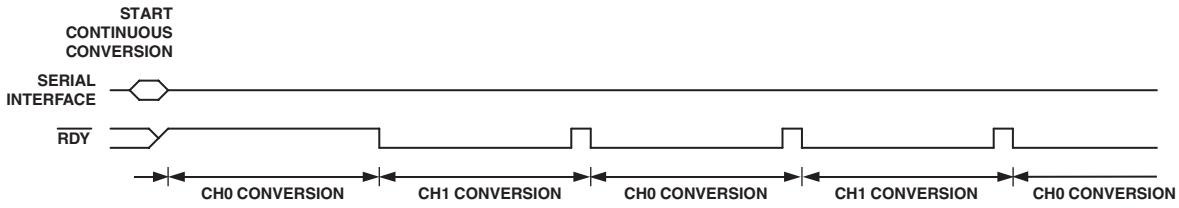


Figure 11. Continuous Conversion, CH0 and CH1, No Data Read

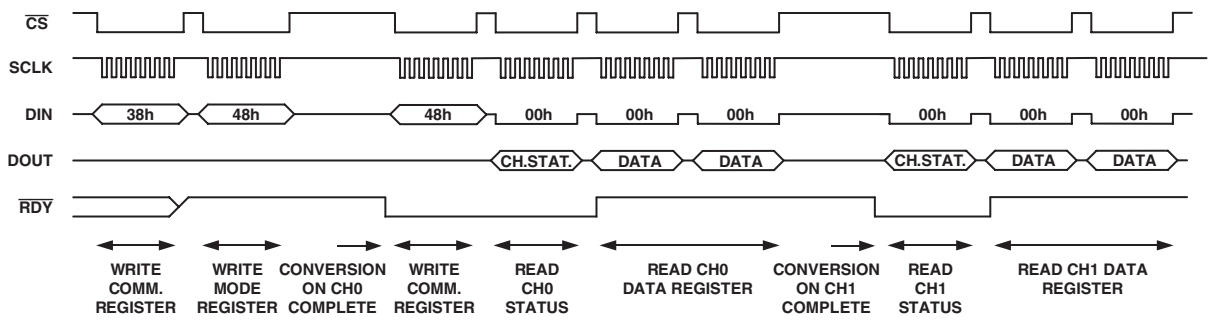


Figure 12. Continuous Conversion CH0 and CH1, Continuous Read

Continuous Read (Continuous Conversion) Mode
When the Continuous RD bit in the Mode register is set, the first write "48h" to the communication register starts the Continuous Read mode. As shown in Figure 12, subsequent accesses to the part sequentially reads the Channel Status and Data registers of the last completed conversion without any further configuration of the Communication register being required.

Note that the Continuous Conversion bit in the Mode register should be set when entering the Continuous Read mode.

Note that the Continuous Read mode is "Dump Mode" reading of the Channel Status and Data register regardless of the Dump bit value. Use the Channel bits in the Channel Status register to check/recognize which channel data is actually being shifted out.

Note that the last completed conversion result is being read. Therefore, the RDYFN bit in the I/O Port register should be 0, and reading the result should always start before the next conversion is completed.

The AD7738 will stay in Continuous Read mode as long as the DIN pin is low while the $\overline{CS}$ pin is low. Therefore, write 0 to the AD7738 while reading in Continuous Read mode. To exit Continuous Read mode, take the DIN pin high for at least 100 ns after a read is complete. (Write "80h" to the AD7738 to exit continuous reading.)

The Continuous RD bit in the Mode register is not changed by taking the DIN pin high. Therefore, the next write "48h" starts the Continuous Read mode again. To completely stop the continuous read mode, write to the Mode register to clear the Continuous RD bit.

CIRCUIT DESCRIPTION

The AD7738 is a sigma-delta A/D converter, intended for the measurement of wide dynamic range, low frequency signals in industrial process control, instrumentation, PLC, and DSC.

It contains a multiplexer, an input buffer, a sigma-delta (or charge-balancing) ADC, digital filter, clock oscillator, digital I/O port, and a serial communications interface.

Analog Front End
The AD7738 has nine analog input pins connected to the ADC through the internal multiplexer. The analog front end can be configured as eight single-ended inputs four differential inputs, or any combination of these. Selection of ADC inputs is determined via the COM0 and COM1 bits in the Channel Setup registers.

The AD7738 contains a wide bandwidth, fast settling time differential input buffer capable of driving the dynamic load of a high speed sigma-delta modulator. With the internal buffer enabled, the analog inputs feature relatively high input impedance. However, if chopping is enabled and/or when switching between channels, there is a dynamic current charging the capacitance of the multiplexer, capacitance of the pins, and any additional capacitance connected to the MUXOUT. In typical configurations with MUXOUT connected directly to the ADCIN, this capacitance could be approximately 20 pF. The AD7738 has been designed to provide adequate settling time after a multiplexer switch and before the actual sampling starts only if the analog inputs resistive source impedance does not exceed 10 kΩ.

An RC connected to the analog inputs may convert the dynamic charging currents to a dc voltage and cause additional gain or offset errors. The recommended low-pass RC filter on the AD7738 analog inputs is 20 Ω and 100 nF.

The multiplexer output and the ADC input are pinned out externally. This facilitates shared signal conditioning between the multiplexer and the ADC. Please note that if chop is enabled and/or when switching between channels, any circuit connected between MUXOUT and ADCIN should be fully settled within the settling time provided by the AD7738. See the Multiplexer, Conversion, and Data Output Timing section.

Σ-Δ ADC
The AD7738 core consists of a charge balancing sigma-delta modulator and a digital filter. The architecture is optimized for fast fully settled conversion. This allows for fast channel-to-channel switching while maintaining inherently excellent linearity, high resolution, and low noise.

Chopping
With chopping enabled, the multiplexer repeatedly reverses the ADC inputs. Every output data result is then calculated as an average of two conversions, the first with positive and the second with negative offset term included. This effectively removes any offset error of the input buffer and sigma-delta modulator, resulting in excellent dc offset and offset drift specifications.

Figure 13 shows the channel signal chain with chopping enabled.

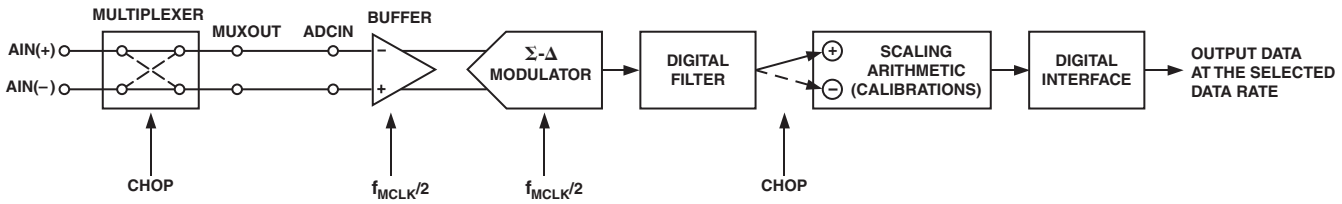


Figure 13. Channel Signal Chain Diagram with Chopping Enabled

Multiplexer, Conversion, and Data Output Timing
The specified "Conversion Time" includes one or two "Settling" and "Sampling" periods and a "Scaling" time.

With chopping enabled (Figure 14), a conversion cycle starts with a "Settling" time of 43 or 44 MCLK cycles (~7 µs with 6.144 MHz MCLK) to allow the circuits following the multiplexer to settle. Then the sigma-delta modulator samples the analog signals, and the digital filter processes the digital data stream. The "Sampling" time depends on FW, i.e., on the Channel Conversion Time register contents. After another "Settling" of 42 MCLK cycles (~6.8 µs), the "Sampling" time is repeated with a reversed (chopped) analog input signal. Then, during the "Scaling" time of 163 MCLK cycles (~26.5 µs), the two results from the digital filter are averaged, scaled using the Calibration registers, and written into the Channel Data register.

With chopping disabled (Figure 15), there is only one "Sampling" time preceded by a "Settling" time of 43 or 44 MCLK cycles and followed by a "Scaling" time of 163 MCLK cycles.

The $\overline{\text{RDY}}$ pin goes high during the "Scaling time" regardless of its previous state. The relevant RDY bit is set in the ADC Status register, and in the Channel Status register the $\overline{\text{RDY}}$ pin goes low when the Channel Data register is updated and the channel conversion cycle is finished. If in Continuous Conversion mode, the part will automatically continue with a conversion cycle on the next enabled channel.

Note, that every channel can be configured independently for conversion time and chopping mode. The overall cycle and effective per channel data rate depends on all enabled channel settings.

Frequency Response
The sigma-delta modulator runs at 1/2 of MCLK frequency, which is effectively the sampling frequency. Therefore, the Nyquist frequency is 1/4 of the MCLK frequency. The digital filter, in association with the modulator, features frequency response of a first order low-pass filter. The –3 dB point is close to the frequency of 1/Channel Conversion Time. The roll-off is –20 dB/dec up to the Nyquist frequency. If chopping is enabled, the input signal is resampled by chopping. Therefore, the overall frequency response features notches close to the frequency of 1/Channel Conversion Time. The top envelope is again the ADC response of –20 dB/dec.

The typical frequency response plots are in Figure 16. The plots are normalized to 1/Channel Conversion Time.

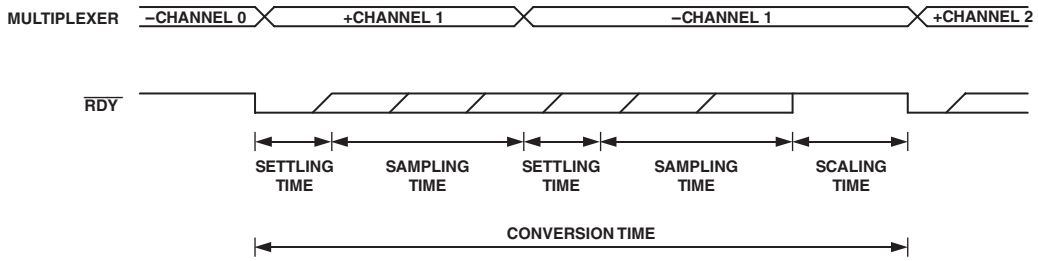


Figure 14. Multiplexer and Conversion Timing—Continuous Conversion on Several Channels with Chopping Enabled

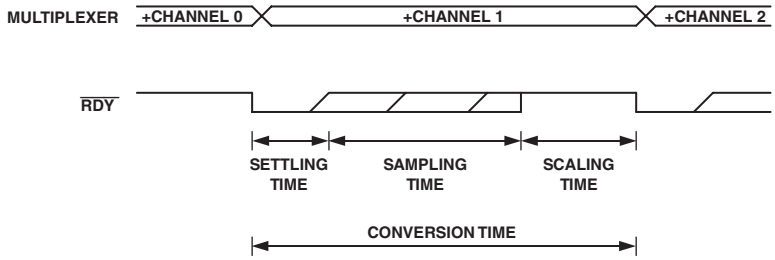
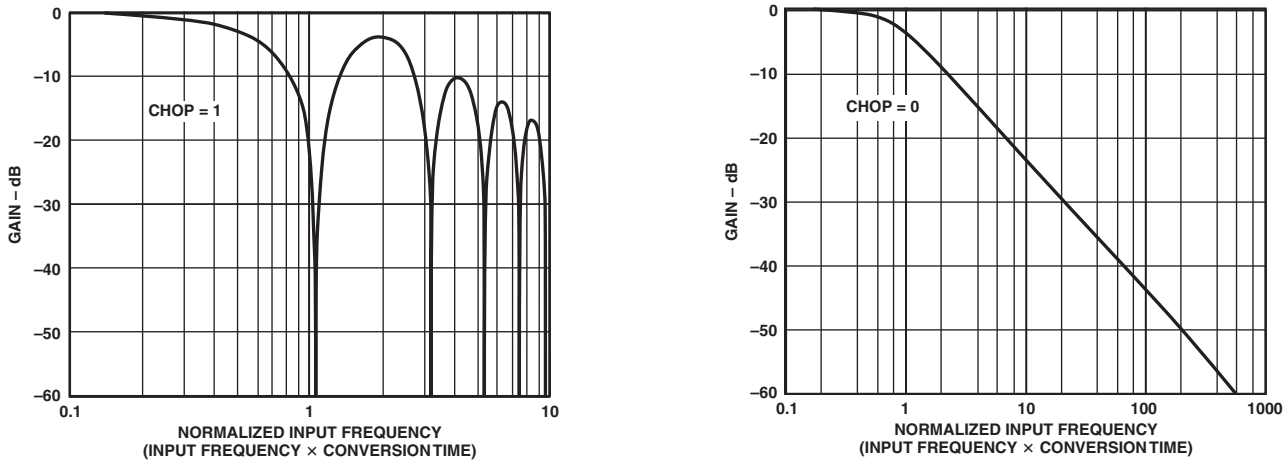


Figure 15. Multiplexer and Conversion Timing—Continuous Conversion on Several Channels with Chopping Disabled



a. Chopping Enabled

b. Chopping Disabled

Figure 16. Typical ADC Frequency Response

Analog Inputs Voltage Range

The absolute input voltage range with input the buffer enabled is restricted from AGND + 200 mV to AV_{DD} – 300 mV, which also places restrictions on the common-mode range. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded, otherwise there will be degradation in linearity performance.

The analog inputs on the AD7738 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages with respect to system ground on its analog inputs. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the respective AIN(–) input.

For example, if AINCOM is 2.5 V and CH0 is configured to measure AIN0 – AINCOM, 0 V to 1.25 V, the input voltage range on the AIN0 input is 2.5 V to 3.75 V. If CH0 is configured to measure AIN0 – AINCOM, ±1.25 V, the input voltage range on the AIN0 input is 1.25 V to 3.75 V.

Analog Inputs Extended Voltage Range

The AD7738 output data code span corresponds to the nominal input voltage range. However, the correct operation of the ADC is guaranteed within the min/max input voltage range.

When the CLAMP bit of the Mode register is set to 1, the Channel Data register will be digitally clamped either to all zeros or all ones when the analog input voltage goes outside the nominal input voltage range.

As shown in Tables XIII and XIV, when CLAMP = 0, the data reflect the analog input voltage outside the nominal voltage range. In this case, the SIGN and OVR bits in the Channel Status register should be considered along with the Data register value to decode the actual conversion result.

Table XIII. Input Voltage Range ±1.25 V, 16 Bits, CLAMP = 0

Input (V)	Data (Hex)	SIGN	OVR
+1.45000	147B	0	1
+1.25008	0001	0	1
+1.25004	0000	0	1
+1.25000	FFFF	0	0
+0.00004	8001	0	0
0.00000	8000	0	0
–0.00004	7FFF	1	0
–1.25000	0000	1	0
–1.25004	FFFF	1	1
–1.25008	FFFE	1	1
–1.45000	EB85	1	1

Table XIV. Input Voltage Range 0 V to 1.25 V, 16 Bits, CLAMP = 0

Input (V)	Data (Hex)	SIGN	OVR
1.45000	28F5	0	1
1.25004	0001	0	1
1.25002	0000	0	1
1.25000	FFFF	0	0
0.00002	0001	0	0
0.00000	0000	0	0
–0.00002	0000	1	1

Voltage Reference Inputs

The AD7738's reference inputs, REFIN(+) and REFIN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The nominal reference voltage for specified operation is 2.5 V. Both reference inputs feature a high impedance, dynamic load. Because the input impedance on each reference input is dynamic, external resistance/capacitance combinations may result in gain errors on the part.

The output noise performance outlined in Tables I to VI is for an analog input of 0 V and is unaffected by noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7738. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7738.

Recommended reference voltage sources for the AD7738 include the ADR421, AD780, REF43, and REF192. It is generally recommended to decouple the output of these references to further reduce the noise level.

Reference Detect

The AD7738 includes on-chip circuitry to detect if the part has a valid reference for conversions.

If the voltage between the REFIN(+) and REFIN(–) pins goes below the NOREF Trigger Voltage (0.5 V typ) and the AD7738 is performing conversion, the NOREF bit in the Channel Status register is set.

I/O Port

The AD7738 Pin $\overline{\text{SYNC}}$/P1 can be used as a general-purpose digital I/O pin or to synchronize the AD7738 with other devices in the system. When the SYNC bit in the I/O Port register is set and the $\overline{\text{SYNC}}$ pin is low, the AD7738 doesn't process any conversion. If it is put into single conversion mode, Continuous Conversion mode, or any Calibration mode, the AD7738 waits until the $\overline{\text{SYNC}}$ pin goes high and then starts operation. This allows the user to start conversion from a known point in time, i.e., the rising edge of the $\overline{\text{SYNC}}$ pin.

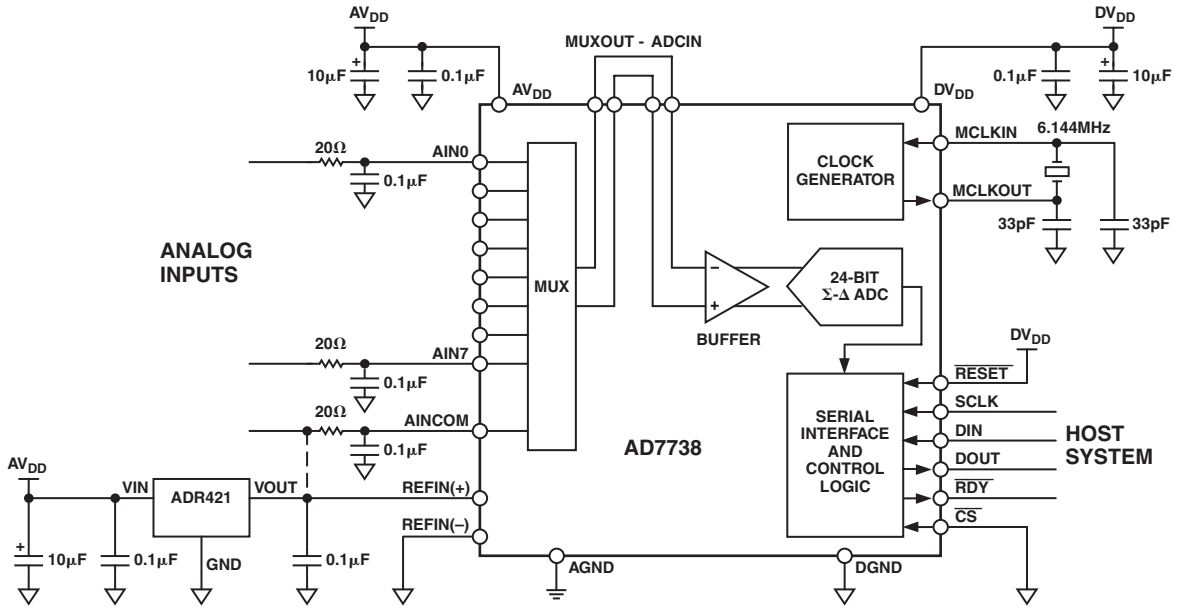


Figure 17. Typical Connection for the AD7738 Application

CALIBRATION

The AD7738 provides zero-scale self-calibration, and zero and full system calibration capability, which can effectively reduce the offset error and gain error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC Calibration Registers and the relevant Channel Calibration registers before being written to the Data register. See the equations shown below.

For unipolar ranges:

Data = ((ADC result – ADC ZS Cal. reg.) × ADC FS reg./200000h – Ch. ZS Cal. reg.) × Ch. FS Cal. reg./200000h

For bipolar ranges:

Data = ((ADC result – ADC ZS Cal. reg.) × ADC FS reg./400000h + 800000h – Ch. ZS Cal. reg.) × Ch. FS Cal. reg./200000h

Where the ADC result is in the range of 0 to FFFFFFh.

Note that the Channel ZS Calibration register has the format of a sign bit + 22 bits Channel offset value.

It is strongly recommended that the user does not change the ADC FS register.

To start any calibration, write the relevant mode bits to the AD7738 Mode register. After the calibration is complete, the contents of the corresponding Calibration registers are updated, all RDY bits in the ADC Status register are set, the $\overline{\text{RDY}}$ pin goes low, and the AD7738 reverts to Idle mode.

The calibration duration is the same as conversion time configured on the selected channel. The longer conversion time gives less noise and yields a more exact calibration. Therefore, use at least the default conversion time to initiate any calibration.

ADC Zero-Scale Self-Calibration

The ADC Zero-Scale Self-Calibration can effectively remove the offset error in Chopping Disabled mode. If repeated after a temperature change, it can also remove the offset drift error in Chopping Disabled mode.

The zero-scale self-calibration is performed on internally shorted ADC inputs. The negative Analog Input terminal on the selected channel is used to set the ADC ZS Calibration common mode. Therefore, either the negative terminal on selected differential pair or AINCOM on single-ended channel configuration should be driven to a proper commwon-mode voltage.

It is strongly recommended that the ADC ZS Calibration register should only be updated as part of a zero-scale self-calibration.

Per Channel System Calibration

If the per channel system calibrations are used, these should be initiated in the following order: first a Channel ZS System Calibration followed by a Channel FS System Calibration.

The System Calibration is affected by the ADC ZS and FS Calibration registers; therefore, if both Self-Calibration and System Calibration are used in a system, an ADC Self-Calibration cycle should be performed first followed by a System Calibration cycle.

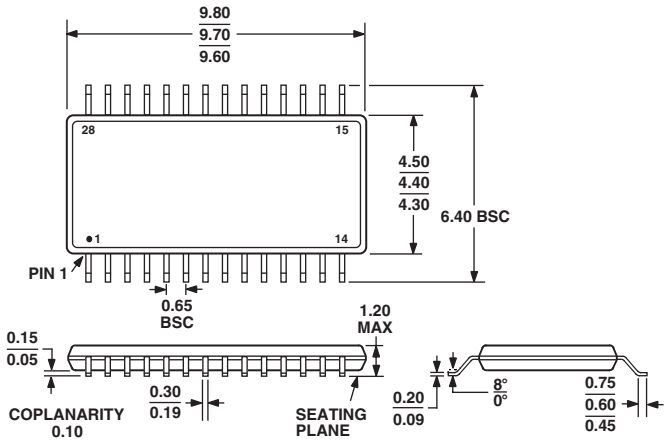
While executing a system calibration, the fully settled system zero-scale voltage signal or system full-scale voltage signal must be connected to the selected channel analog inputs.

The per channel Calibration registers can be read, stored, or modified and written back to the AD7738. Note, when writing the Calibration registers the AD7738 must be in the idle mode. Note that outside the specified calibration range, the calibration is possible but the performance may degrade. (See the System Calibration section in the specification pages of this data sheet.)

OUTLINE DIMENSIONS

28-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-28)

Dimensions shown in millimeters



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