CD74HC4024, CD74HCT4024

High Speed CMOS Logic
7-Stage Binary Ripple Counter

November 1997

Features

- Fully Static Operation
- Buffered Inputs
- Common Reset
- Negative Edge Clocking
- Typical f_{MAX} = 60 MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The Harris CD74HC4024 and CD74HCT4024 are 7-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.
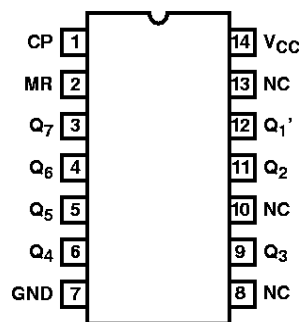
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC4024E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT4024M	-55 to 125	14 Ld SOIC	M14.15
CD74HC4024M	-55 to 125	14 Ld SOIC	M14.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

**CD74HC4024, CD74HCT4024
(PDIP, SOIC)
TOP VIEW**

```
        CP  [1      14]  VCC
        MR  [2      13]  NC
        Q7  [3      12]  Q1'
        Q6  [4      11]  Q2
        Q5  [5      10]  NC
        Q4  [6       9]  Q3
       GND  [7       8]  NC
```

File Number **1683.1**

Functional Diagram

CP — 1
MR — 2

12 — Q₁'
11 — Q₂
9 — Q₃
6 — Q₄
5 — Q₅
4 — Q₆
3 — Q₇
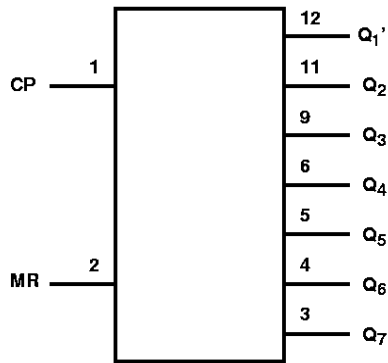
TRUTH TABLE

CP COUNT	MR	OUTPUT STATE
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

Logic Diagram

CP 1
MR 2
GND 7
V_CC 14

CP Q 1 Q1 / CP Q̄ / R̄
CP Q 2 / CP Q̄ / R̄
CP Q 3 / CP Q̄ / R̄
CP Q 4 / CP Q̄ / R̄
CP Q 5 / CP Q̄ / R̄
CP Q 6 / CP Q̄ / R̄
CP Q 7 / CP Q̄ / R̄

12 Q₁'
11 Q₂
9 Q₃
6 Q₄
5 Q₅
4 Q₆
3 Q₇

2
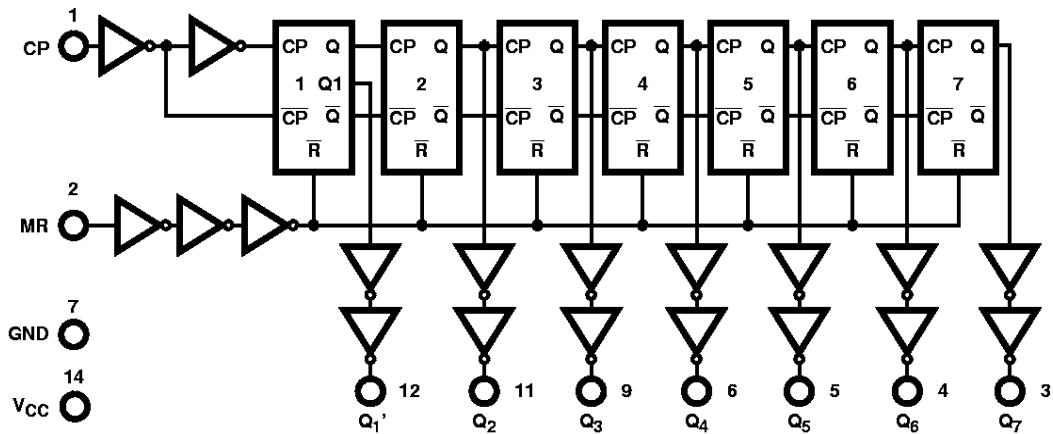
Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V

DC Input Diode Current, I_{IK}

    For $V_I < $ -0.5V or $V_I > V_{CC} + 0.5V$ . . . .±20mA

DC Output Diode Current, I_{OK}

    For $V_O < $ -0.5V or $V_O > V_{CC} + 0.5V$ . . . .±20mA

DC Output Source or Sink Current per Output Pin, I_O

    For $V_O > $ -0.5V or $V_O < V_{CC} + 0.5V$ . . . .±25mA

DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (^{O}C/W)

    PDIP Package 90

    SOIC Package. 175

Maximum Junction Temperature . . . . .150°C

Maximum Storage Temperature Range . . . .-65°C to 150°C

Maximum Lead Temperature (Soldering 10s). . . . . .300°C

    (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) . . . .-55°C to 125°C

Supply Voltage Range, V_{CC}

    HC Types . . . . .2V to 6V

    HCT Types . . . . .4.5V to 5.5V

DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}

Input Rise and Fall Time

    2V . . . . 1000ns (Max)

    4.5V. . . . . 500ns (Max)

    6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

3

CD74HC4024, CD74HCT4024

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
CP, MR	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C MIN	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES									
Maximum Input Pulse Frequency	f_{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	29	-	24	-	MHz
Input Pulse Width	t_W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Reset Removal Time	t_{REM}	2	50	-	65	-	75	-	ns
		4.5	10	-	13	-	15	-	ns
		6	9	-	11	-	13	-	ns

Prerequisite for Switching Specifications   (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25°C MIN	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Reset Pulse Width	t_W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
HCT TYPES									
Maximum Input Pulse Frequency	f_{MAX}	4.5	25	-	20	-	16	-	MHz
Input Pulse Width	t_W	4.5	20	-	25	-	30	-	ns
Reset Recovery Time	t_{REC}	4.5	10	-	13	-	15	-	ns
Reset Pulse Width	t_W	4.5	20	-	25	-	30	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
Propagation Delay Time (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	140	-	175	-	210	ns
CP to Q1' Output			4.5	-	-	28	-	35	-	42	ns
		C_L =15pF	5	-	11	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	24	-	30	-	36	ns
Q_n to $Q_n + 1$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
		C_L =15pF	5	-	6	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	13	-	13	-	19	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
			5	-	14	-	-	-	-	-	ns
			6	-	-	29	-	27	-	43	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	C_L =15pF	5	-	30	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Time (Figure 2)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
CP to Q1' Output		C_L =15pF	5	-	17	-	-	-	-	-	ns
Q_n to $Q_n + 1$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C_L =15pF	5	-	6	-	-	-	-	-	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C_L =15pF	5	-	17	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns   **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Output Transition	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	C_L =15pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	C_L =15pF	5	-	30	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per package.

5. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 fi/M)$ where: $M = 2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7$ f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.


Test Circuits and Waveforms
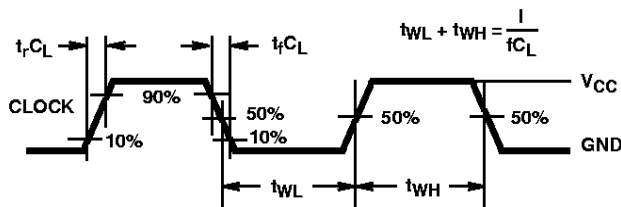
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
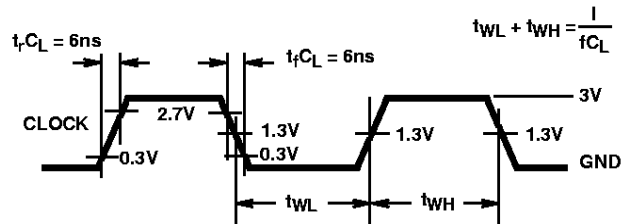
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
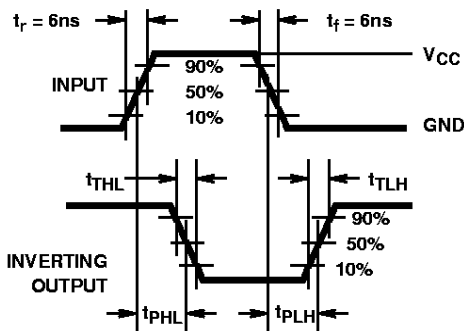
FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC
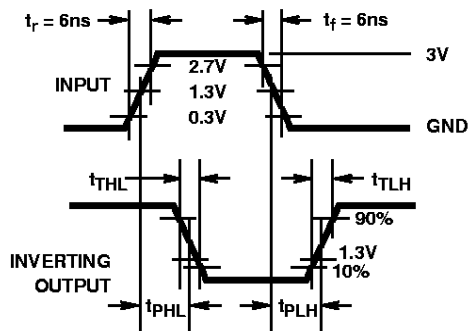
FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC