

# CD74HC126, CD74HCT126

## High Speed CMOS Logic Quad Buffer, Three-State

November 1997

### Features

- Three-State Outputs
- Separate Output Enable Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC126 and CD74HCT126 contain four independent three-state buffers, each having its own output enable input, which when "low" puts the output in the high-impedance state.

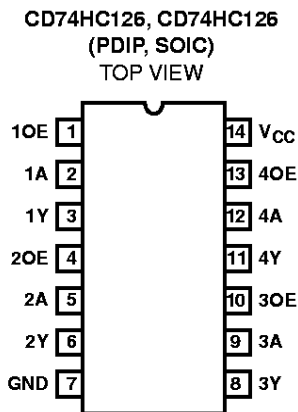
### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE    | PKG. NO. |
|-------------|------------------|------------|----------|
| CD74HC126E  | -55 to 125       | 14 Ld PDIP | E14.3    |
| CD74HCT126E | -55 to 125       | 14 Ld PDIP | E14.3    |
| CD74HC126M  | -55 to 125       | 14 Ld SOIC | M14.15   |
| CD74HCT126M | -55 to 125       | 14 Ld SOIC | M14.15   |

#### NOTES:

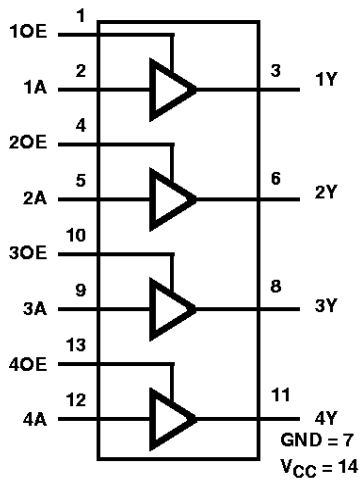
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout



# CD74HC126, CD74HCT126

## Functional Diagram

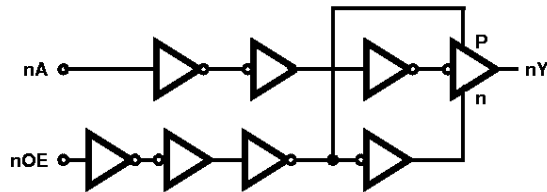


## TRUTH TABLE

| INPUTS |     | OUTPUTS |
|--------|-----|---------|
| nA     | nOE | nY      |
| H      | H   | H       |
| L      | H   | L       |
| X      | L   | Z       |

NOTE:  
 H = High Voltage Level  
 L = Low Voltage Level  
 X = Don't Care  
 Z = High Impedance, OFF State

## Logic Diagram



## CD74HC126, CD74HCT126

### Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                      | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$ .....                | $\pm 35mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....       | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ .....          | $\pm 70mA$  |

### Thermal Information

|  |   |
|--|---|
| Thermal Resistance (Typical, Note 3)           | $\theta_{JA}$ ( $^{\circ}C/W$ )           |
| PDIP Package .....                             | 90  |
| SOIC Package .....                             | 175                                       |
| Maximum Junction Temperature .....             | $150^{\circ}C$                            |
| Maximum Storage Temperature Range .....        | $-65^{\circ}C$ to $150^{\circ}C$          |
| Maximum Lead Temperature (Soldering 10s) ..... | $300^{\circ}C$<br>(SOIC - Lead Tips Only) |

### Operating Conditions

|   |                                  |
|---|----------------------------------|
| Temperature Range ( $T_A$ ) .....               | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$                  |                                  |
| HC Types .....                                  | 2V to 6V                         |
| HCT Types .....                                 | 4.5V to 5.5V                     |
| DC Input or Output Voltage, $V_I$ , $V_O$ ..... | 0V to $V_{CC}$                   |
| Input Rise and Fall Time                        |                                  |
| 2V .....  | 1000ns (Max)                     |
| 4.5V .....                                      | 500ns (Max)                      |
| 6V .....  | 400ns (Max)                      |

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

| PARAMETER                               | SYMBOL   | TEST CONDITIONS         |            | $V_{CC}$ (V) | 25 $^{\circ}C$ |     |           | -40 $^{\circ}C$ TO 85 $^{\circ}C$ |         | -55 $^{\circ}C$ TO 125 $^{\circ}C$ |         | UNITS   |
|---|----------|-------------------------|------------|--------------|----------------|-----|-----------|-----------------------------------|---------|------------------------------------|---------|---------|
|   |          | $V_I$ (V)               | $I_O$ (mA) |              | MIN            | TYP | MAX       | MIN                               | MAX     | MIN                                | MAX     |         |
| <b>HC TYPES</b>                         |          |                         |            |              |                |     |           |                                   |         |                                    |         |         |
| High Level Input Voltage                | $V_{IH}$ | -                       | -          | 2            | 1.5            | -   | -         | 1.5                               | -       | 1.5                                | -       | V       |
|   |          |                         |            | 4.5          | 3.15           | -   | -         | 3.15                              | -       | 3.15                               | -       | V       |
|   |          |                         |            | 6            | 4.2            | -   | -         | 4.2                               | -       | 4.2                                | -       | V       |
| Low Level Input Voltage                 | $V_{IL}$ | -                       | -          | 2            | -              | -   | 0.5       | -                                 | 0.5     | -                                  | 0.5     | V       |
|   |          |                         |            | 4.5          | -              | -   | 1.35      | -                                 | 1.35    | -                                  | 1.35    | V       |
|   |          |                         |            | 6            | -              | -   | 1.8       | -                                 | 1.8     | -                                  | 1.8     | V       |
| High Level Output Voltage<br>CMOS Loads | $V_{OH}$ | $V_{IH}$ or<br>$V_{IL}$ | -0.02      | 2            | 1.9            | -   | -         | 1.9                               | -       | 1.9                                | -       | V       |
|   |          |                         | -0.02      | 4.5          | 4.4            | -   | -         | 4.4                               | -       | 4.4                                | -       | V       |
|   |          |                         | -0.02      | 6            | 5.9            | -   | -         | 5.9                               | -       | 5.9                                | -       | V       |
| High Level Output Voltage<br>TTL Loads  | $V_{OH}$ | $V_{IH}$ or<br>$V_{IL}$ | -6         | 4.5          | 3.98           | -   | -         | 3.84                              | -       | 3.7                                | -       | V       |
|   |          |                         | -7.8       | 6            | 5.48           | -   | -         | 5.34                              | -       | 5.2                                | -       | V       |
| Low Level Output Voltage<br>CMOS Loads  | $V_{OL}$ | $V_{IH}$ or<br>$V_{IL}$ | 0.02       | 2            | -              | -   | 0.1       | -                                 | 0.1     | -                                  | 0.1     | V       |
|   |          |                         | 0.02       | 4.5          | -              | -   | 0.1       | -                                 | 0.1     | -                                  | 0.1     | V       |
|   |          |                         | 0.02       | 6            | -              | -   | 0.1       | -                                 | 0.1     | -                                  | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads   | $V_{OL}$ | $V_{IH}$ or<br>$V_{IL}$ | 6          | 4.5          | -              | -   | 0.26      | -                                 | 0.33    | -                                  | 0.4     | V       |
|   |          |                         | 7.8        | 6            | -              | -   | 0.26      | -                                 | 0.33    | -                                  | 0.4     | V       |
| Input Leakage Current                   | $I_I$    | $V_{CC}$ or<br>GND      | -          | 6            | -              | -   | $\pm 0.1$ | -                                 | $\pm 1$ | -                                  | $\pm 1$ | $\mu A$ |

## CD74HC126, CD74HCT126

### DC Electrical Specifications (Continued)

| PARAMETER   | SYMBOL          | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |          | UNITS   |
|---|-----------------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|----------|---------|
|   |                 | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX      |         |
| Quiescent Device Current  | $I_{CC}$        | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160      | $\mu A$ |
| Three-State Leakage Current   | $I_{OZ}$        | $V_{IL}$ or $V_{IH}$ | -          | 6            | -    | -   | $\pm 0.5$ | -             | $\pm 5$ | -              | $\pm 10$ | $\mu A$ |
| <b>HCT TYPES</b>  |                 |                      |            |              |      |     |           |               |         |                |          |         |
| High Level Input Voltage  | $V_{IH}$        | -                    | -          | 4.5 to 5.5   | 2    | -   | -         | 2             | -       | 2              | -        | V       |
| Low Level Input Voltage   | $V_{IL}$        | -                    | -          | 4.5 to 5.5   | -    | -   | 0.8       | -             | 0.8     | -              | 0.8      | V       |
| High Level Output Voltage<br>CMOS Loads                                 | $V_{OH}$        | $V_{IH}$ or $V_{IL}$ | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -        | V       |
| High Level Output Voltage<br>TTL Loads                                  |                 |                      | -6         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -        | V       |
| Low Level Output Voltage<br>CMOS Loads                                  | $V_{OL}$        | $V_{IH}$ or $V_{IL}$ | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1      | V       |
| Low Level Output Voltage<br>TTL Loads                                   |                 |                      | 6          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4      | V       |
| Input Leakage Current   | $I_I$           | $V_{CC}$ to GND      | 0          | 5.5          | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$  | $\mu A$ |
| Quiescent Device Current  | $I_{CC}$        | $V_{CC}$ or GND      | 0          | 5.5          | -    | -   | 8         | -             | 80      | -              | 160      | $\mu A$ |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4) | $\Delta I_{CC}$ | $V_{CC} - 2.1$       | -          | 4.5 to 5.5   | -    | 100 | 360       | -             | 450     | -              | 490      | $\mu A$ |
| Three-State Leakage Current   | $I_{OZ}$        | $V_{IL}$ or $V_{IH}$ | -          | 5.5          | -    | -   | $\pm 0.5$ | -             | $\pm 5$ | -              | $\pm 10$ | $\mu A$ |

NOTE:

4. For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

### HCT Input Loading Table

| INPUT   | UNIT LOADS |
|---------|------------|
| nA, nOE | 1          |

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360 $\mu A$  max at 25°C.

## CD74HC126, CD74HCT126

### Switching Specifications Input $t_r, t_f = 6\text{ns}$

| PARAMETER                                  | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|--|--------------------|---------------------|--------------|------|-----|---------------|----------------|-------|
|  |                    |                     |              | TYP  | MAX | MAX           | MAX            |       |
| <b>HC TYPES</b>                            |                    |                     |              |      |     |               |                |       |
| Propagation Delay Data to Outputs          | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 2            | -    | 100 | 125           | 150            | ns    |
|  |                    |                     | 4.5          | -    | 20  | 25            | 30             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 8    | -   | -             | -              | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6            | -    | 17  | 21            | 36             | ns    |
| Enable Delay Time                          | $t_{PZL}, t_{PZH}$ | $C_L = 50\text{pF}$ | 2            | -    | 125 | 155           | 190            | ns    |
|  |                    |                     | 4.5          | -    | 25  | 31            | 38             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 10   | -   | -             | -              | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6            | -    | 21  | 26            | 32             | ns    |
| Disabling Delay Time                       | $t_{PLZ}, t_{PHZ}$ | $C_L = 50\text{pF}$ | 2            | -    | 125 | 155           | 190            | ns    |
|  |                    | $C_L = 50\text{pF}$ | 4.5          | -    | 25  | 31            | 38             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 10   | -   | -             | -              | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6            | -    | 21  | 26            | 32             | ns    |
| Output Transition Times                    | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2            | -    | 60  | 75            | 90             | ns    |
|  |                    |                     | 4.5          | -    | 12  | 15            | 18             | ns    |
|  |                    |                     | 6            | -    | 10  | 13            | 15             | ns    |
| Input Capacitance                          | $C_I$              | -                   | -            | -    | 10  | 10            | 10             | pF    |
| Three-State Output Capacitance             | $C_O$              | -                   | -            | -    | 20  | 20            | 20             | pF    |
| Power Dissipation Capacitance (Notes 5, 6) | $C_{PD}$           | -                   | 5            | 30   | -   | -             | -              | pF    |
| <b>HCT TYPES</b>                           |                    |                     |              |      |     |               |                |       |
| Propagation Delay Time to Outputs          | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 24  | 30            | 36             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 9    | -   | -             | -              | ns    |
| Output Enable Time                         | $t_{PZL}, t_{PZH}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 25  | 31            | 38             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 10   | -   | -             | -              | ns    |
| Output Disabling Time                      | $t_{PLZ}, t_{PHZ}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 28  | 35            | 42             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 11   | -   | -             | -              | ns    |
| Output Transition Times                    | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 12  | 15            | 18             | ns    |
| Input Capacitance                          | $C_I$              | -                   | -            | -    | 10  | 10            | 10             | pF    |
| Three-State Output Capacitance             | $C_O$              | -                   | -            | -    | 20  | 20            | 20             | pF    |
| Power Dissipation Capacitance (Notes 5, 6) | $C_{PD}$           | -                   | 5            | 36   | -   | -             | -              | pF    |

**NOTES:**

5.  $C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.
6.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

Test Circuits and Waveforms

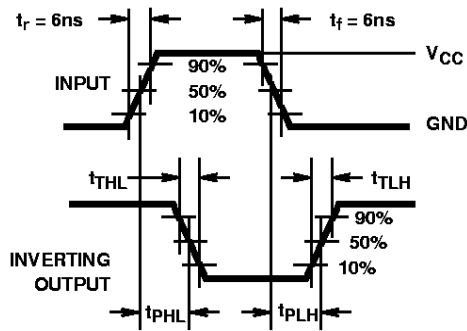


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

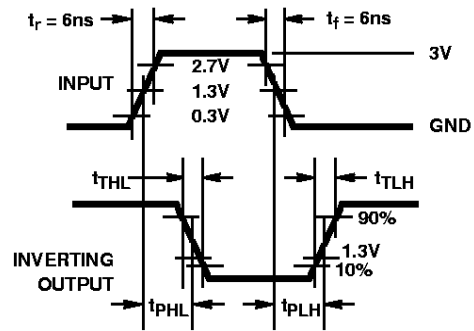


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

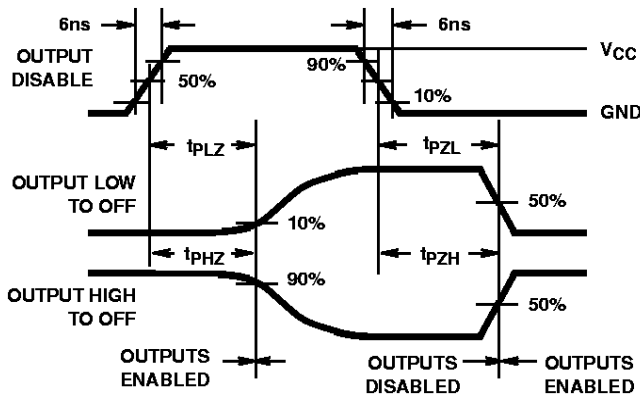


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

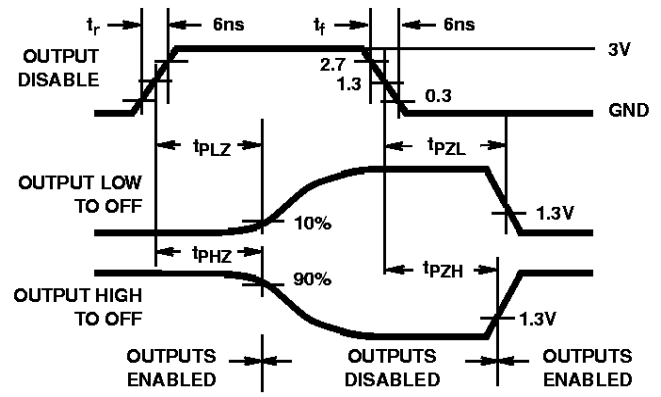
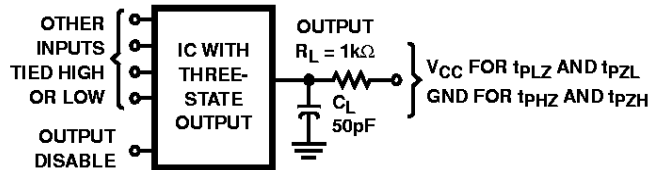


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT