CYWB0120AB

West Bridge® Antioch™-Lite USB/SD Controller

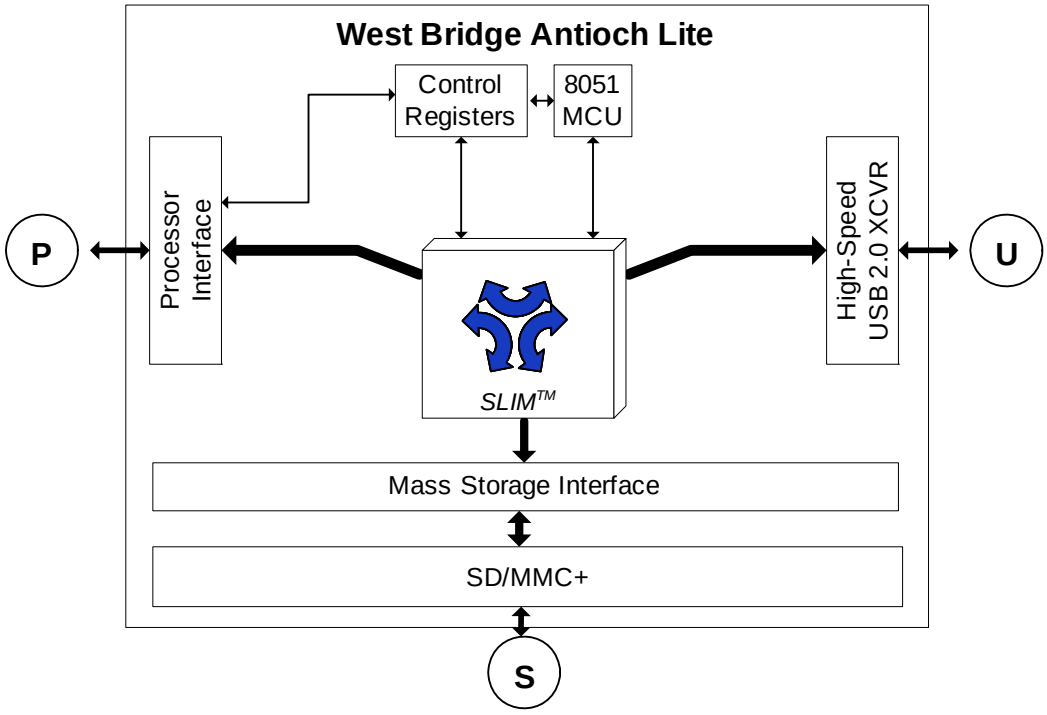
Features

- SLIM® architecture, enabling simultaneous and independent data paths between processor and USB, and between USB and mass storage
- High Speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB 2.0 transceiver, smart serial interface engine
  - 16 programmable endpoints
- Mass storage device supports MMC/MMC+/SD
- Memory mapped interface to main processor
- DMA slave support
- Ultra low power, 1.8 V core operation
- Low power modes
- Small footprint, 6x6 mm VFBGA
- Selectable clock input frequencies: 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Digital Cameras
- Portable Video Recorder

Logic Block Diagram



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Functional Overview

The SLIM® Architecture

The Simultaneous Link to Independent Multimedia (SLIM) architecture allows three different interfaces (the P-port, the S-port, and the U-port) to connect to one another independently.

With this architecture, using West Bridge® Antioch™ to connect a device to a PC through an USB does not disturb any of the functions of the device. It still accesses mass storage at the same time the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a PC accesses a mass storage device independent of the main processor, or enumerates access to both the mass storage and the main processor at the same time.

In a handset, this typically enables the user to use the phone as a thumb drive or download media files to the phone while still having full functionality available on the phone. The same phone functions as a modem to connect the PC to the web.

8051 Microprocessor

The 8051 microprocessor embedded in Antioch does basic transaction management for all the transactions between the P-port, the S-port, and the U-port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports SD and MMC devices at the S-port.

Configuration and Status Registers

The West Bridge Antioch device includes configuration and status registers that are accessible as memory mapped registers through the processor interface. The configuration registers enable the system to specify specific behavior from Antioch. For example, it masks some status registers from raising an interrupt. The status registers convey the status of the different parameters of Antioch, such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface supports both synchronous and asynchronous SRAM mapped memory accesses. This ensures straightforward electrical communications with the processor that also has other devices connected on a shared memory bus. Asynchronous accesses reach a bandwidth of up to 66.7 MBps. Synchronous accesses are performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Antioch. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers through the memory interface.

Access to these buffers is controlled by using either a DMA protocol or an interrupt to the main processor. These two modes are configured by the external processor.

As a DMA slave, Antioch generates a DMA request signal to signify to the main processor that it is ready to read from or write to a specific buffer. The external processor monitors this signal and polls Antioch for the specific buffers ready for read or write. It then performs the appropriate read or write operations on the buffer through the processor interface. This way, the external processor only deals with the buffers to access a multitude of storage devices connected to Antioch.

In the Interrupt mode, Antioch communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Antioch for the specific buffers ready for read or write and performs the appropriate read or write operations through the processor interface.

USB Interface (U-Port)

In accordance with the USB 2.0 specification, Antioch operates in Full Speed USB mode in addition to High Speed USB mode. The USB interface consists of the USB transceiver. The USB interface accesses and also is accessed by both the P-port and the S-port.

The Antioch USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Mass Storage Support (S-Port)

The S-port is configured to support SD/MMC+ port.

SD/MMC Port (S-Port)

Antioch Lite is configured to support MMC/SD. This interface supports:

- The MultiMediaCard System Specification, MMCA Technical Committee, Version 4.1
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004, and Version 2.0, November 9, 2005

West Bridge Antioch provides support for 1-bit and 4-bit SD cards: 1-bit, 4-bit, and 8-bit MMC, and MMC+. For the SD, MMC/MMC+ card, this block supports one card for one physical bus interface.

Antioch supports SD commands including the multisector program command that is handled by the API.

Clocking

Antioch allows either to connect a crystal between the XTALIN and XTALOUT balls or connect an external clock at the XTALIN ball. The power supply level at the crystal supply XVDDQ determines whether a crystal or a clock is provided. If XVDDQ is detected as 1.8 V, Antioch assumes that a clock input is provided. To connect a crystal, XVDDQ must be 3.3 V. Note that the clock inputs at 3.3 V level are not supported.

CYWB0120AB supports crystals only at 19.2, 24, and 26 MHz. At 48 MHz, only clock inputs are supported. Clock inputs are supported at all frequencies.

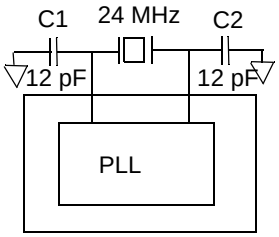
Antioch has an on-chip oscillator circuit that uses an external 19.2/24/26 MHz (±150 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 1 mW drive level
- 12 pF (5% tolerance) load capacitors[1]

Note

1. Specified as typical for 24 MHz frequency. Load capacitance varies with crystal vendor specifications and frequency used.

Figure 1. Capacitor.



12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four-layer FR4 PCA

Table 1. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
PN_100Hz	Input phase noise at 100 Hz offset	–	–75	dBc/Hz
PN_1k	Input phase noise at 1 kHz offset	–	–104	dBc/Hz
PN_10k	Input phase noise at 10 kHz offset	–	–120	dBc/Hz
PN_100k	Input phase noise at 100 kHz offset	–	–128	dBc/Hz
PN_1M	Input phase noise at 1 MHz offset	–	–130	dBc/Hz
	Duty cycle	30	70	%
	Maximum frequency deviation	–	150	ppm
	Overshoot	–	3	%
	Undershoot	–	–3	%

This on-chip PLL multiplies the 19.2/24/26/48 MHz frequency up to 480 MHz, as required by the transceiver/PHY. The internal counters divide it down for use as the 8051 clock. The 8051 clock frequency is 48 MHz. The XTALIN frequency is independent of the clock/data rate of the 8051 microprocessor or any of the device interfaces (including P-port and S-port). The internal PLL applies the proper clock multiply option depending on the input frequency.

For applications that use an external clock source to drive XTALIN, the XTALOUT Ball is left floating. The external clock is a square wave that conforms to high and low voltage levels mentioned in Table 3 on page 10 and the rise and fall time specifications in Figure 17 on page 20. The external clock source also stops high or low and is not toggling to achieve the lowest possible current consumption. The requirements for an external clock source are shown in Table 4 on page 11.

Power Domains

Antioch has multiple power domains that serve different purposes within the chip.

***VDDQ:** This refers to a group of five independent supply domains for the digital I/Os. The nominal voltage level on these supplies are 1.8 V, 2.5 V, or 3.3 V. Specifically, the three separate I/O power domains are:

- PVDDQ – P-port processor interface I/O
- SVDDQ – S-port SD interface I/O
- GVDDQ – Other miscellaneous I/O

UVDDQ: This is the 3.3 V nominal supply for the USB I/O and some analog circuits. It also supplies power to the USB transceiver.

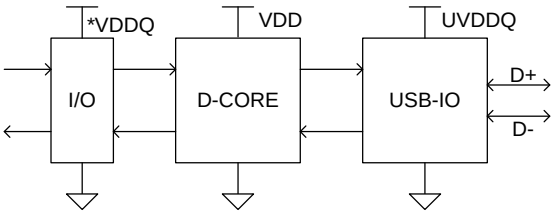
VDD33: This supply is required for the power sequence control circuits. For more information, see Table 2 on page 6.

VDD: This is the supply voltage for the logic core. The nominal supply voltage level is 1.8 V. This supplies the core logic circuits. The same supply is also used for AVDDQ.

AVDDQ: This is the 1.8 V supply for PLL and USB serializer analog components. The same supply is also used for V_{DD}. The maximum noise permitted on AVDDQ is 20 mV p-p.

XVDDQ: This is the clock I/O supply. 3.3 V for XTAL or 1.8 V for an external clock.

Figure 2. Antioch Power Supply Domains



Noise guideline for all supplies except AVDDQ is a maximum of 100 mV p-p. All I/O supplies of Antioch are ON when a system is active, even if Antioch is not used. The core V_{DD} is also deactivated at any time to preserve power, provided that there is a minimum impedance of 1 kΩ between the V_{DD} Ball and ground. All I/Os tristate when the core is disabled.

Power Supply Sequence

The power supplies are independently sequenced without damaging the part. All power supplies are up and stable before the device operates. If all supplies are not stable, the remaining domains are in low power (standby) mode.

Flexible IOs

Each of Antioch's ports operates between 1.8 V and 3.3 V with an adjustable slew rate for each port, and adjustable drive strength for each port for the I/Os. The slew rate and drive strength are controlled by registers.

Power Modes

In addition to the normal operating mode, Antioch contains several low power modes when normal operation is not required.

Normal Mode

In this mode, Antioch is fully functional. This is the mode, in which data transfer functions described in this datasheet are performed.

Suspend Mode

This mode is entered internally by 8051 (external processor only initiates entry into this mode through Mailbox commands). This mode is exited by the D+ bus going low, GPIO[0] going to a predetermined state, or by asserting CE# LOW.

In Suspend mode of Antioch:

- The clocks are shut off.
- All I/Os maintain their previous state.
- Core power supply is retained.
- The states of the Configuration registers, endpoint buffers, and the program RAM are maintained. All transactions are completed before Antioch enters Suspend mode (state of outstanding transactions are not preserved).
- The firmware resumes its operation from where it has suspended, because the program counter is not reset.
- The only inputs that are sensed are RESET#, GPIO[0], D+, and CE#. The last three are wakeup sources (each is individually enabled or disabled).
- Hard reset is performed by asserting the RESET# input and Antioch performs initialization.

Standby Mode

Standby mode is a low-power state. This is the lowest power mode of Antioch while still maintaining external supply levels. This mode is entered through the deassertion of the WAKEUP input ball or through internal register settings. It is exited by asserting the WAKEUP Ball if the mode is entered by deasserting the WAKEUP Ball. Exiting Standby mode is also accomplished by asserting CE# LOW or processor writes to Internal registers.

In this mode, the following characteristics apply:

- All Configuration register settings and program RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed in values. As a result, the external processor ensures that the required data is read before the Antioch is moved into this Standby mode.
  - The program counter is reset upon waking up from Standby mode.
  - All outputs are tri-stated (except UVALID), and I/O is placed in input only configuration. Values of IOs in Standby mode are listed in the Table 2 on page 6.
  - Core power supply is retained.
  - Hard reset is performed by asserting the RESET# input, and Antioch performs initialization.
  - PLL is disabled.

Core Power Down Mode

The core power supply V_{DD} is powered down in this mode. AVDDQ is tied to the same supply as V_{DD} and as a result, is also powered down. The endpoint buffers, configuration registers, and the program RAM do not maintain state. It is necessary to reload the firmware upon exiting from this mode. All VDDQ power supplies (except AVDDQ) must be on and not powered down in this mode. VDD33 must remain ON and the requirement of a minimum impedance of 1 kΩ between the V_{DD} ball and ground remains unchanged.

The Ball Assignment table for CYWB0120AB follows.[2, 3, 4]

Table 2. Ball Assignment

	VFBGA	Ball Name	I/O	Ball Description	Standby	Reset[5]	Power Domain
P-port	J2	CLK	I	Clock for P-port	–	–	PVDDQ VGND
	G1	CE#	I	Chip Select for P-port. Active LOW	–	–	
	H3	A[7]	I	Bit 7 of Address Bus for P-port	–	–	
	H2	A[6]	I	Bit 6 of Address Bus for P-port	–	–	
	H1	A[5]	I	Bit 5 of Address Bus for P-port	–	–	
	J3	A[4]	I	Bit 4 of Address Bus for P-port	–	–	
	J1	A[3]	I	Bit 3 of Address Bus for P-port	–	–	
	K3	A[2]	I	Bit 2 of Address Bus for P-port	–	–	
	K2	A[1]	I	Bit 1 of Address Bus for P-port	–	–	
	K1	A[0]	I	Bit 0 of Address Bus for P-port	–	–	
	G2	DQ[15]	I/O	Bit 15 of Data Bus for P-port	Z	Z	
	G3	DQ[14]	I/O	Bit 14 of Data Bus for P-port	Z	Z	
	F1	DQ[13]	I/O	Bit 13 of Data Bus for P-port	Z	Z	
	F2	DQ[12]	I/O	Bit 12 of Data Bus for P-port	Z	Z	
	F3	DQ[11]	I/O	Bit 11 of Data Bus for P-port	Z	Z	
	E1	DQ[10]	I/O	Bit 10 of Data Bus for P-port	Z	Z	
	E2	DQ[9]	I/O	Bit 9 of Data Bus for P-port	Z	Z	
	E3	DQ[8]	I/O	Bit 8 of Data Bus for P-port	Z	Z	
	D1	DQ[7]	I/O	Bit 7 of Data Bus for P-port	Z	Z	
	D2	DQ[6]	I/O	Bit 6 of Data Bus for P-port	Z	Z	
	D3	DQ[5]	I/O	Bit 5 of Data Bus for P-port	Z	Z	
	C1	DQ[4]	I/O	Bit 4 of Data Bus for P-port	Z	Z	
	C2	DQ[3]	I/O	Bit 3 of Data Bus for P-port	Z	Z	
	C3	DQ[2]	I/O	Bit 2 of Data Bus for P-port	Z	Z	
	B1	DQ[1]	I/O	Bit 1 of Data Bus for P-port	Z	Z	
	B2	DQ[0]	I/O	Bit 0 of Data Bus for P-port	Z	Z	
	A1	ADV#	I	Address Valid for P-port. Valid during asynchronous mode. ADV# deassertion causes to latch the address.	–	–	
	B3	OE#	I	Output Enable. Controls the data bus output drive. Ignored during write cycle. Active LOW.	–	–	
	A2	WE#	I	Write Enable. Signals a read (HIGH) or write (LOW) access cycle.	–	–	
	A3	INT#	O	Interrupt Request. Assertion indicates that an interrupt event has occurred. Active LOW.	Z	Z	
	A4	DRQ#	O	DMA Request. Assertion indicates to Processor that it is ready to read or write one or more endpoints. It reflects register CY_AN_MEM_P0_DRQ EPnDRQ assertions. Active LOW or HIGH (programmable).	Z	Z	
	B4	DACK#	I	DMA Acknowledgement. Assertion indicates DMA acknowledgement from processor. Is configured in ACK mode (asserted throughout DMA transfer) or EOB mode (pulsed at end of DMA transfer). Active LOW or HIGH (programmable).	–	–	

Notes
2. Unused inputs: Must be connected to HIGH/VDD or LOW/GND (negligible difference in current drawn) logic level, through a single 10 K pull-up resistor. The only exceptions are WAKEUP, SDCFG and CLK. WAKEUP is tied HIGH for normal operation.CLK is tied LOW for asynchronous P-port operation.
3. Unused I/Os: For lowest leakage, unused I/Os must be connected to a HIGH logic level. It is recommended that connection to the power supply is through a single 10 kΩ pull-up resistor for all unused I/Os.
4. No Antioch balls have internal pull-up or pull-down resistors. Input/output balls may require external pull-up or pull-down resistors depending on the application. The pull-up resistors used to indicate speed capability on the USB are included in Antioch and need not be connected externally.
5. The Reset column indicates the state of signals during reset (RESET# asserted). The Standby column indicates signal state during Standby (low power operating mode through WAKEUP deassertion) or core V_{DD} deactivation.

Table 2. Ball Assignment (continued)

	VFBGA	Ball Name	I/O	Ball Description	Standby	Reset[5]	Power Domain
S-port	G9	SD_D[7]	I/O	Serve as SD_D[7] for SD port	Z	Z	SVDDQ VGND
	G10	SD_D[6]	I/O	Serve as SD_D[6] for SD port	Z	Z	
	F9	SD_D[5]	I/O	Serve as SD_D[5] for SD port	Z	Z	
	F10	SD_D[4]	I/O	Serve as SD_D[4] for SD port	Z	Z	
	E9	SD_D[3]	I/O	Serve as SD_D[3] for SD port	Z	Z	
	E10	SD_D[2]	I/O	Serve as SD_D[2] for SD port	Z	Z	
	D9	SD_D[1]	I/O	Serve as SD_D[1] for SD port	Z	Z	
	D10	SD_D[0]	I/O	Serve as SD_D[0] for SD port	Z	Z	
	F8	SD_CLK	O	Clock output for the SD interface. Frequency is changed and clock is disabled through firmware control.	Z	Z	
	G8	SD_CMD	I/O	SD Command/Response Ball.	Z	Z	
	H8	SD_POW	O	SD Power Control. This GPIO is used to control SD/MMC card power FET if present. HIGH indicates on, LOW indicates off.	Z	Z	
	H10	SD_WP	I	SD Write Protection Detection. Connected to GPIO for firmware detection. HIGH indicates that the device connected to the SD port has write protect enabled.	–	–	
	K7	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	Z	Z	SVDDQ VGND
	K8	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	J8	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	K9	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	J9	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	H9	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	K10	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	J10	SD_RSV	I/O	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	K6	NC	O	Left floating	Z	Z	
	J6	NC	O	Left floating	Z	Z	
	J5	NC	O	Left floating	Z	Z	
	K4	NC	O	Left floating	Z	Z	
	H6	NC	O	Left floating	Z	Z	
	J7	NC	O	Left floating	Z	Z	
	J4	SD_RSV	I	Connect to SVDDQ with 10 K pull-up resistor	–	–	
	K5	NC	O	Left floating	Z	Z	
U-port	A5	D+	I/O/Z	USB D+	Z	Z	UVDDQ UVSSQ
	A6	D–	I/O/Z	USB D–	Z	Z	
	A7	UVALID	O	External USB Switch Control. Reflects value of register CY_AN_MEM_PMU_UPDATE.UVALID.	Low	Low	
Others	A8	XTALIN	I	Input for either crystal or clock signal. XVDDQ is 3.3 V for crystal input; XVDDQ is 1.8 V for clock input.	–	–	XVDDQ VGND
	B8	XTALOUT[6]	O	Output to connect to feedback input of crystal. Is left floating when external clock at XTALIN.	Z	Z	
	C10	RESET#	I	Reset. Asserted to place Antioch into reset mode and subsequent initialization. Active LOW.	–	–	GVDDQ VGND
	B10	RESETOUT	O	Reset Out. Deasserted LOW when RESET# is asserted LOW. Asserted HIGH after RESET# is deasserted and initialization is complete. Reflects value of RSTCMPT bit.	Z	Low	
	C9	GPIO[1]	I/O	General purpose input/output	Z	Z	
	D8	GPIO[0]	I/O	General purpose input/output.GPIO[0] is used for SD Card Detect with firmware detection. LOW indicates card is inserted.	Z	Z	
	C7	WAKEUP[7]	I	Wake Up Signal. 1 = normal operation, 0 = low power “sleep” mode. Is asserted for Antioch to initialize.	–	–	

Notes
6. XTALOUT is driven HIGH during Standby mode. XTALOUT operates the same during RESET# assertion and Normal mode: fixed HIGH when XVDDQ is 1.8 V (ext clock) and actively toggles when XVDDQ is 3.3 V (crystal).
7. When RESET# is asserted, the device enters reset state and WAKEUP is ignored.

Table 2. Ball Assignment (continued)

	VFBGA	Ball Name	I/O	Ball Description	Standby	Reset[5]	Power Domain
Config	C5	XTALSLC[1]	I	Clock Select. For CYWB0120AB, XTALSLC[1:0] is decoded as: 00 = 19.2 MHz, 01 = 24 MHz, 10 = 48 MHz, 11 = 26 MHz.	–	–	**GVDDQ VGND**
	C4	XTALSLC[0]	I	Clock Select. For CYWB0120AB, XTALSLC[1:0] is decoded as: 00 = 19.2 MHz, 01 = 24 MHz, 10 = 48 MHz, 11 = 26 MHz.	–	–	
	C6	SDCFG	-	S-port Configuration. Must be set to ‘1’	–	–	
	E8	TEST[2]	I	Test mode selection. Is tied to VGND for normal operation (CMOS level inputs).	–	–	
	C8	TEST[1]	I	Test mode selection. Is tied to VGND for normal operation (CMOS level inputs).	–	–	
	D7	TEST[0]	I	Test mode selection. Is tied to VGND for normal operation (CMOS level inputs).	–	–	
Power	D4, H4	PVDDQ	Power	Power for P-port I/O. 1.8 V, 2.5 V, or 3.3 V nominal.	–	–	
	H5	SVDDQ	Power	Power for SD port I/O. 1.8 V, 2.5 V, or 3.3 V nominal.	–	–	
	B5	UVDDQ	Power	Power for USB I/O. 3.3 V nominal.	–	–	
	H5, H7	SVDDQ	Power	Power for SD port	–	–	
	D6	GVDDQ	Power	Power for miscellaneous I/O. 1.8 V, 2.5 V, or 3.3 V nominal.	–	–	
	B9	AVDDQ	Power	Power for internal PLL and USB serializer. 1.8 V nominal.	–	–	
	B7	XVDDQ	Power	Power for crystal or clock I/O. 1.8 V (clock) or 3.3 V (crystal) nominal.	–	–	
	D5, G4, G5, G6, G7, F7	VDD	Power	Power for core. 1.8 V nominal.	–	–	
	A10	VDD33[8]	Power	Power sequence control supply. 3.3 V nominal.	–	–	
	B6	UVSSQ	Power	Ground for all USB	–	–	
	A9	AVSSQ	Power	Ground for PLL	–	–	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Ground for core	–	–	

Note

8. VDD33: In CYWB0120AB, the Ball is no-connect internally. It handles power sequence control in future West Bridge products. When migrating to Astoria, it is connected to the highest supply to the device. If USB is used, for example, then VDD33 is connected to nominal 3.3 V (because 3.3 V is required for USB). VDD33 is always supplied in Astoria.

Figure 3. CYWB0120AB 100 VFBGA

Top View

	1	2	3	4	5	6	7	8	9	10	
A	ADV#	WE#	INT#	DRQ#	D+	D-	UVALID	XTALIN	AVSSQ	VDD33	A
B	DQ[1]	DQ[0]	OE#	DACK#	UVDDQ	UVSSQ	XVDDQ	XTALOUT	AVDDQ	RESETOUT	B
C	DQ[4]	DQ[3]	DQ[2]	XTALSLC[0]	XTALSLC[1]	SDCFG	WAKEUP	TEST[1]	GPIO[1]	RESET#	C
D	DQ[7]	DQ[6]	DQ[5]	PVDDQ	VDD	GVDDQ	TEST[0]	GPIO[0]	SD_D[1]	SD_D[0]	D
E	DQ[10]	DQ[9]	DQ[8]	VGND	VGND	VGND	VGND	TEST[2]	SD_D[3]	SD_D[2]	E
F	DQ[13]	DQ[12]	DQ[11]	VGND	VGND	VGND	VDD	SD_CLK	SD_D[5]	SD_D[4]	F
G	CE#	DQ[15]	DQ[14]	VDD	VDD	VDD	VDD	SD_CMD	SD_D[7]	SD_D[6]	G
H	A[5]	A[6]	A[7]	PVDDQ	SVDDQ	NC	SVDDQ	SD_POW	SD_RSV	SD_WP	H
J	A[3]	CLK	A[4]	SD_RSV	NC	NC	NC	SD_RSV	SD_RSV	SD_RSV	J
K	A[0]	A[1]	A[2]	NC	NC	NC	SD_RSV	SD_RSV	SD_RSV	SD_RSV	K
	1	2	3	4	5	6	7	8	9	10	

POWER DOMAIN KEY	
	UVDDQ
	GVDDQ
	SVDDQ
	VGND
	PVDDQ

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Supplied (Industrial) ..... –40 °C to +85 °C

Supply Voltage to Ground Potential

VDD, AVDDQ .....–0.5 V to +2.0 V

GVDDQ, PVDDQ, SVDDQ, UVDDQ and VDD33 and XVDDQ .....–0.5 V to +4.0 V

DC Input Voltage to Any Input Ball .....1.89 V to 3.6 V

(Depends on I/O supply voltage. Inputs are not over voltage tolerant)

DC Voltage Applied to Outputs in High Z State ..... –0.5 V to VDDQ+0.5 V

Static Discharge Voltage (ESD) from JESD22-A114> 2,000 V

Latch-Up Current .....> 200 mA

Maximum Output Short Circuit Current for all I/O Configurations. (Vout = 0 V)[9] ..... –100 mA

Operating Conditions

T_A (Ambient Temperature Under Bias) Industrial ..... –40 °C to +85 °C

VDD, AVDDQ Supply Voltage .....1.7 V to 1.9 V

UVDDQ Supply Voltage.....3.0 V to 3.6 V

PVDDQ, GVDDQ, SVDDQ Supply Voltage.....1.7 V to 3.6 V

XVDDQ (Crystal I/O) Supply Voltage .....3.0 V to 3.6 V

XVDDQ (Ext. Clock I/O) Supply Voltage .....1.7 V to 1.9 V

DC Characteristics

Table 3. DC Specifications for All Voltage Supplies

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDD	Core voltage supply		1.7	1.8	1.9	V
AVDDQ	Analog voltage supply		1.7	1.8	1.9	V
XVDDQ	Crystal voltage supply		3.0	3.3	3.6	V
XVDDQ	Clock voltage supply		1.7	1.8	1.9	V
PVDDQ[11]	Processor interface I/O		1.7	1.8, 2.5, 3.3	3.6	V
GVDDQ[11]	Miscellaneous I/O voltage supply		1.7	1.8, 2.5, 3.3	3.6	V
SVDDQ[10,11]	S-port SD I/O voltage supply		1.7	1.8, 2.5, 3.3	3.6	V
UVDDQ[13]	USB voltage supply		3.0	3.3	3.6	V
VDD33	Power sequence control supply		3.0	3.3	3.6	V
V_{IH1}[12]	Input HIGH voltage 1	All ports except USB, 2.0 V ≤ V_{CC} ≤ 3.6 V	0.625*V_{CC}		V_{CC} + 0.3	V
V_{IH2}[12]	Input HIGH voltage 2	All ports except USB, 1.7 V ≤ V_{CC} < 2.0 V	V_{CC} – 0.4		V_{CC} + 0.3	
V_{IL}	Input LOW voltage		–0.3		0.25*V_{CC}	V
V_{OH}	Output HIGH voltage	I_{OH}(MAX) = –0.1 mA	0.9*V_{CC}			V
V_{OL}	Output LOW voltage	I_{OL}(MIN) = 0.1 mA			0.1*V_{CC}	V
I_{IX}	Input leakage current	All I/O signals held at VDDQ	–1		1	µA
I_{OZ}	Output leakage current	All I/O signals held at VDDQ	–1		1	µA
I_{CC} Core	Operating current of core voltage supply (VDD) and analog voltage supply (AVDDQ)	Outputs tristated			110	mA

Notes

9. Do not test more than one output at a time. Duration of the short circuit does not exceed 1 second. Tested initially, and after any redesign or process changes, may affect these parameters.
10. The SVDDQ I/O voltage is dynamically changed (for example, from high range to low range) as long as the supply voltage undershoot does not surpass the lower minimum voltage limit. SVDDQ levels for SD modes: 2.0 V–3.6 V, MMC modes: 1.7 V–3.6 V.
11. Interfaces with a voltage range are adjustable with respect to the I/O voltage and thus support multiple I/O voltages.
12. V_{CC} = pertinent VDDQ value.
13. When U-port is in a disabled state, UVDDQ goes down to 2.4 V, provided UVDDQ is still the highest supply voltage level.

Table 3. DC Specifications for All Voltage Supplies (continued)

Parameter	Description	Conditions		Min	Typ	Max	Unit
I_{CC} Crystal	Operating current of crystal voltage supply (XVDDQ)[16]	XTALOUT Floating				5	mA
I_{CC} USB	Operating current of USB voltage supply (UVDDQ)[16]	Operating and terminated for High Speed mode				25	mA
I_{SB1}	Total standby current of Antioch when device is in suspend mode	1. *VDDQ = 3.3 V Nominal (3.0–3.6 V) 2. Outputs and Bidirs High or Floating[15] 3. XTALOUT Floating 4. D+ Floating (no current drawn through internal 1.5 kΩ pull-up), D– Grounded, UVALID Driven LOW 5. Device in Suspend Mode			250[14]	2500	µA
I_{SB2}	Total standby current of Antioch when device is in standby mode	1. *VDDQ = 3.3 V Nominal (3.0–3.6 V) 2. Outputs and Bidirs High or Floating[15] 3. XTALOUT Floating 4. D+ Floating, D– Grounded, UVALID Driven LOW	25 °C			45	µA
			85 °C			290	
I_{SB3}	Total standby current of Antioch when device is in core power-down mode	1. Outputs and Bidirs High or Floating[15] 2. XTALOUT Floating 3. D+ Floating, D– Grounded, UVALID Driven LOW 4. Core Powered Down	25 °C			25	µA
			85 °C			139	

Table 4. Capacitance

Parameter	Description	Conditions	Typ	Max	Unit
C_{IN}	Input Ball Capacitance, Except D+/D–	TA = 25 °C, f = 1 MHz, $V_{CC} = V_{CCIO}$		9	pF
	Input Ball Capacitance, D+/D–			15	
C_{OUT}	Output Ball Capacitance			10	pF

USB Transceiver

USB 2.0 compliant in full speed and high speed modes.

Notes
14. Isb1 typical value is not a maximum specification but a typical value. Isb1 maximum current value specified for 85 °C.
15. The Outputs/Bidirs that are forced low in Standby mode increases I/O supply standby current beyond specified value.
16. Active Current Conditions:
    -UVDDQ: USB transmitting 50% of the time, receiving 50% of the time.
    -PVDDQ/SVDDQ/GVDDQ: Active Current Depends on IO activity, bus load, and supply level.
    -XVDDQ: Assume highest frequency clock (48 MHz) or crystal (26 MHz).

AC Characteristics

USB Transceiver

USB 2.0 compliant in full speed and high speed modes.

P-Port Interface

Asynchronous Mode Timing Parameters

Table 5. Asynchronous Mode Timing Parameters

Parameter	Description	Min	Max	Unit
Read Timing Parameters				
tAA	Address to data valid	–	30	ns
tOH	Data output hold from address change	3	–	ns
tEA	Chip enable to data valid	–	30	ns
tAADV	ADV# to data valid access time	–	30	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2[18]	–	ns
tCVS	CE# Low setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15[17]	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tOE	OE# LOW to data valid	–	22.5	ns
tOLZ	OE# LOW to Low Z	3	–	ns
tOHZ	OE# HIGH to High Z	0	22.5	ns
tLZ	CE# LOW to Low Z	3	–	ns
tHZ	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	0	–	ns
tADVS	ADV# setup to write start	0	–	ns
tWP	WE# pulse width	22	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2[18]	–	ns
tCVS	CE# LOW setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15[17]	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tVS	ADV# LOW to End of Write	30	–	ns
tDW	Data setup to write end	18	–	ns
tDH	Data hold from write end	0	–	ns
tWHZ	WE# Low to DQ High Z output	–	22.5	ns
tWLZ	WE# High to DQ Low Z output	3	–	ns

Notes
17. In applications where access cycle time is at least 60 ns, t_{VPH} is relaxed to 12 ns.
18. In applications where back-to-back accesses are not performed on different endpoint addresses, the minimum t_{AVH} specification is relaxed to 0 ns.

Figure 4. Asynchronous Single Read Timing

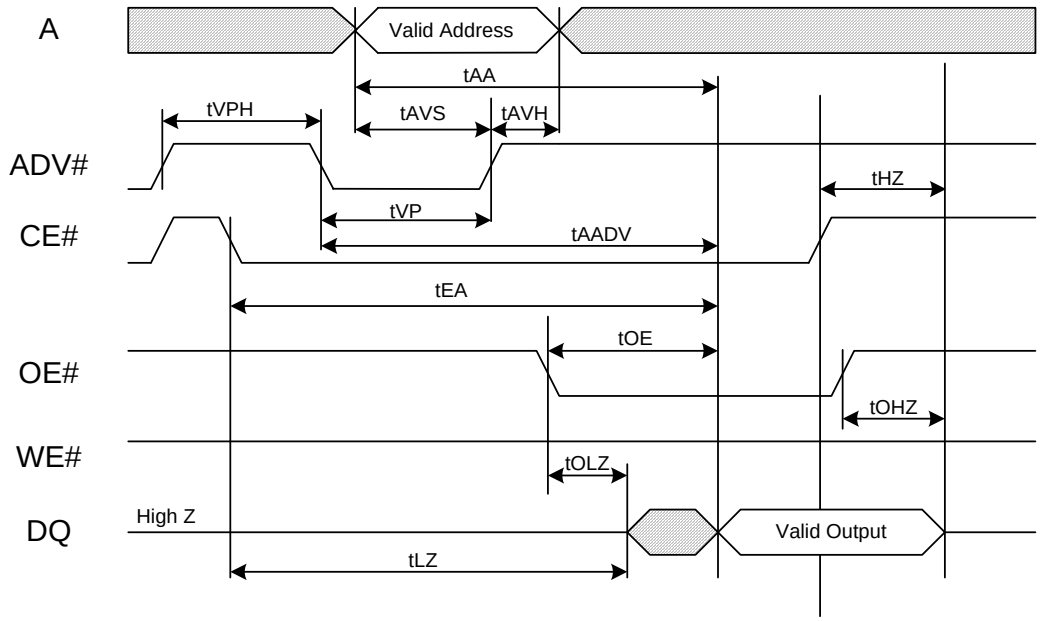


Figure 5. Asynchronous Back-to-Back Read Timing

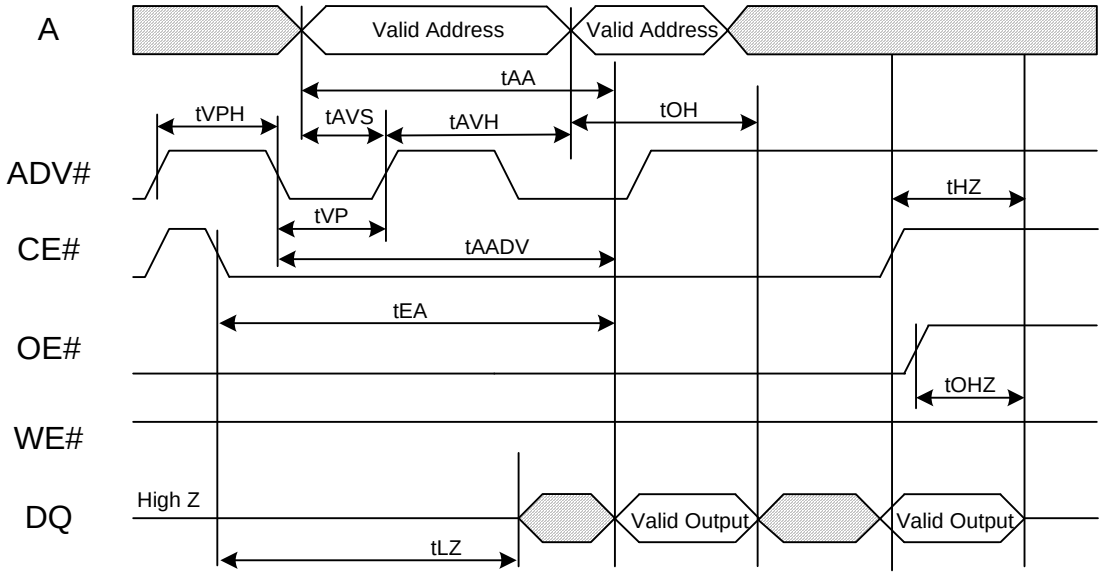


Figure 6. Asynchronous Back-to-Back Write Timing

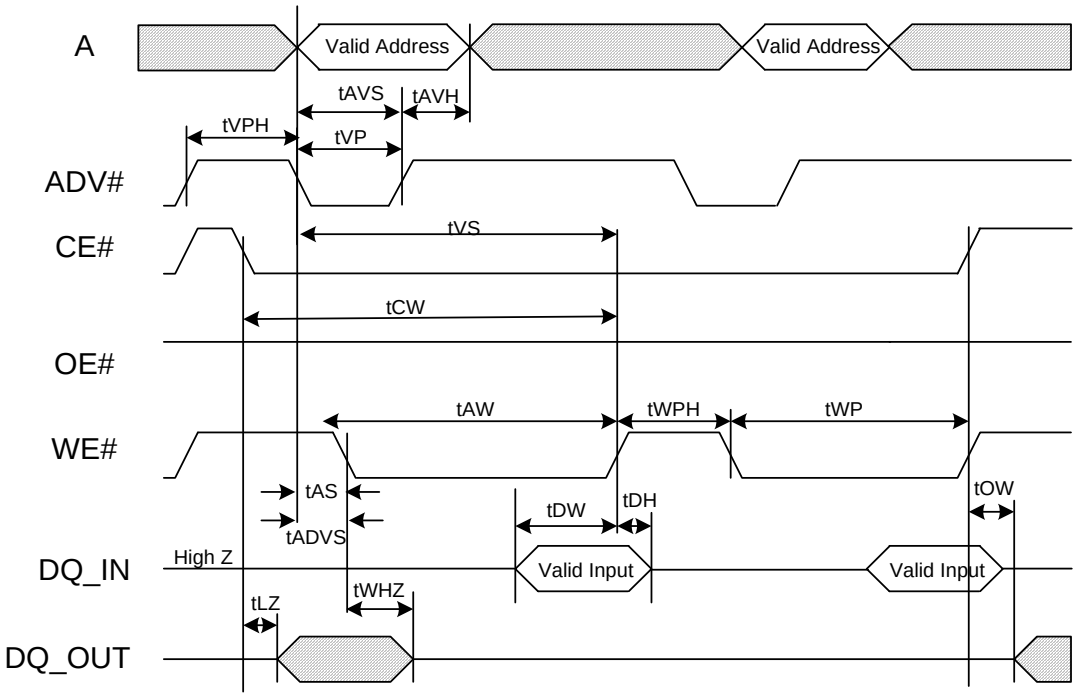


Figure 7. Asynchronous Read to Write Timing

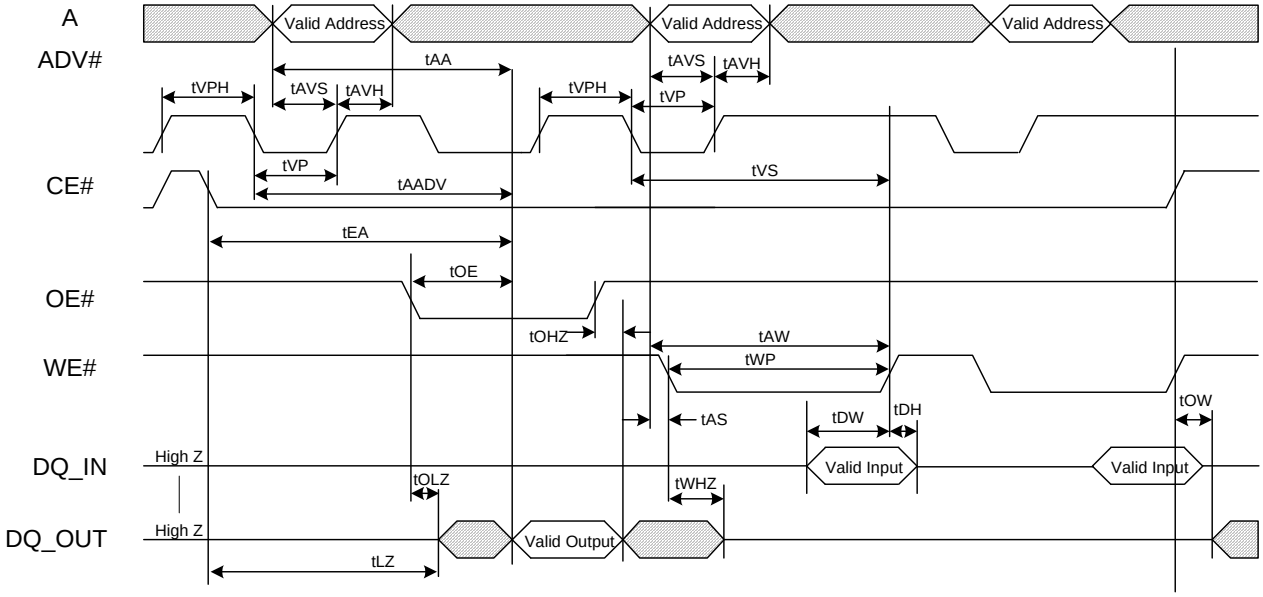
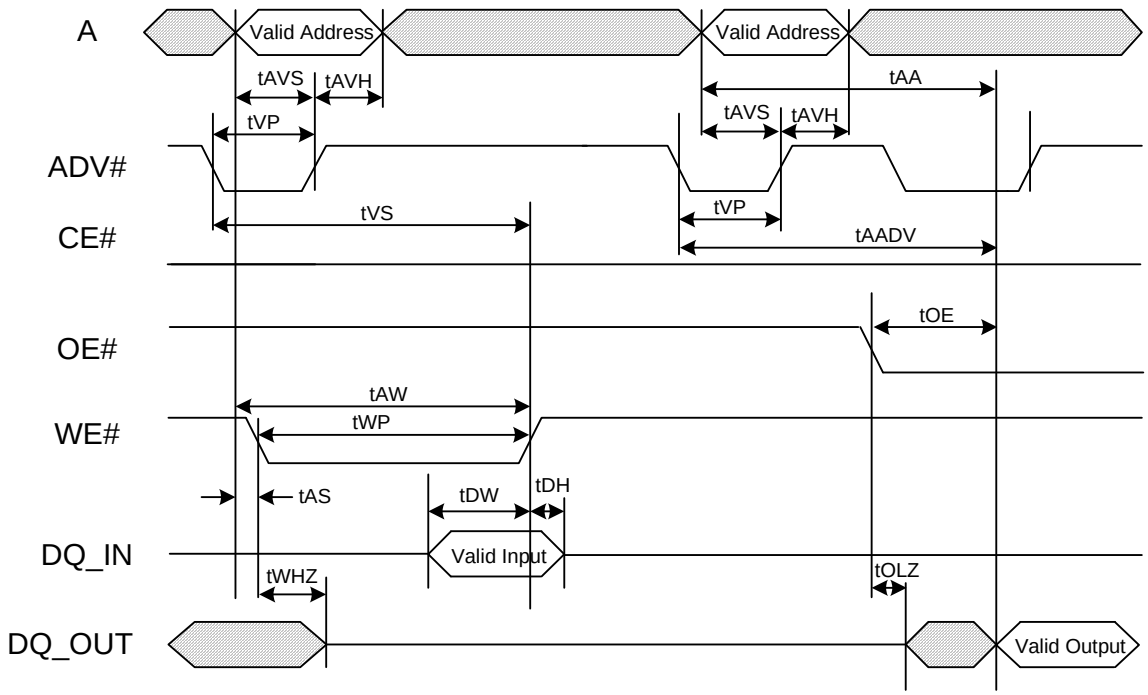


Figure 8. Asynchronous Write to Read Timing

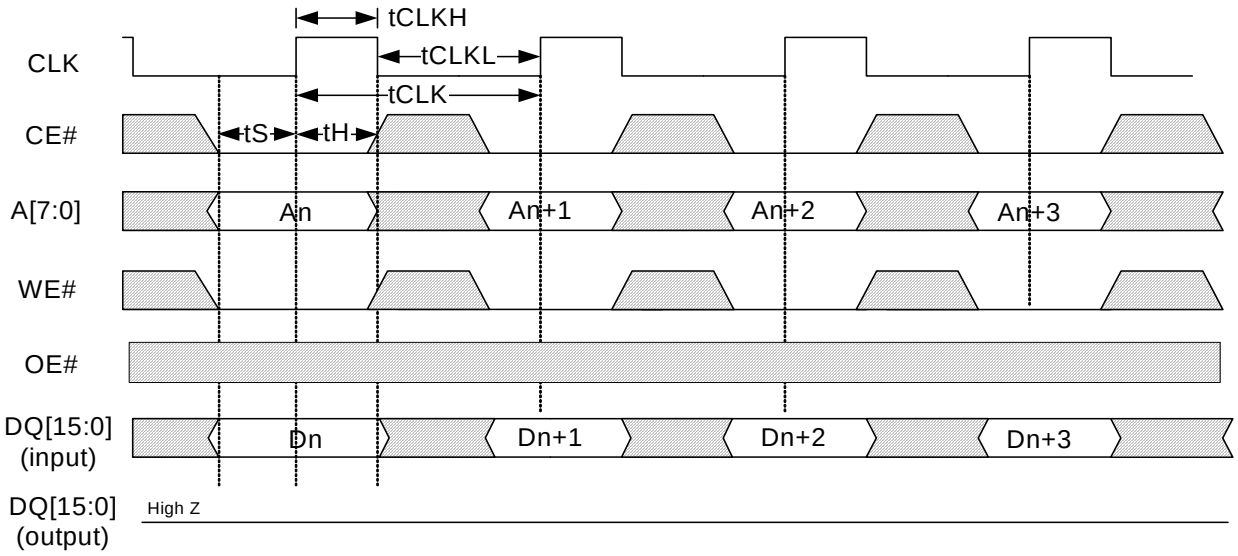


Synchronous Mode Timing Parameters

Table 6. Synchronous Mode Timing Parameters

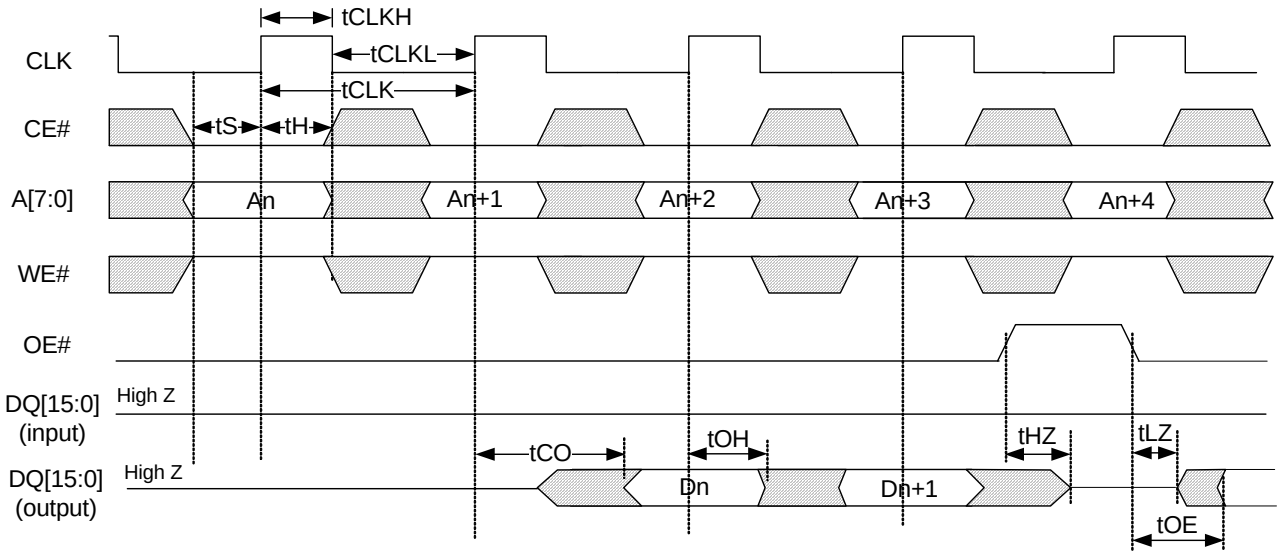
Parameter	Description	Conditions	Min	Max	Unit
FREQ	Interface clock frequency		–	33	MHz
tCLK	Clock Period		30	–	ns
tCLKH	Clock HIGH time		12	–	ns
tCLKL	Clock LOW time		12	–	ns
tS	CE#/WE#/ADDR/DQ setup time		7.5	–	ns
tH	CE#/WE#/ADDR/DQ hold time		1.5	–	ns
tCO	Clock to valid data		–	18	ns
tOH	Clock to data hold time		2	–	ns
tHZ	OE# HIGH to data High Z		–	22.5	ns
tLZ	OE# LOW to data Low Z		3	–	ns
tOE	OE# LOW to data valid		–	22.5	ns
tWHZ	WE# Low to DQ High Z output		–	22.5	ns
tWLZ	WE# High to DQ Low Z output		3	–	ns
tCKHZ	Clock to Data High Z (Figure 12 on page 17)	Measured from the rising edge of the second clock after the deassertion of CE# is latched by the rising edge of the clock.	–	18	ns
tCKLZ	Clock to Data Low Z (Figure 14 on page 18)		3	–	ns

Figure 9. Synchronous Write Timing



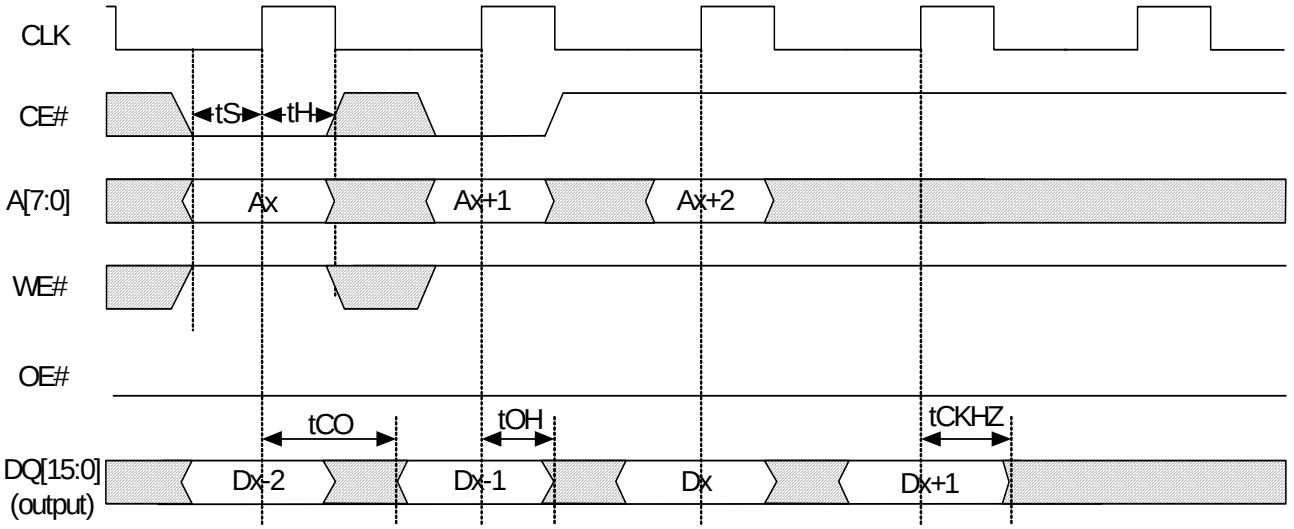
Note:
- Assumes previous cycle had CE# deselected
- OE# is don't care during write operations

Figure 10. Synchronous Read Timing



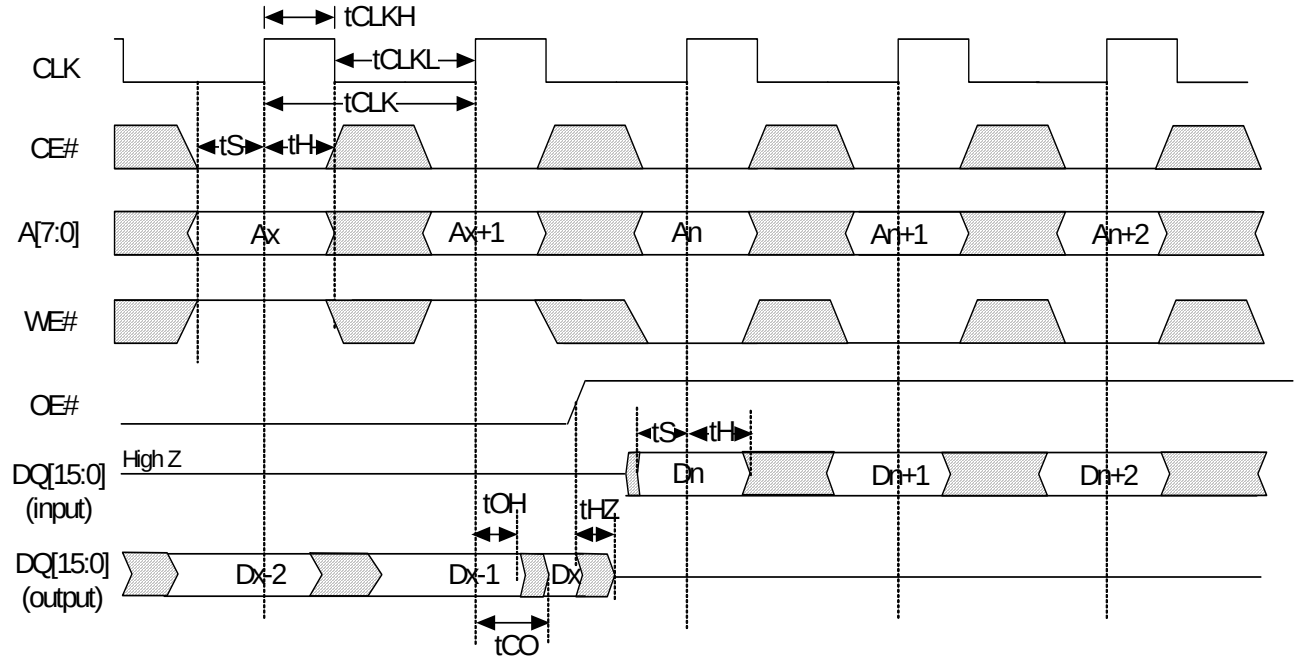
Note:
- Assumes previous cycle had CE# deselected

Figure 11. Synchronous Read (OE# Fixed LOW) Timing



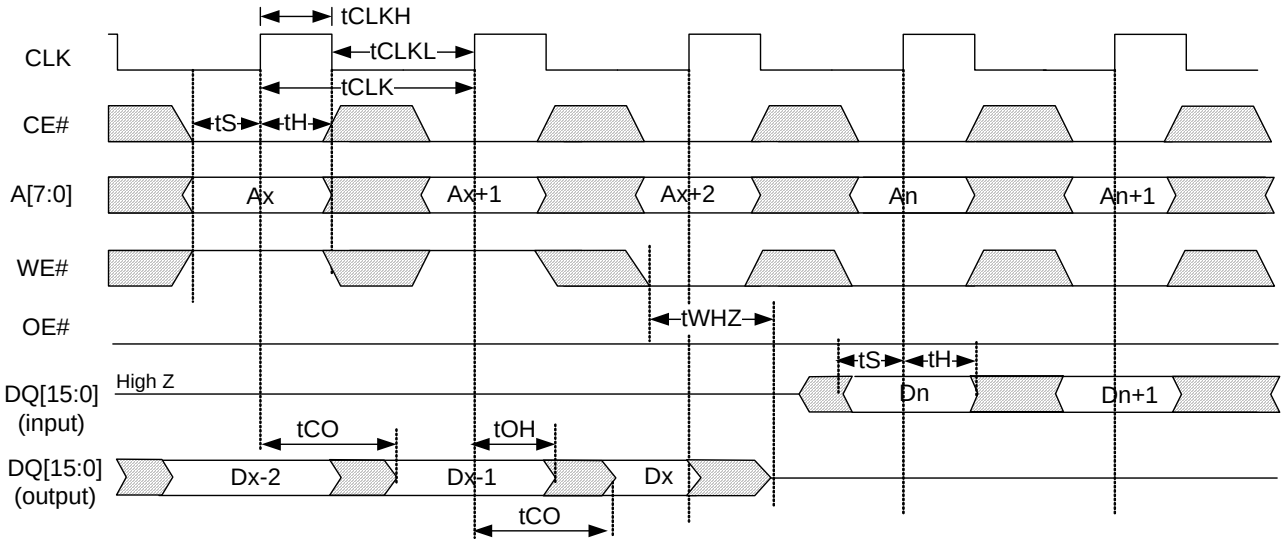
Note:
- Assumes previous several cycles were Read

Figure 12. Synchronous Read to Write (OE# Controlled) Timing



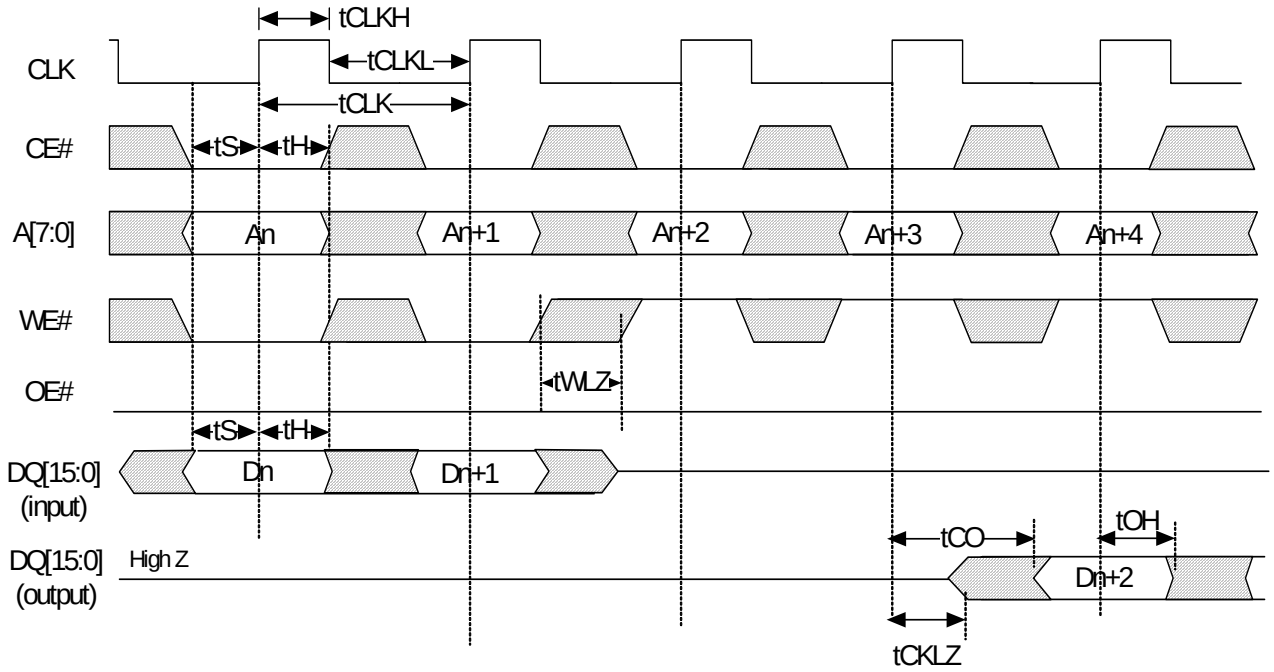
Note:
- Assumes previous several cycles were Read
- (Ax) and (Ax+1) cycles are turnaround. (Ax+1) operation does not cross pipeline.

Figure 13. Synchronous Read to Write (OE# Fixed LOW) Timing



Note:
- Assumes previous several cycles were Read
- In this scenario, OE# is held LOW
- (Ax) and (Ax+1) cycles are turnaround. (Ax+1) operation does not cross pipeline.
- No operation is performed during the Ax+2 cycle (true turnaround operation)

Figure 14. Synchronous Write to Read Timing



Note:
- Assumes previous cycle has CE# deselected
- In this scenario, OE# is held LOW

SD/MMC Parameters

Figure 15. SD/MMC Timing Waveform - All Modes

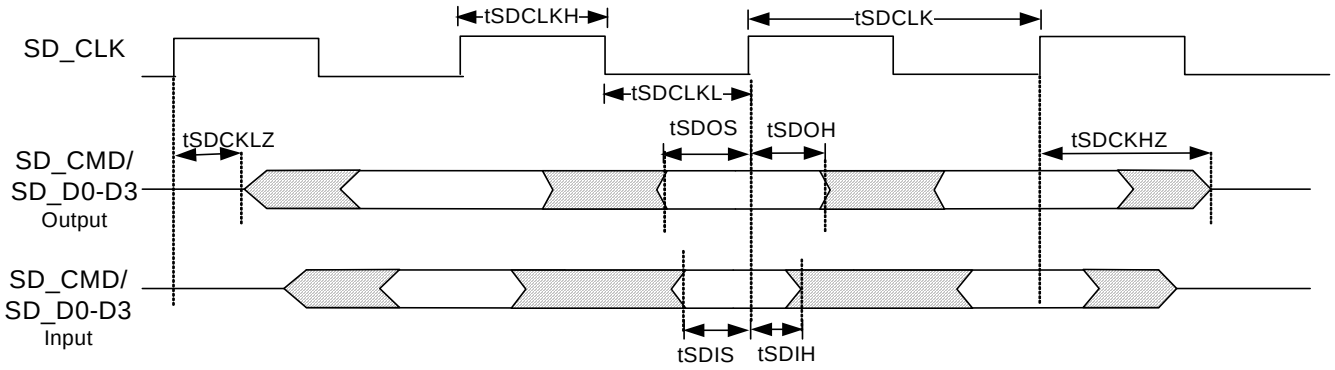


Table 7. Common Timing Parameters for SD and MMC – During Identification Mode

Parameter	Description	Min	Max	Unit
SDFREQ	SD_CLK interface clock frequency	–	400	kHz
tSDCLK	Clock period	2.5	–	µs
tSDCLKH	Clock high time	1.0	–	µs
tSDCLKL	Clock low time	1.0	–	µs

Table 8. Common Timing Parameters for SD and MMC – During Data Transfer Mode

Parameter	Description	Min	Max	Unit
SDFREQ	SD_CLK interface clock frequency	5	48	MHz
tSDCLK	Clock period	20.8	200	ns
tSDCLKOD	Clock duty cycle	40	60	%
tSCLKR	Clock rise time	–	3	ns
tSCLKF	Clock fall time	–	3	ns

Table 9. Timing Parameters for SD – All Modes

Parameter	Description	Min	Max	Unit
tSDIS	Input setup time	4	–	ns
tSDIH	Input hold time	2.5	–	ns
tSDOS	Output setup time	7	–	ns
tSDOH	Output hold time	6	–	ns
tSDCKHZ	Clock to Data High Z	–	18	ns
tSDCKLZ	Clock to Data Low Z	3	–	ns

Table 10. Timing Parameters for MMC – All Modes

Parameter	Description	Min	Max	Unit
tSDIS	Input setup time	4	–	ns
tSDIH	Input hold time	4	–	ns
tSDOS	Output setup time	6	–	ns
tSDOH	Output hold time	6	–	ns
tSDCKHZ	Clock to Data High Z	–	18	ns
tSDCKLZ	Clock to Data Low Z	3	–	ns

Reset and Standby Timing Parameters

Figure 16. Reset and Standby Timing Diagram

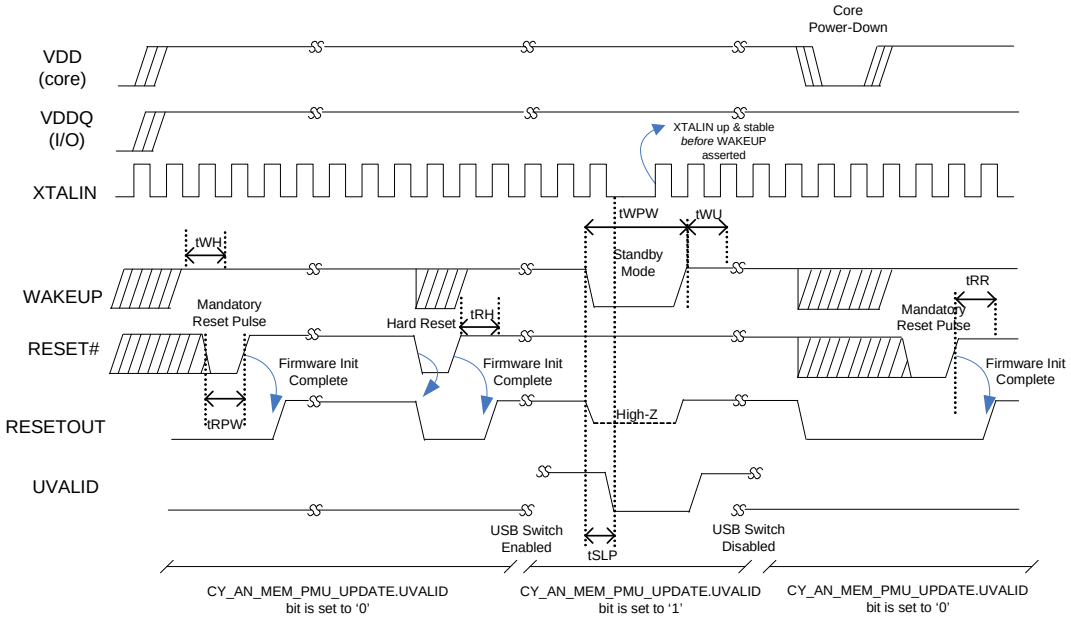
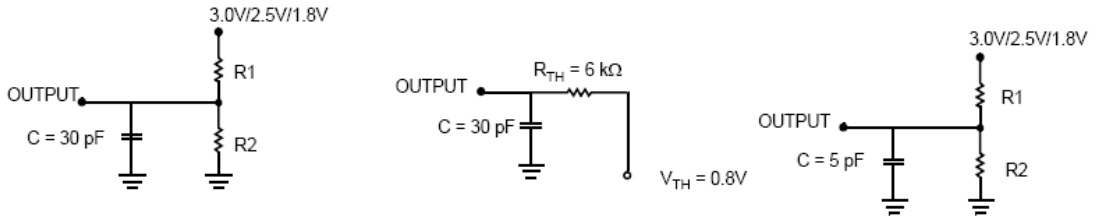


Table 11. Reset and Standby Timing Parameters

Parameter	Description	Conditions	Min	Max	Unit
tSLP	Sleep time		–	1	ms
tWU	WAKEUP time from standby mode	Clock on XTALIN	1	–	ms
		Crystal on XTALIN-XTALOUT	5	–	ms
tWH	WAKEUP high time		5	–	ms
tWPW	WAKEUP pulse width		5	–	ms
tRH	RESET# high time		5	–	ms
tRPW	RESET# pulse width	Clock on XTALIN	1	–	ms
		Crystal on XTALIN-XTALOUT	5	–	ms
tRR	RESET# recovery time		1	–	ms

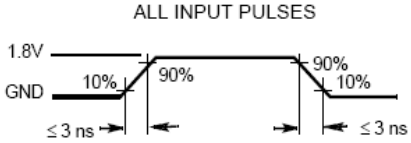
Figure 17. AC Test Loads and Waveforms



(a) Normal Load (Load 1)

	3.0V/2.5V/1.8V
R1	13500Ω
R2	10800Ω

(b) Thévenin Equivalent (Load 1)



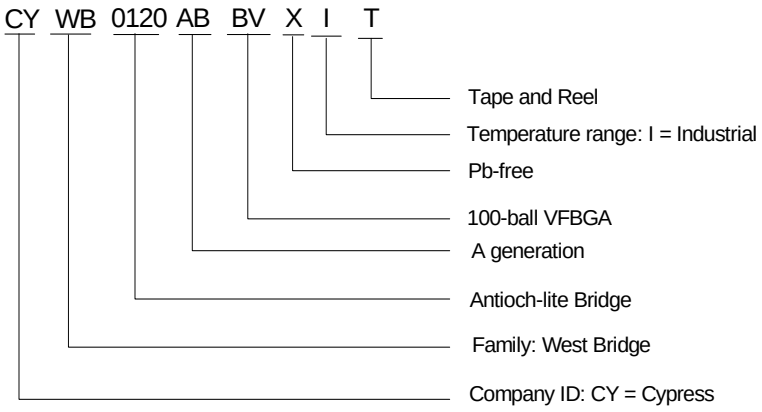
(c) Three-State Delay (Load 2)

(Used for t_{LZ}, t_{HZ}, t_{HZWE}, and t_{LZWE} including scope and jig)

Ordering Information

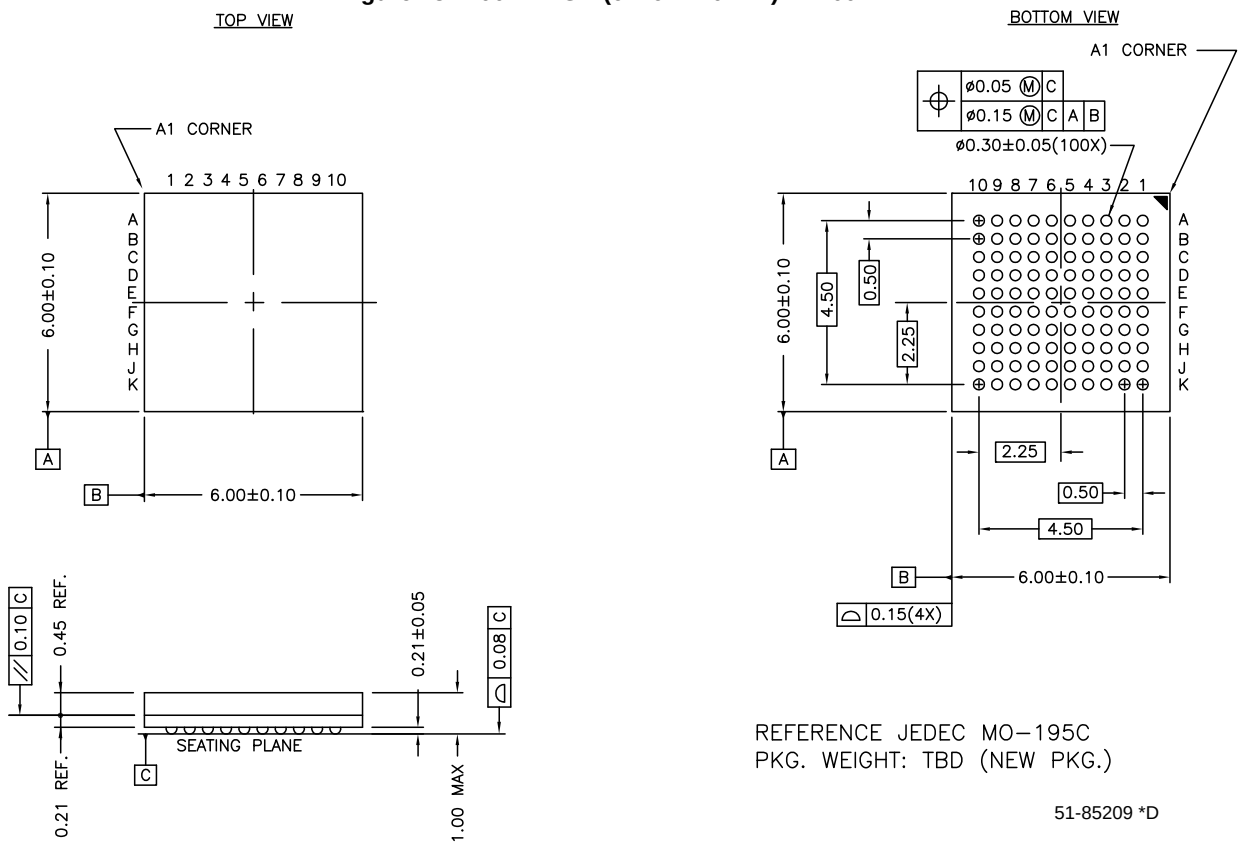
Ordering Code	Turbo-MTP Enabled	Package Type	Available Clock Input Frequencies (MHz)
CYWB0120AB-BVXI	No	100 VFBGA – Pb-Free	19.2, 24, 26, 48
CYWB0120AB-BVXIT			

Ordering Code Definitions



Package Diagrams

Figure 18. 100 VFBGA (6 x 6 x 1.0 MM) BZ100A



Acronyms

Acronym	Description
DMA	direct memory access
MMC	multimedia card
MTP	media transfer protocol
PLL	phase-locked loop
SD	secure digital
I/O	input / output
USB	universal serial bus

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
ms	millisecond
mA	milliampere
Mbps	megabytes per second
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt

Document History Page

Document Title: CYWB0120AB West Bridge® Antioch™-Lite USB/SD Controller Document Number: 001-49144				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2574764	OGC/AESA	11/11/2008	New release
*A	2746360	OGC	07/30/2009	Replaced NC on ball map J4 with SD_RSV
*B	3525332	PRVE	02/15/2012	Updated Ordering Information (CYWB0120AB-BVXIT). Package Diagrams updated 51-85209 from Rev *B to *D. Added Acronyms, Document Conventions, Ordering Code Definitions, and Table of Contents.
*C	3555122	AASI	03/19/2012	Post the datasheet to Cypress.com.

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