ADVANCE

CYWB012X Family

West Bridge®: Antioch™

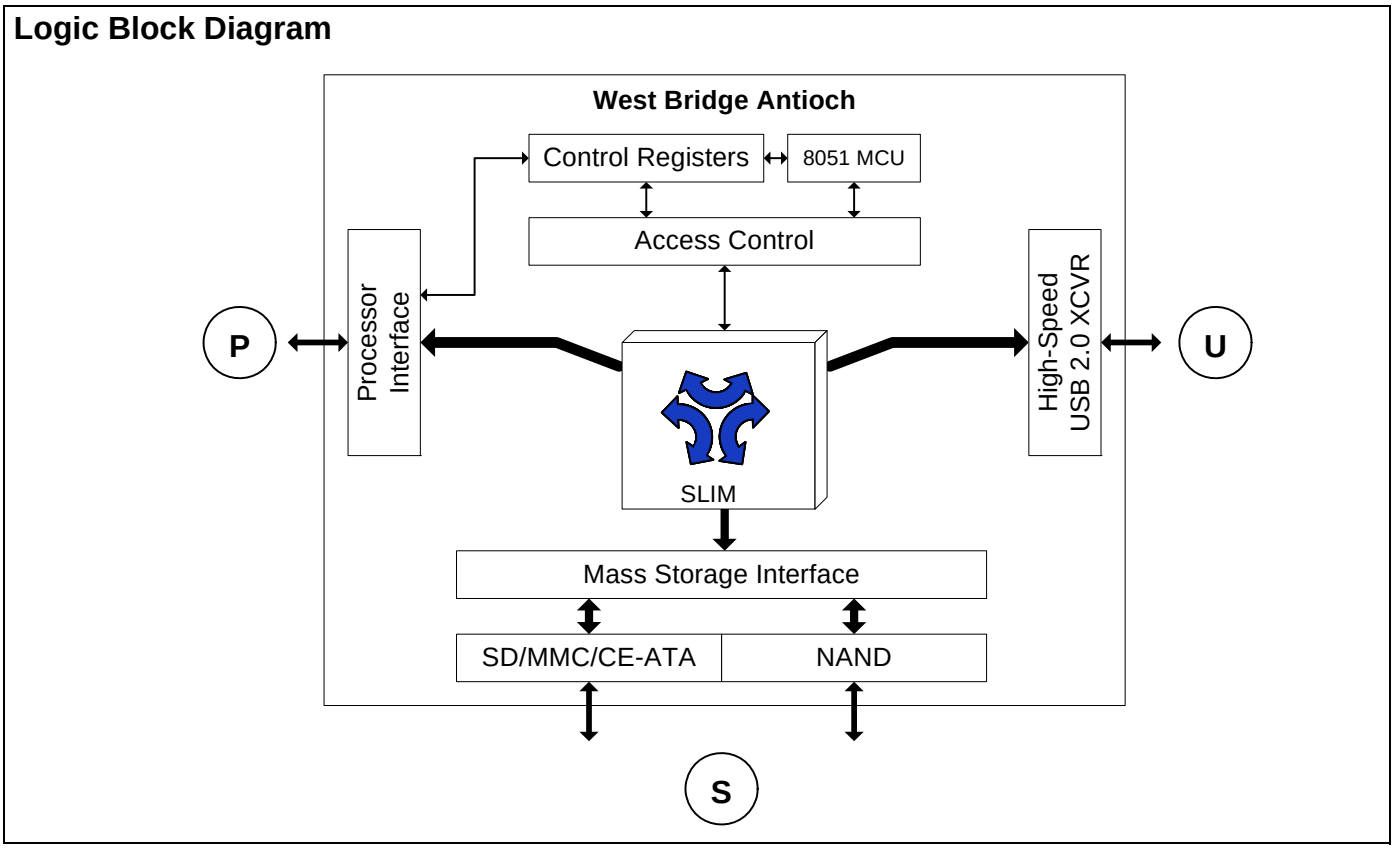
Features

- SLIM® architecture, allowing simultaneous and independent data paths between processor and USB, and between USB and mass storage
- High speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB 2.0 transceiver, smart Serial Interface Engine
  - 16 programmable endpoints
- Mass storage device support
  - MMC/MMC+/SD
  - NAND Flash: x8 or x16, SLC
  - Full NAND management (ECC, wear-leveling)
- Memory-mapped interface to main processor
- DMA slave support
- Ultra low power, 1.8V core operation
- Small footprint, 6x6 mm VFBGA and WLCSP
- Selectable clock input frequencies
  - 19.2 MHz, 24 MHz, 48 MHz
- Expanded mass storage device support
  - MMC/MMC+/SD
  - CE-ATA for micro-HDD
  - NAND Flash: x8 or x16, SLC
  - Full NAND management (ECC, wear-leveling)
- Expanded selectable clock input frequencies
  - 19.2 MHz, 24 MHz, 26 MHz, 48 MHz

Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Digital Cameras
- Portable Video Recorder

Logic Block Diagram



Description

West Bridge® Antioch™ is a peripheral mass storage controller that enhances a processor system with flexible mass storage support and high speed USB connectivity.

Antioch has three different ports that enable connections among a main processor (P-Port), one or more mass storage devices (S-Port), and a USB host (U-Port). Antioch's unique SLIM architecture allows these three ports to interact simultaneously and independently of each other. This offers connectivity from USB to Storage (typically used for PC high speed data download), from USB to Processor (used for synchronization operations), and from Processor to Storage.

Connected as a slave to a main processor, Antioch adds support for high speed USB and mass storage access including MMC, MMC+, SDIO, CE-ATA, SLC and MLC NAND. Antioch further enables new usage models by allowing USB to directly connect to a storage device independent of the main processor.

Antioch is primarily targeted at handsets, to enable high speed connectivity to a PC through USB, and support for the latest mass storage devices.

Antioch can, for instance, enable a multimedia phone to support HDD or NAND MLC storage, with the ability to download multimedia data at high speed from a PC directly to the storage device.

The SLIM Architecture

The Simultaneous Link to Independent Multimedia (SLIM) architecture allows three interfaces (P-port, S-port, and U-port) to connect to one another independent of each other.

With this architecture, connecting the device using Antioch to a PC through USB does not disturb any of the functions of the device, which can still access mass storage, at the same time the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a PC can access a mass storage device independent of the main processor, or enumerate access to both the mass storage and the main processor at the same time.

In a handset, this enables to use the phone as a thumb drive or download media files to the phone while still having full functionality available on the phone. It also allows using the same phone as a modem to connect the PC to the web.

Mass Storage Support (S-Port)

The S-Port can be configured in two different modes, either simultaneously supporting an SDIO/MMC+/CE-ATA port and a x8 NAND port, or supporting a unique x16 NAND access port.

Antioch, as part of its mass storage management functions, can fully manage a NAND device. An embedded 8051 manages the actual reading and writing of the NAND, along with its required protocols, including Single Level Cell (SLC) and Multi-Level Cell (MLC) NAND. It performs standard NAND management functions such as ECC and wear leveling.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface supports both synchronous and asynchronous SRAM-mapped memory accesses. This ensures straightforward electrical communications with the processor, which may also have other devices connected on a shared memory bus.

The memory address is decoded to access any of the multiple endpoint buffers inside Antioch. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers via the memory interface.

Access to these buffers is controlled by either using a DMA protocol or an interrupt to the main processor. These two modes are configurable by the external processor.

As a DMA slave, Antioch generates a DMA request signal to signify to the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Antioch for the specific buffers ready for read or write. It then performs the appropriate read or write operations on the buffer through the processor interface. This way, the external processor only deals with the buffers to access a multitude of storage devices connected to Antioch.

In the Interrupt mode, Antioch communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Antioch for the specific buffers ready for read or write, and it performs the appropriate read or write operations via the processor interface.

Configuration

The West Bridge Antioch device includes configuration and status registers that are accessible as memory-mapped registers through the processor interface. The configuration registers allow the system to specify certain behavior of Antioch. For example, it can mask certain status registers from raising an interrupt. The status registers convey various status of Antioch, such as the addresses of buffers for read operations.

Packaging

The West Bridge Antioch is available in two packaging options: As a bare die or in a 6x6 mm, 100-pin, very fine BGA (VFBGA). As a 100-pin VFBGA, it consumes a small amount of space and allows for easy debug and connections to the other devices in the system.

Pin List

	Pin Name		I/O	Pin Description	Standby	Reset	Power Domain
P-Port	CLK		I	Clock	-	-	PVDDQ VGND
	CE#		I	Chip Select	-	-	
	A[7:0]		I	Address Bus	-	-	
	DQ[15:0]		I/O	Data Bus	Z	Z	
	ADV#		I	Address Valid	-	-	
	OE#		I	Output Enable	-	-	
	WE#		I	Write Enable	-	-	
	INT#		O	Interrupt Request	Z	Z	
	DRQ#		O	DMA Request	Z	Z	
	DACK#		I	DMA Acknowledgement	-	-	
S-Port	SDIO and 8-bit NAND Configuration	16-bit NAND Configuration					
	SD_D[7:0]	NAND_IO[15:8]	I/O	SD Data bus/NAND Upper I/O bus	Z	Z	SSVDDQ VGND
	SD_CLK	N/A	O	SD Clock	Z	Z	
	SD_CMD	N/A	I/O	SD Command	Z	Z	
	SD_POW	N/A	O	SD Power Control	Z	Z	
	SD_WP	N/A	I	GPIO (SD Write Protection Microswitch)	-	-	
	NAND_IO[7:0]	NAND_IO[7:0]	I/O	NAND Lower I/O bus	Z	Z	SNVDDQ VGND
	NAND_CLE	NAND_CLE	O	CMD Latch Enable	Z	Z	
	NAND_ALE	NAND_ALE	O	Address Latch Enable	Z	Z	
	NAND_CE#	NAND_CE#	O	Chip Enable	Z	Z	
	NAND_RE#	NAND_RE#	O	Read Enable	Z	Z	
	NAND_WE#	NAND_WE#	O	Write Enable	Z	Z	
	NAND_WP#	NAND_WP#	O	Write Protect	Z	Z	
	NAND_R/B#	NAND_R/B#	I	Ready/Busy	-	-	
	NAND_CE2#	NAND_CE2#	O	Chip Enable 2	Z	Z	
U-Port	D+		I/O/Z	USB D+	Z	Z	UVDDQ UVSSQ
	D-		I/O/Z	USB D-	Z	Z	
	UVALID		O	External USB Switch Control	Low	Low	
Others	XTALIN		I	Crystal/Clock IN	-	-	XVDDQ VGND
	XTALOUT		O	Crystal Out	Z	Z	
	RESET#		I	RESET	-	-	GVDDQ VGND
	RESETOUT		O	RESET OUT	Z	Low	
	GPIO[1:0]		I/O	General Input/Output	Z	Z	
	WAKEUP		I	Wake Up Signal	-	-	
Config	XTALSLC[1:0]		I	Clock Select 0 and 1	-	-	
	NANDCFG		I	S Port Configuration	-	-	
	TEST[2:0]		I	Test Configuration	-	-	
Power	PVDDQ		Power	Processor interface VDD	-	-	
	SNVDDQ		Power	NAND VDD	-	-	
	UVDDQ		Power	USB VDD	-	-	
	SSVDDQ		Power	SDIO VDD	-	-	
	GVDDQ		Power	Miscellaneous I/O VDD	-	-	
	AVDDQ		Power	Analog VDD	-	-	
	XVDDQ		Power	Crystal VDD	-	-	
	VDD		Power	Core VDD	-	-	
	VDD33		Power	Power Seq Control 3.3V	-	-	
	UVSSQ		Power	USB GND	-	-	
	AVSSQ		Power	Analog GND	-	-	
	VGND		Power	Core GND	-	-	

VDD33: In CYWB0124AB, the pin is no-connect internally. However, to migrate to CYWB0224AB, it must be connected to the highest supply to the device. This supply must always be connected. If USB is used, then VDD33 must be connected to nominal 3.3V (because 3.3V is required for USB). VDD33 must be constantly supplied in CYWB0224AB.

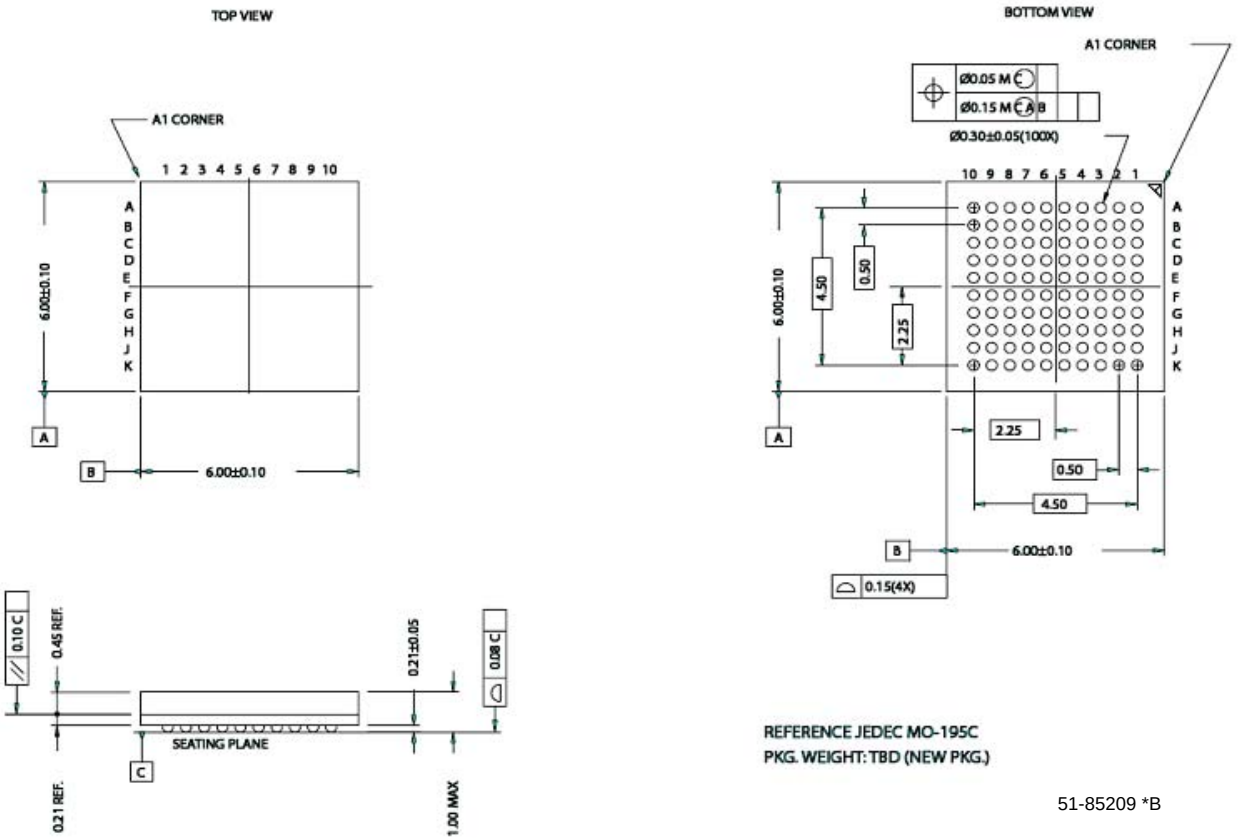
Figure 1. 100 VFBGA Package Top View

Top View

	1	2	3	4	5	6	7	8	9	10	
A	ADV#	WE#	INT#	DRQ#	D+	D-	UVALID	XTALIN	AVSSQ	VDD33	A
B	DQ[1]	DQ[0]	OE#	DACK#	UVDDQ	UVSSQ	XVDDQ	XTALOUT	AVDDQ	RESETOUT	B
C	DQ[4]	DQ[3]	DQ[2]	XTALSLC[0]	XTALSLC[1]	NANDCFG	WAKEUP	TEST[1]	GPIO[1]	RESET#	C
D	DQ[7]	DQ[6]	DQ[5]	PVDDQ	VDD	GVDDQ	TEST[0]	GPIO[0]	SD_D[1]	SD_D[0]	D
E	DQ[10]	DQ[9]	DQ[8]	VGND	VGND	VGND	VGND	TEST[2]	SD_D[3]	SD_D[2]	E
F	DQ[13]	DQ[12]	DQ[11]	VGND	VGND	VGND	VDD	SD_CLK	SD_D[5]	SD_D[4]	F
G	CE#	DQ[15]	DQ[14]	VDD	VDD	VDD	VDD	SD_CMD	SD_D[7]	SD_D[6]	G
H	A[5]	A[6]	A[7]	PVDDQ	SNVDDQ	NAND_WE#	SSVDDQ	SD_POW	NAND_IO[2]	SD_WP	H
J	A[3]	CLK	A[4]	NAND_R/B#	NAND_CE#	NAND_ALE	NAND_WP#	NAND_IO[5]	NAND_IO[3]	NAND_IO[0]	J
K	A[0]	A[1]	A[2]	NAND_RE#	NAND_CE2#	NAND_CLE	NAND_IO[7]	NAND_IO[6]	NAND_IO[4]	NAND_IO[1]	K
	1	2	3	4	5	6	7	8	9	10	

Package Diagram

Figure 2. 100 VFBGA (6 x 6 x 1.0 mm) BZ100A



Ordering Information

Ordering Code	Turbo-MTP Enabled	Package Type	Available Clock Input Frequencies (MHz)
CYWB0124AB-BVXI	No	100 VFBGA (Pb-free)	19.2, 24, 26, 48
CYWB0125AB-BVXI	Yes	100 VFBGA (Pb-free)	19.2, 24, 26, 48
CYWB0124ABX-FDXI	No	WLCSP (Pb-free)	19.2, 24, 26, 48
CYWB0125ABX-FDXI	Yes	WLCSP (Pb-free)	19.2, 24, 26, 48

This table contains advance information. Contact your local Cypress sales representative for availability of these parts.

Document History Page

Document Title: CYWB012X Family West Bridge® Antioch™ Document Number: 001-05898				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	410919	QJL	See ECN	New release
*A	460471	QJL, RUY	See ECN	Updated pin table, pin diagram
*B	2763925	OGC/AESA	09/15/09	Added Ordering Information table

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