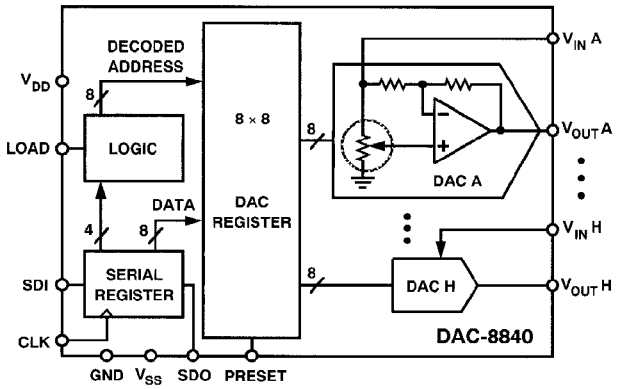
8-Bit, Octal, 4-Quadrant Multiplying, CMOS TrimDAC

DAC8840

FEATURES
Replaces 8 Potentiometers
1 MHz 4-Quadrant Multiplying Bandwidth
No Signal Inversion
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 Volt Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC-8840 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC® capability allows replacement of the mechanical trimmer function in new designs. The DAC-8840 is ideal for ac or dc gain control of up to 1 MHz bandwidth signals. The 4-quadrant multiplying capability is useful for signal inversion and modulation often found in video convergence circuitry.

Internally the DAC-8840 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a registered trademark of Analog Devices, Inc.

The DAC-8840 consumes only 190 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC-8841.

The DAC-8840 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages.

REV. A

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DAC8840—SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL			±1/4	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic			±1	LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		3	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		10		μV/°C
REFERENCE INPUTS		Applies to All Inputs $V_{IN}X$				
Voltage Range	IVR	Note 1	±3			V
Input Resistance	R_{IN}	D = $2B_H$, Code Dependent	3	6		kΩ
Input Capacitance	C_{IN}	D = FF_H, Code Dependent		19	30	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	±3			V
Output Current	I_{OUT}	ΔV_{OUT} <1 LSB	±5	±10		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p–p	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}X$= +6 V	1.3	4.0		V/μs
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	2.5		V/μs
Total Harmonic Distortion	THD	$V_{IN}X$ = 4 V p–p, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		$\mu V/\sqrt{Hz}$
Output Settling Time	t_S	±1 LSB Error Band, D = 0 to FF_H		3.5	6	μs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	80		dB
Digital Feedthrough	Q	V_{INX} = 0 V, D = 0 to 255_{10}		6		nVs
POWER SUPPLIES						
Power Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			190	260	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0002	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS}\rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	μA
Input Capacitance	C_{IL}			7	10	pF
Input Coding			Offset Binary			
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V

NOTE
[1]Maximum input voltage is always 2 V less than V_{DD}.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = −40°C to +85°C apply for DAC-8840F, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Clock Pulse Width	t_{CH}, t_{CL}	80		ns
Data Setup Time	t_{DS}	40		ns
Data Hold Time	t_{DH}	20		ns
CLK to SDO Propagation Delay	t_{PD}		120	ns
DAC Register Load Pulse Width	t_{LD}	70		ns
Preset Pulse Width	t_{PR}	50		ns
Clock Edge to Load Time	t_{CKLD}	30		ns
Load Edge to Next Clock Edge	t_{LDCK}	60		ns

WAFER TEST LIMITS: (V_{DD} = +5 V, V_{SS} = −5 V, All $V_{IN}X$ = +3 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	DAC8840GBC Limits	Units
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL	All Devices Monotonic	±1	LSB max
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H	25	mV max
Input Resistance ($V_{IN}X$)	R_{IN}	D = $2B_H$; Code Dependent	3	kΩ min
DAC Output Voltage Range	OVR	R_L = 10 kΩ	±3	V min
DAC Output Current	I_{OUT}	ΔV_{OUT} < 1 LSB	±5	mA min
Slew Rate		Measured 10% to 90%		
Positive	SR+	$\Delta V_{OUT}X$ = +6 V	1.3	V/μs min
Negative	SR−	$\Delta V_{OUT}X$ = −6 V	1.3	V/μs min
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V	26	mA max
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V	26	mA max
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%	0.01	%/% max
Logic Input High	V_{IH}		2.4	V min
Logic Input Low	V_{IL}		0.8	V max
Logic Input Current	I_L		±10	μA max
Logic Output High	V_{OH}	I_{OH} = −0.4 mA	3.5	V min
Logic Output Low	V_{OL}	I_{OL} = 1.6 mA	0.4	V max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

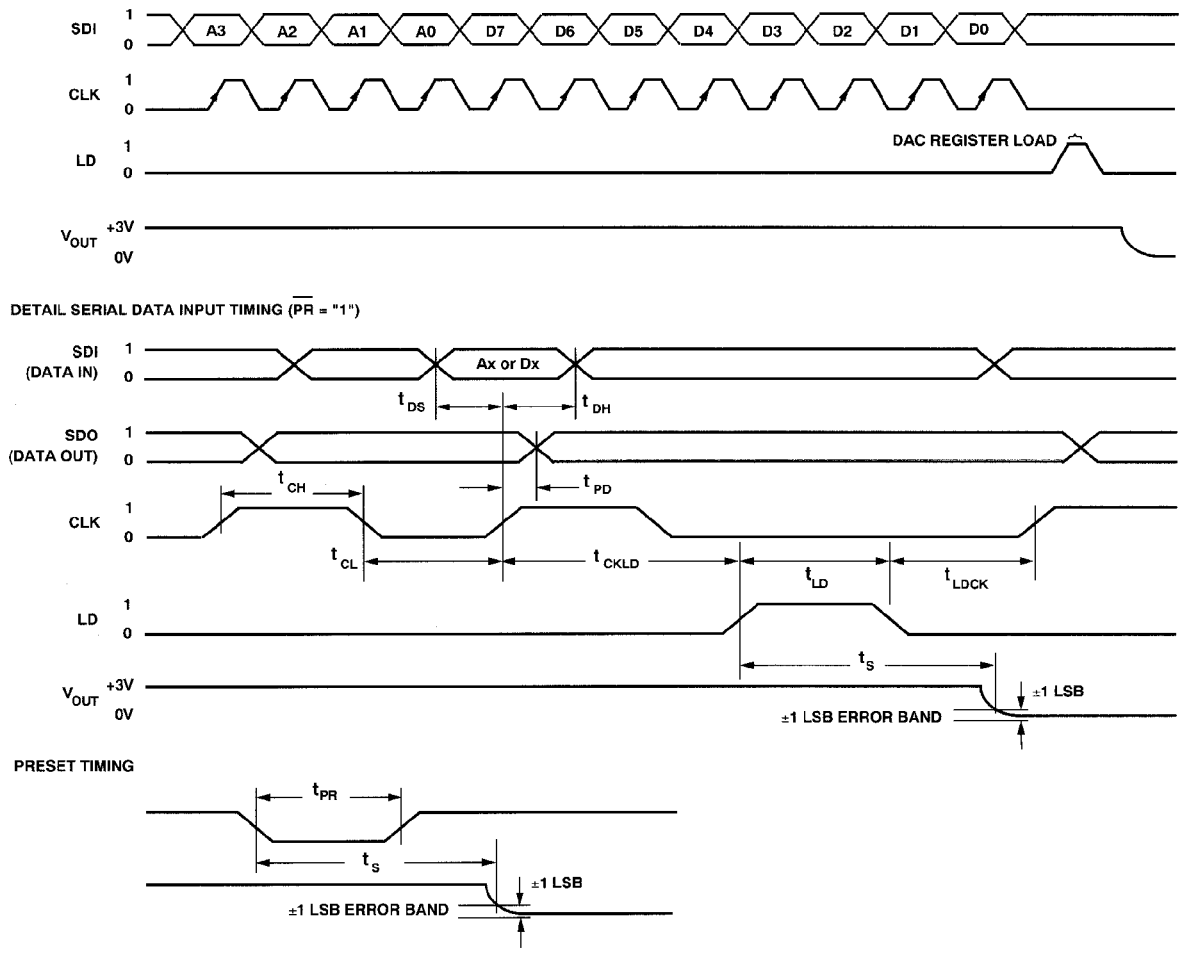
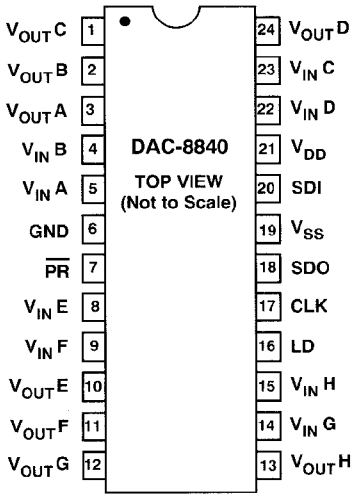


Figure 1. Timing Diagram

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input That Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I.
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

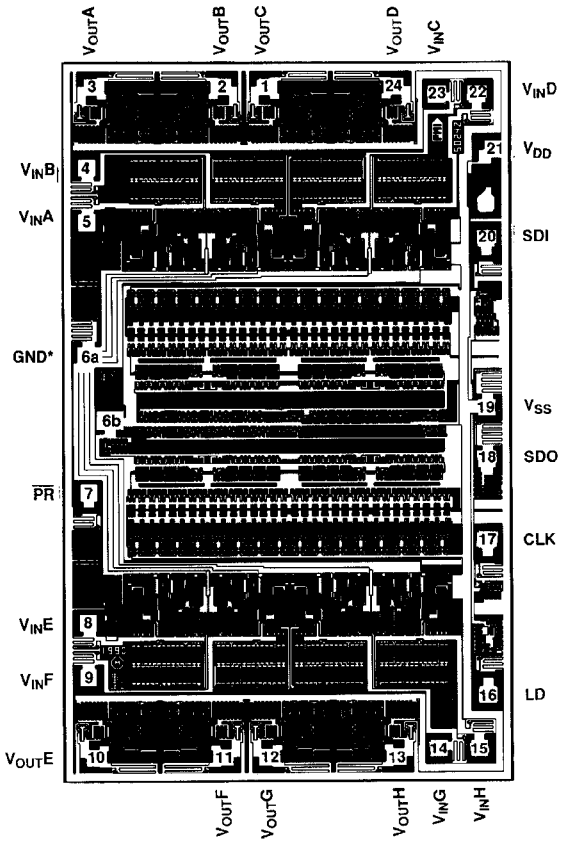
V_{DD} to GND . . . . . −0.3, +7 V
V_{SS} to GND . . . . . +0.3, −7 V
$V_{IN}X$ to GND . . . . . V_{DD}, V_{SS}
$V_{OUT}X$ to GND . . . . . V_{DD}, V_{SS}
Short Circuit $I_{OUT}X$ to GND . . . . . Continuous
Digital Input & Output Voltage to GND . . . . . V_{DD}, V_{SS}
Operating Temperature Range
Extended Industrial: DAC8840F . . . . . −40°C to +85°C
Maximum Junction Temperature (T_J max) . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . (T_J Max − T_A)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip . . . . . 64°C/W
P-DIP . . . . . 57°C/W
SOIC-24 . . . . . 70°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
DAC8840FP	−40°C to +85°C	Plastic DIP	N-24
DAC8840FW	−40°C to +85°C	Cerdip	Q-24
DAC8840FS	−40°C to +85°C	SOL-24	R-24
DAC8840GBC	25°C	DICE	

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.
The DAC8840 contains 3236 transistors.



*BOTH GND PADS (6a, 6b) ARE BONDED TO PIN 6 OF PACKAGE.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

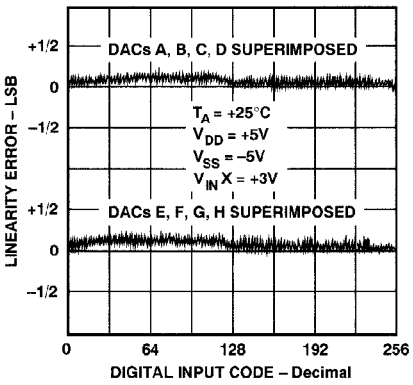


Figure 2. Linearity Error vs. Digital Input Code

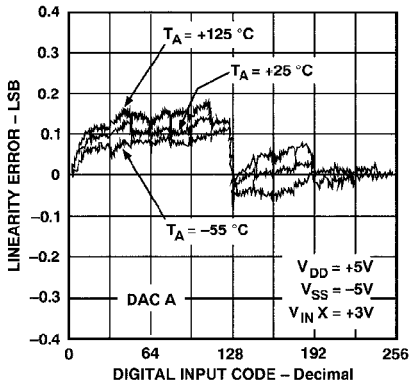


Figure 3. Linearity Error vs. Digital Code vs. Temperature

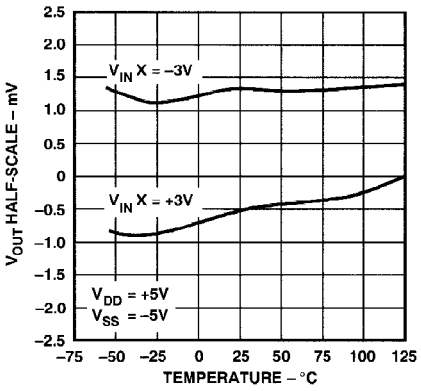


Figure 4. V_{OUT} Half-Scale (80_H) vs. Temperature

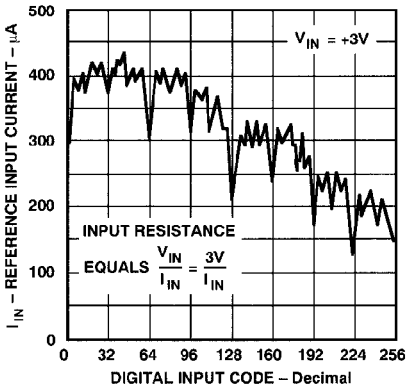


Figure 5. Input Resistance vs. Code

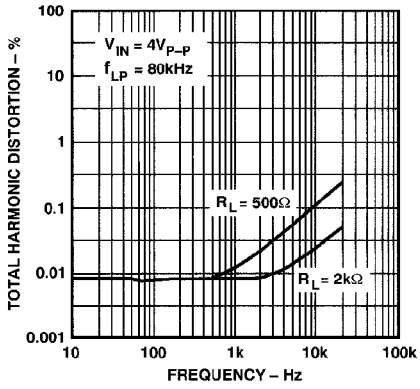


Figure 6. Total Harmonic Distortion vs. Frequency

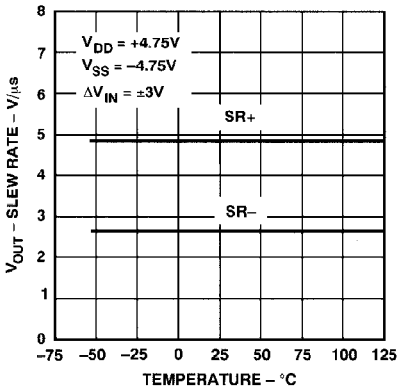


Figure 7. V_{OUT} Slew Rate vs. Temperature

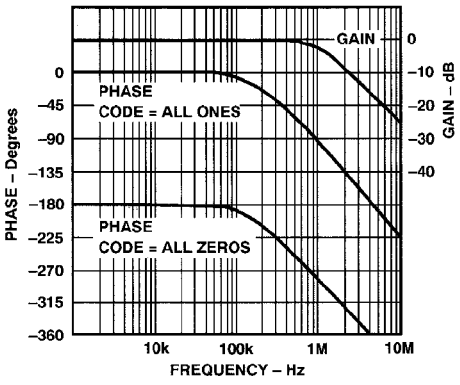


Figure 8. Gain and Phase vs. Frequency (Digital Input = 0 or 255_{10})

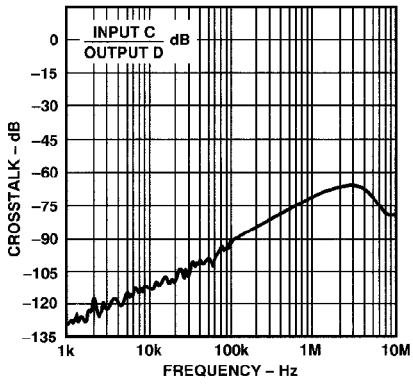


Figure 9. DAC Crosstalk vs. Frequency

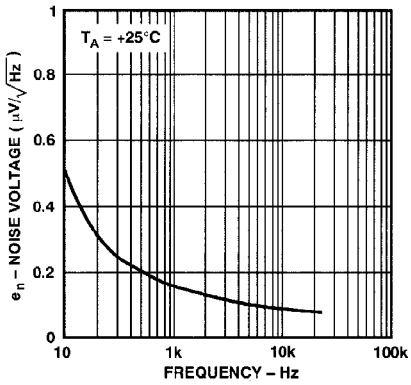


Figure 10. Voltage Noise Density vs. Frequency

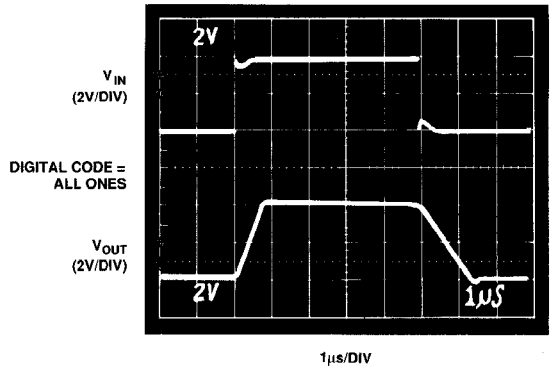


Figure 11. Pulse Response

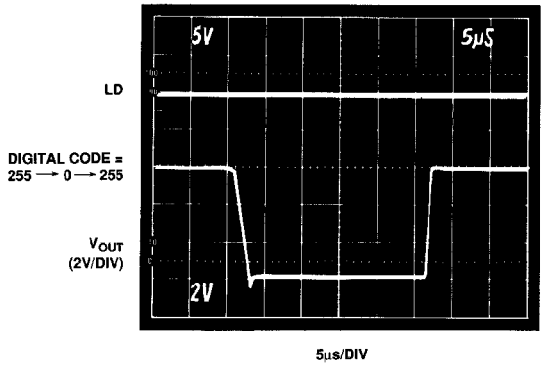


Figure 12. Settling Time

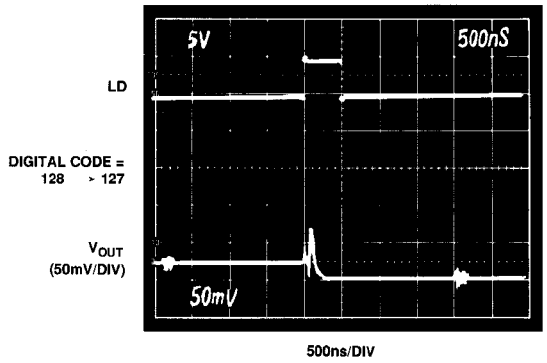


Figure 13. Worst Case 1 LSB Digital Step Change

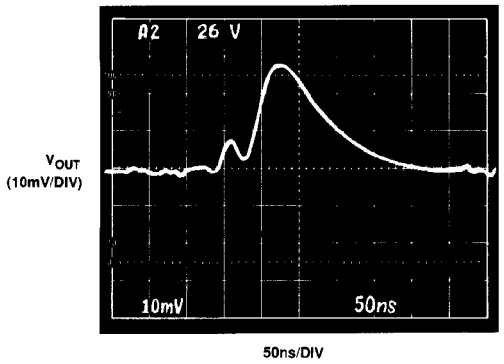


Figure 14. Digital Feedthrough

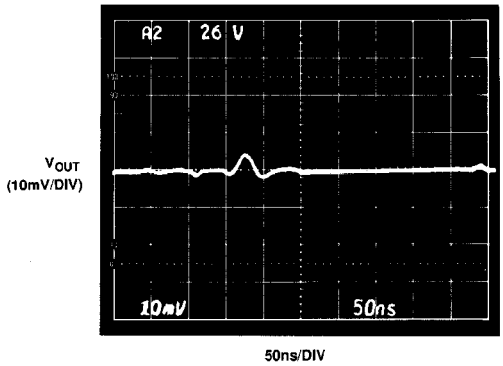


Figure 15. Digital Crosstalk

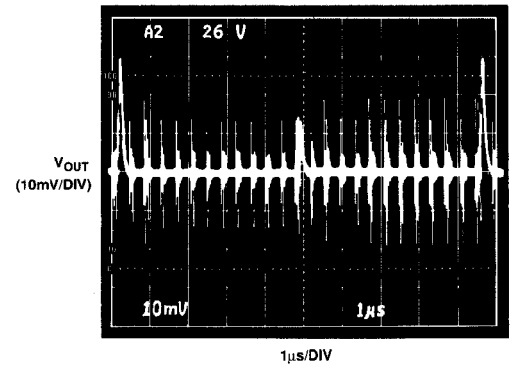


Figure 16. Clock Feedthrough

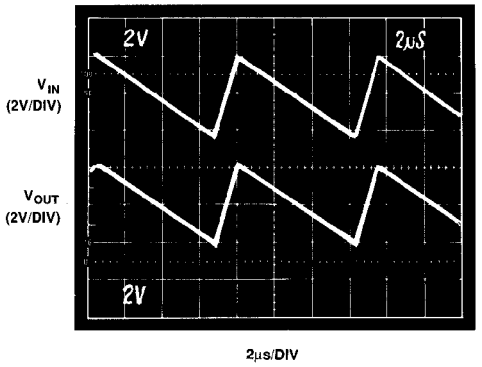


Figure 17. 128 kHz Sawtooth Waveform

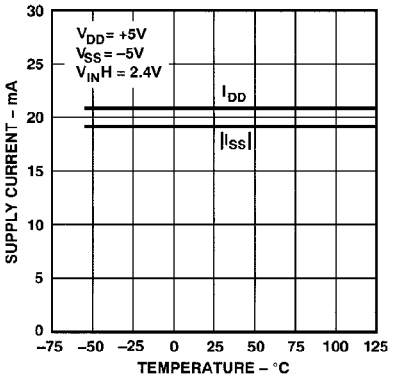


Figure 18. Supply Current vs. Temperature

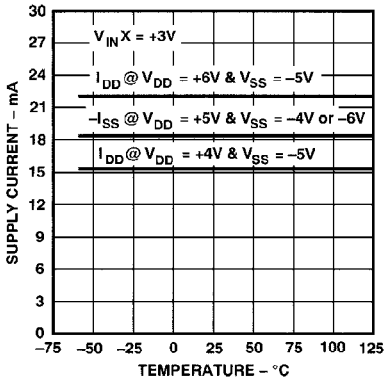


Figure 19. Supply Current vs. Supply Voltage vs. Temperature

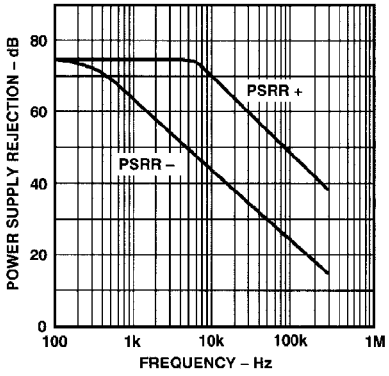


Figure 20. PSRR vs. Frequency

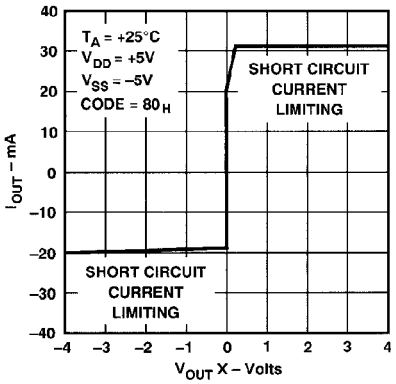


Figure 21. DAC Output Current vs. $V_{OUT}X$

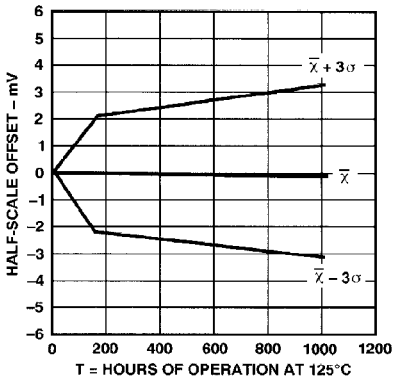


Figure 22. Output Drift Delta Accelerated by Burn-In

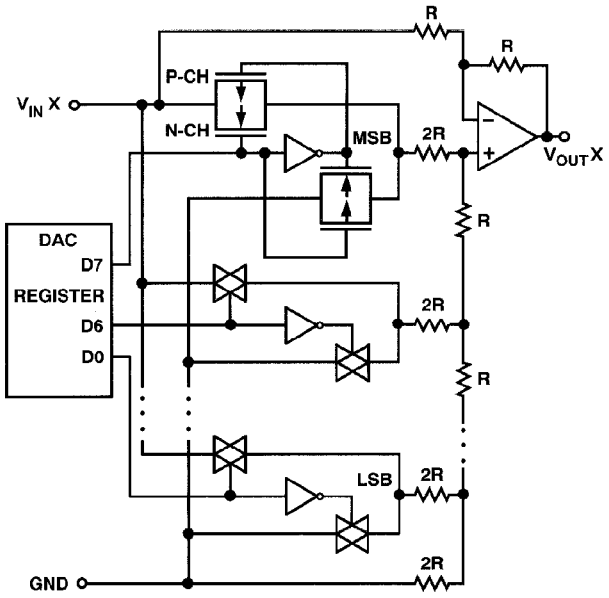


Figure 23. DAC-8840 TrimDAC Equivalent Circuit

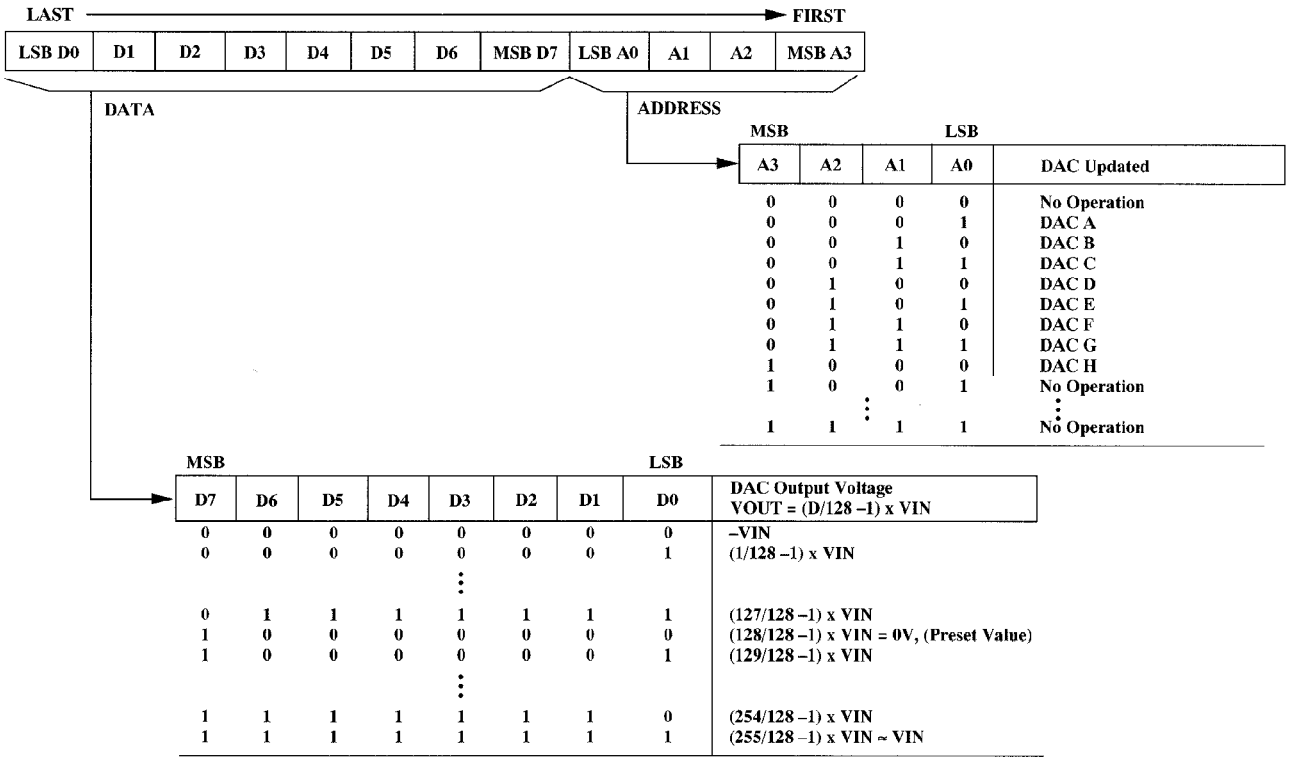


Table I. Serial Input Decode Table

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X	↓	L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

Table II. Logic Control Input Truth Table

CIRCUIT OPERATION

The DAC-8840 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of output drive-current to drive external loads. The DAC and amplifier combination shown in Figure 24 produces four-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition, the DAC-8840 provides a 1 MHz gain-bandwidth product in the four-quadrant multiplying channel. Operating from plus and minus 5 V power supplies, analog inputs and outputs of ±3 V are easily accommodated.

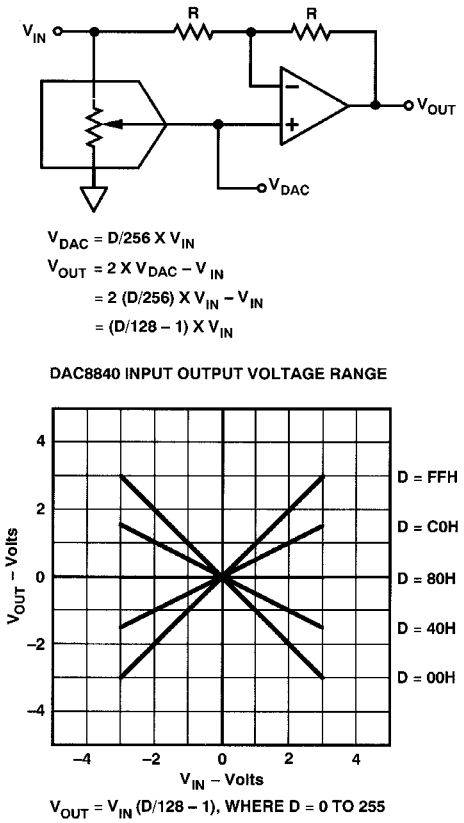


Figure 24. DAC Plus Amplifier Combine to Produce Four Quadrant Multiplication

In order to simplify use with a controlling microprocessor, a simple layout-efficient three-wire serial-data-interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8 bits of data. Using this word combination any DAC register can be changed at a given time without disturbing the other channels. A serial data output SDO pin simplifies cascading multiple DAC-8840s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to zero volts. This asynchronous input pin $\overline{PR}$ can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start general purpose adjustment procedures.

ADJUSTING AC OR DC SIGNAL LEVELS

The four quadrant multiplication operation of the DAC-8840 is shown in Figure 24. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128 - 1) \times V_{IN} \quad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 3V dc input applied to V_{IN} are summarized in this table.

Decimal Input (D)	V_{OUT}(D)	Comments (V_{IN} = 3 V)
0	−3.00 V	Inverted FS
1	−2.98	
127	−0.02	
128	0.00	Zero Output
129	0.02	
254	2.95	
255	2.98	Full Scale (FS)

Table III.

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal the input voltage. This is a result of the R-2R ladder DAC architecture chosen. When the DAC register is loaded with 0, the output polarity is inverted and exactly equals the magnitude of the input voltage V_{IN}. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the DAC-8840. The calculated voltage error would be ±0.023 V (= ±3 V/128).

If V_{IN} is an ac signal such as a sinewave then we can use equation 2 to describe circuit performance.

$$V_{OUT}(t,D) = (D/128 - 1) \times A \sin(\omega t) \quad (2)$$

where $\omega = 2\pi f$, A = sinewave amplitude, and D = decimal input code.

This transfer characteristic Equation 2 lends itself to amplitude and phase control of the incoming signal V_{IN}. When the DAC is loaded with all zeros, the output sinewave is shifted by 180° with respect to the input sinewave. This powerful multiplying capability can be used for a wide variety of modulation, waveform adjustment and amplitude control.

REFERENCE INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a code dependent input resistance whose worst case minimum value 3 kΩ is specified in the electrical characteristics table. The graph (Figure 5) titled "Reference Input Current versus Code" shown in the typical performance characteristics section displays the incremental changes. Use a suitable amplifier capable of driving this input resistance in parallel with the specified 19 pF typical input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design (see Figure 23). The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from near the negative supply (V_{SS}) to within 2 V of the positive supply (V_{DD}). That is, the operating input voltage range is:

$$V_{SS} + 0.5\ V < V_{IN}X < (V_{DD}-2\ V) \quad (3)$$

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8840's internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 100 pF. However, in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation.

The low output impedance of the buffers minimizes crosstalk between analog input channels. A graph (Figure 9) of analog crosstalk between channels is provided in the typical performance characteristics section. At 1 MHz, 72 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1–10 μF tantulum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, $\overline{PR}$) of the DAC-8840 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8840s.

The Logic Control input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge sensitive input. If mechanical switches are used for breadboarding product evaluation, they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the serial input decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8840 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. The packages not requiring data changes would receive the NOP address, that is, all zeros. It takes 12 clocks on the CLK pin to fully load the serial input shift register. Data on the SDI input pin is subject to the timing diagram (Figure 1) data setup and data hold time requirements. After the twelfth clock pulse the processor needs to activate the LD strobe to have the DAC-8840 decode the serial register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are provided in the electrical characteristic table and in the Figure 1 timing diagram. After twelve clock edges, data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels. Measurements of DAC switch feedthrough shown in the electrical characteristics table were accomplished by grounding the $V_{IN}X$ inputs and cycling the data codes between all zeros and all ones. Under this condition 6 nVs of feedthrough was measured on the output of the switched DAC channel. An adjacent channel measured less than 1 nVs of digital crosstalk. The digital feedthrough photographs shown in the typical performance characteristics section displays these characteristics (Figures 14, 15, and 16).

Figure 25 shows a three-wire interface for a single DAC-8840 that easily cascades for multiple packages.

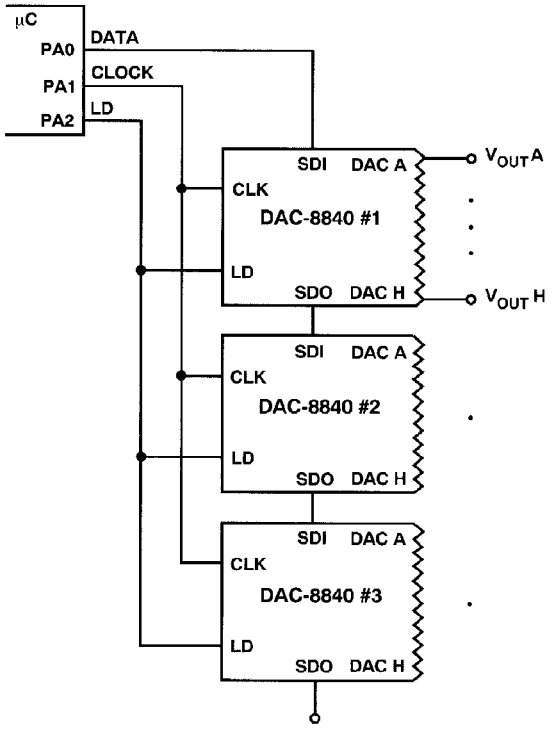
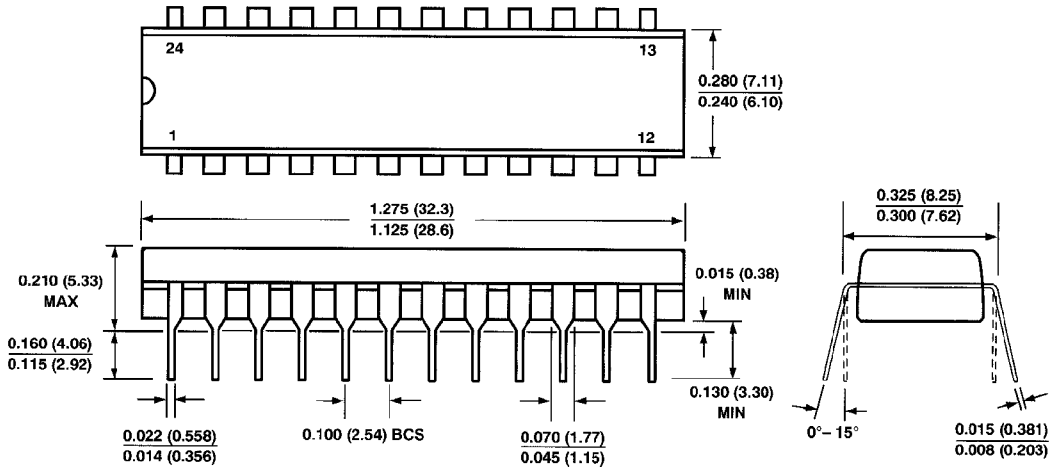


Figure 25. Three-Wire Interface Updates Multiple DAC-8840s

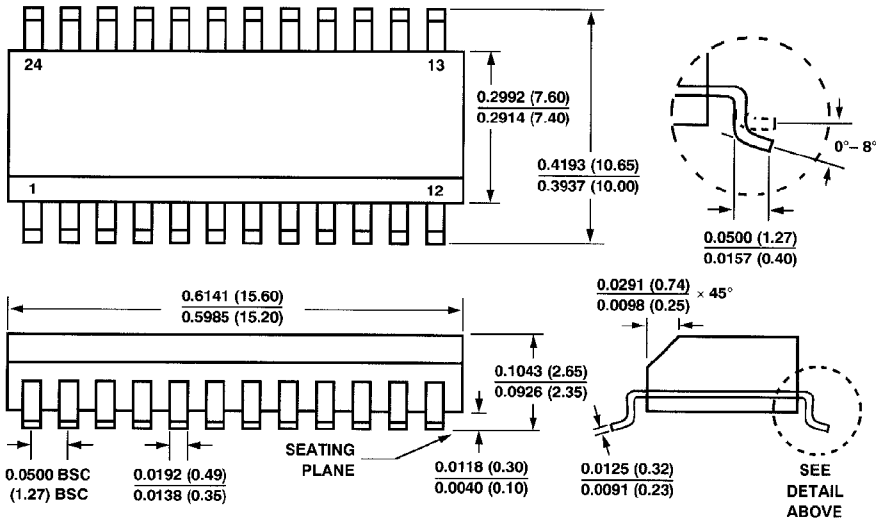
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

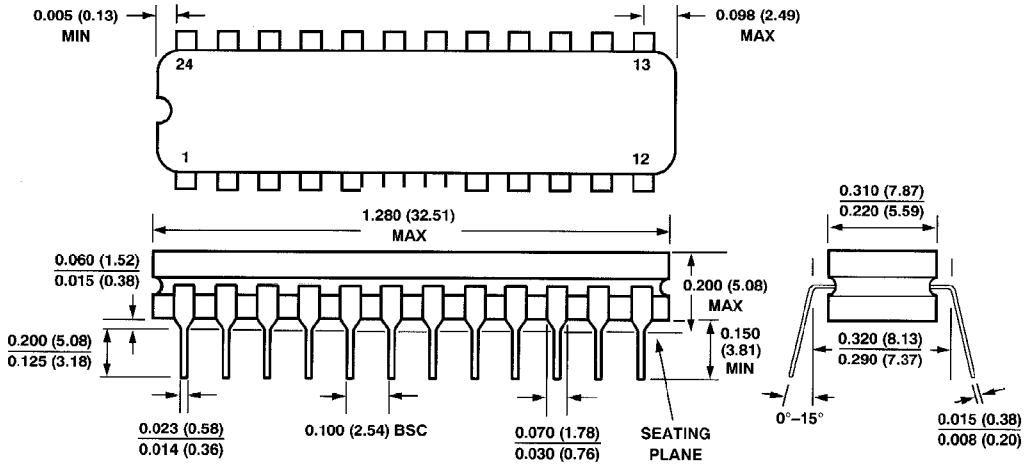
24-Pin Narrow Body Plastic DIP Package



24-Pin Wide Body SOIC Package



24-Pin Narrow-Body Cerdip Package



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