

## 80V, 0.5A Three Phase Driver

The HIP4086 is a Three Phase Bridge N-Channel MOSFET driver IC. The HIP4086 is specifically targeted for PWM motor control. It makes bridge based designs simple and flexible. Like the HIP4081, the HIP4086 has a flexible input protocol for driving every possible switch combination. Unlike the HIP4081, the user can override the shoot-through protection for switched reluctance applications. The HIP4086 has reduced drive current compared to the HIP4081 (0.5A vs 2.5A) and a much wider range of programmable dead times (0.25 $\mu$ s to 4.5 $\mu$ s) - like the HIP4082. The HIP4086 is suitable for applications requiring DC to 100kHz. Unlike the previous family members, the HIP4086 has a programmable undervoltage set point.

Also refer to the HIP4083, three phase upper only MOSFET driver, for a lower current solution optimized for smaller motors.

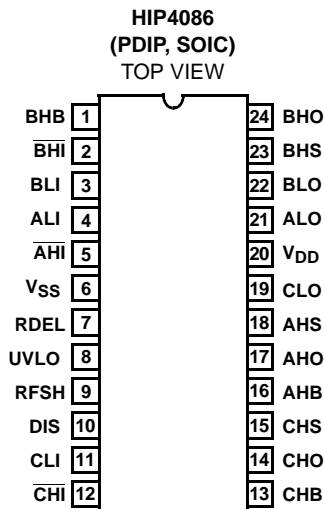
## Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP4086AB*	-40 to 125	24 Ld SOIC	M24.3
HIP4086ABZ* (See Note)	-40 to 125	24 Ld SOIC (Pb-free)	M24.3
HIP4086AP	-40 to 125	24 Ld PDIP	E24.3
HIP4086APZ (See Note)	-40 to 125	24 Ld PDIP (Pb-free)	E24.3

\*Add "-T" suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

## Pinout



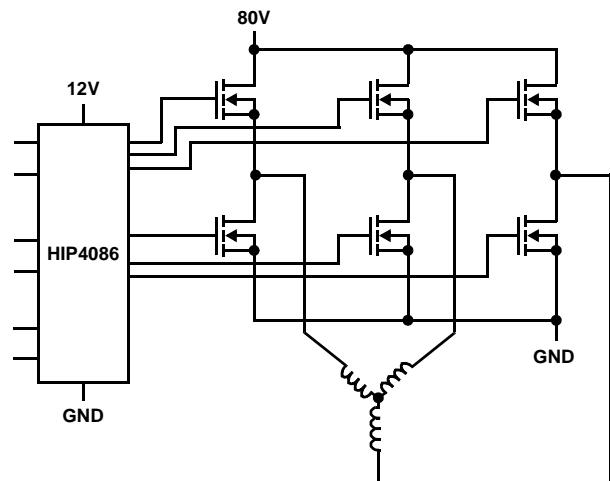
## Features

- Independently Drives 6 N-Channel MOSFETs in Three Phase Bridge Configuration
- Bootstrap Supply Max Voltage to 95VDC
- Bias Supply Operation from 7V to 15V
- 1.25A Peak Turn-Off Current
- User-Programmable Dead Time (0.25 $\mu$ s to 4.5 $\mu$ s)
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- Programmable Bootstrap Refresh Time
- Drives 1000pF Load with Typical Rise Time of 20ns and Fall Time of 10ns
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Dead Time Disable Capability
- Programmable Undervoltage Set Point
- Pb-free available

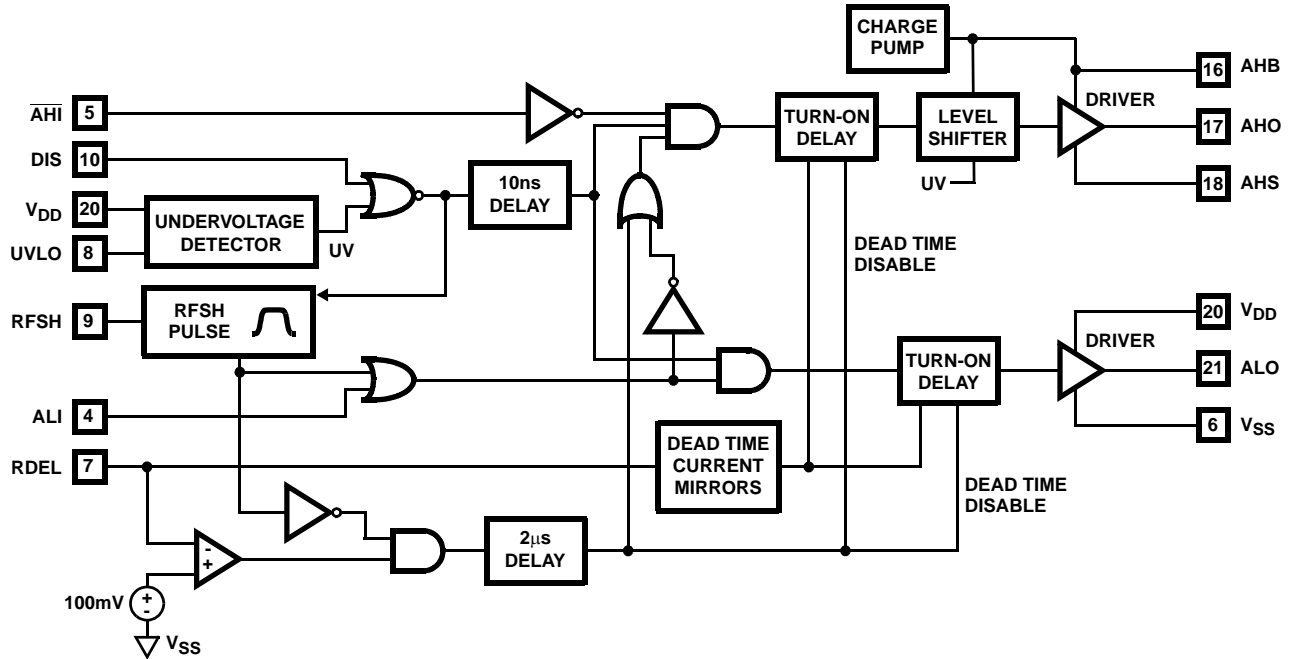
## Applications

- Brushless Motors
- AC Motor Drives
- Switched Reluctance Motor Drives
- Battery Powered Vehicles

## Application Block Diagram



Functional Block Diagram (1/3 of HIP4086)

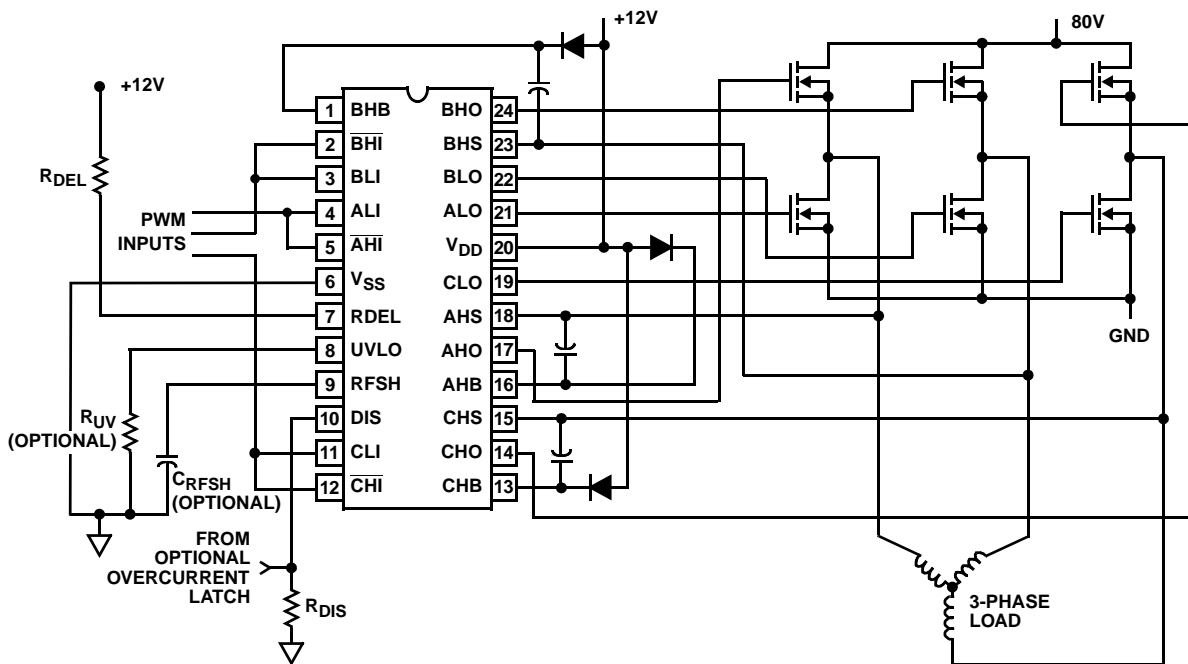


TRUTH TABLE

INPUT			OUTPUT			
ALI, BLI, CLI	$\overline{AH\bar{I}}$ , $\overline{BH\bar{I}}$ , $\overline{CH\bar{I}}$	UV	DIS	RDEL	ALO, BLO, CLO	AHO, BHO, CHO
X	X	X	1	X	0	0
X	X	1	X	X	0	0
1	X	0	0	>100mV	1	0
0	0	0	0	X	0	1
0	1	0	0	X	0	0
1	0	0	0	<100mV	1	1

NOTE: X signifies that input can be either a "1" or "0".

Typical Application (PWM Mode Switching)



**Pin Descriptions**

PIN NUMBER	SYMBOL	DESCRIPTION
16 1 13	AHB BHB CHB (xHB)	High-Side Bootstrap supplies. One external bootstrap diode and one capacitor are required for each. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to each xHB pin.
5 2 12	$\overline{\text{AHI}}$ $\overline{\text{BHI}}$ $\overline{\text{CHI}}$ (xHI)	High-Side Logic Level Inputs. Logic at these three pins controls the three high side output drivers, AHO (Pin 17), BHO (Pin 24) and CHO (Pin 14). When $\overline{\text{xHI}}$ is low, xHO is high. When $\overline{\text{xHI}}$ is high, xHO is low. Unless the dead time is disabled by connecting RDEL (Pin 7) to ground, the low side input of each phase will override the corresponding high side input on that phase - see Truth Table on previous page. If RDEL is tied to ground, dead time is disabled and the outputs follow the inputs. Care must be taken to avoid shoot-through in this application. DIS (Pin 10) also overrides the high side inputs. $\overline{\text{xHI}}$ can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ).
4 3 11	ALI BLI CLI (xLI)	Low-Side Logic Level Inputs. Logic at these three pins controls the three low side output drivers ALO (Pin 21), BLO (Pin 22) and CLO (Pin 19). If the upper inputs are grounded then the lower inputs control both xLO and xHO drivers, with the dead time set by the resistor at RDEL (Pin 7). DIS (Pin 10) high level input overrides xLI, forcing all outputs low. xLI can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ).
6	$V_{SS}$	Ground. Connect the sources of the Low-Side power MOSFETs to this pin.
7	RDEL	Dead Time Setting. Connect a resistor from this pin to $V_{DD}$ to set timing current that defines the dead time between drivers - see Figure 15. All drivers turn-off with no adjustable delay, so the RDEL resistor guarantees no shoot-through by delaying the turn-on of all drivers. When RDEL is tied to $V_{SS}$ , both upper and lowers can be commanded on simultaneously. While not necessary in most applications, a decoupling capacitor of 0.1 $\mu$ F or smaller may be connected between RDEL and $V_{SS}$ .
8	UVLO	Undervoltage Setting. A resistor can be connected between this pin and $V_{SS}$ to program the undervoltage set point, see Figure 16. With this pin not connected, the undervoltage disable is typically 6.6V. When this pin is tied to $V_{DD}$ , the undervoltage disable is typically 6.2V.
9	RFSH	Refresh Pulse Setting. An external capacitor can be connected from this pin to $V_{SS}$ to increase the length of the start up refresh pulse - see Figure 14. If this pin is not connected, the refresh pulse is typically 1.5 $\mu$ s.
10	DIS	Disable Input. Logic level input that when taken high sets all six outputs low. DIS high overrides all other inputs. With DIS low, the outputs are controlled by the other inputs. DIS can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$ ).
17 24 14	AHO BHO CHO (xHO)	High-Side Outputs. Connect to the gates of the High-Side power MOSFETs in each phase.
15 23 15	AHS BHS CHS (xHS)	High-Side Source Connection. Connect the sources of the High-Side power MOSFETs to these pins. The negative side of the bootstrap capacitors should also be connected to these pins.
20	$V_{DD}$	Positive Supply. Decouple this pin to $V_{SS}$ (Pin 6).
21 22 19	ALO BLO CLO (xLO)	Low-Side Outputs. Connect the gates of the Low-Side power MOSFETs to these pins.

NOTE: x = A, B and C.

**Absolute Maximum Ratings**

Supply Voltage, $V_{DD}$ .....	-0.3V to 16V
Logic I/O Voltages .....	-0.3V to $V_{DD} + 0.3V$
Voltage on xHS .....	-6V (Transient) to 85V (-40°C to 150°C)
Voltage on xHB .....	$V_{xHS} - 0.3V$ to $V_{xHS} + V_{DD}$
Voltage on xLO .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Voltage on xHO .....	$V_{xHS} - 0.3V$ to $V_{xHB} + 0.3V$
Phase Slew Rate .....	20V/ns

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
SOIC Package .....	75
PDIP Package .....	70
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Junction Temperature .....	150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C (SOIC - Lead Tips Only)

**Operating Conditions**

Supply Voltage, $V_{DD}$ .....	+7V to +15V
Voltage on xHB .....	$V_{xHS} + V_{DD}$
Voltage on xHS .....	.0V to 80V
Ambient Temperature Range .....	-40°C to 125°C
Junction Temperature Range .....	-40°C to 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.
2. All voltages are relative to  $V_{SS}$  unless otherwise specified.
3. x = A, B and C. For example, xHS refers to AHS, BHS and CHS.

**Electrical Specifications**  $V_{DD} = V_{xHB} = 12V$ ,  $V_{SS} = V_{xHS} = 0V$ ,  $R_{DEL} = 20K$ ,  $R_{UV} = \infty$ , Gate Capacitance ( $C_{GATE}$ ) = 1000pF

PARAMETER	TEST CONDITIONS	$T_J = 25^\circ C$			$T_J = -40^\circ C$ TO $150^\circ C$		UNITS
		MIN	TYP	MAX	MIN	MAX	
<b>SUPPLY CURRENTS AND UNDER VOLTAGE PROTECTION</b>							
$V_{DD}$ Quiescent Current	$\overline{xHI} = 5V$ , $xLI = 5V$	2.7	3.4	4.2	2.1	4.3	mA
$V_{DD}$ Operating Current	$f = 20kHz$ , 50% Duty Cycle	6.3	8.25	10.5	5	11	mA
xHB On Quiescent Current	$\overline{xHI} = 0V$	-	40	80	-	100	$\mu A$
xHB Off Quiescent Current	$\overline{xHI} = V_{DD}$	0.6	0.8	1.3	0.5	1.4	mA
xHB Operating Current	$f = 20kHz$ , 50% Duty Cycle	0.7	0.9	1.3	-	2.0	mA
Qpump Output Voltage	No Load	11.5	12.5	14	10.5	14.5	V
Qpump Output Current	$V_{xHS} = 12V$ , $V_{xHB} = 22V$	50	100	130	-	140	$\mu A$
xHB, xHS Leakage Current	$V_{xHS} = 80V$ , $V_{xHB} = 93V$	7	24	45	-	50	$\mu A$
$V_{DD}$ Rising Undervoltage Threshold	$R_{UV}$ open	6.2	7.1	8.0	6.1	8.1	V
$V_{DD}$ Falling Undervoltage Threshold	$R_{UV}$ open	5.75	6.6	7.5	5.6	7.6	V
Minimum Undervoltage Threshold	$R_{UV} = V_{DD}$	5	6.2	6.8	4.9	6.9	V
<b>INPUT PINS: ALI, BLI, CLI, <math>\overline{AHI}</math>, <math>\overline{BHI}</math>, <math>\overline{CHI}</math>, AND DIS</b>							
Low Level Input Voltage		-	-	1.0	-	0.8	V
High Level Input Voltage		2.5	-	-	2.7	-	V
Input Voltage Hysteresis		-	35	-	-	-	mV
Low Level Input Current	$V_{IN} = 0V$	-60	-100	-135	-55	-140	$\mu A$
High Level Input Current	$V_{IN} = 5V$	-1	-	+1	-10	+10	$\mu A$
<b>GATE DRIVER OUTPUT PINS: ALO, BLO, CLO, AHO, BHO, AND CHO</b>							
Low Level Output Voltage ( $V_{OUT} - V_{SS}$ )	$I_{SINKING} = 30mA$	-	100	-	-	200	mV
Peak Turn-On Current	$V_{OUT} = 0V$	0.3	0.5	0.7	-	1.0	A
Peak Turn-Off Current	$V_{OUT} = 12V$	0.7	1.1	1.5	0.5	1.7	A

# HIP4086

**Switching Specifications**  $V_{DD} = V_{xHB} = 12V$ ,  $V_{SS} = V_{xHS} = 0V$ ,  $C_{GATE} = 1000pF$ ,  $R_{DEL} = 10k$

PARAMETER	TEST CONDITIONS	$T_J = 25^{\circ}C$			$T_J = -40^{\circ}C$ TO $150^{\circ}C$		UNITS
		MIN	TYP	MAX	MIN	MAX	
<b>TURN-ON DELAY AND PROPAGATION DELAY</b>							
Dead Time	$R_{DEL} = 100K$	3.8	4.5	6	3	7	$\mu s$
	$R_{DEL} = 10K$	0.38	0.5	0.65	0.3	0.7	$\mu s$
Dead Time Channel Matching	$R_{DEL} = 10K$	-	7	15	-	20	%
Lower Turn-Off Propagation Delay (xLI-xLO)	No Load	-	30	45	-	65	ns
Upper Turn-Off Propagation Delay (xHI-xHO)	No Load	-	75	90	-	100	ns
Lower Turn-On Propagation Delay (xLI-xLO)	No Load	-	45	75	-	90	ns
Upper Turn-On Propagation Delay (xHI-xHO)	No Load	-	65	90	-	100	ns
Rise Time	$C_{GATE} = 1000pF$	-	20	40	-	50	ns
Fall Time	$C_{GATE} = 1000pF$	-	10	20	-	25	ns
Disable Turn-Off Propagation Delay (DIS - Lower Outputs)		-	55	80	-	90	ns
Disable Turn-Off Propagation Delay (DIS - Upper Outputs)		-	80	90	-	100	ns
Disable to Lower Turn-On Propagation Delay (DIS - xLO)		-	55	80	-	100	ns
Disable to Upper Enable (DIS - xHO)	$R_{DEL} = 10K$ , $C_{RFSH}$ Open	-	2.0	-	-	-	$\mu s$
Refresh Pulse Width (xLO)	$C_{RFSH}$ Open	-	1.5	-	-	-	$\mu s$

Timing Diagrams

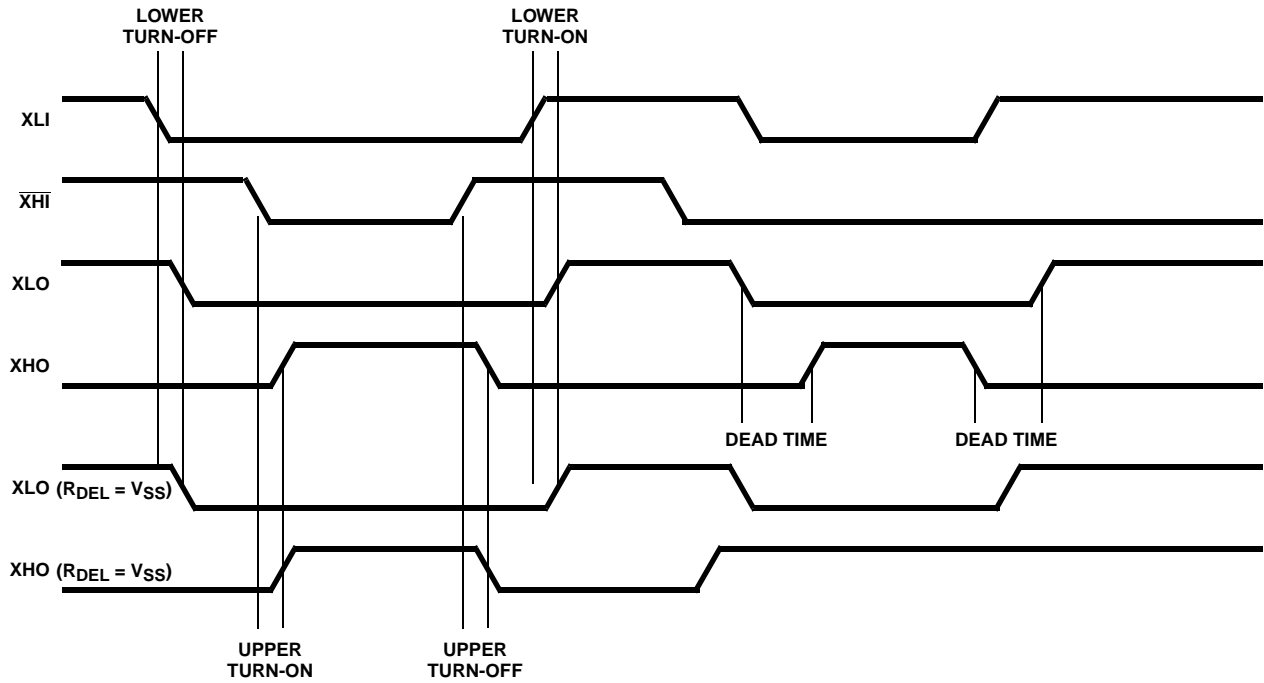


FIGURE 1.

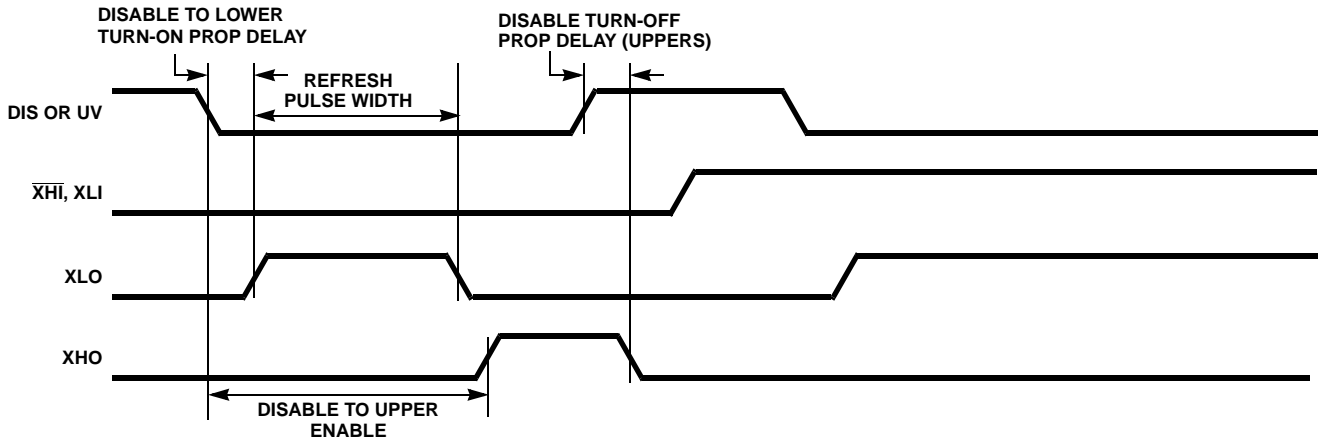


FIGURE 2. DISABLE FUNCTION

NOTES:

- 4. X means any "A", "B", or "C" phase.
- 5. With RDEL resistor tied to  $V_{DD}$ , lowers and uppers cannot be turned on at the same time. Low side logic overrides high side logic unless  $R_{DEL} < 100mV$ .

Typical Performance Curves

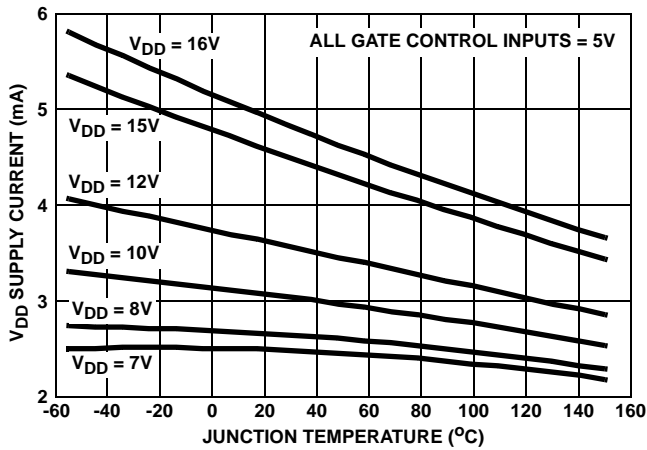


FIGURE 3.  $V_{DD}$  SUPPLY CURRENT vs  $V_{DD}$  SUPPLY VOLTAGE

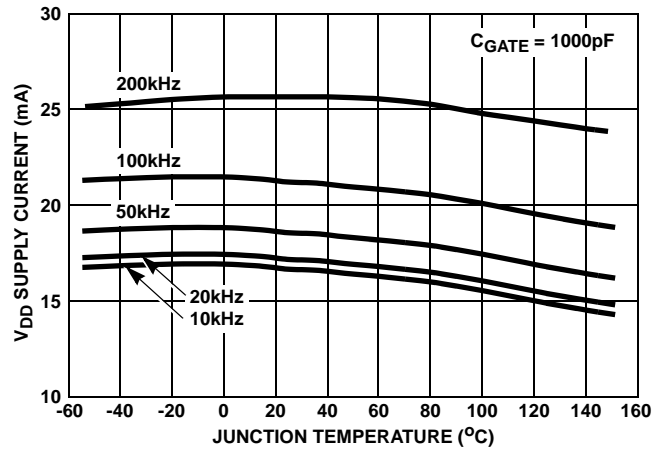


FIGURE 4.  $V_{DD}$  SUPPLY CURRENT vs SWITCHING FREQUENCY

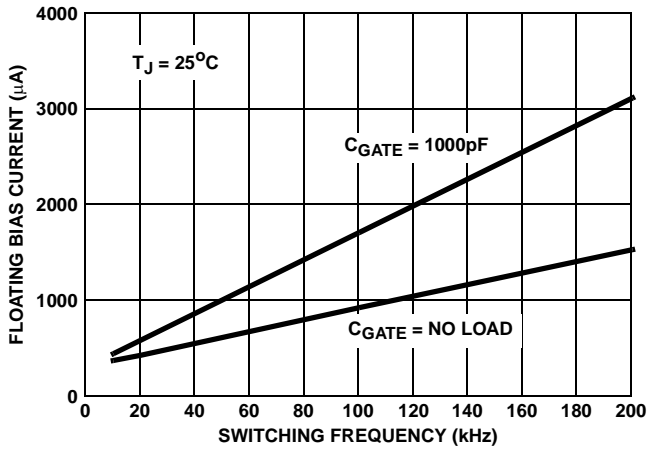


FIGURE 5. FLOATING  $I_{xHB}$  BIAS CURRENT

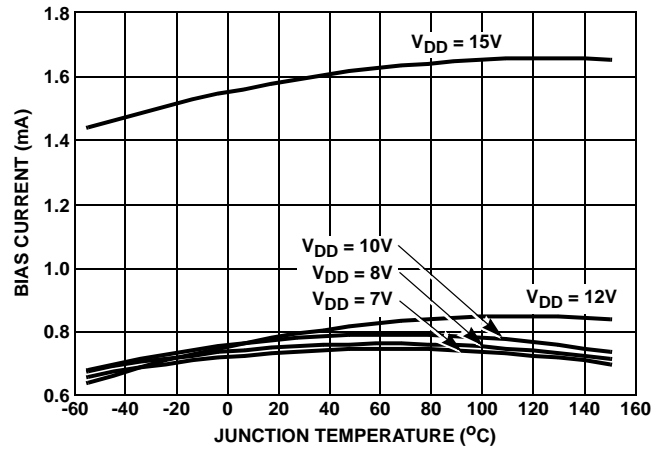


FIGURE 6. OFF-STATE  $I_{xHB}$  BIAS CURRENT

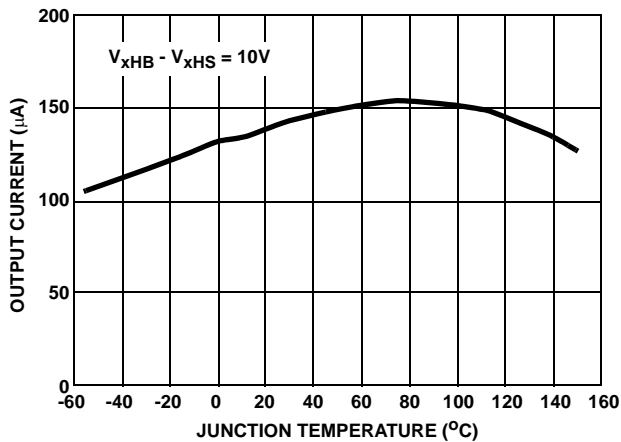


FIGURE 7. CHARGE PUMP OUTPUT CURRENT

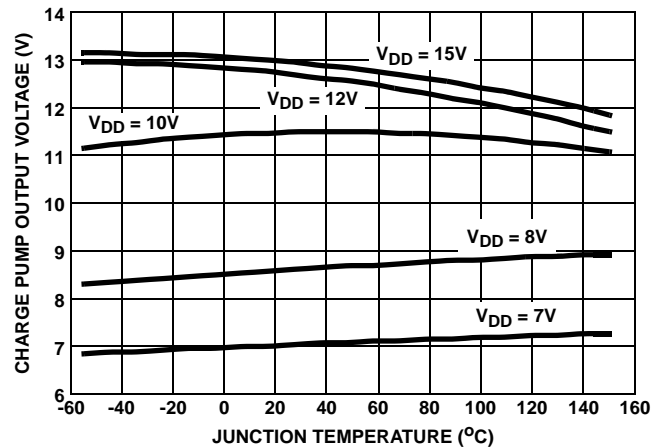


FIGURE 8. CHARGE PUMP OUTPUT VOLTAGE

Typical Performance Curves (Continued)

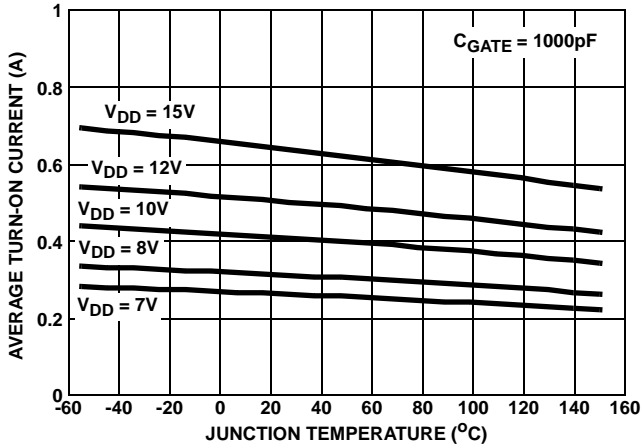


FIGURE 9. AVERAGE TURN-ON CURRENT (0 TO 5V)

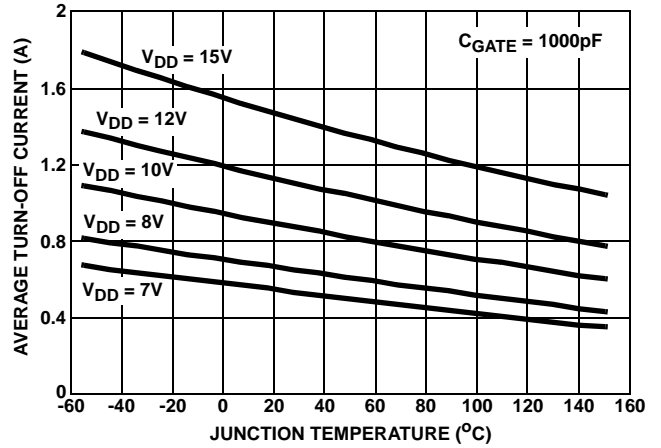


FIGURE 10. AVERAGE TURN-OFF CURRENT ( $V_{DD}$  TO 4V)

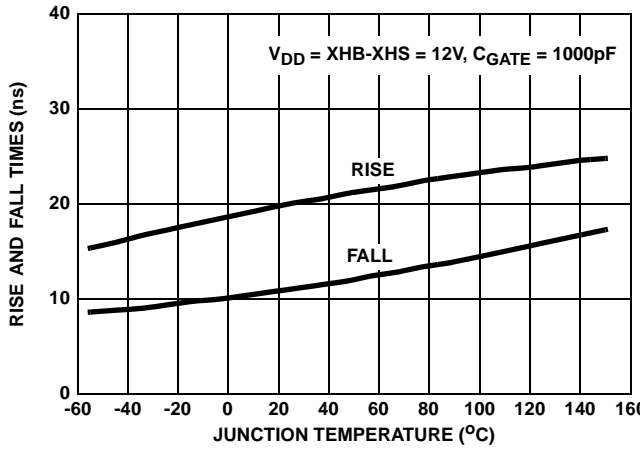


FIGURE 11. RISE AND FALL TIMES (10-90%)

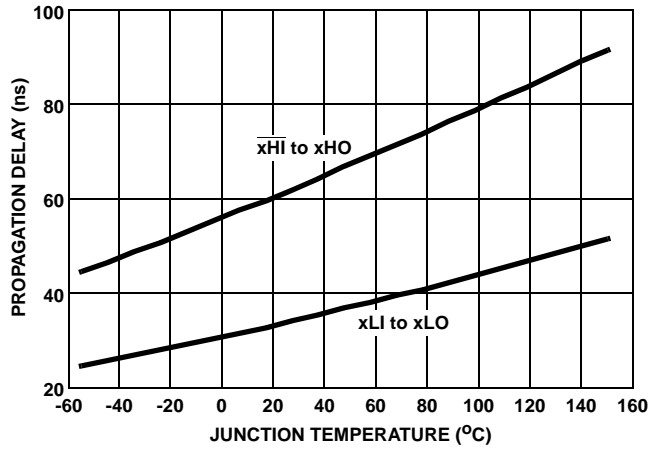


FIGURE 12. PROPAGATION DELAY

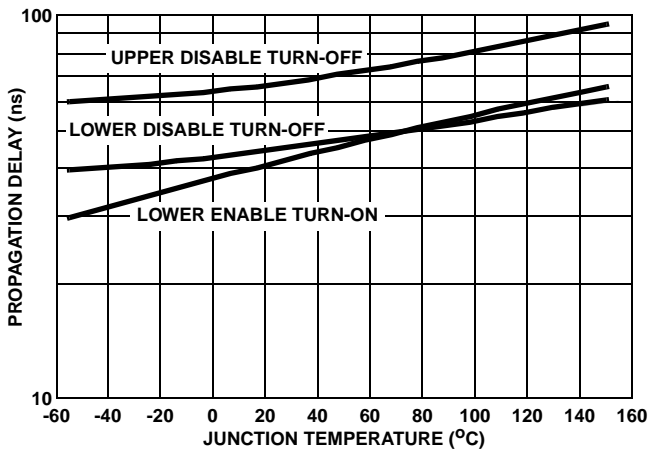


FIGURE 13. DISABLE PIN PROPAGATION DELAY

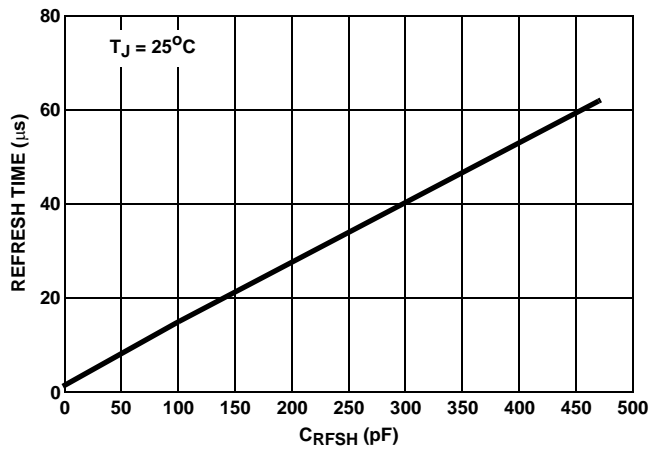


FIGURE 14. REFRESH TIME



Typical Performance Curves (Continued)

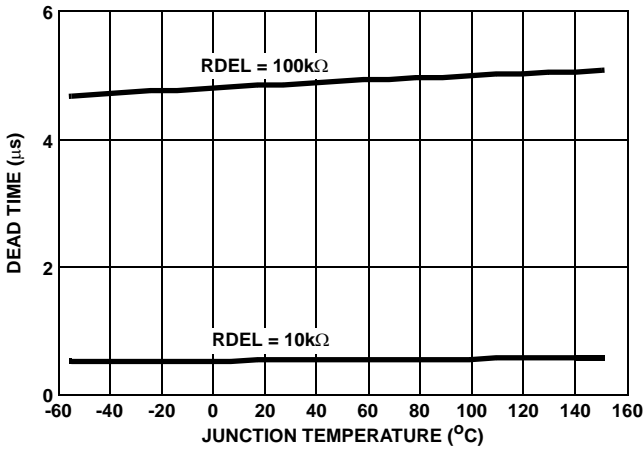


FIGURE 15. DEAD TIME

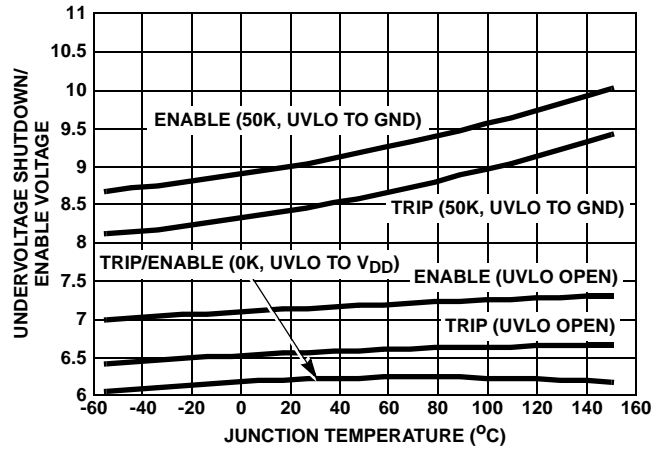


FIGURE 16. UNDERVOLTAGE THRESHOLD

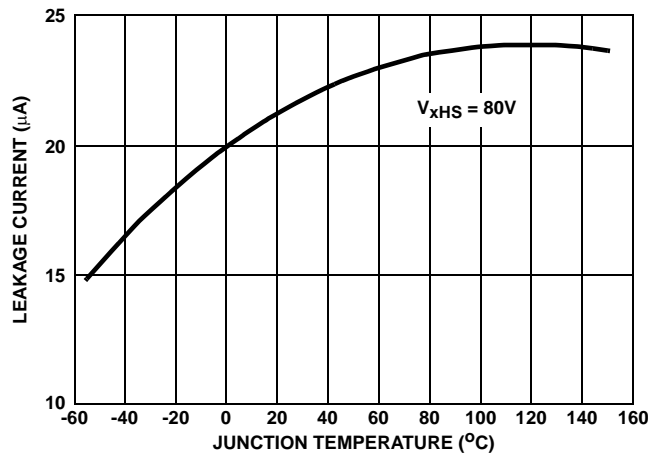


FIGURE 17. I<sub>xHS</sub> LEAKAGE CURRENT

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