



Product Overview

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MC100LVELT20: LVTTTL/LVCMOS to Differential LVPECL Translator

For complete documentation, see the data sheet

Product Description

The MC100LVELT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only +3.3 V and ground are required. The small outline SOIC8 package and the single gate of the MC100LVELT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

Features

- 390 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 0.8 GHz Typical
- Operating Range VCC = 3.0 V to 3.6 V with GND = 0 V
- PNP TTL Input for Minimal Loading
- Pb-Free Packages are Available

Applications

- Single ended to differential level translation.

Part Electrical Specifications

Product	Compliance	Status	Channels	Input Level	Output Level	V _{CC} Typ (V)	f _{Max} Typ (MHz)	t _{pd} Typ (ns)	t _R & t _F Max (ps)	Package Type
MC100LVELT20DG	Pb-free Halide free	Active	1	CMOS TTL	ECL	3.3	1000	0.37	180	SOIC-8
MC100LVELT20DR2 G	Pb-free Halide free	Active	1	CMOS TTL	ECL	3.3	1000	0.37	180	SOIC-8

Package Availability

Type	Pb-free	Standard
SOIC-8	✓	

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