

MC74VHCT139A

Dual 2-to-4 Decoder/ Demultiplexer

The MC74VHCT139A is an advanced high speed CMOS 2-to-4 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL devices while maintaining CMOS low power dissipation.

When the device is enabled ($\bar{E} = \text{low}$), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device output is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS logic, or from 1.8 V CMOS logic to 3.0 V CMOS logic while operating at the high-voltage power supply

The MC74VHCT139A input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHCT139A to be used to interface 5.0 V circuits to 3.0 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage-input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 5.0$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- Pb-Free Packages are Available*

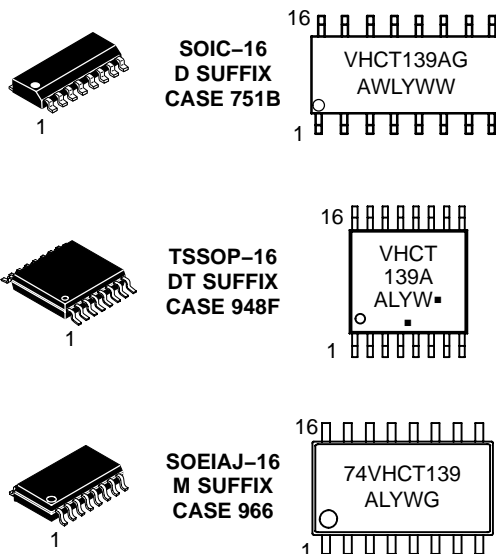
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or \blacksquare = Pb-Free Package
 (Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | | Outputs | | | |
|--------|----|----|---------|----|----|----|
| E | A1 | A0 | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74VHCT139A

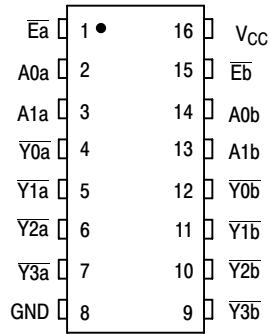


Figure 1. Pin Assignment

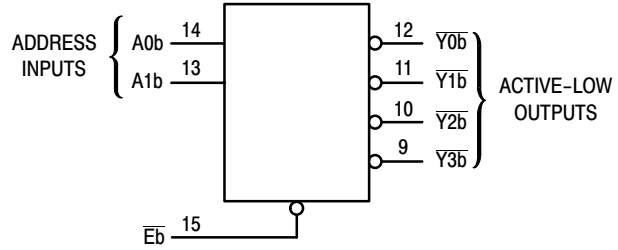
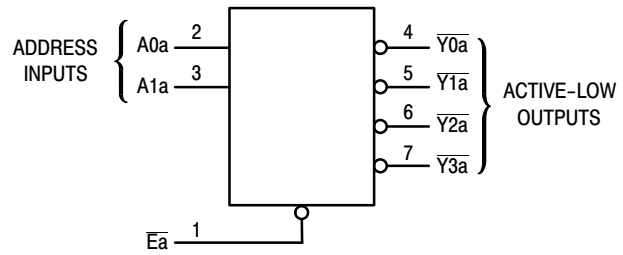


Figure 2. Logic Diagram

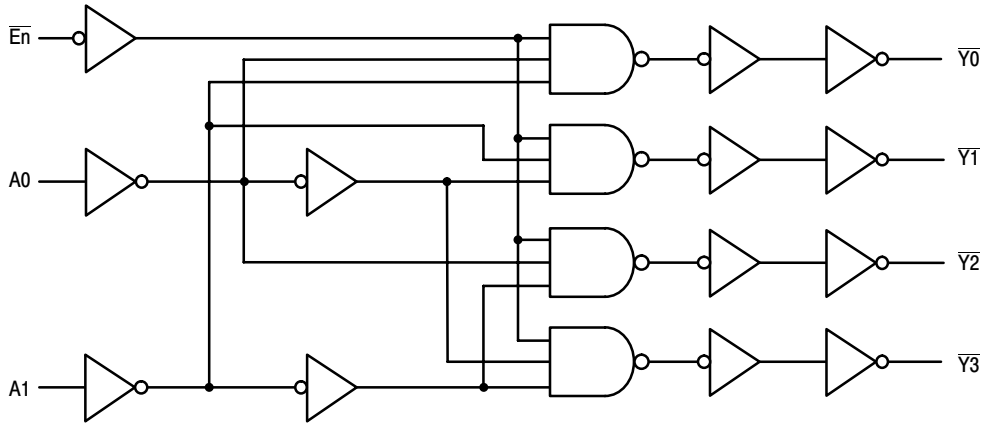


Figure 3. Expanded Logic Diagram
(1/2 of Device)

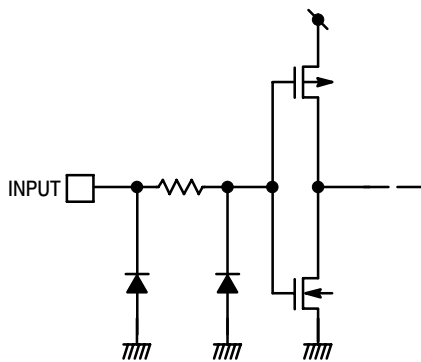


Figure 4. Input Equivalent Circuit

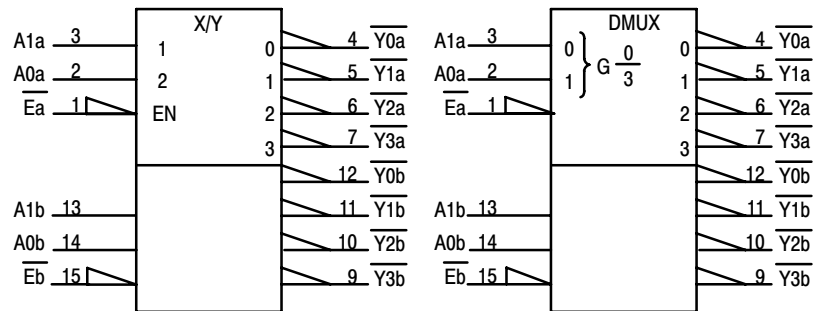


Figure 5. IEC Logic Diagram

MC74VHCT139A

MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Value | Unit |
|----------------------|---|--|------|
| V _{CC} | Positive DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | Digital Input Voltage | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage Output in 3-State High or Low State | -0.5 to +7.0 -0.5 to V _{CC} +0.5 | V |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current | ± 20 | mA |
| I _{OUT} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 75 | mA |
| P _D | Power Dissipation in Still Air SOIC Package TSSOP | 200 180 | mW |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| V _{ESD} | ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) | >2000 >200 >2000 | V |
| I _{LATCHUP} | Latchup Performance Above V _{CC} and Below GND at 125°C (Note 5) | ± 300 | mA |
| θ _{JA} | Thermal Resistance, Junction-to-Ambient SOIC Package TSSOP | 143 164 | °C/W |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

2. Tested to EIA/JESD22-A114-A

3. Tested to EIA/JESD22-A115-A

4. Tested to JESD22-C101-A

5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---------------------------------|--|--------|------------------------|------|
| V _{CC} | DC Supply Voltage | 4.5 | 5.5 | V |
| V _{IN} | DC Input Voltage | 0 | 5.5 | V |
| V _{OUT} | DC Output Voltage Output in 3-State High or Low State | 0 0 | 5.5 V _{CC} | V |
| T _A | Operating Temperature Range, all Package Types | -55 | 125 | °C |
| t _r , t _f | Input Rise or Fall Time V _{CC} = 5.0 V ± 0.5 V | 0 | 20 | ns/V |

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

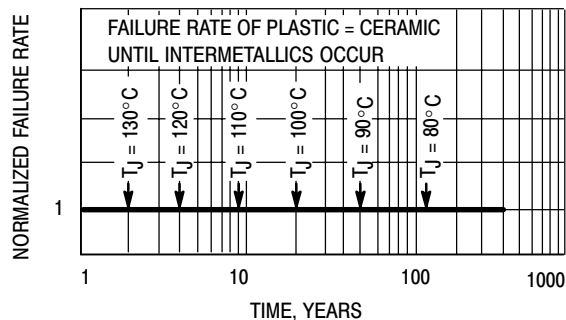


Figure 6. Failure Rate vs. Time Junction Temperature

MC74VHCT139A

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | T _A = -55 to 125°C | | Unit |
|--------------------|---|--|------------------------|-----------------------|-----|------|-----------------------|------|-------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| V _{IL} | Maximum Low-Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| V _{OH} | Maximum High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 4.5 | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -8 mA | 4.5 | 3.94 | | | 3.8 | | 3.66 | | V |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 4.5 | | 0 | 0.1 | | 0.1 | | 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 8 mA | 4.5 | | | 0.36 | | 0.44 | | 0.52 | V |
| I _{IN} | Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 4.0 | | 40.0 | | 40.0 | μA |
| I _{CC(T)} | Additional Quiescent Supply Current (per Pin) | Any one input: V _{IN} = 3.4 V All other inputs: V _{IN} = V _{CC} or GND | 5.5 | | | 1.35 | | 1.5 | | 1.5 | μA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5 V | 0 | | | 0.5 | | 5 | | 5 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | T _A = -55 to 125°C | | Unit |
|--|---|--|-----------------------|------------|--------------|-----------------------|--------------|-------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 7.2 9.7 | 11.0 14.5 | 1.0 1.0 | 13.0 16.5 | 1.0 1.0 | 13.0 16.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 5.0 6.5 | 7.2 9.2 | 1.0 1.0 | 8.5 10.5 | 1.0 1.0 | 8.5 10.5 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, \bar{E} to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 6.4 8.9 | 9.2 12.7 | 1.0 1.0 | 11.0 14.5 | 1.0 1.0 | 11.0 14.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 4.4 5.9 | 6.3 8.3 | 1.0 1.0 | 7.5 9.5 | 1.0 1.0 | 7.5 9.5 | |
| C _{IN} | Maximum Input Capacitance | | | 4 | 10 | | 10 | | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 6) | Typical @ 25°C, V _{CC} = 5.0V | | pF |
|-----------------|--|--|--|----|
| | | 26 | | |
| | | | | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per decoder). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHCT139A

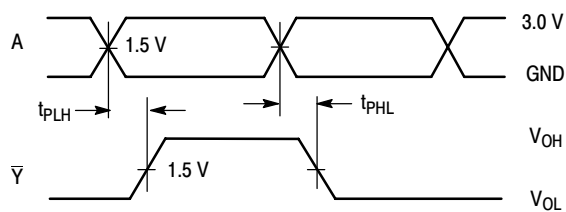


Figure 7. Switching Waveform

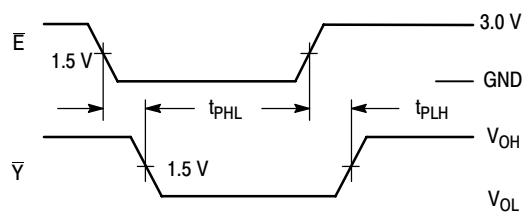
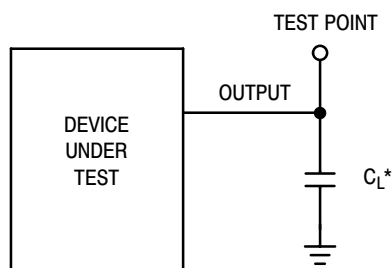


Figure 8. Switching Waveform



*Includes all probe and jig capacitance

Figure 9. Test Circuit

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|---------------------|-----------------------|
| MC74VHCT139AD | SOIC-16 | 48 Units / Rail |
| MC74VHCT139ADG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC74VHCT139ADR2 | SOIC-16 | 2500 Tape & Reel |
| MC74VHCT139ADR2G | SOIC-16 (Pb-Free) | 2500 Tape & Reel |
| MC74VHCT139ADT | TSSOP-16* | 96 Units / Rail |
| MC74VHCT139ADTG | TSSOP-16* | 96 Units / Rail |
| MC74VHCT139ADTR2 | TSSOP-16* | 2500 Tape & Reel |
| MC74VHCT139ADTRG | TSSOP-16* | 2500 Tape & Reel |
| MC74VHCT139AM | SOEIAJ-16 | 50 Units / Rail |
| MC74VHCT139AMG | SOEIAJ-16 (Pb-Free) | 50 Units / Rail |
| MC74VHCT139AMEL | SOEIAJ-16 | 2000 Tape & Reel |
| MC74VHCT139AMELG | SOEIAJ-16 (Pb-Free) | 2000 Tape & Reel |

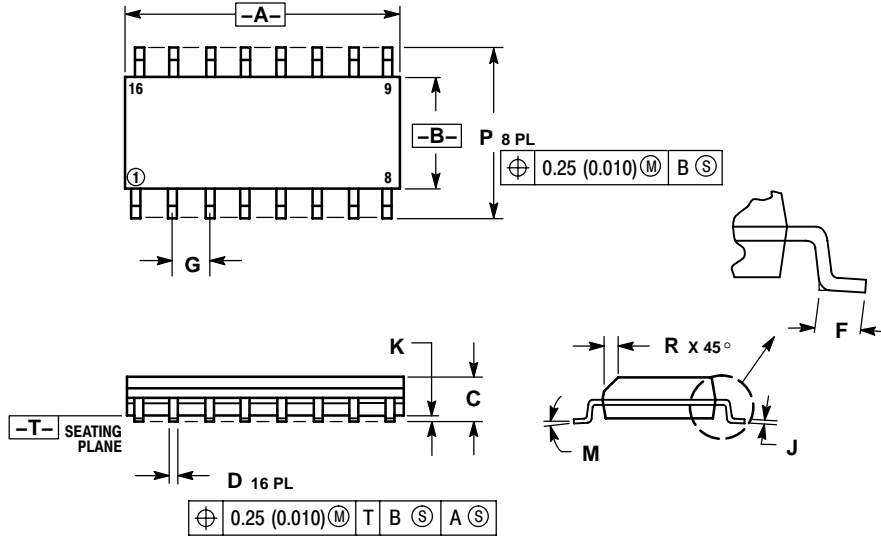
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74VHCT139A

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J

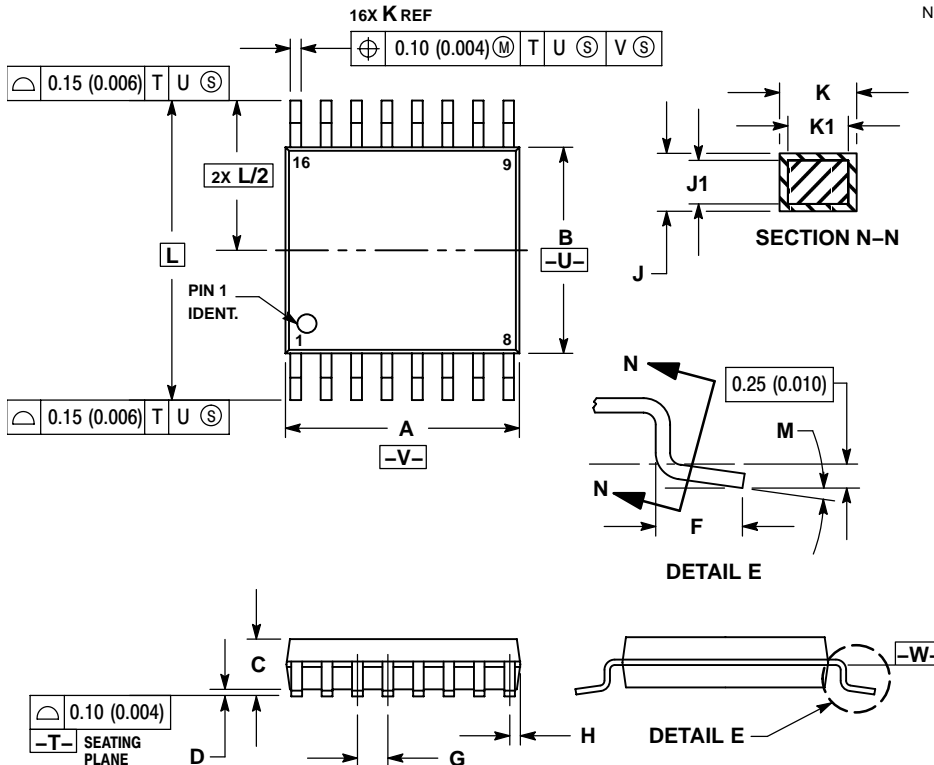


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE A



NOTES:

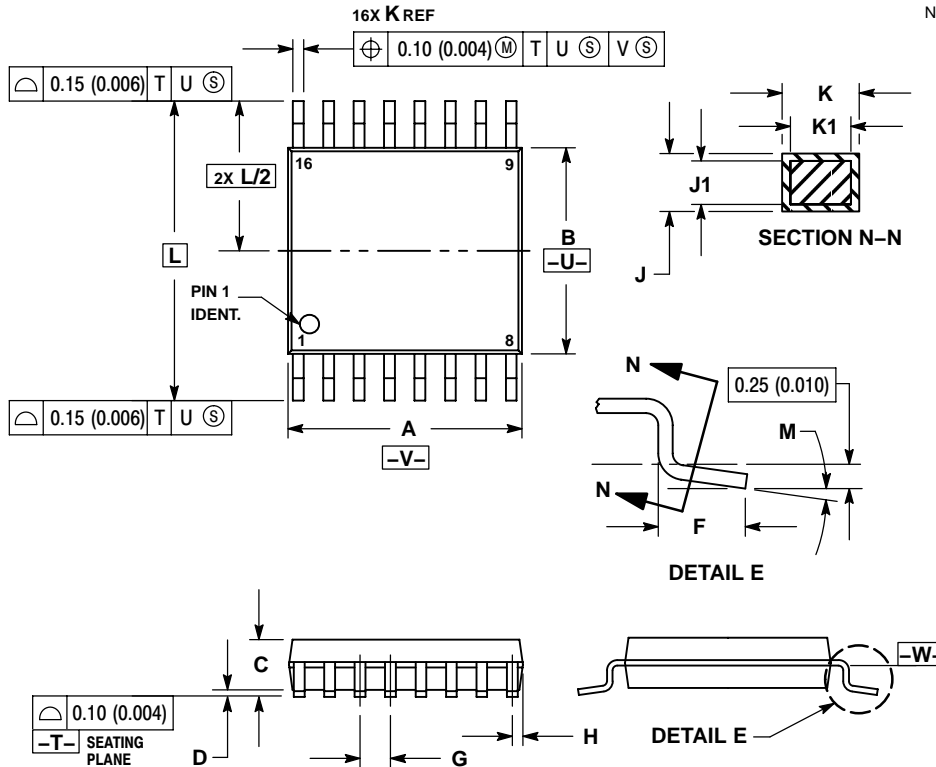
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74VHCT139A

PACKAGE DIMENSIONS

SOEIAJ-16
M SUFFIX
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.