SN54AS250A, SN74AS250A 1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDAS137A - DECEMBER 1983 - REVISED DECEMBER 1994

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:

Boolean Function Generator Parallel-to-Serial Converter Data Source Selector

- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

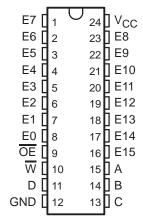
The 'AS250A devices provide full binary decoding to select 1-of-16 data inputs or use sources as an input with an inverting \overline{W} output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered output-enable (\overline{OE}) input can be used for n-line to 1-line cascading. Taking \overline{OE} high places the output in the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

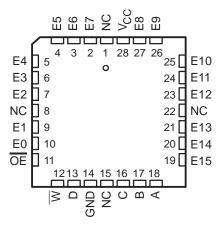
OE does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

The SN54AS250A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS250A is characterized for operation from 0°C to 70°C.

SN54AS250A . . . JT PACKAGE SN74AS250A . . . DW OR NT PACKAGE (TOP VIEW)



SN54AS250A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

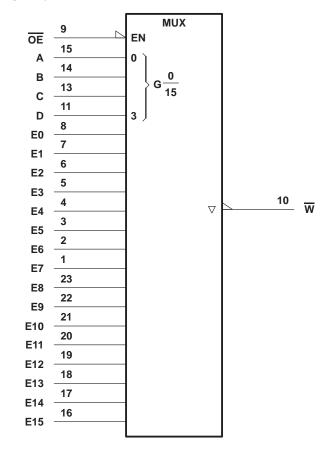
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FUNCTION TABLE

	OUTPUT					
ŌĒ	Α	В	С	D	Ei	W
L	L	L	L	L	E0	E0
L	Н	L	L	L	E1	E ₁
L	L	Н	L	L	E2	E ₂
L	Н	Н	L	L	E3	E 3
L	L	L	Н	L	E4	E 4
L	Н	L	Н	L	E5	<u>E</u> 5
L	L	Н	Н	L	E6	E 6
L	Н	Н	Н	L	E7	E7
L	L	L	L	Н	E8	E8
L	Н	L	L	Н	E9	E 9
L	L	Н	L	Н	E10	E 10
L	Н	Н	L	Н	E11	E11
L	L	L	Н	Н	E12	E12
L	Н	L	Н	Н	E13	E13
L	L	Н	Н	Н	E14	E14
L	Н	Н	Н	Н	E15	E15
Н	Χ	Χ	Χ	Χ	Χ	Z

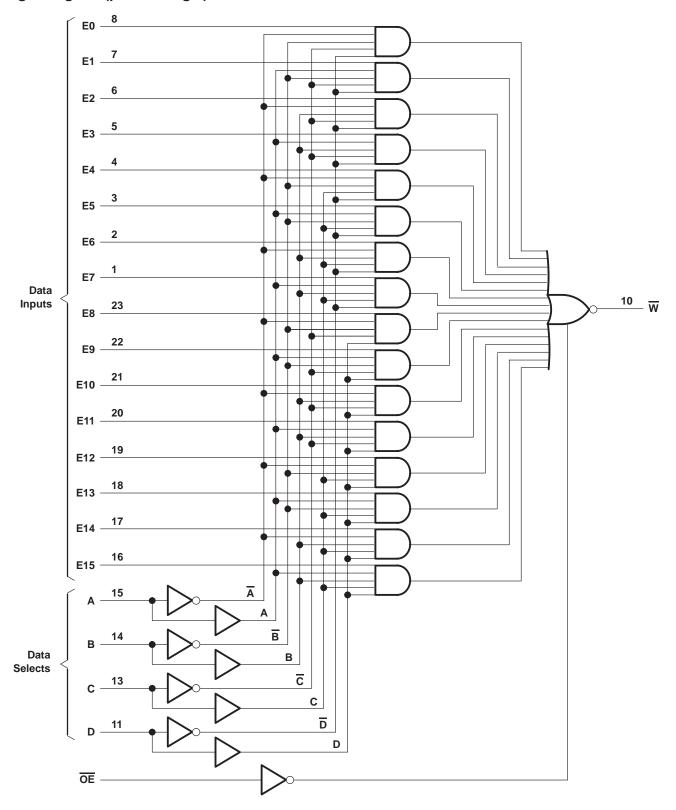
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}		 7 V
Input voltage, V _I		
Operating free-air temperature range, T _A :	SN54AS250A	 –55°C to 125°C
	SN74AS250A	 0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SN54AS250A			SN74AS250A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			8.0			8.0	V
IOH	High-level output current			-12			-15	mA
loL	Low-level output current			32			48	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD AMETER	TEST CONDITIONS			54AS25	0A	SN74AS250A				
PARAMETER				TYP‡	MAX	MIN	TYP‡	MAX	UNIT	
VIK	$V_{CC} = 4.5 \text{ V},$	$I_1 = -18 \text{ mA}$			-1.2			-1.2	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2			
Voн	V 45V	I _{OH} = -12 mA	2.4	3.3					V	
	V _{CC} = 4.5 V	$I_{OH} = -15 \text{ mA}$				2.4	3.3			
V	V _{CC} = 4.5 V	I _{OL} = 32 mA		0.35	0.5				V	
VOL		I _{OL} = 48 mA					0.35	0.5	V	
lozh	$V_{CC} = 5.5 \text{ V},$	V _O = 2.7 V			50			50	μΑ	
lozL	$V_{CC} = 5.5 \text{ V},$	V _O = 0.4 V			-50			-50	μΑ	
lį	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA	
lіН	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ	
I _{IL}	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.5			-0.5	mA	
IO [§]	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA	
	V _{CC} = 5.5 V	Outputs high		26	42		26	42		
ICC		Outputs low		31	50		31	50	mA	
		Outputs disabled		30	48		30	48		

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

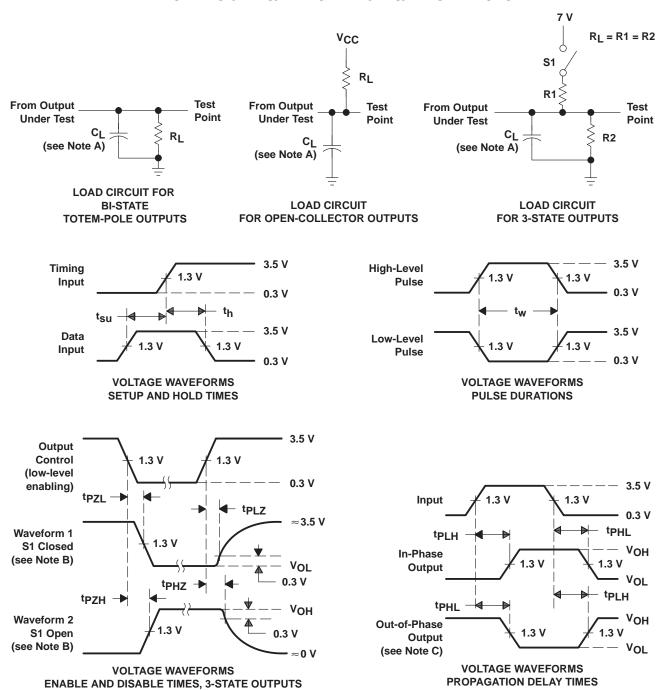
[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	= 50 pF = 500 Ω = 500 Ω = MIN t	2,		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	Data	$\overline{\mathbb{W}}$	2	9.5	2	8	
t _{PHL}	Data	VV	2	8.5	2	7	ns
t _{PLH}	A B C B	$\overline{\mathbb{W}}$	4	15.5	4	13	20
t _{PHL}	A, B, C, D	VV	4	12	4	10.5	ns
^t PZH	ŌĒ	$\overline{\mathbb{W}}$	2	7.5	2	7	
t _{PZL}	ÜE	VV	2	10	2	9	ns
^t PHZ	ŌĒ	$\overline{\mathbb{W}}$	1.5	6.5	1.5	6	ne
t _{PLZ}	OE	VV	2	8.5	2	6.5	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_{\Gamma} = t_{f} = 2$ ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGE OPTION ADDENDUM

www.ti.com 29-Apr-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9056201LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN74AS250ANT	NRND	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS250ANT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN74AS250ANTE4	NRND	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54AS250AJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



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