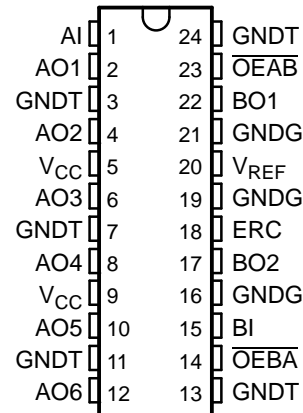


FEATURES

- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTL8-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTL8 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGV, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTL817 is a medium-drive fanout driver that provides LVTTL-to-GTL8 and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, and OEC™ circuitry. The improved GTLP OEC circuitry minimizes bus settling time and has been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω. BO1 and BO2 can be tied together to drive an equivalent load impedance down to 11 Ω.

GTL8 is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTL817 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

GNDT is the TTL output ground, while GNDG is the GTLP output ground, and both may be separated from each other for a quieter device.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

OEC, TI are trademarks of Texas Instruments.

SN74GTLP817

GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E–OCTOBER 1999–REVISED APRIL 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load. ERC automatically is selected to the same speed as alternate source 1-to-6 fanout drivers that use pin 18 for 3.3-V or 5-V V_{CC} .

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP817DW	GTLP817
		Tape and reel	SN74GTLP817DWR	
	TSSOP – PW	Tape and reel	SN74GTLP817PWR	GT817
	TVSOP – DGV	Tape and reel	SN74GTLP817DGVR	GT817

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTLP translation and GTLP-to-LVTTL translation in the same package.

The LVTTL-to-GTLP direction is a 1-to-2 fanout driver with a single output enable (\overline{OEAB}).

The GTLP-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable ($\overline{OEB A}$).

Data polarity is inverting for both directions.

FUNCTION TABLES

OUTPUT CONTROL
(A TO B)

INPUTS		OUTPUT BOn	MODE
AI	\overline{OEAB}		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

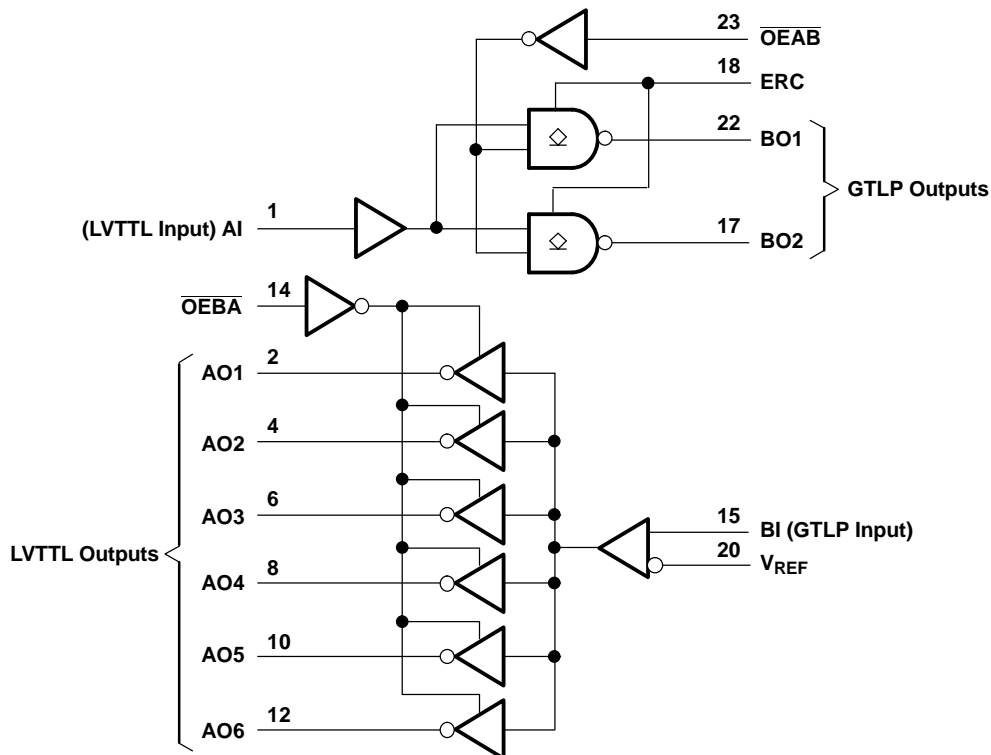
OUTPUT CONTROL
(B TO A)

INPUTS		OUTPUT AOn	MODE
BI	\overline{OEBA}		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V _{CC}	Slow
L	GND	Fast

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74GTLP817

GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E—OCTOBER 1999—REVISED APRIL 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage range	-0.5	4.6	V	
$ V_{GNDG} - V_{GNDT} $	Ground dc voltage difference		0.3	V	
V_I	Input voltage range ⁽²⁾	AI port and control inputs	-0.5	7	V
		BI port and V_{REF}	-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	AO port	-0.5	7	V
		BO port	-0.5	4.6	
I_O	Current into any output in the low state	AO port		24	mA
		BO port		100	
I_O	Current into any A output in the high state ⁽³⁾		24	mA	
	Continuous current through each V_{CC} or GND		± 100	mA	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA	
I_{OK}	Output clamp current	$V_O < 0$	-50	mA	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGV package		86	°C/W
		DW package		46	
		PW package		88	
T_{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	BI			V_{TT}	V
		AI, \overline{OE}		V_{CC}	5.5	
V_{IH}	High-level input voltage	BI	$V_{REF} + 0.05$			V
		ERC	$V_{CC} - 0.6$	V_{CC}	5.5	
		AI, \overline{OE}	2			
V_{IL}	Low-level input voltage	BI			$V_{REF} - 0.05$	V
		ERC		GND	0.6	
		AI, \overline{OE}			0.8	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO port			-12	mA
I_{OL}	Low-level output current	AO port			12	mA
		BO port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			μ s/V
T_A	Operating free-air temperature		-40		85	$^{\circ}$ C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Normal connection sequence is GND first and $V_{CC} = 3.3$ V, I/O, control inputs, V_{TT} , V_{REF} (any order) last.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} .

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V	
V_{OH}	AO port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OH} = -100\text{ }\mu\text{A}$			$V_{CC} - 0.2$	V	
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -100\text{ }\mu\text{A}$			$V_{CC} - 0.2$		
			$I_{OH} = -6\text{ mA}$			2.4		
			$I_{OH} = -12\text{ mA}$			2.2		
V_{OL}	AO port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V	
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2		
			$I_{OL} = 6\text{ mA}$			0.4		
			$I_{OL} = 12\text{ mA}$			0.5		
	BO port	$V_{CC} = 3.15\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2		
			$I_{OL} = 40\text{ mA}$			0.5		
$I_{OL} = 50\text{ mA}$					0.55			
I_I	BI, AI, \overline{OE} , ERC	$V_{CC} = 3.45\text{ V}$,	$V_I = 0\text{ or }5.5\text{ V}$			± 5	μA	
I_{OZH}	AO port	$V_{CC} = 3.45\text{ V}$	$V_O = V_{CC}$			10	μA	
	BO port		$V_O = 1.5\text{ V}$			5		
I_{OZL}	AO port	$V_{CC} = 3.45\text{ V}$	$V_O = \text{GND}$			-10	μA	
	BO port		$V_O = 5.5\text{ V}$			-5		
I_{CC}	AO or BO port	$V_{CC} = 3.45\text{ V}$, $I_O = 0$, V_I (AI or control input) = V_{CC} or GND, V_I (BI input) = V_{TT} or GND	Outputs high			10	mA	
			Outputs low			10		
			Outputs disabled			10		
$\Delta I_{CC}^{(2)}$	AI, \overline{OE}	$V_{CC} = 3.45\text{ V}$, One A-port or control input at $V_{CC} - 0.6\text{ V}$, Other A-port or control inputs at V_{CC} or GND				1	mA	
C_i	AI, \overline{OE} , ERC	$V_I = V_{CC}$ or 0				4	4.4	pF
	BI	$V_I = V_{TT}$ or 0				3.5	3.9	
C_o	AO port	$V_O = V_{CC}$ or 0				4	4.5	pF
	BO port	$V_O = V_{TT}$ or 0				5	5.4	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the increase in supply current for each input that is at the specified LVTTTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0\text{ to }5.5\text{ V}$			10	μA
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$,	$V_O = 0.5\text{ V to }3\text{ V}$,	$\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$,	$V_O = 0.5\text{ V to }3\text{ V}$,	$\overline{OE} = 0$		± 30	μA

Hot-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0\text{ to }1.5\text{ V}$			10	μA
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$,	$V_O = 0.5\text{ V to }1.5\text{ V}$,	$\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$,	$V_O = 0.5\text{ V to }1.5\text{ V}$,	$\overline{OE} = 0$		± 30	μA

Switching Characteristics

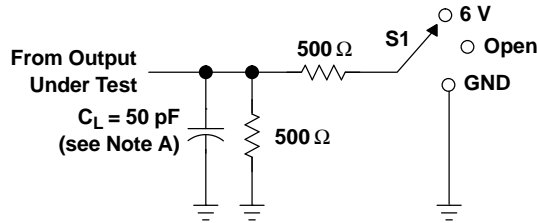
over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
t_{PLH}	AI	BO	Slow	3		6	ns
t_{PHL}				1.8		4.7	
t_{PLH}	AI	BO	Fast	2		5	ns
t_{PHL}				1.5		4.2	
t_{en}	\overline{OEAB}	BO	Slow	3		6.1	ns
t_{dis}				2		4.7	
t_{en}	\overline{OEAB}	BO	Fast	2.1		6	ns
t_{dis}				1.5		4.7	
t_r	Rise time, B outputs (20% to 80%)		Slow	2.5		ns	
			Fast	1.4			
t_f	Fall time, B outputs (80% to 20%)		Slow	1.7		ns	
			Fast	1			
t_{PLH}	BI	AO		2.3		6	ns
t_{PHL}				1.9		4.7	
t_{en}	\overline{OEBA}	AO		1.1		6.3	ns
t_{dis}				1.2		5	

(1) Slow (ERC = V_{CC}) and Fast (ERC = GND)

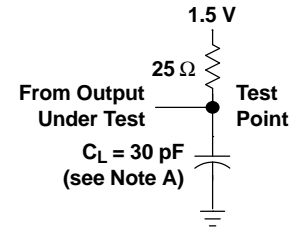
(2) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

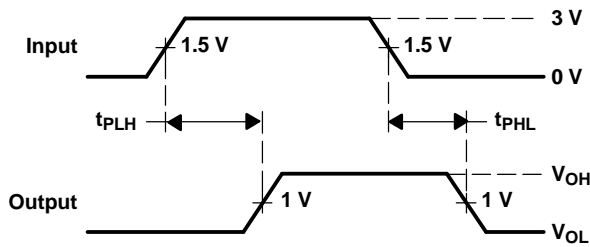


LOAD CIRCUIT FOR AO PORTS

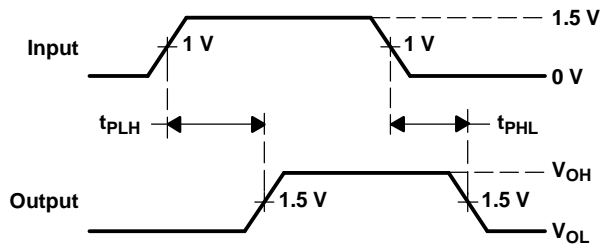
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



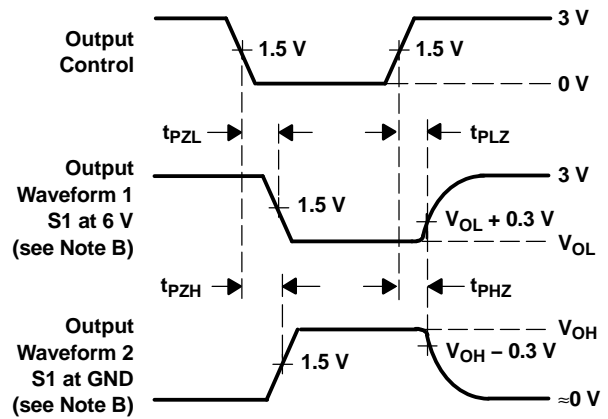
LOAD CIRCUIT FOR BO PORTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to BO port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(BI to AO port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO ports)

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

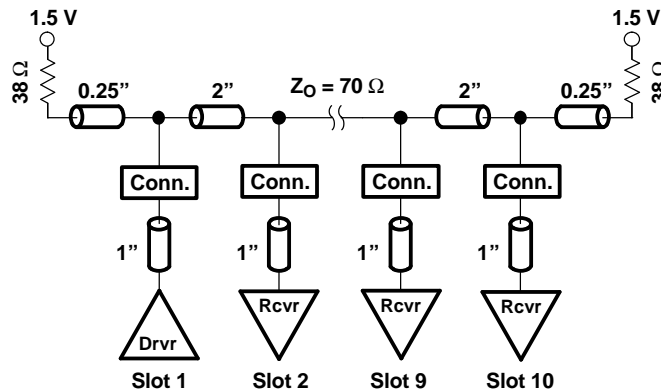


Figure 2. Medium-Drive Test Backplane

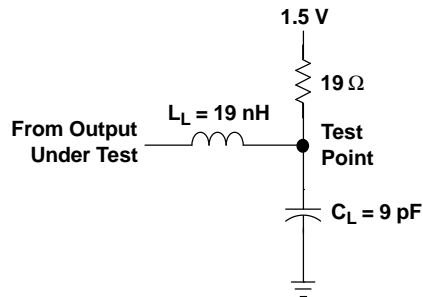


Figure 3. Medium-Drive RLC Network

SN74GTL817

GTL817-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E—OCTOBER 1999—REVISED APRIL 2005

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE ⁽¹⁾	TYP ⁽²⁾	UNIT
t_{PLH}	AI	BO	Slow	4.4	ns
t_{PHL}				4.4	
t_{PLH}	AI	BO	Fast	3.2	ns
t_{PHL}				3.2	
t_{en}	\overline{OEAB}	BO	Slow	4	ns
t_{dis}				4.4	
t_{en}	\overline{OEAB}	BO	Fast	2.9	ns
t_{dis}				3.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	1.8	ns
			Fast	1	
t_f	Fall time, B outputs (80% to 20%)		Slow	2	ns
			Fast	1.6	

(1) Slow (ERC = V_{CC}) and Fast (ERC = GND)

(2) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74GTL817PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL817PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL817PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL817PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL817PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL817PWG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL817PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

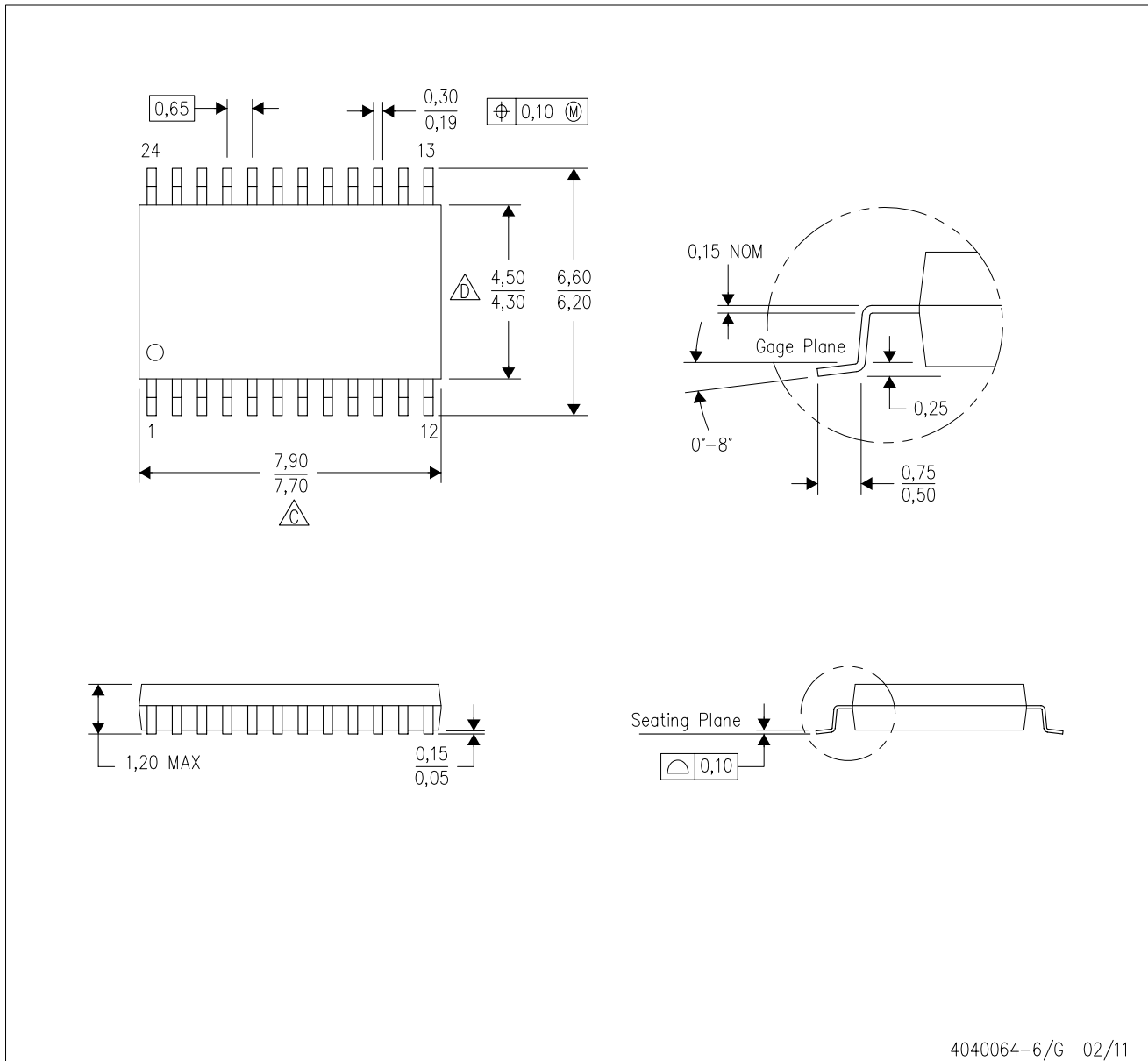
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLP817PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

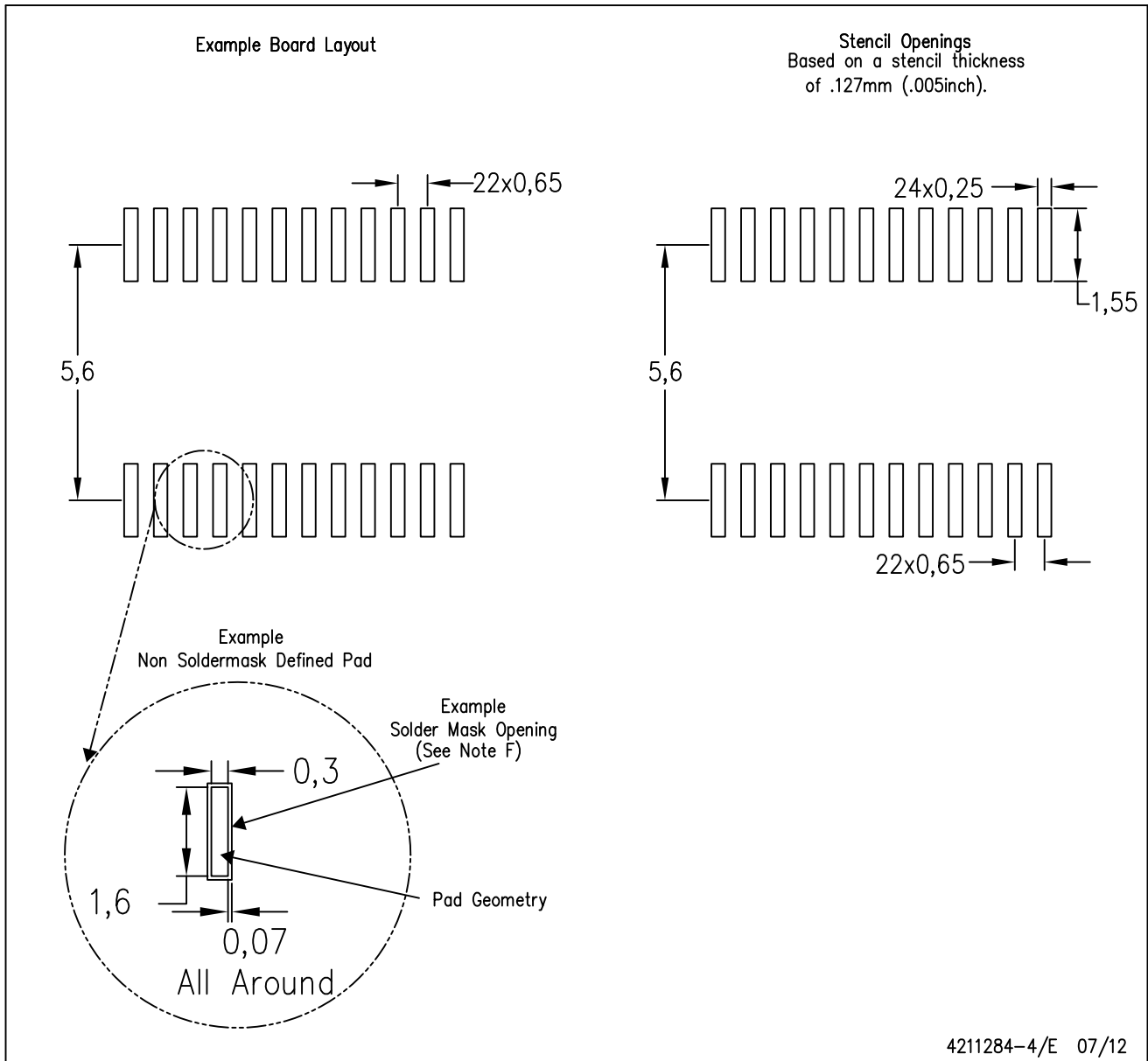


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4211284-4/E 07/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com