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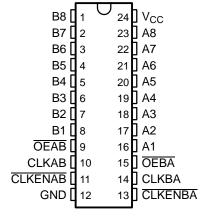
SN74LVC2952A OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS311I-JANUARY 1993-REVISED MARCH 2005

FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 8.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC2952A consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC - DW	Tube of 25	SN74LVC2952ADW	LVC2952A
	201C - DVV	Reel of 2000	SN74LVC2952ADWR	LVC2932A
SOP - NS		Reel of 2000	SN74LVC2952ANSR	LVC2952A
-40°C to 85°C	SSOP - DB	Reel of 2000	SN74LVC2952ADBR	LE952A
	TSSOP – PW	Tube of 60	SN74LVC2952APW	
		Reel of 2000	SN74LVC2952APWR	LE952A
		Reel of 250	SN74LVC2952APWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

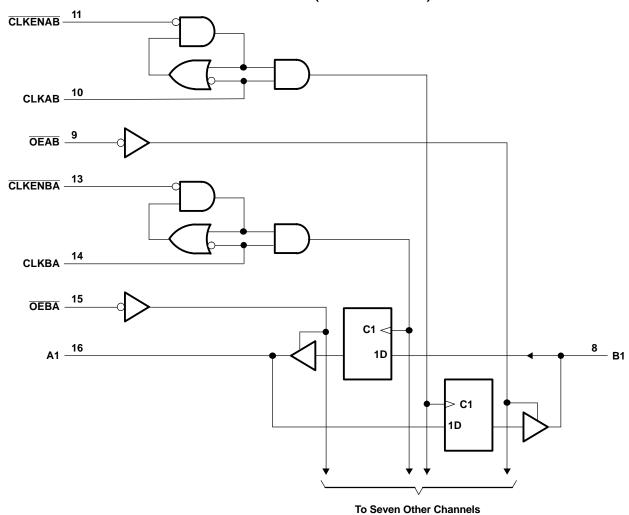


FUNCTION TABLE(1)

	INPUTS			OUTPUT
CLKENAB	CLKAB	OEAB	Α	В
Н	Χ	L	Х	B ₀ ⁽²⁾
X	H or L	L	Χ	B ₀ ⁽²⁾ B ₀ ⁽²⁾
L	\uparrow	L	L	L
L	\uparrow	L	Н	Н
X	Χ	Н	Χ	Z

- (1) A-to-B data flow is shown; B-to-A data flow is similar, but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
- (2) Level of B before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)





WITH 3-STATE OUTPUTS
SCAS311I-JANUARY 1993-REVISED MARCH 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range ⁽²⁾		-0.5	6.5	V	
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state ⁽²⁾	-0.5	6.5	V	
Vo	Voltage range applied to any output in the h	-0.5	V _{CC} + 0.5	V		
I _{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current			±50	mA	
	Continuous current through V _{CC} or GND			±100	mA	
		DB package		63		
0	Package thermal impedance (4)	DW package		46	°C/W	
θ_{JA}	Package thermal impedance (*)	NS package		65	-C/VV	
		PW package		88		
T _{stg}	Storage temperature range		-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT			
V	Cumply voltage	Operating	1.65	3.6	V			
V_{CC}	Supply voltage	Data retention only	1.5		V			
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$					
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V			
		V _{CC} = 2.7 V to 3.6 V	2					
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$				
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V			
		V _{CC} = 2.7 V to 3.6 V						
VI	Input voltage	·	0	5.5	V			
V	Output valtage	High or low state	0	V _{CC}	V			
Vo	Output voltage	3-state	0	5.5	V			
		V _{CC} = 1.65 V		-4				
	High level output ourrent	V _{CC} = 2.3 V		-8	mA			
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12	mA			
		V _{CC} = 3 V		-24				
		V _{CC} = 1.65 V		4				
	Low lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		8	A			
l _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA			
		V _{CC} = 3 V		24				
Δt/Δν	Input transition rise or fall rate			10	ns/V			
T _A	Operating free-air temperature		-40	85	°C			

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC2952A **OCTAL BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS

SCAS311I-JANUARY 1993-REVISED MARCH 2005



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
		$I_{OH} = -100 \mu A$		1.65 V to 3.6 V	V _{CC} – 0.2			
		I _{OH} = -4 mA		1.65 V	1.2			
.,		$I_{OH} = -8 \text{ mA}$	2.3 V	1.7			V	
V _{OH}		12 m		2.7 V	2.2			V
		$I_{OH} = -12 \text{ mA}$		3 V	2.4			
		$I_{OH} = -24 \text{ mA}$	3 V	2.2				
I _{OL} = 100 μA				1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45		
V _{OL}		I _{OL} = 8 mA	2.3 V			0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
I	Control inputs	V _I = 0 to 5.5 V		3.6 V			±5	μΑ
I _{off}		V_I or $V_O = 5.5 \text{ V}$		0			±10	μΑ
I _{OZ} ⁽²⁾		V _O = 0 to 5.5 V		3.6 V			±10	μΑ
Icc		V _I = V _{CC} or GND	1 - 0	3.6 V			10	^
		$3.6 \text{ V} \le \text{V}_1 \le 5.5 \text{ V}^{(3)}$	$I_0 = 0$	3.0 V	10		μΑ	
ΔI_{CC}	ΔI_{CC} One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{C}		at V _{CC} or GND	2.7 V to 3.6 V			500	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		5		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		рF

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = ± 0.1		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V \pm 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock} Clock frequency			(1)		(1)		150		150	MHz		
t _w	t _w Pulse duration, CLK high or low		(1)		(1)		3.3		3.3		ns	
	Catua tima	Data before CLK high	(1) (1)		1.7		1.3		20			
L _{su}	t _{su} Setup time	CLKEN before CLK high	(1)		(1)		1.3		1.1		ns	
	t _h Hold time	Data after CLK high	(1)		(1)		1.8		1.1		20	
^t h		CLKEN after CLK high	(1)		(1)		1.4		1.1		ns	

⁽¹⁾ This information was not available at the time of publication.

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) For I/O ports, the parameter I_{OZ} includes the input leakage current. (3) This applies in the disabled state only.



SCAS311I-JANUARY 1993-REVISED MARCH 2005

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	1.8 V 5 V	V _{CC} = ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = 3 ± 0.3	3.3 V 3 V	UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		(1)		150		150		MHz
t _{pd}	CLKAB or CLKBA	B or A	(1)	(1)	(1)	(1)		8.8	1	8.2	ns
t _{en}	ŌĒ	A or B	(1)	(1)	(1)	(1)		9	1	7.8	ns
t _{dis}	ŌĒ	A or B	(1)	(1)	(1)	(1)		8.8	1	7.8	ns
t _{sk(o)}										1	ns

⁽¹⁾ This information was not available at the time of publication.

Operating Characteristics

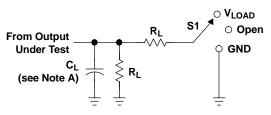
 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT		
C	Power dissipation capacitance	Outputs enabled	f = 10 MHz	(1)	(1)	79	pF	
C_{pd}	per transceiver	Outputs disabled	I = IO WINZ	(1)	(1)	41	pΕ	

⁽¹⁾ This information was not available at the time of publication.



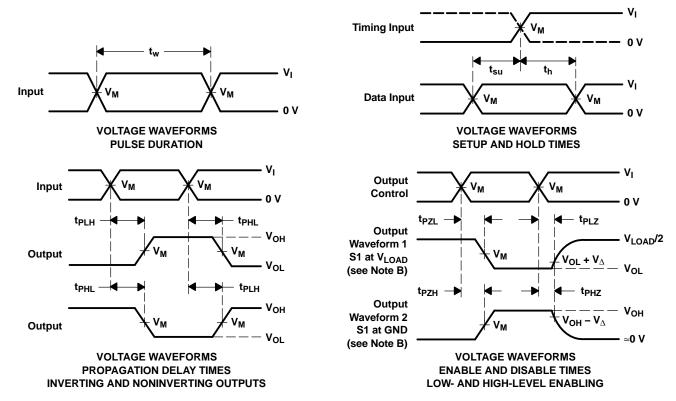
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

v	INF	PUTS	.,	V	•		.,
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



28-Aug-2010

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC2952ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	Samples Not Available
SN74LVC2952ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952ADGVR	OBSOLETE	TVSOP	DGV	24		TBD	Call TI	Call TI	Samples Not Available
SN74LVC2952ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	Samples Not Available
SN74LVC2952APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWTE4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74LVC2952APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples



PACKAGE OPTION ADDENDUM

28-Aug-2010

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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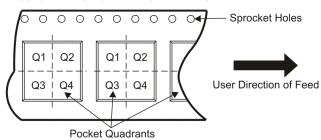
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2952ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC2952APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC2952APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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*All dimensions are nominal

Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LVC2952ADBR	SSOP	DB	24	2000	346.0	346.0	33.0	
SN74LVC2952APWR	TSSOP	PW	24	2000	346.0	346.0	33.0	
SN74LVC2952APWT	TSSOP	PW	24	250	346.0	346.0	33.0	

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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