

TIBPAL20L8-25C, TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C LOW-POWER HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

SRPS022A – D2920, MAY 1987 – REVISED DECEMBER 2010

- **Low-Power, High-Performance**
Reduced I_{CC} of 105 mA Max
 f_{max} :
Without Feedback . . . 33 MHz Min
With Feedback . . . 25 MHz Min
 t_{pd} . . . 25 ns Max
- **Direct Replacement for PAL20L8A, PAL20R4A, PAL20R6A, PAL20L8A, with at Least 50% Reduction in Power**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Plastic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

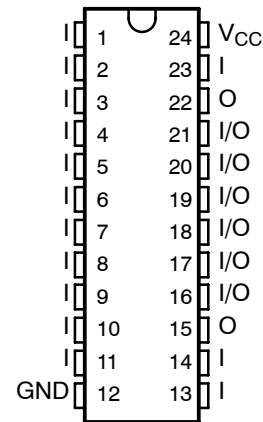
description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest AdvancedLow-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

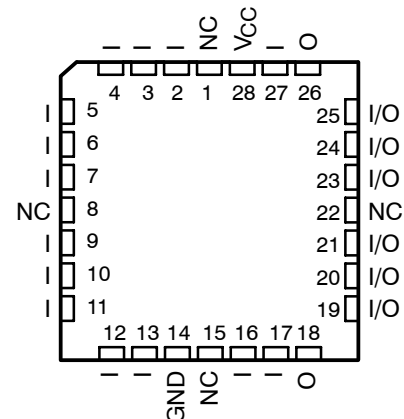
All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20¹ C series is characterized from 0°C to 75°C.

TIBPAL20L8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



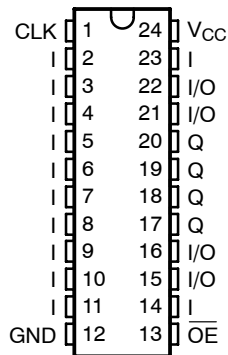
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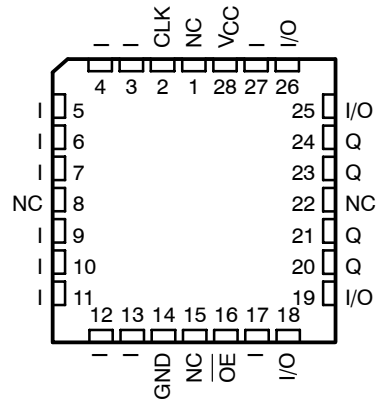
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SRPS022A – D2920, MAY 1987 – REVISED DECEMBER 2010

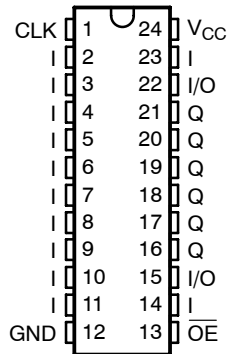
TIBPAL20R4'
JT OR NT PACKAGE
(TOP VIEW)



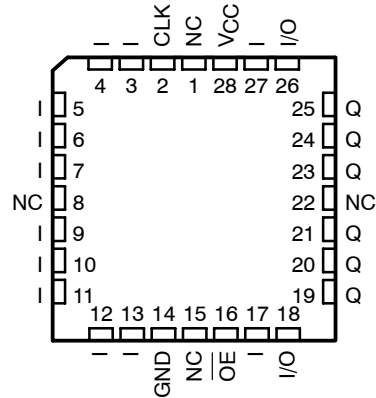
TIBPAL20R4'
FN PACKAGE
(TOP VIEW)



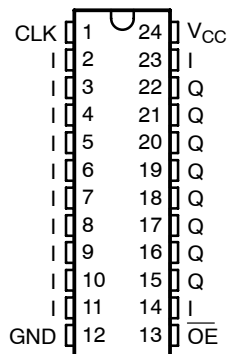
TIBPAL20R6'
JT OR NT PACKAGE
(TOP VIEW)



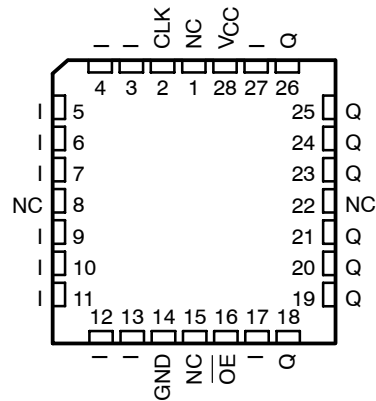
TIBPAL20R6'
FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC – No internal connection

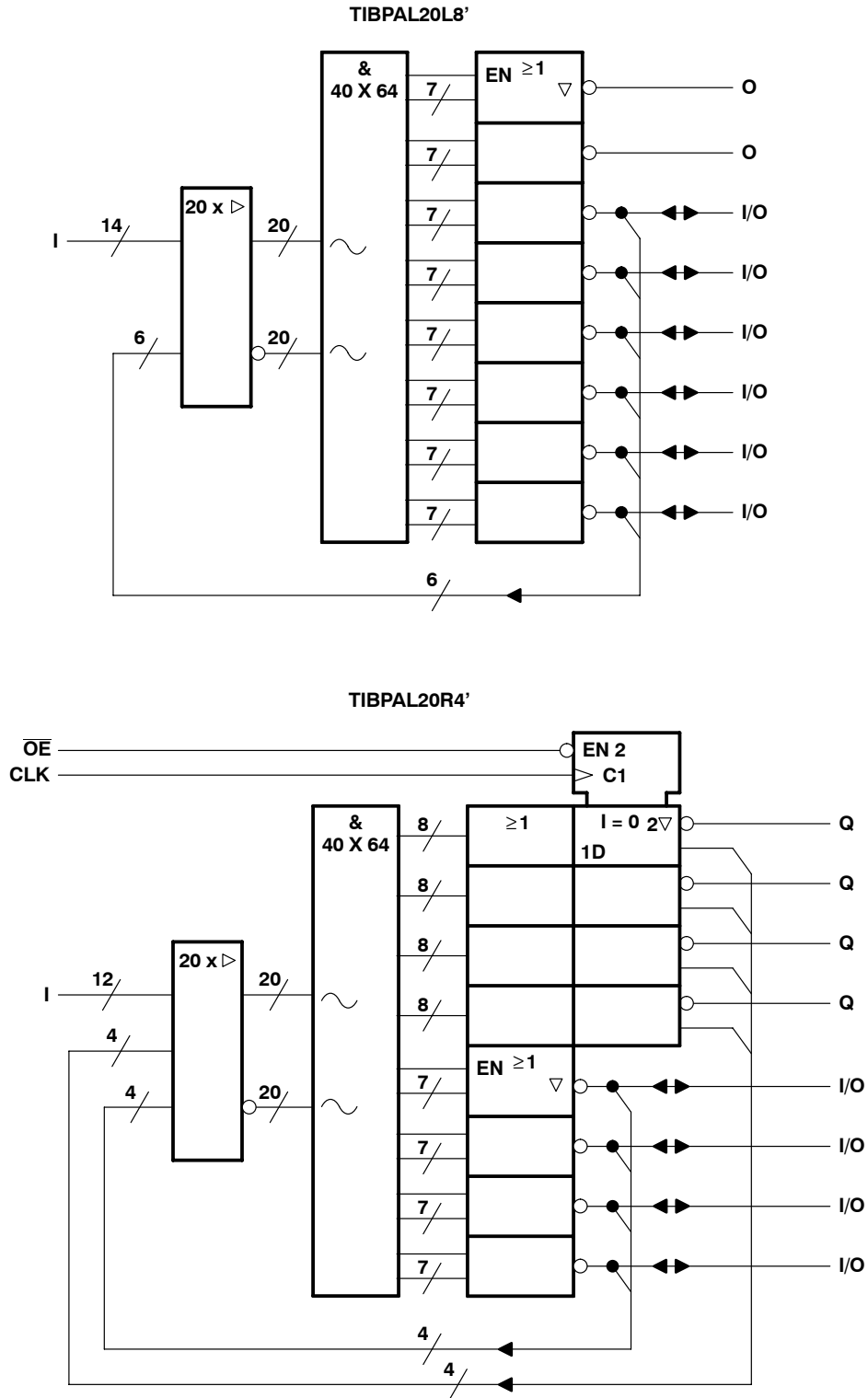


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SRPS022A - D2920, MAY 1987 - REVISED DECEMBER 2010

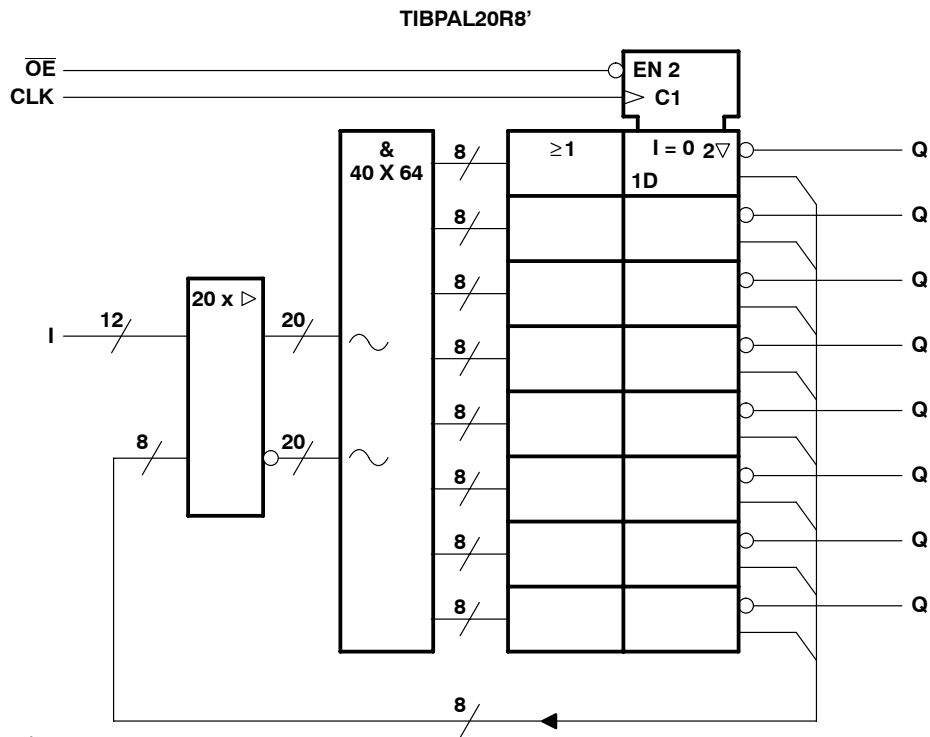
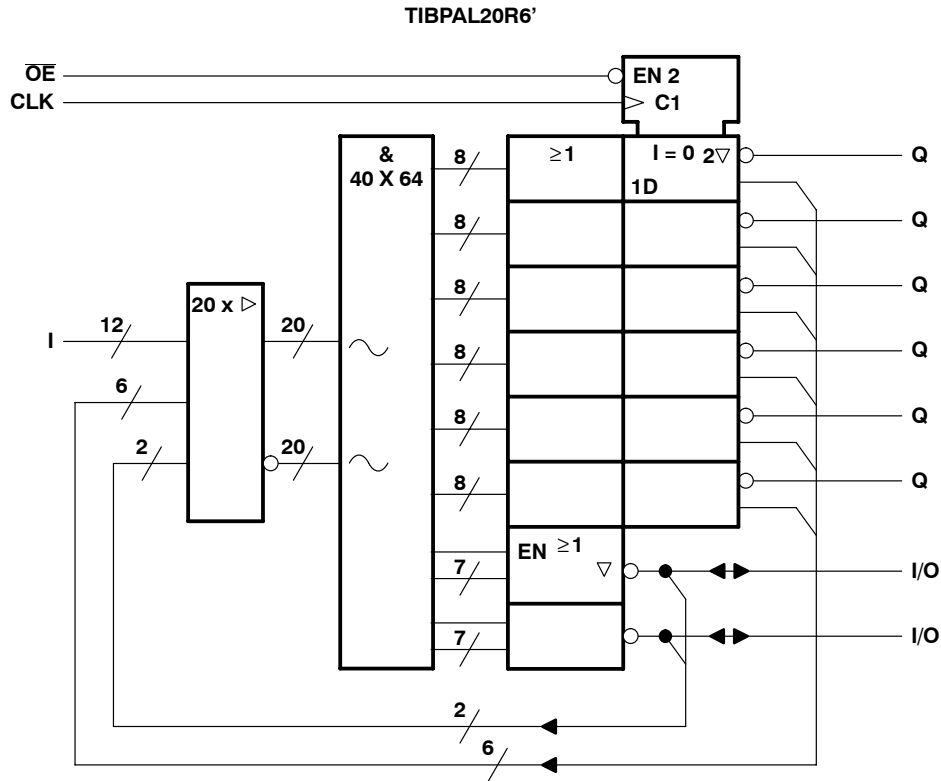
functional block diagrams (positive logic)



TIBPAL20R6-25C, TIBPAL20R8-25C LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

SRPS022A - D2920, MAY 1987 - REVISED DECEMBER 2010

functional block diagrams (positive logic)

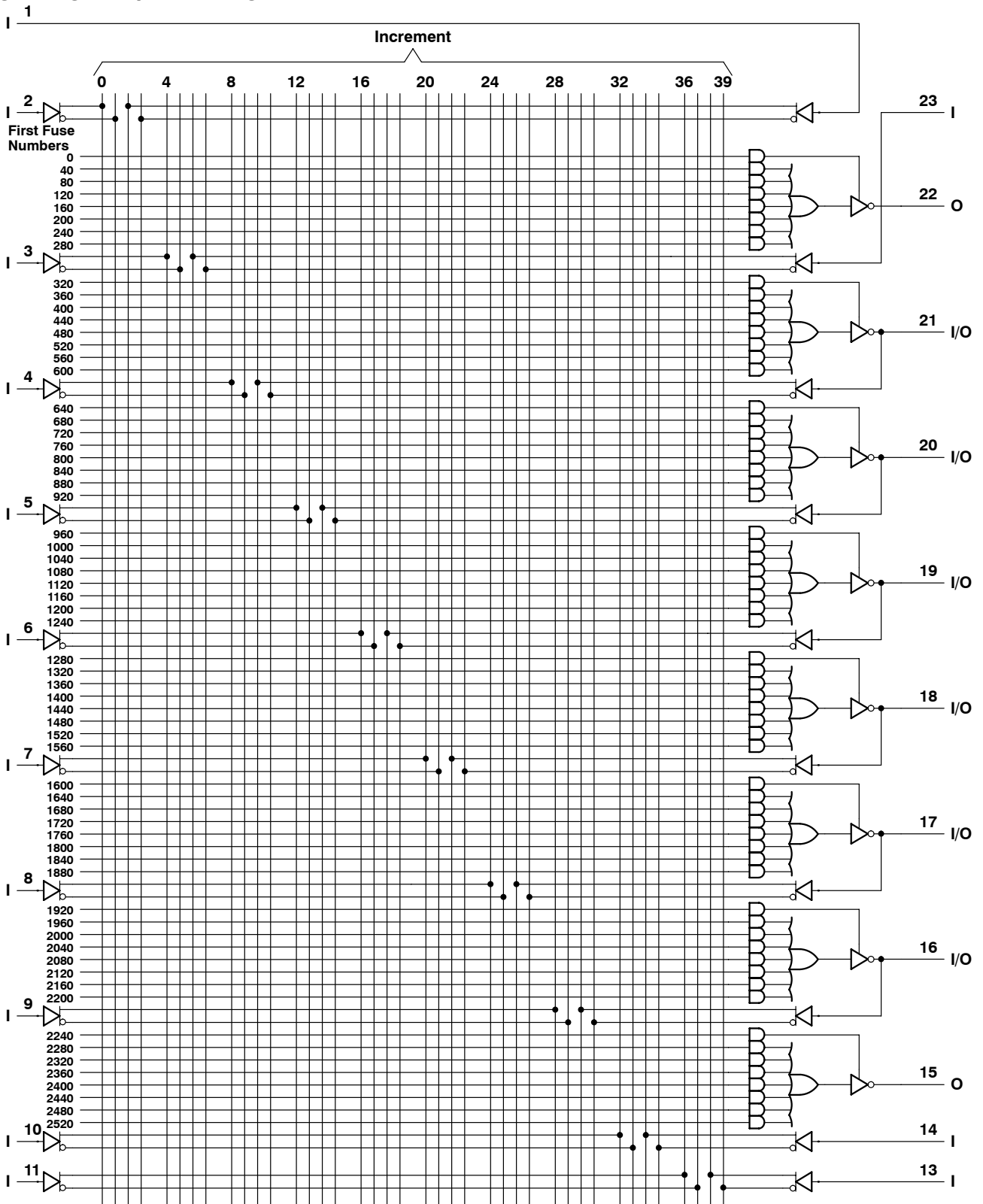


~ denotes fused inputs



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logic diagram (positive logic)



Fuse number = First fuse number + Increment
 Pin numbers shown are for JT and NT packages.

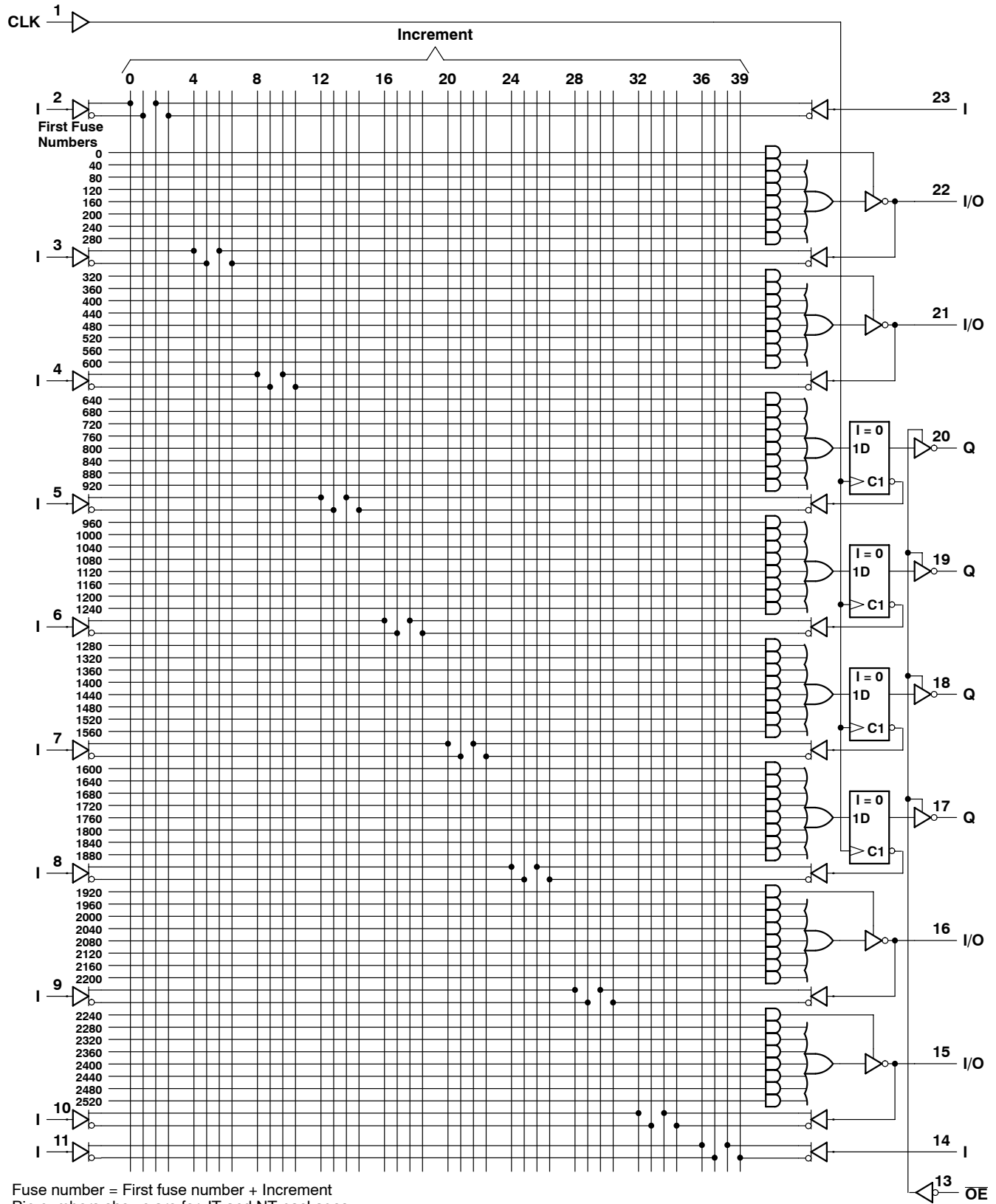


TIBPAL20R4-25C

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logic diagram (positive logic)

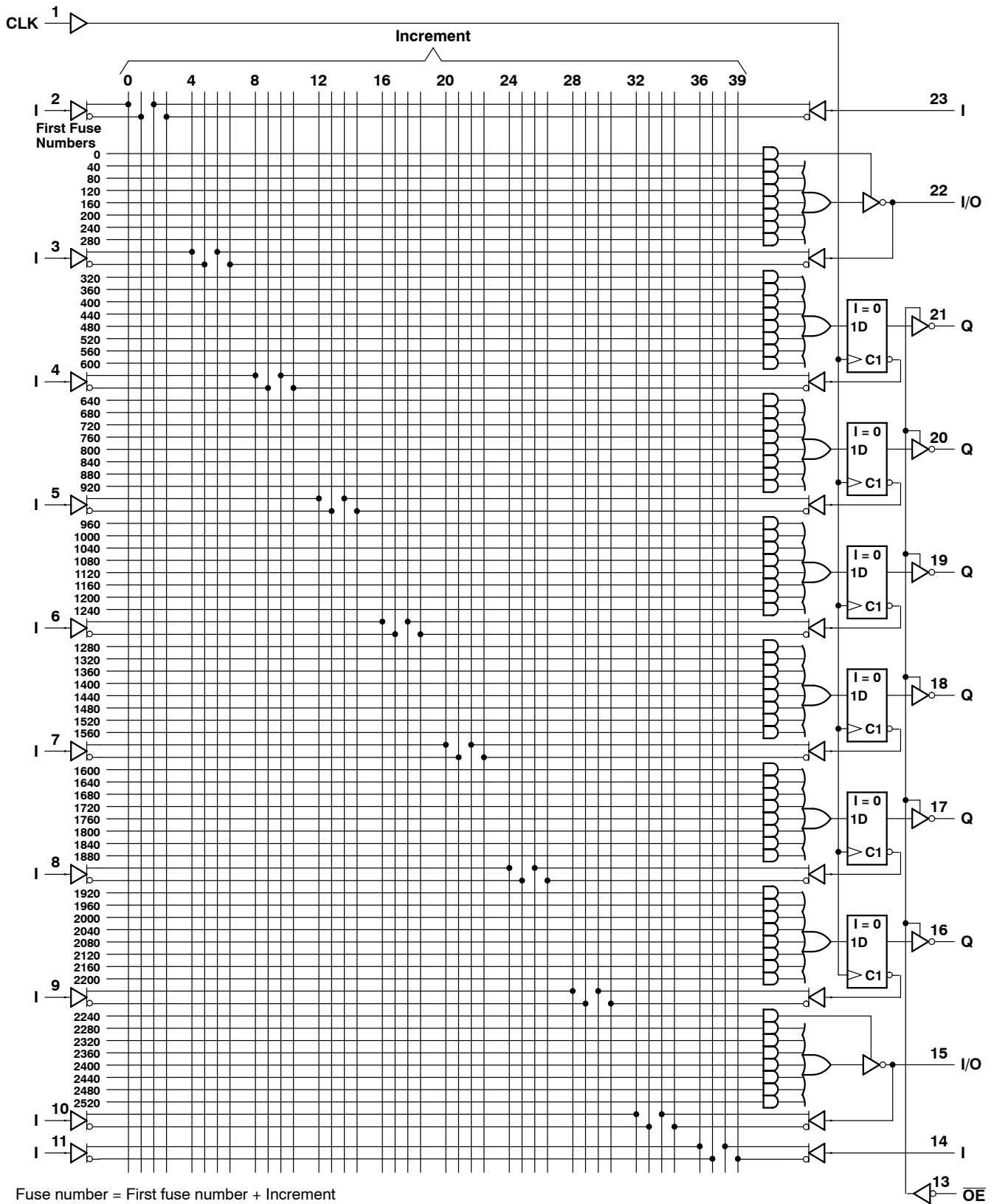


Fuse number = First fuse number + Increment
 Pin numbers shown are for JT and NT packages.



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logic diagram (positive logic)



Fuse number = First fuse number + Increment
 Pin numbers shown are for JT and NT packages.

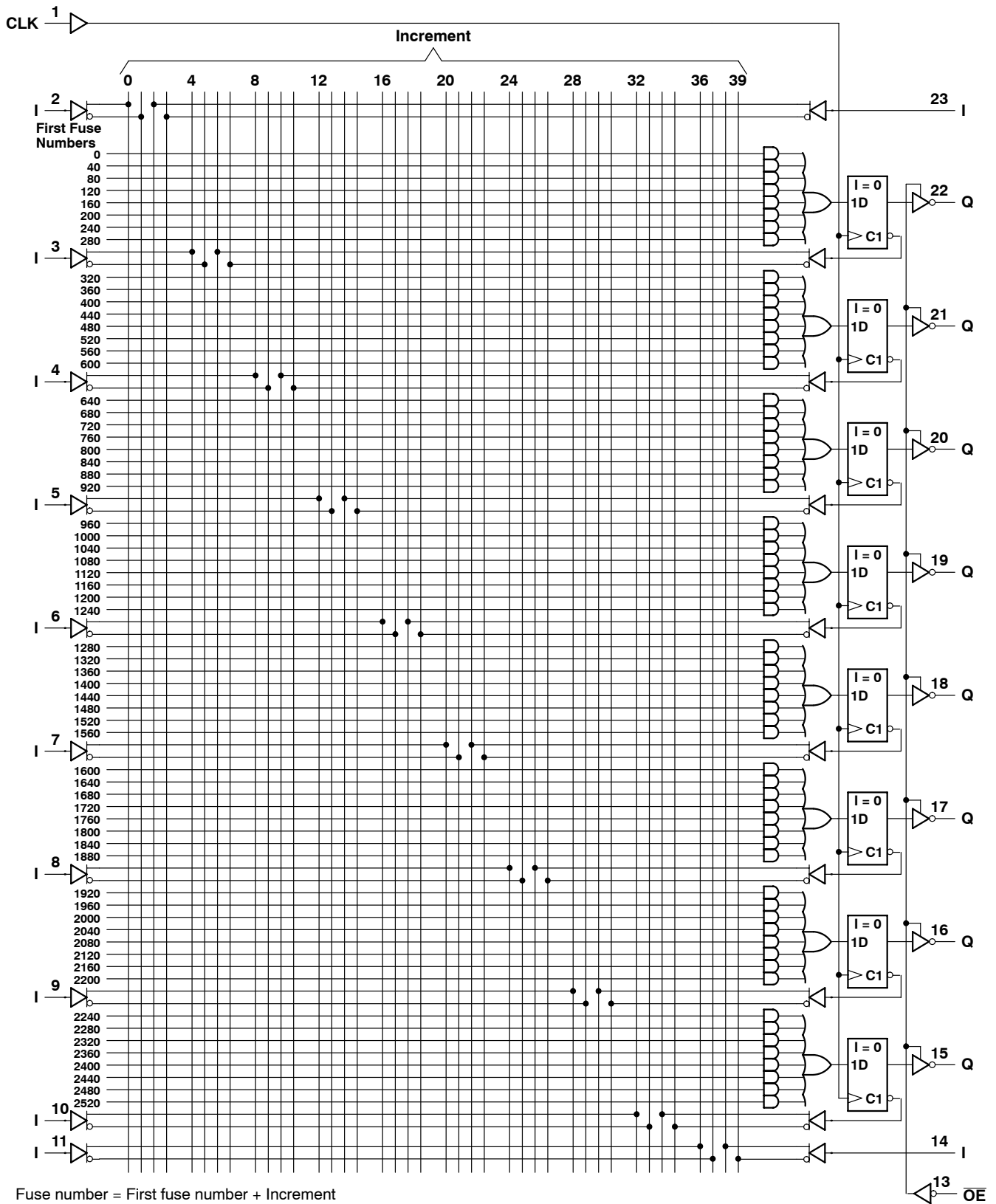


TIBPAL20R8-25C

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logic diagram (positive logic)



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SRPS022A – D2920, MAY 1987 – REVISED DECEMBER 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}^\dagger	Clock frequency	0		33	MHz
t_w^\dagger	Pulse duration, clock	High	15		ns
		Low	15		
t_{su}^\dagger	Setup time, input or feedback before clock \uparrow	25		ns	
t_h^\dagger	Hold time, input or feedback after clock \uparrow	0		ns	
T_A	Operating free-air temperature	0	25	75	°C

$^\dagger f_{clock}$, t_w , t_{su} , and t_h do not apply for TIBPAL20L8'.



TIBPAL20L8-25C, TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS022A – D2920, MAY 1987 – REVISED DECEMBER 2010

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.75 V,	I _I = -18 mA		-0.8	-1.5	V
V _{OH}		V _{CC} = 4.75 V,	I _{OH} = -3.2 mA	2.4	3.3		V
V _{OL}		V _{CC} = 4.75 V,	I _{OL} = 24 mA		0.3	0.5	V
I _{OZH}	O, Q outputs	V _{CC} = 5.25 V,	V _O = 2.7 V			20	μA
	I/O ports					100	
I _{OZL}	O, Q outputs	V _{CC} = 5.25 V,	V _O = 0.4 V			-20	μA
	I/O ports					-250	
I _I		V _{CC} = 5.25 V,	V _I = 5.5 V			0.1	mA
I _{IH} ‡		V _{CC} = 5.25 V,	V _I = 2.7 V			20	μA
I _{IL} ‡		V _{CC} = 5.25 V,	V _I = 0.4 V			-0.25	mA
I _{OS} §		V _{CC} = 5.25 V,	V _O = 0	-30	-70	-130	mA
I _{CC}		V _{CC} = 5.25 V, Outputs open,	V _I = 0, \overline{OE} at V _{IH}		75	105	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f _{max} ¶	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 3	25	40		MHz
	Without feedback			33	50		
t _{pd}	I, I/O	O, I/O		3	14	25	ns
t _{pd}	CLK↑	Q		2	10	15	ns
t _{en}	\overline{OE}	Q		2	8	15	ns
t _{dis}	\overline{OE} ↑	Q		2	8	15	ns
t _{en}	I, I/O	O, I/O		3	15	25	ns
t _{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

$$¶ f_{\max}(\text{with feedback}) = \frac{1}{t_{\text{su}} + t_{\text{pd}}(\text{CLK to Q})}, \quad f_{\max}(\text{without feedback}) = \frac{1}{t_{\text{w high}} + t_{\text{w low}}}$$

f_{max} does not apply for TIBPAL20L8.



programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL} , raise Pin 13 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 13 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

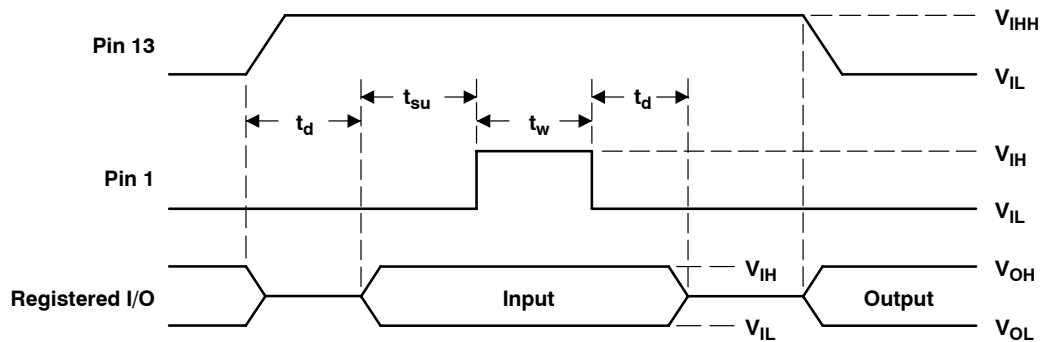


Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

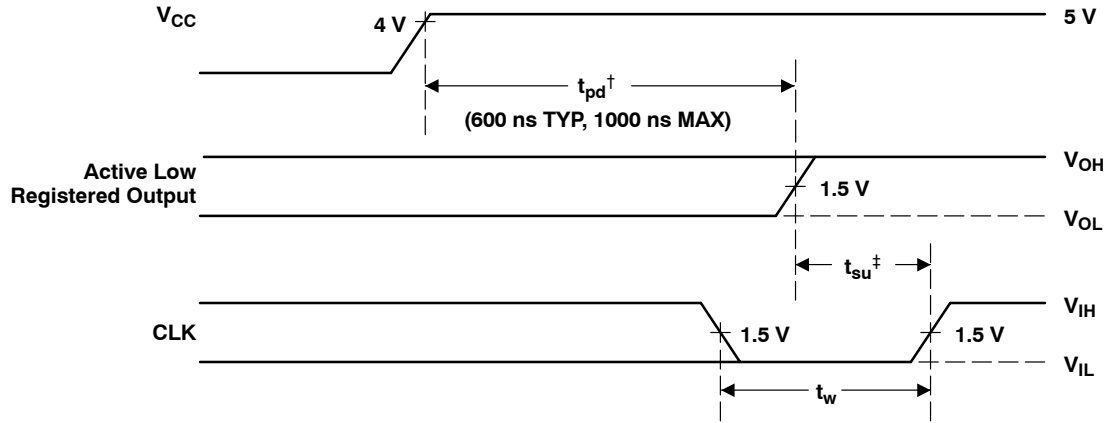
3. $t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns}$ $V_{IHH} = 10.25 \text{ V to } 10.75 \text{ v}$

TIBPAL20L8-25C, TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS022A – D2920, MAY 1987 – REVISED DECEMBER 2010

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

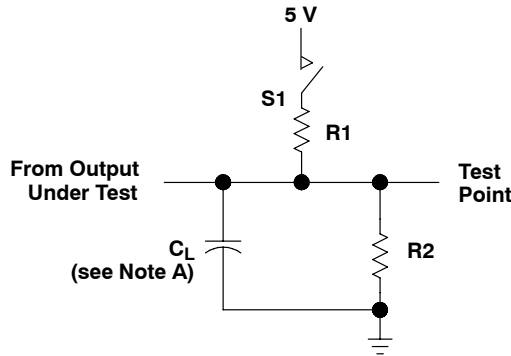


[†] This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

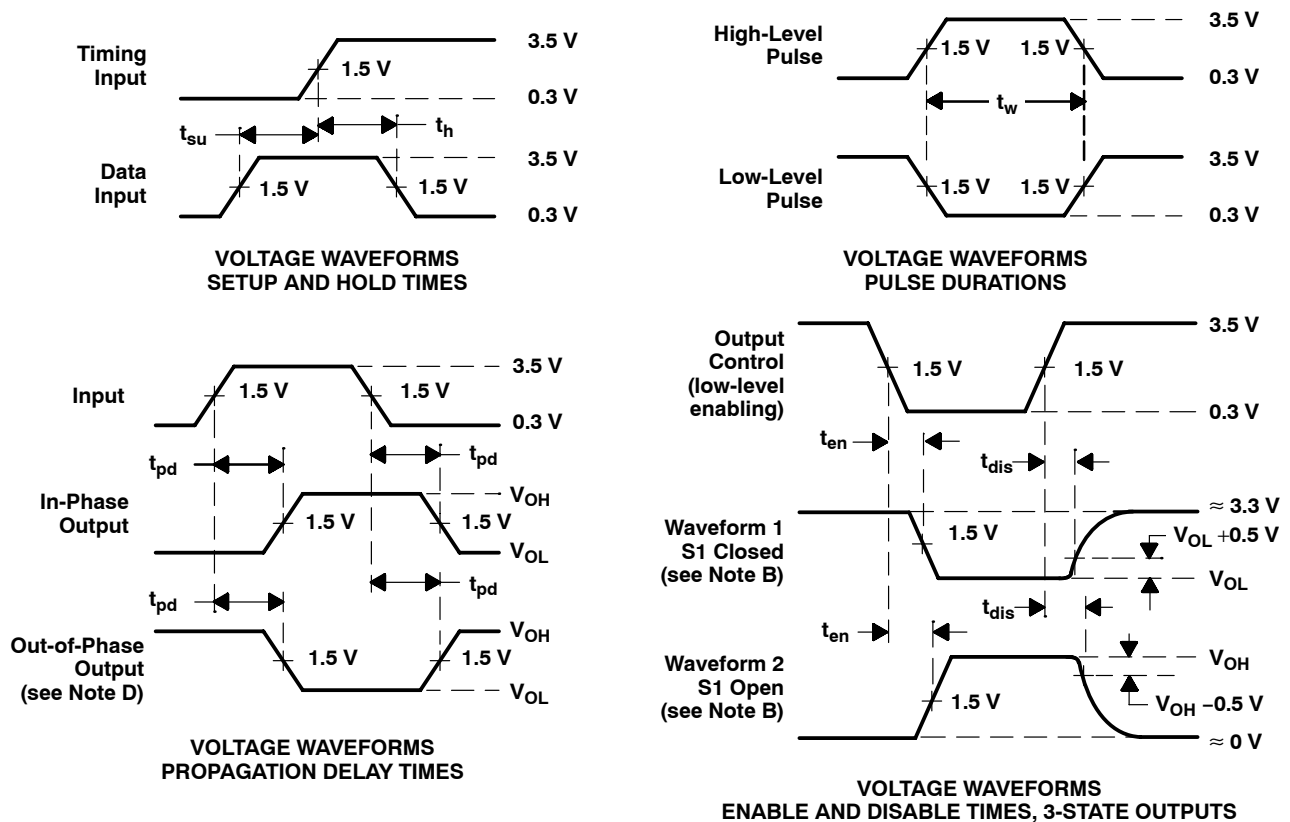
[‡] This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

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KOREA: Texas Instruments Korea Ltd., 28th Floor, Trade Tower, 159, Samsung-Dong, Kangnam-ku Seoul, Korea, 2 551-2800.

MALAYSIA: Texas Instruments Malaysia, Sdn. Bhd., Asia Pacific, Lot 36.1 #Box 93, Menara Maybank, 100 Jalan Tun Perak, 50050 Kuala Lumpur, Malaysia, 2306001.

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D0892

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIBPAL20L8-25CFN	LIFEBUY	PLCC	FN	28	37	TBD	CU SN	Level-1-220C-UNLIM	0 to 75	20L8-25CFN	
TIBPAL20L8-25CJT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI			
TIBPAL20L8-25CNT	LIFEBUY	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL20L8-25C NT	
TIBPAL20R4-25CFN	LIFEBUY	PLCC	FN	28	37	TBD	CU SN	Level-1-220C-UNLIM	0 to 75	20R4-25CFN	
TIBPAL20R4-25CNT	LIFEBUY	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL20R4-25C NT	
TIBPAL20R6-25CNT	LIFEBUY	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL20R6-25C NT	
TIBPAL20R8-25CFN	LIFEBUY	PLCC	FN	28	37	TBD	CU SN	Level-1-220C-UNLIM	0 to 75	20R8-25CFN	
TIBPAL20R8-25CNT	LIFEBUY	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL20R8-25C NT	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

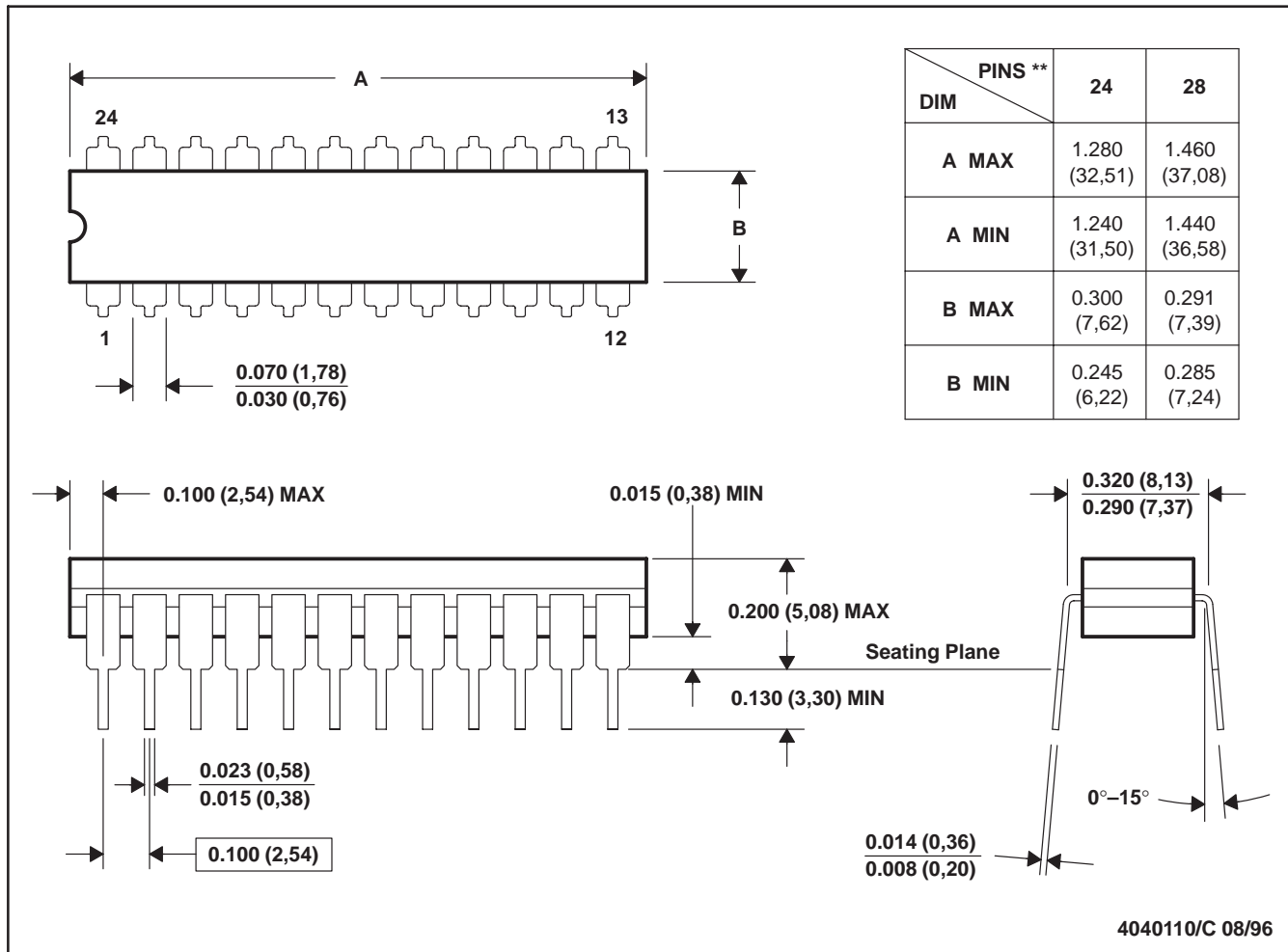
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JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN

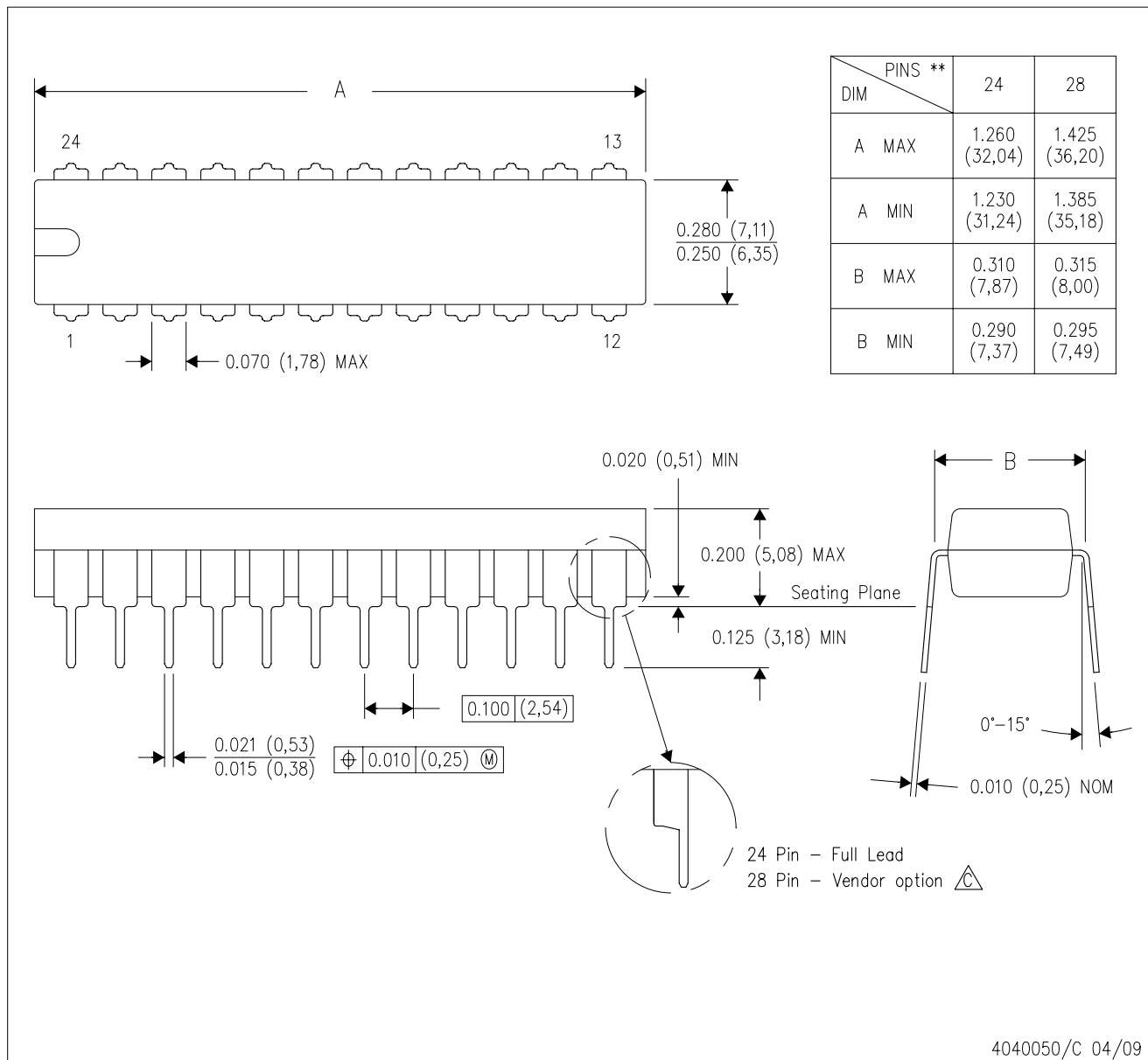



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

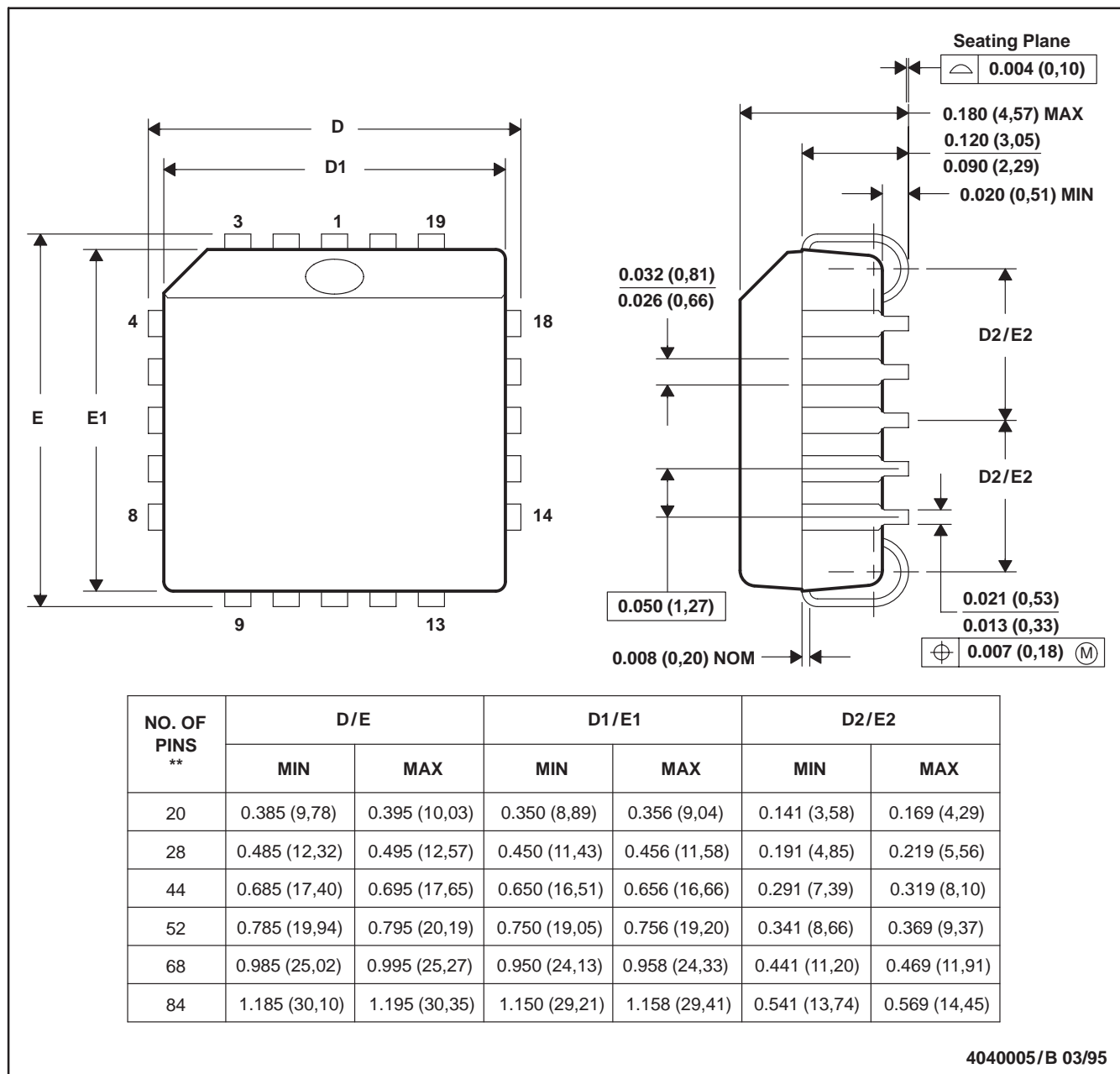


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

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