INTEGRATED CIRCUITS
UNITRODE

**UC1832**
**UC2832/3**
**UC3832/3**

# Precision Low Dropout Linear Controllers

## FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5 V to 36 V Operation
- 100mA Output Drive, Source, or Sink
- Under-Voltage Lockout

Additional Features of the UC2832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate +$V_{IN}$ terminal
- Programmable Driver Current Limit
- Access to $V_{REF}$ and E/A(+)
- Logic-Level Disable Input

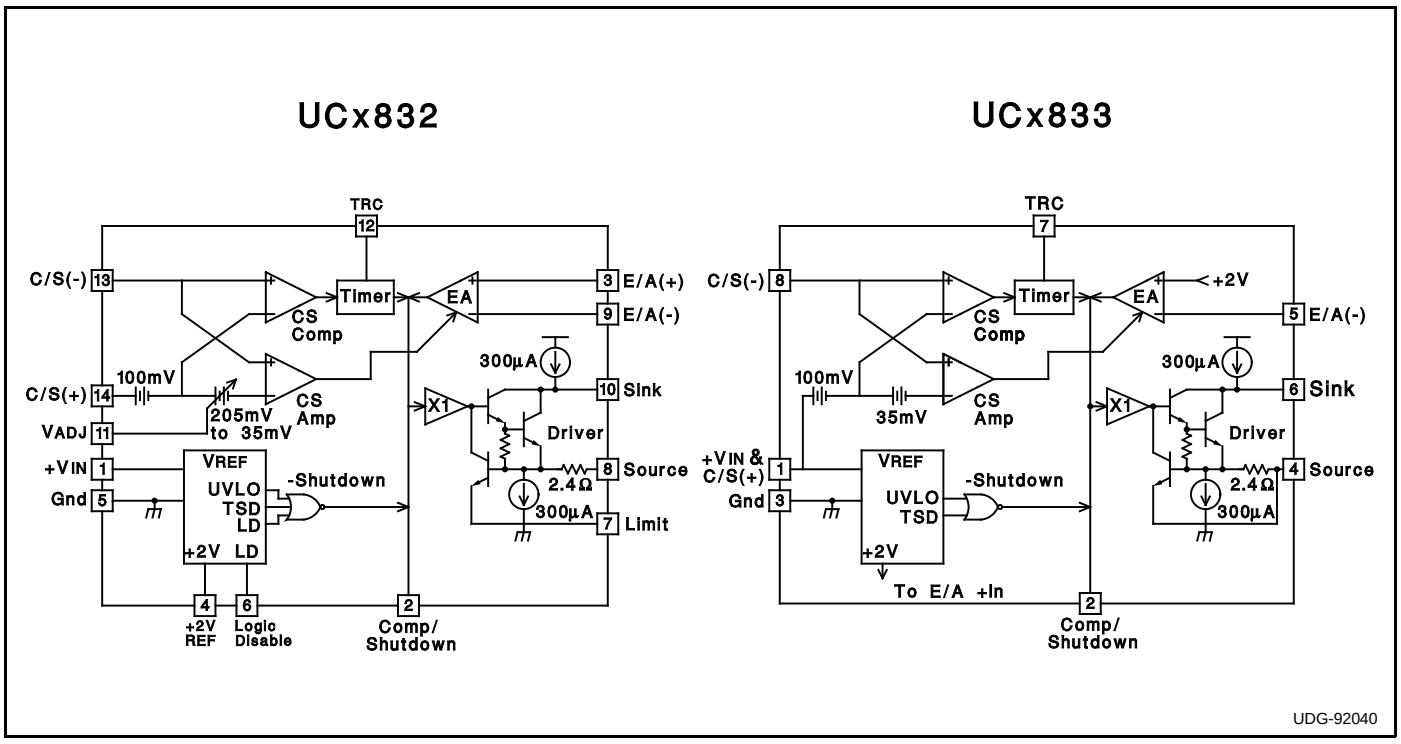
## DESCRIPTION

The UC2832 and UC3833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCx832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The UC3833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC2832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); and industrial (–40°C to 85°C), order UC2832/3 (N or J). Surface mount packaging is also available.

## BLOCK DIAGRAMS




UDG-92040

## ABSOLUTE MAXIMUM RATINGS

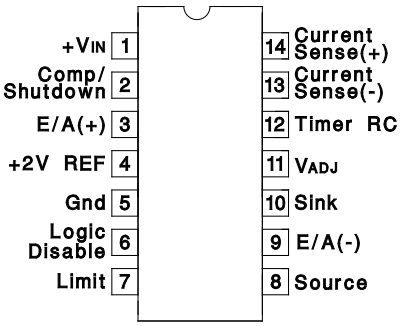
Supply Voltage $+V_{IN}$ . . . . . 40V
Driver Output Current (Sink or Source) . . . . . 450mA
Driver Sink to Source Voltage . . . . . 40V
TRC Pin Voltage . . . . . –0.3V to 3.2V
Other Input Voltages. . . . . –0.3V to $+V_{IN}$
Operating Junction Temperature (note 2) . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

*Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.*
*Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.*

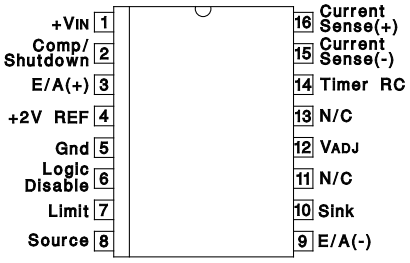
## CONNECTION DIAGRAMS

### UC2832

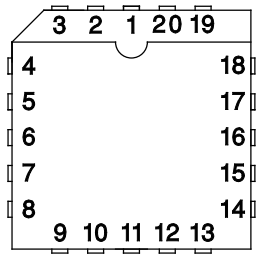
**DIL-14 (Top View)**
**J Or N Package**




**SOIC-16 (Top View)**
**DW Package**



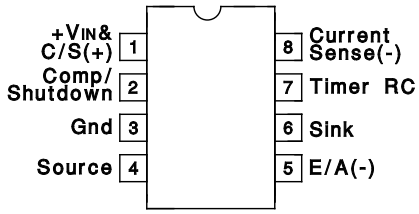

**LCC-20 & PLCC-20**
**L & Q Package**
**(Top View)**



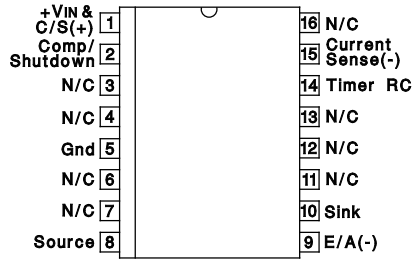

| PACKAGE PIN FUNCTION | |
|---|---|
| FUNCTION | PIN |
| N/C | 1 |
| $+V_{IN}$ | 2 |
| Comp/Shutdown | 3 |
| E/A(+) | 4 |
| +2V REF | 5 |
| N/C | 6 |
| Gnd | 7 |
| Logic Disable | 8 |
| Limit | 9 |
| Source | 10 |
| N/C | 11 |
| E/A(-) | 12 |
| Sink | 13 |
| $V_{ADJ}$ | 14 |
| N/C | 15-17 |
| Timer RC | 18 |
| Current Sense(-) | 19 |
| Current Sense(+) | 20 |

### UC3833

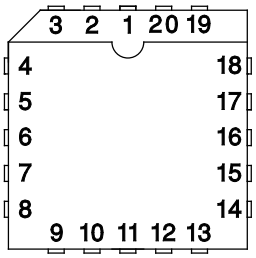
**DIL-8 (Top View)**
**J Or N Package**




**SOIC-16 (Top View)**
**DW Package**




**LCC-20 & PLCC-20**
**L & Q Package**
**(Top View)**




| PACKAGE PIN FUNCTION | |
|---|---|
| FUNCTION | PIN |
| $+V_{IN}$ & C/S(+) | 1 |
| N/C | 2 |
| N/C | 3 |
| N/C | 4 |
| Comp/Shutdown | 5 |
| Gnd | 6 |
| N/C | 7 |
| N/C | 8 |
| N/C | 9 |
| Source | 10 |
| N/C | 11 |
| E/A(-) | 12 |
| N/C | 13 |
| N/C | 14 |
| Sink | 15 |
| Timer RC | 16 |
| Current Sense(+) | 17 |
| N/C | 18-20 |

## ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to 70°C for the UC3832/3, –40°C to 85°C for the UC2832/3, $+V_{IN}$ = 15V, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$. $T_A$=$T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Input Supply** | | | | | |
| Supply Current | $+V_{IN}$ = 6 V | | 6.5 | 10 | mA |
| | $+V_{IN}$ = 36 V | | 9.5 | 15 | mA |
| | Logic Disable = 2 V (UCx832 only) | | 3.3 | | mA |
| **Reference Section** | | | | | |
| Output Voltage (Note 3) | $T_J$ = 25°C, $I_{DRIVER}$ = 10 mA | 1.98 | 2.00 | 2.02 | V |
| | over temperature, $I_{DRIVER}$ = 10 mA | 1.96 | 2.00 | 2.04 | V |
| Load Regulation (UCx832 only) | $I_O$ = 0 to 10 m | -10 | -5.0 | | mV |
| Line Regulation | $+V_{IN}$ = 4.5 V to 36 V, $I_{DRIVER}$ = 10 m | | 0.033 | 0.5 | mV/V |
| Under-Voltage Lockout Threshold | | | 3.6 | 4.5 | V |
| **Logic Disable Input (UCx832 only)** | | | | | |
| Threshold Voltage | | 1.3 | 1.4 | 1.5 | V |
| Input Bias Current | Logic Disable = 0 V | -5.0 | -1.0 | | µA |
| **Current Sense Section** | | | | | |
| Comparator Offset | | 95 | 100 | 105 | mV |
| | Over Temperature | 93 | 100 | 107 | mV |
| Amplifier Offset (UCx833 only) | | 110 | 135 | 170 | mV |
| Amplifier Offset (UCx832 only) | $V_{ADJ}$ = Open | 110 | 135 | 170 | mV |
| | $V_{ADJ}$ = 1 V | 180 | 235 | 290 | mV |
| | $V_{ADJ}$ = 0 V | 250 | 305 | 360 | mV |
| Input Bias Current | $V_{CM}$ = $+V_{IN}$ | 65 | 100 | 135 | µA |
| Input Offset Current (UCx832 only) | $V_{CM}$ = $+V_{IN}$ | -10 | | 10 | µA |
| Amplifier CMRR (UCx832 only) | $V_{CM}$ = 4.1 V to + $V_{IN}$ + 0.3 | | 80 | | dB |
| Transconductance | $I_{COMP}$ = ±100 µA | | 65 | | mS |
| $V_{ADJ}$ Input Current (UCx832 only) | $V_{ADJ}$ = 0V | -10 | -1 | | µA |
| **Timer** | | | | | |
| Inactive Leakage Current | C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2 V | | 0.25 | 1.0 | µA |
| Active Pullup Current | C/S(+) = $+V_{IN}$, C/S(-) = $+V_{IN}$ - 0.4V; TRC pin = 0 V | -345 | -270 | -175 | µA |
| Duty Ratio (note 4) | ontime/period, $R_T$ = 200k, $C_T$ = 0.27µF | | 4.8 | | % |
| Period (notes 4,5) | ontime + offtime, $R_T$ = 200k, $C_T$ = 0.27µF | | 36 | | ms |
| Upper Trip Threshold (Vu) | | | 1.8 | | V |
| Lower Trip Threshold (Vl) | | | 0.9 | | V |
| Trip Threshold Ratio | Vu/Vl | | 2.0 | | V/V |
| **Error Amplifier** | | | | | |
| Input Offset Voltage (UCx832 only) | $V_{CM}$ = $V_{COMP}$ = 2 V | -8.0 | | 8.0 | mV |
| Input Bias Current | $V_{CM}$ = $V_{COMP}$ = 2 V | -4.5 | -1.1 | | µA |
| Input Offset Current (UCx832 only) | $V_{CM}$ = $V_{COMP}$ = 2 V | -1.5 | | 1.5 | µA |
| AVOL | $V_{COMP}$ = 1 V to 13 V | 50 | 70 | | dB |
| CMRR (UCx832 only) | $V_{CM}$ = 0V to $+V_{IN}$ - 3 V | 60 | 80 | | dB |
| PSRR (UCx832 only) | $V_{CM}$ = 2 V, $+V_{IN}$ = 4.5 V to 36 | | 90 | | dB |
| Transconductance | $I_{COMP}$ = ±10 µA | | 43 | | mS |
| VOH | $I_{COMP}$ = 0, Volts below $+V_{IN}$ | | .95 | 1.3 | V |
| VOL | $I_{COMP}$ = 0 | | .45 | 0.7 | V |
| IOH | $V_{COMP}$ = 2 V | -700 | -500 | -100 | µA |

## ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, specifications hold for TA = 0°C to 70°C for the UC3832/3, –40°C to 85°C for the UC2832/3, +VIN = 15 V, Driver sink = +VIN, C/S(+) voltage = +VIN. TA=TJ.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Error Amplifier (cont.)** | | | | | |
| IOL | VCOMP = 2 V, C/S(-) = +VIN | 100 | 500 | 700 | µA |
| | VCOMP = 2 V, C/S(-) = +VIN - 0.4 V | 2 | 6 | | mA |
| **Driver** | | | | | |
| Maximum Current | Driver Limit & Source pins common; TJ = 25°C | 200 | 300 | 400 | mA |
| | Over Temperature | 100 | 300 | 450 | mA |
| Limiting Voltage (UCx832 only) | Driver Limit to Source voltage at current limit, ISOURCE = -10 mA; TJ = 25°C (Note 6) | | .72 | | V |
| Internal Current Sense Resistance | TJ = 25°C (Note 6) | | 2.4 | | Ω |
| Pull-Up Current at Driver Sink | Compensation/Shutdown = 0.4 V; Driver Sink = +VIN - 1V | -800 | -300 | -100 | µA |
| | Compensation/Shutdown = 0.4 V, +VIN = 36 V; Driver Sink = 35 V | -1000 | -300 | -75 | µA |
| Pull-Down Current at Driver Source | Compensation/Shutdown = 0.4 V; Driver Source = 1 V | 150 | 300 | 700 | µA |
| Saturation Voltage Sink to Source | Driver Source = 0 V; Driver Current = 100 mA | | 1.5 | | V |
| Maximum Source Voltage | Driver Sink = +VIN, Driver Current = 100 mA Volts below + VIN | | 3.0 | | V |
| UVLO Sink Leakage | +VIN = C/S(+) = C/S(-) = 2.5 V, Driver Sink = 15 V, Driver Source = 0 V, TA = 25°C | | 25 | | µA |
| Maximum Reverse Source Voltage | Compensation/Shutdown = 0 V; ISOURCE = 100 µA, +VIN = 3 V | | 1.6 | | V |
| Thermal Shutdown | | | 160 | | °C |

*Note 3: On the UCx833 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving VSOURCE to 2 V.*

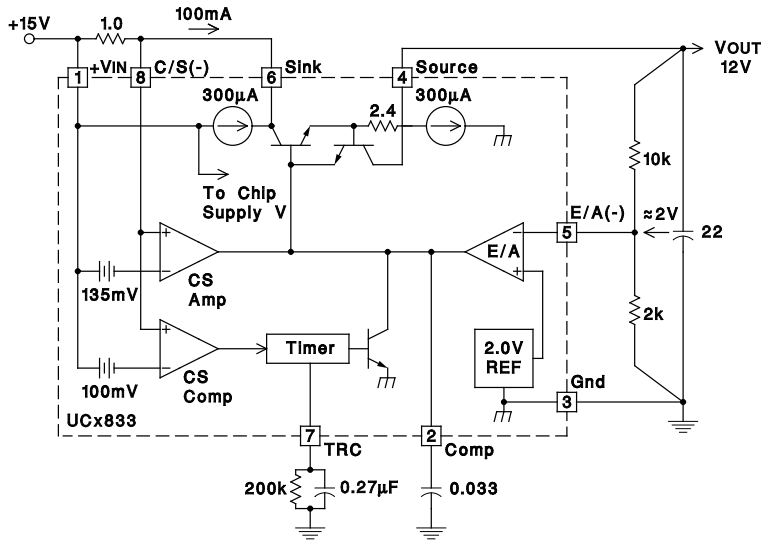
*Note 4: These parameters are first-order supply-independent, however both may vary with supply for +VIN less than about 4 V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.*

*Note 5: With recommended RT value of 200k, TOFF ≈ RT CT * ln(Vu/Vl) ±10%.*

*Note 6: The internal current limiting voltage has a temperature dependence of approximately -2.0 mV/°C, or -2800 ppm/°C. The internal 2.4 Ω sense resistor has a temperature dependance of approximately +1500 ppm/°C.*

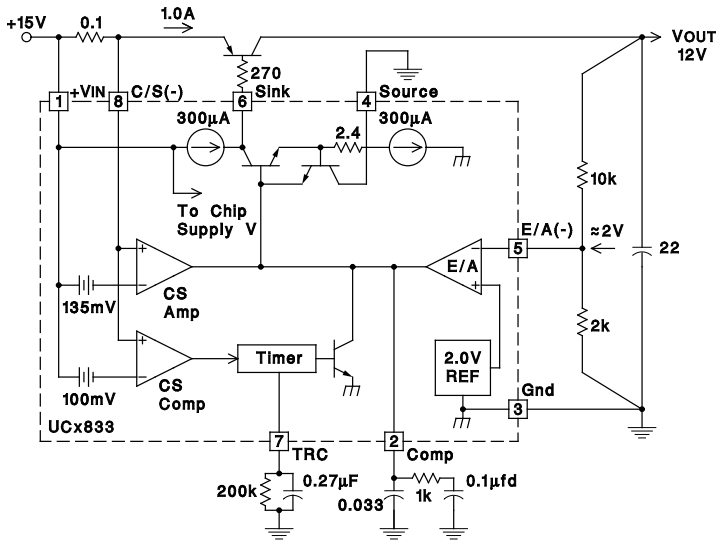
## APPLICATION AND OPERATION INFORMATION

**NPN Pass (Local 100mA Regulator) (UCx833)**



## APPLICATION AND OPERATION INFORMATION (cont.)

**PNP Pass (Low Drop-Out Regulator) (UCx833)**

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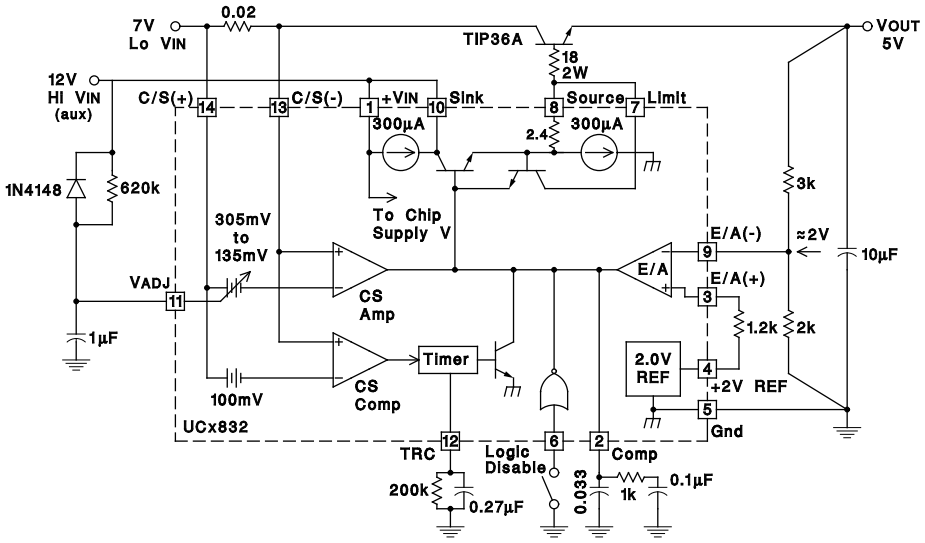
**NPN Pass (Medium Power, Low Drop-Out Regulator) (UCx832)**




UDG-92043-1

### Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10k \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where $I_{TH}$ is the timer trip-point current,

and $$K = \frac{Current\ Sense\ Amplifier\ Offset\ Voltage}{100mA}$$

≈1.35 for UCx833, and is variable from 1.35 to 3.05 with $V_{ADJ}$ for the UCx832.

For a worst-case constant-current load of value just less than $I_{TH}$, $C_{MAX}$ can be estimated from:

$$C_{MAX} = ((K-1)I_{TH})\left(\frac{T_{ON}}{V_{OUT}}\right),$$

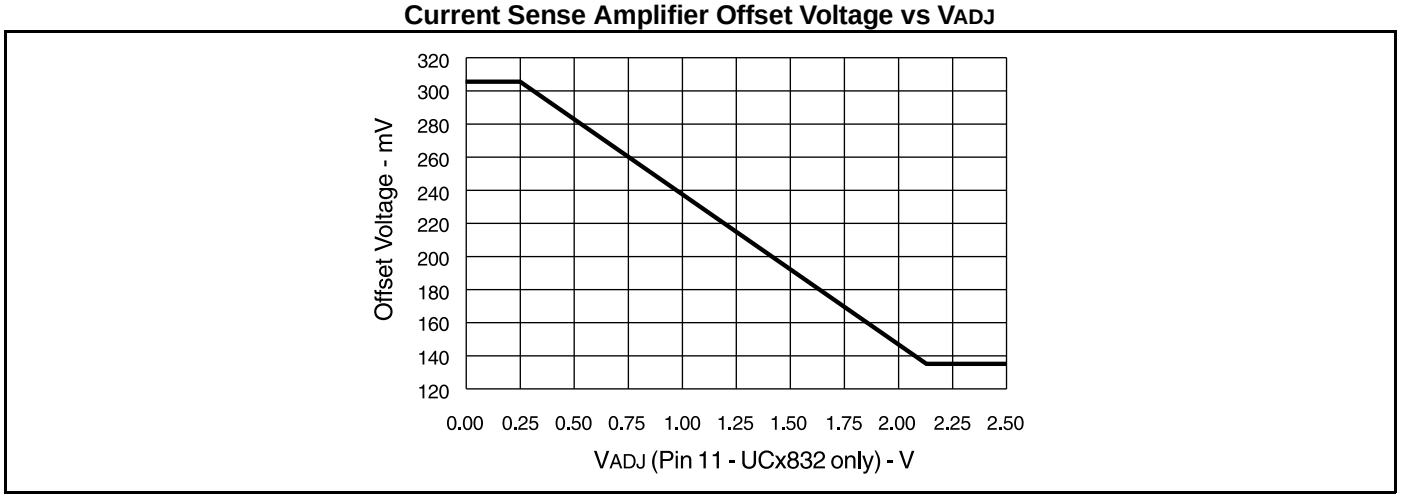
where $V_{OUT}$ is the nominal regulator output voltage.

For a resistive load of value $R_L$, the value of $C_{MAX}$ can be estimated from:

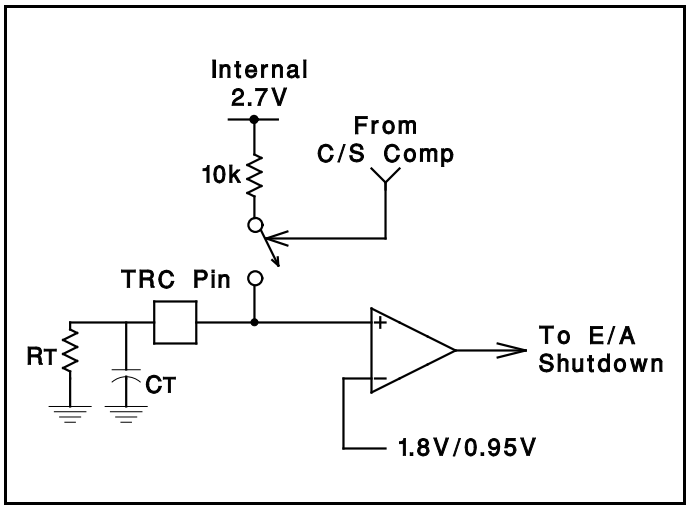
$$C_{MAX} = \frac{T_{ON}}{R_L} \bullet \frac{1}{In\left[\left(1-\frac{V_{OUT}}{K \bullet I_{TH} \bullet R_L}\right)^{-1}\right]}.$$

## APPLICATION AND OPERATION INFORMATION (cont.)

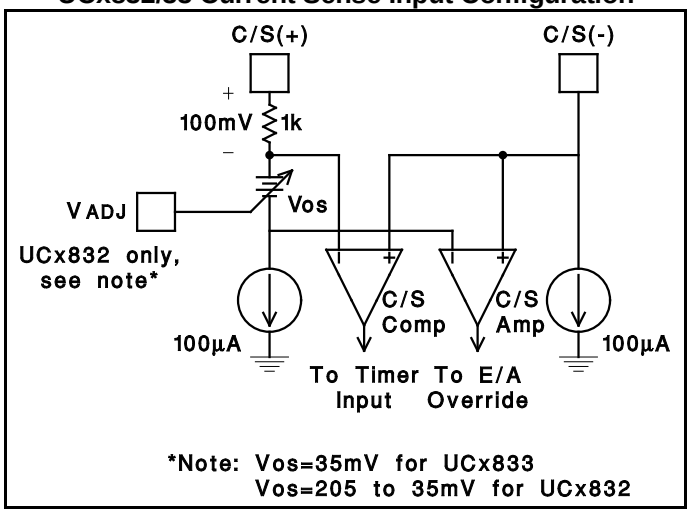
**Current Sense Amplifier Offset Voltage vs $V_{ADJ}$**



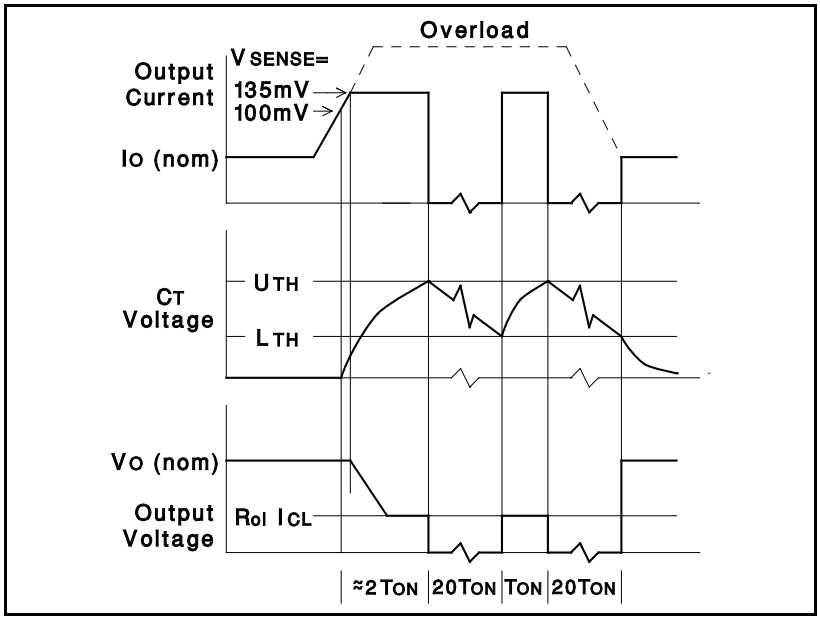

**UCx832/33 Timer Function**




**UCx832/33 Current Sense Input Configuration**



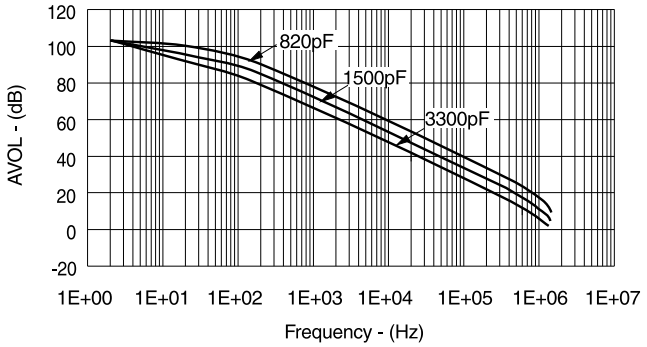

**Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.**



## APPLICATION AND OPERATION INFORMATION (cont.)

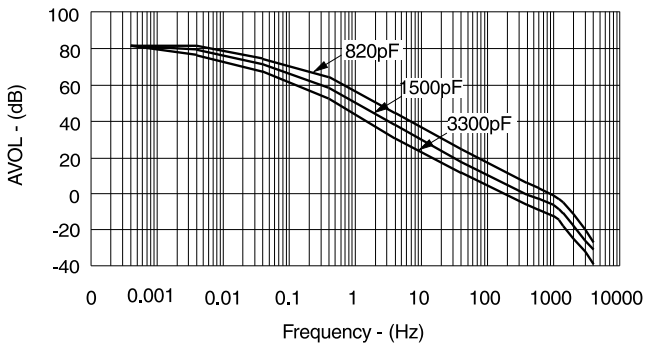
**UCx832 Error Amplifier**

AVOL vs Frequency and CC



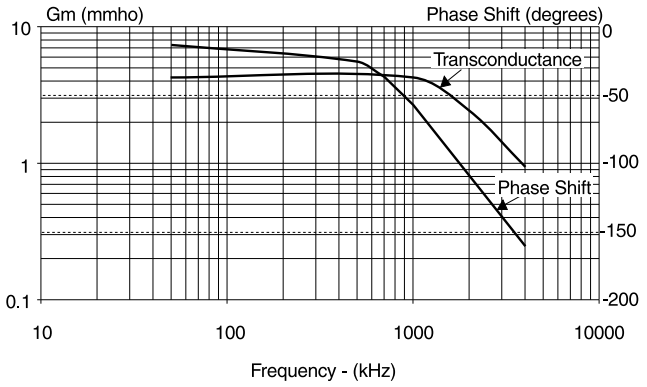

**UCx832 Current Sense Amplifier**

AVOL vs Frequency and CC



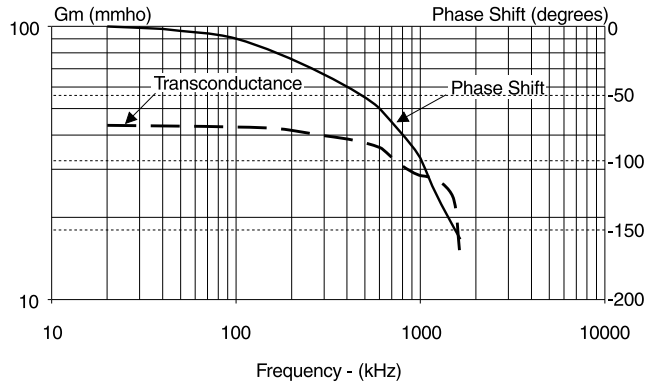

**UCx832 Error Amplifier**

Transconductance and Phase vs Frequency




**UCx832 Current Sense Amplifier**

Transconductance and Phase vs Frequency




UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9326501M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9326501M2A UC1832L/ 883B | Samples |
| 5962-9326501MCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9326501MCA UC1832J/883B | Samples |
| 5962-9326501V2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | | 5962-9326501V2A UC1832L QMLV | Samples |
| 5962-9326501VCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | | 5962-9326501VCA UC1832JQMLV | Samples |
| UC1832J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | UC1832J | Samples |
| UC1832J883B | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9326501MCA UC1832J/883B | Samples |
| UC1832L883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9326501M2A UC1832L/ 883B | Samples |
| UC2832DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | UC2832DW | Samples |
| UC2832DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | UC2832DW | Samples |
| UC2833DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2833DW | Samples |
| UC2833DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2833DW | Samples |
| UC2833DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2833DW | Samples |
| UC2833J | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI | -40 to 85 | | |
| UC2833N | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | UC2833N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UC3832DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3832DW | Samples |
| UC3832DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3832DW | Samples |
| UC3832DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3832DW | Samples |
| UC3832N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3832N | Samples |
| UC3832NG4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3832N | Samples |
| UC3833DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3833DW | Samples |
| UC3833DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3833DW | Samples |
| UC3833J | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI | 0 to 70 | | |
| UC3833N | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3833N | Samples |
| UC3833NG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3833N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF UC1832, UC1832-SP, UC2832, UC3832, UC3833 :**

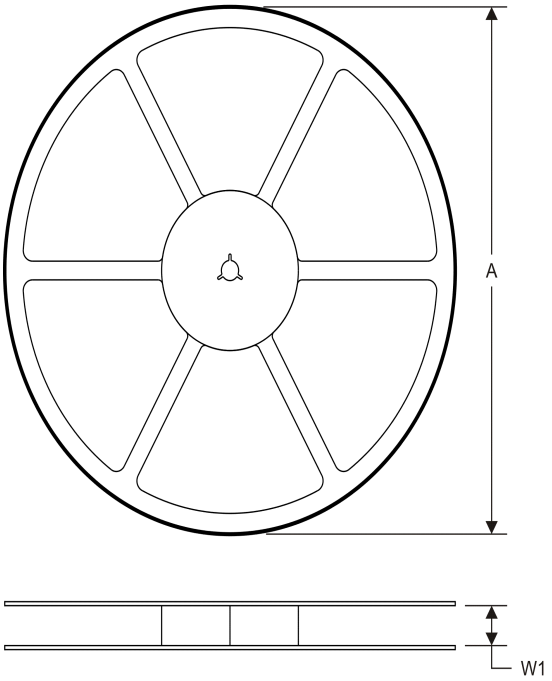
- Catalog: UC3832, UC1832
- Enhanced Product: UC2832-EP
- Military: UC1832, UC1833
- Space: UC1832-SP

NOTE: Qualified Version Definitions:

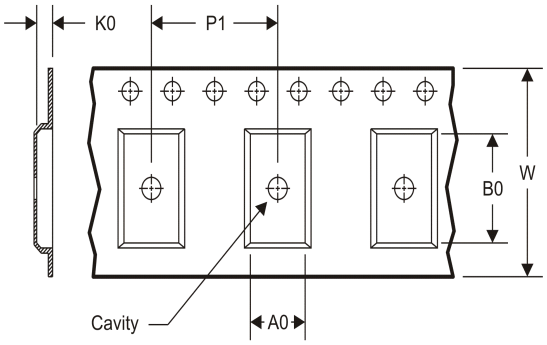
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



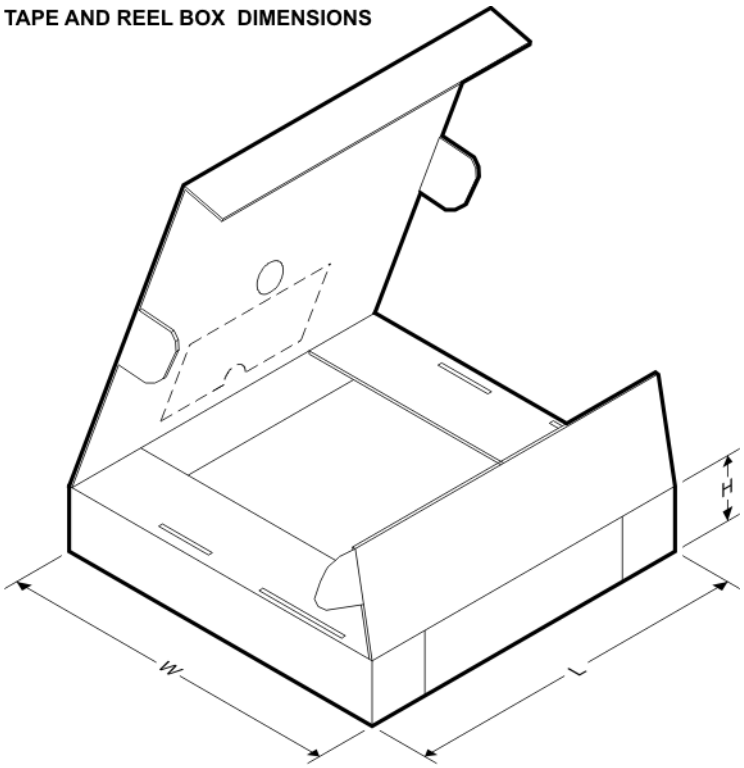

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2832DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC2833DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3832DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3833DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

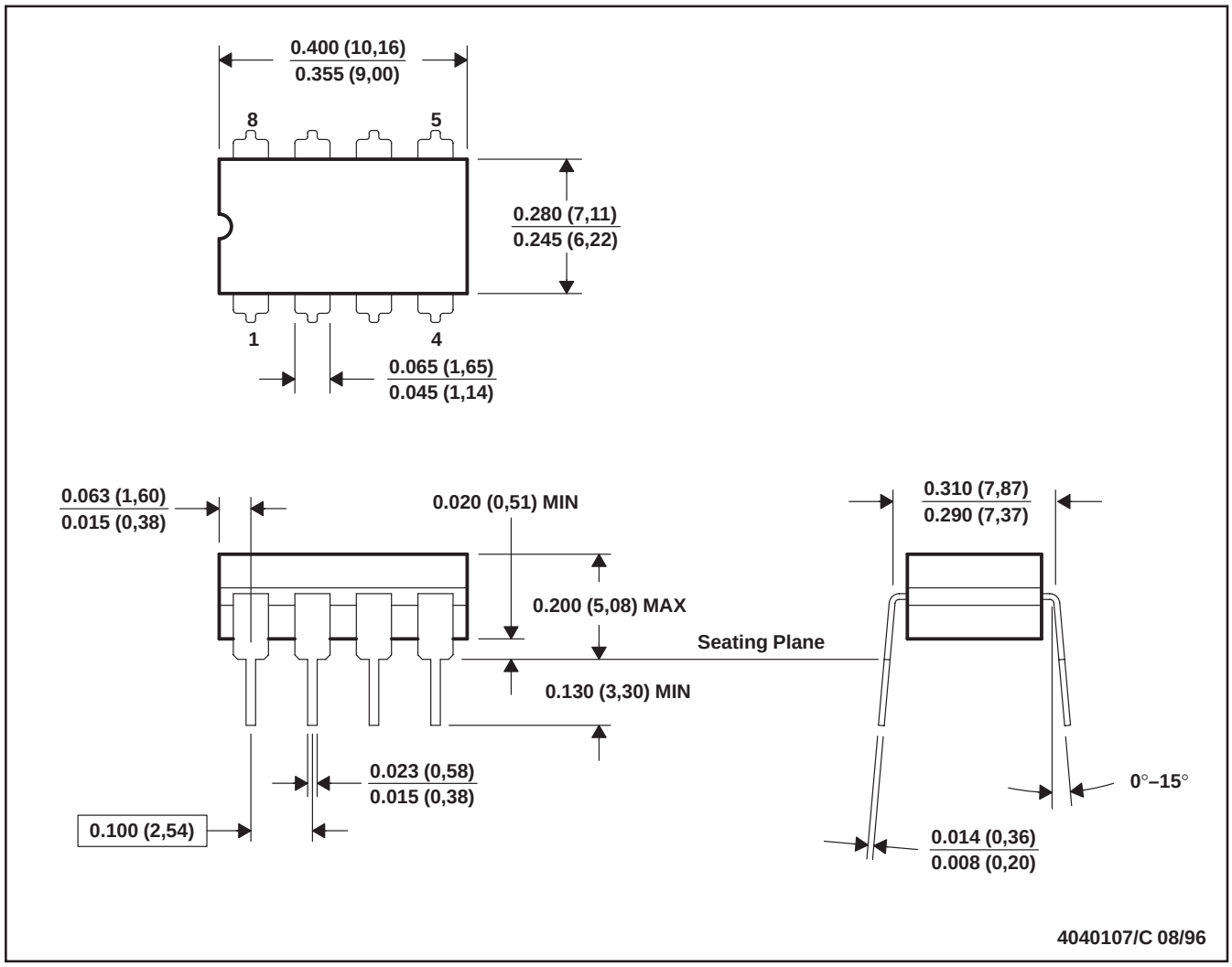



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2832DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| UC2833DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| UC3832DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| UC3833DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**

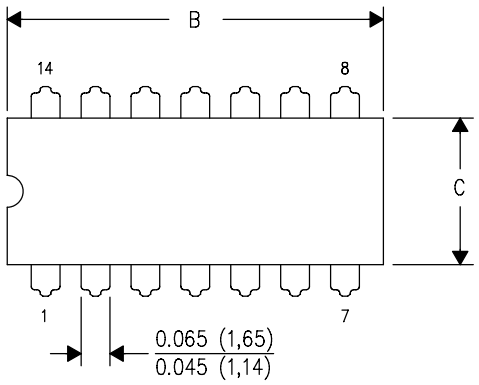



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

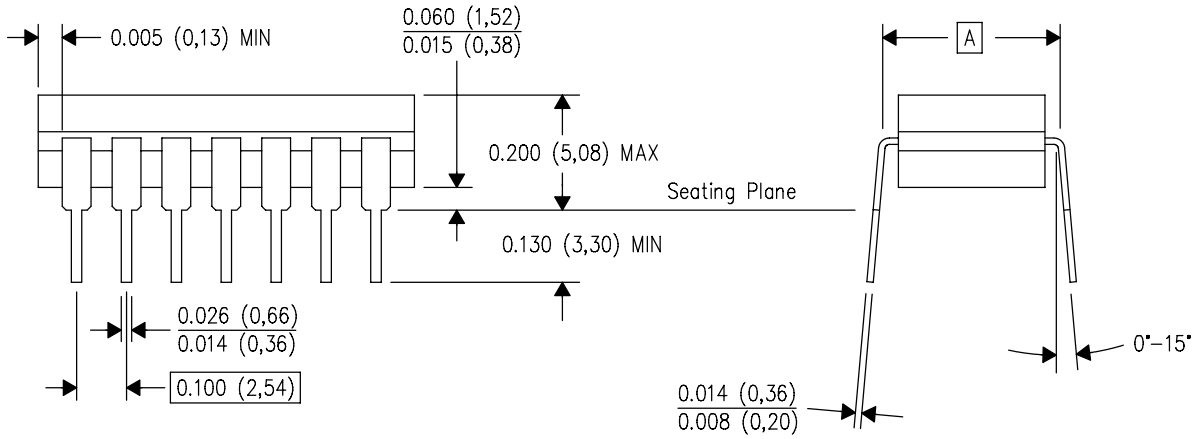
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

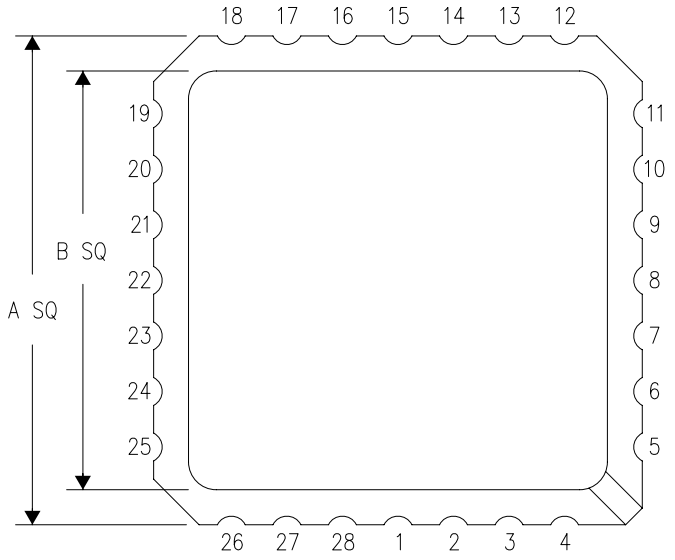



4040083/F 03/03

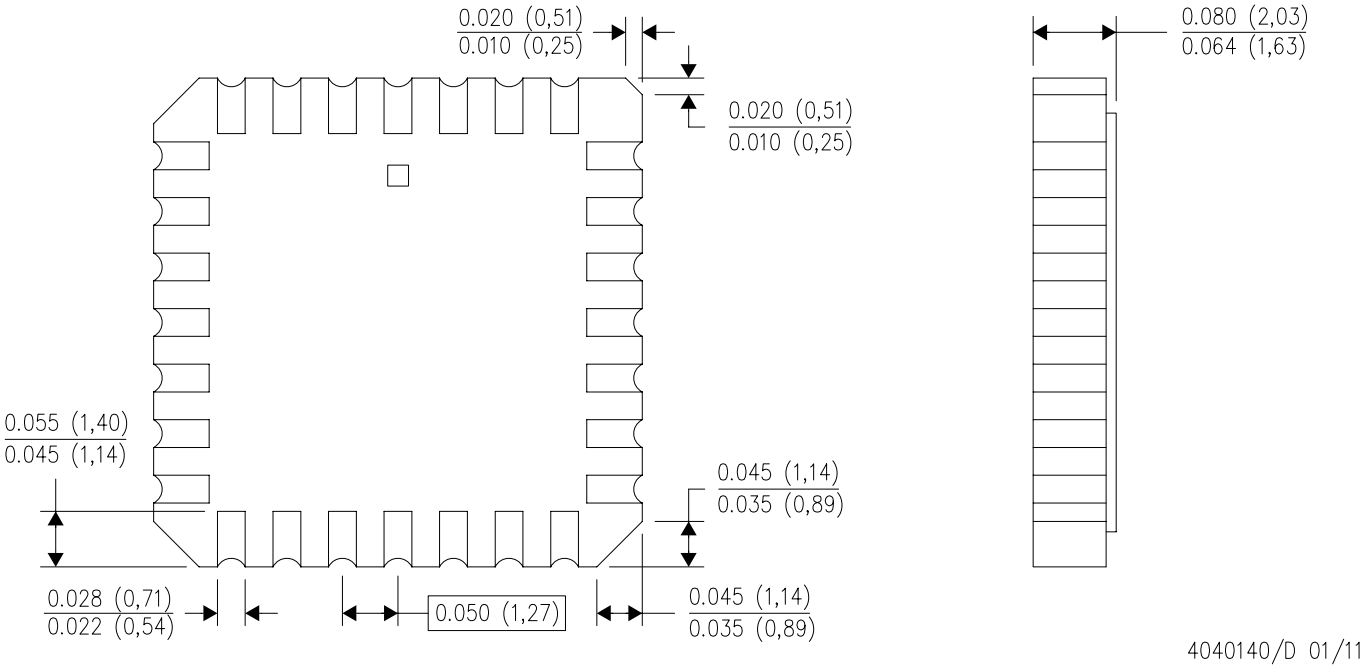
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



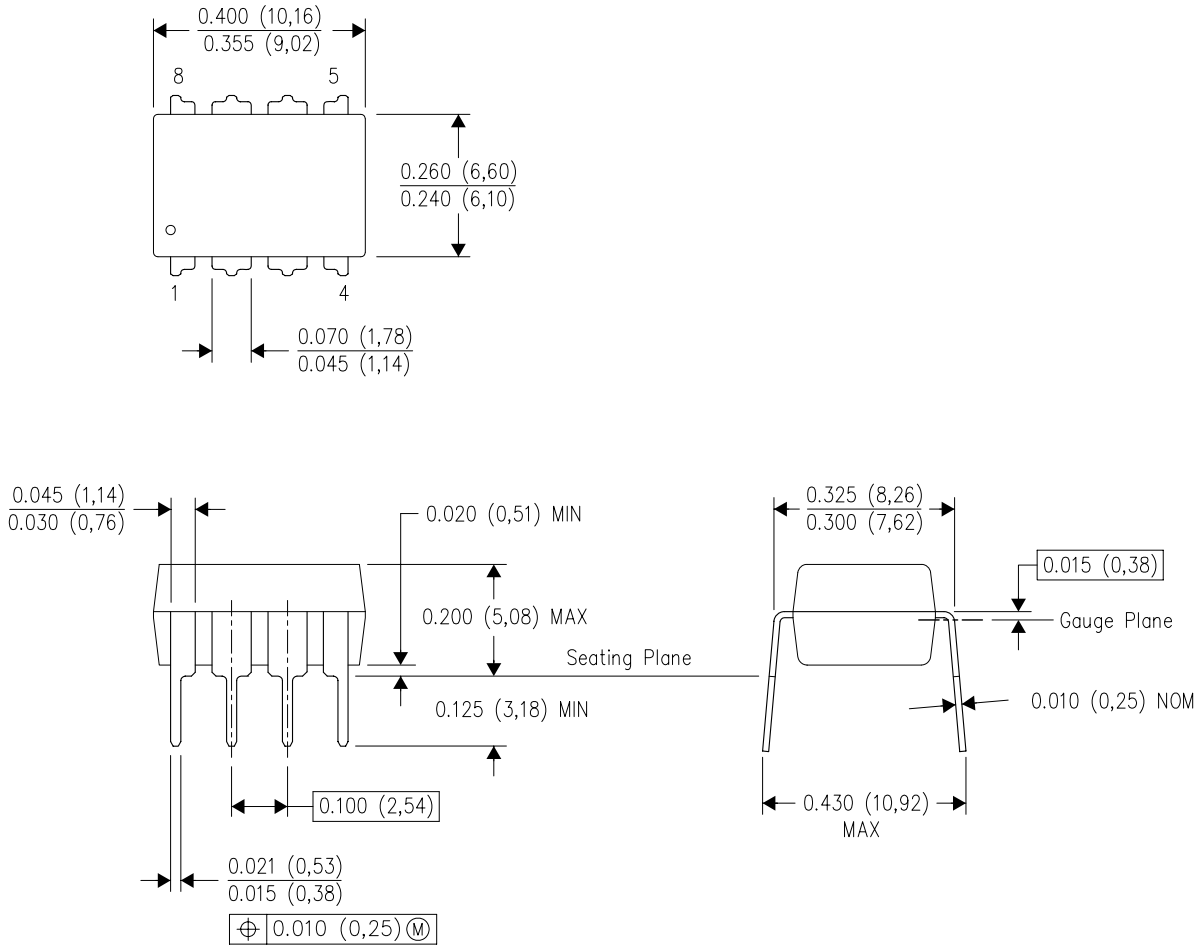

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

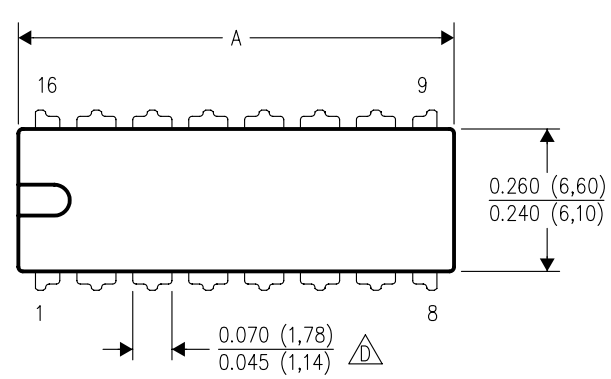



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

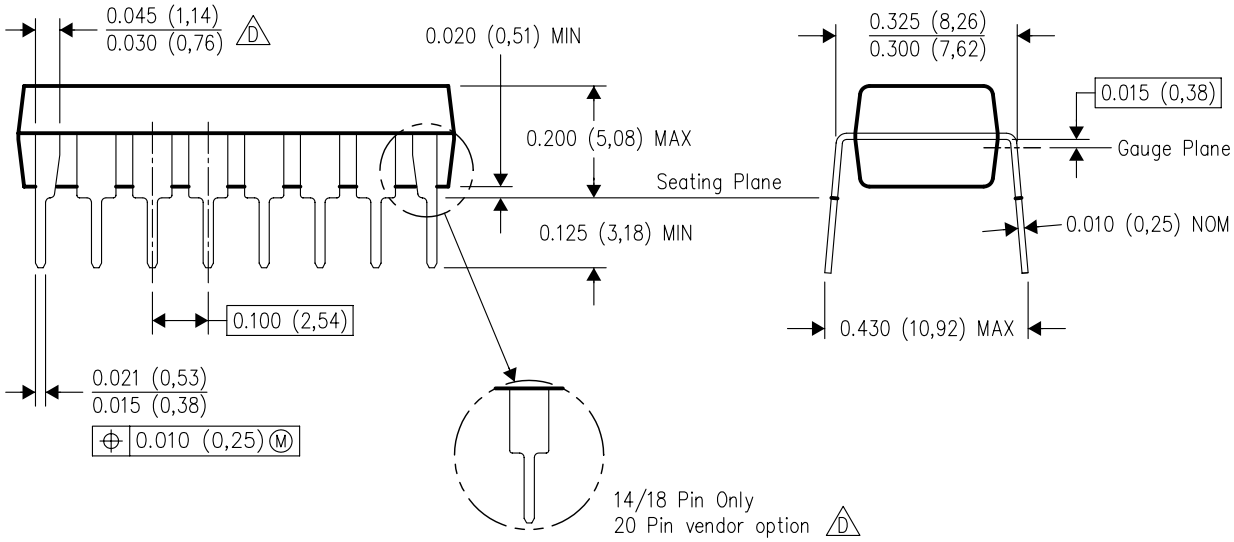
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



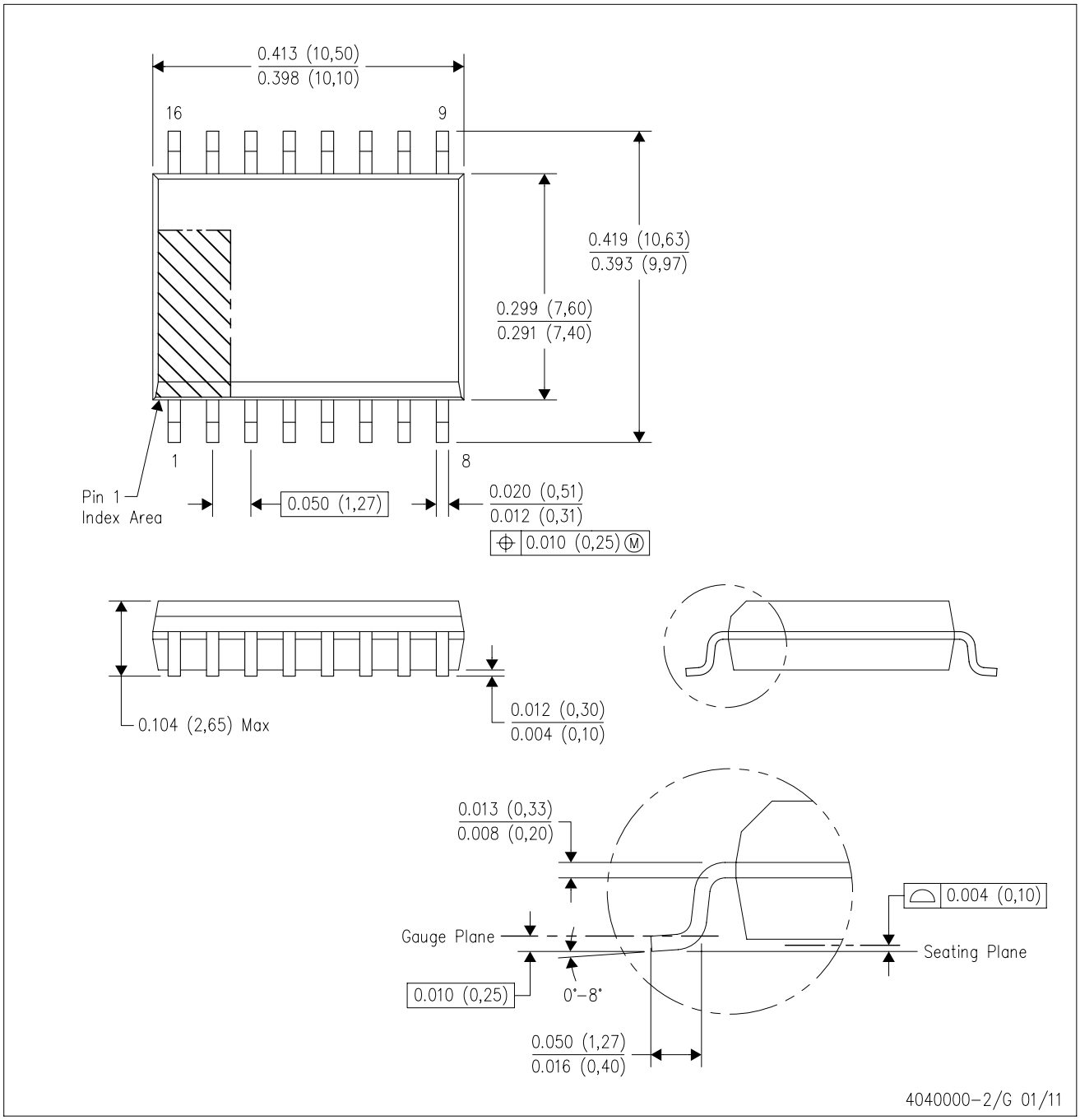

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

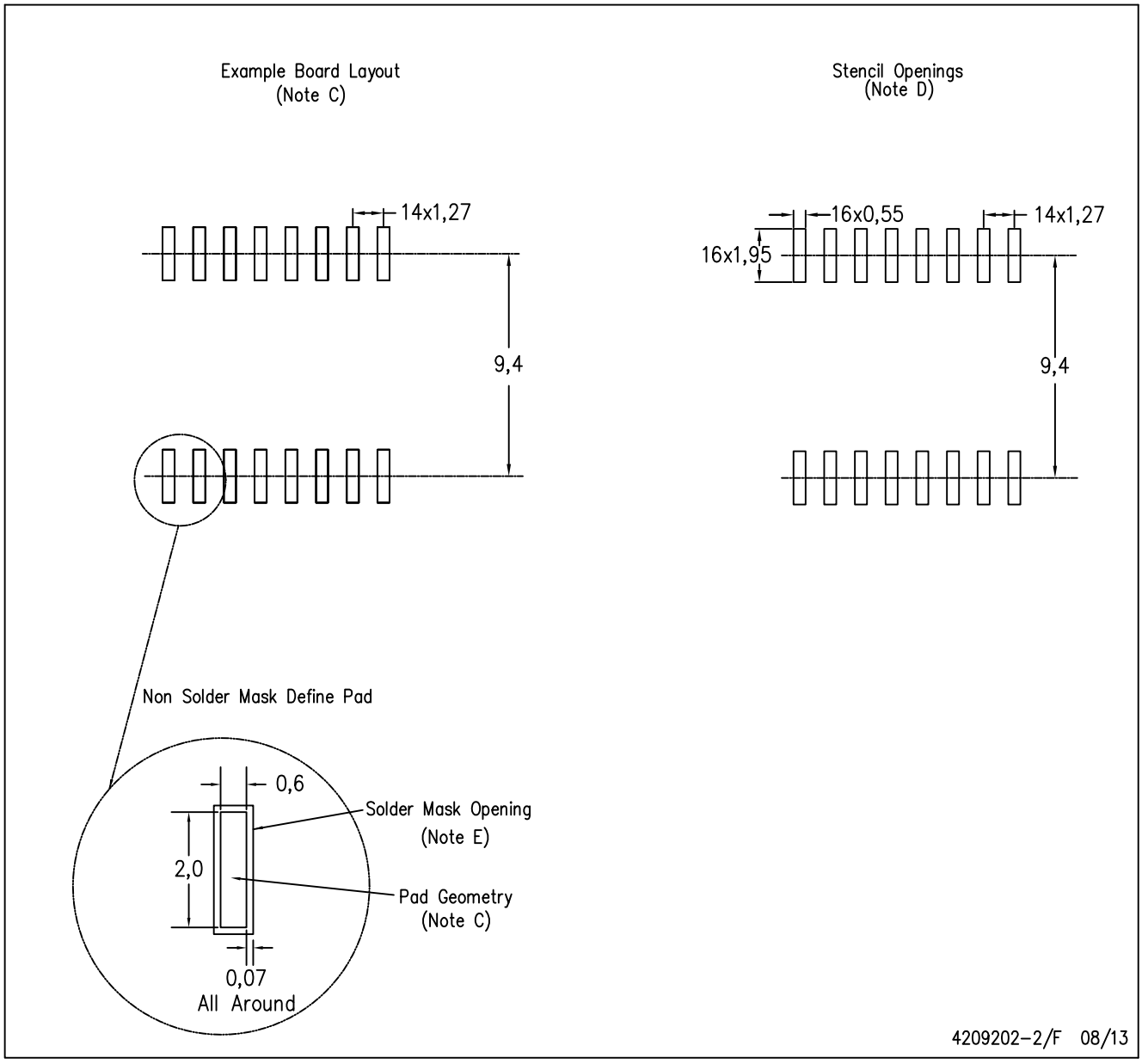
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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