LVDS Interface ICs

35bit LVDS Receiver 5:35 DeSerializer

BU90R104

No.11057EBT09

●Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operates from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

●Features

1) Five channels of LVDS data stream are converted to 35bits data of parallel LVCMOS level outputs.
2) 30bits of RGB output data, 5bits of timing and control output data(HSYNC, VSYNC, DE, CTL1 and CTL2) are transmitted available.
3) Support clock frequency from 8MHz up to 112MHz.
4) Support consumer video format including 480i, 480P, 720P and 1080i as well.
5) Support many kinds of PC video formats such as VGA, SVGA, XGA and SXGA.
6) Provide 784Mbps per 1ch or 3.92Gbps per device throughput rate using 112MHz clock rate.
7) User programmable LVCMOS data output triggering timing by using either rising or falling edge of clock.
8) 30bit LVDS transmitter is recommended to use BU8254KVT.

●Applications

Flat Panel Display

●Absolute maximum ratings

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Supply voltage	V_{DD}	-0.3	4.0	V
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Output voltage	V_{OUT}	-0.3	V_{DD}+0.3	V
Storage temperature range	Tstg	-55	125	℃

●Package power

Package	PD(mW)	DERATING(mW/℃) *1
TQFP64V	700	7.0
	1000*2	10.0*2

*1 At temperature Ta > 25℃
*2 Package power when mounting on the PCB board.
The size of PCB board :70×70×1.6(mm^3)
The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area)

●Recommended operating conditions

Parameter	Symbol	Ratings			Unit	Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.3	3.3	3.6	V	VDD, LVDD, PVDD
Supply Noise Voltage	V_{NOZ}	-	-	0.1	V	
Operating temperature range	Topr	-20	-	85	℃	Clock frequency from 8MHz up to 90MHz
		0	-	70	℃	Clock frequency from 90MHz up to 112MHz

●Block Diagram

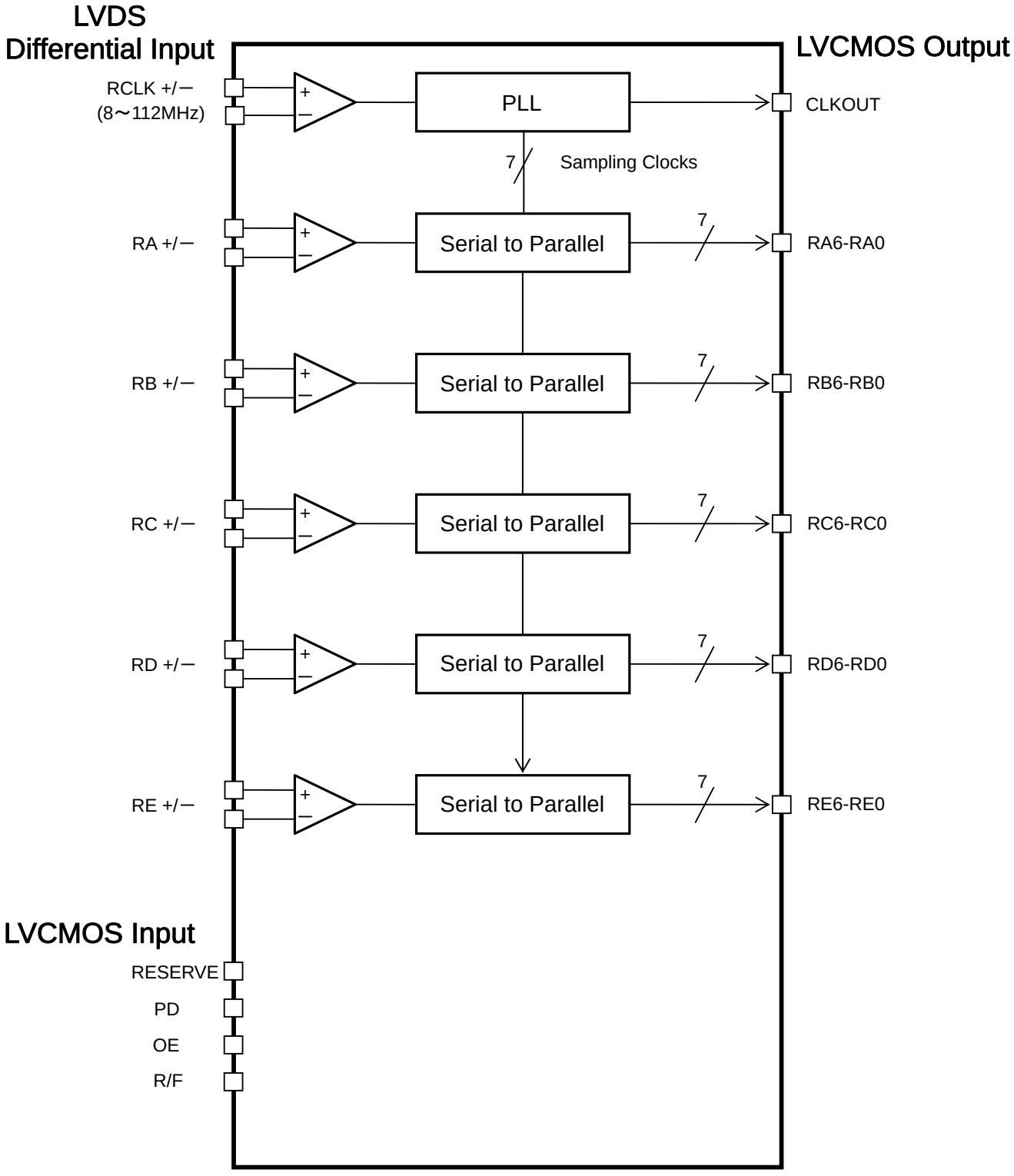


Fig.1 Block Diagram

●TQFP64V Package Specification

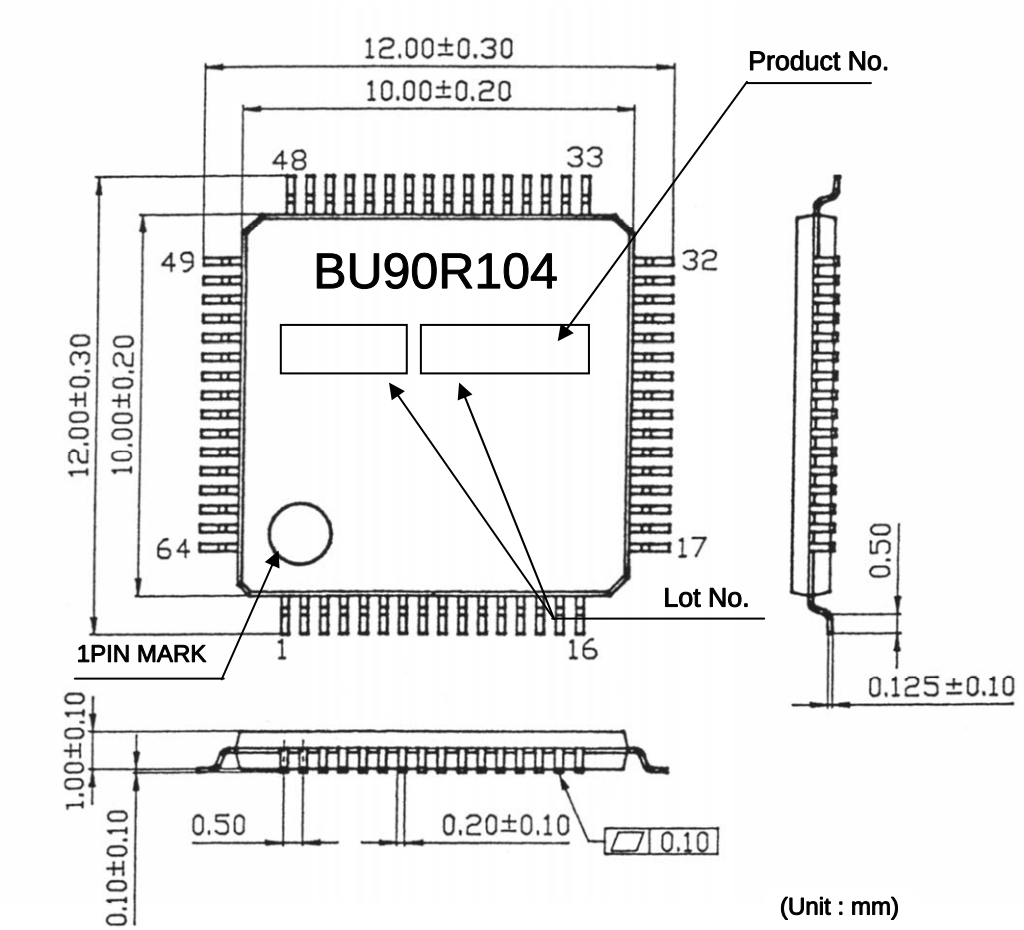


Fig.2 TQFP64V Package

●Pin Diagram

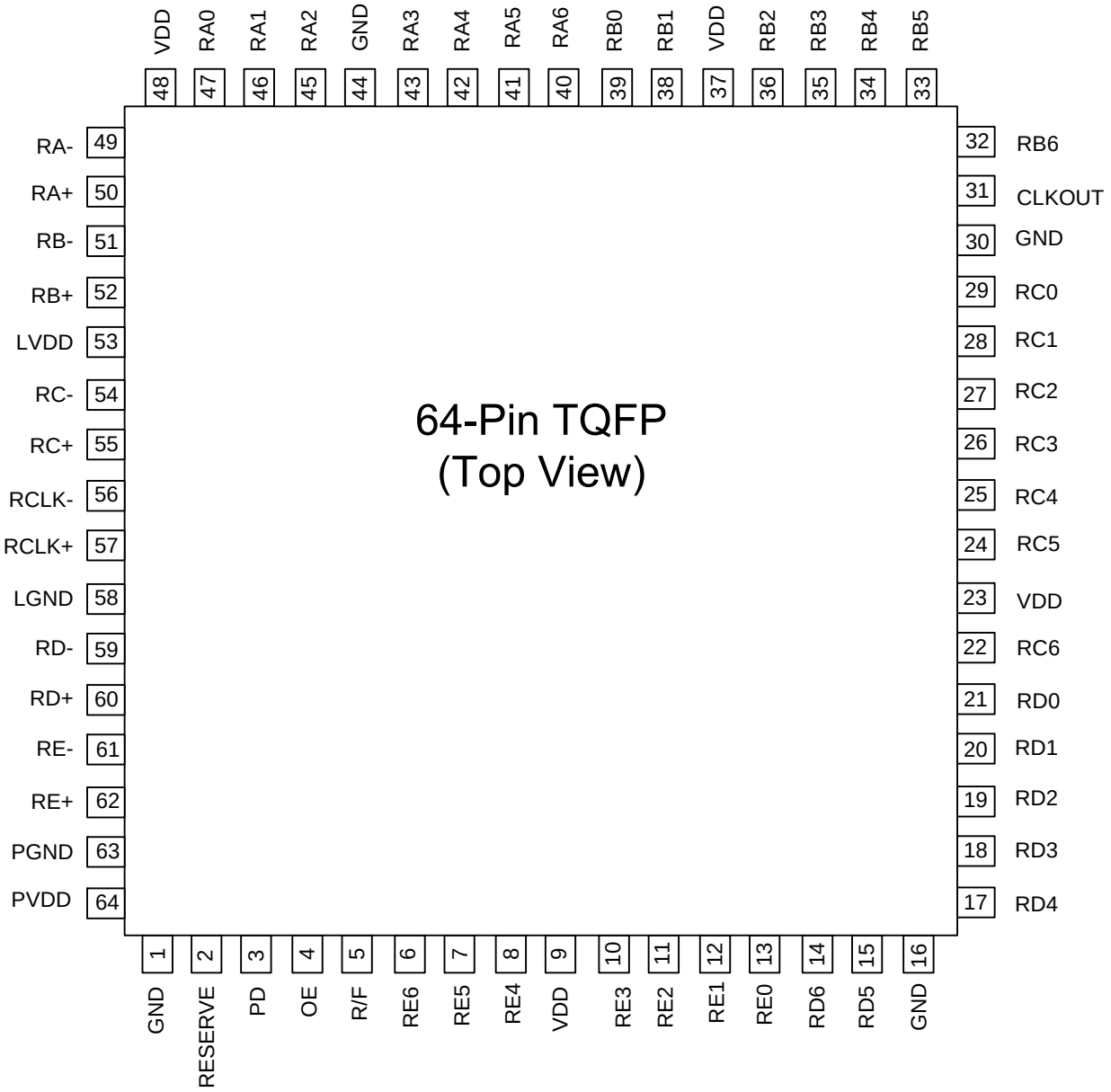


Fig.3 Pin diagram (Top view)

●Pin Description

Pin Name	Pin No.	I/O	Description
RA+, RA-	50,49	LVDS Input	LVDS data input + : Positive input of LVDS data differential pair. - : Negative input of LVDS data differential pair.
RB+, RB-	52,51	LVDS Input	
RC+, RC-	55,54	LVDS Input	
RD+, RD-	60,59	LVDS Input	
RE+, RE-	62,61	LVDS Input	
RCLK+, RCLK-	57,56	LVDS Input	LVDS clock input
RA6～RA0	40,41,42,43, 45,46,47	Output	LVCMOS data outputs.
RB6～RB0	32,33,34,35, 36,38,39	Output	
RC6～RC0	22,24,25,26, 27,28,29	Output	
RD6～RD0	14,15,17,18, 19,20,21	Output	
RE6～RE0	6,7,8,10, 11,12,13	Output	
RESERVE	2	Input	Reserved input must be “Low” for normal operation.
PD	3	Input	Power down input for the internal system. H : Normal operation. L : Power down (All output are “Low”).
OE	4	Input	Power down input for the data output driver. H : Output enable (Normal operation). L : Output disable (All outputs are “Hi-Z”).
R/F	5	Input	Select input pin for data output clock triggering edge. H : Output data is latched on rising edge. L : Output data is latched on falling edge.
VDD	9,23,37,48	Power	3.3V output driver and digital core power supply pin.
CLKOUT	31	Output	LVCMOS level clock output.
GND	1,16,30,44	Ground	GND pin for both data output driver cells and the digital cores.
LVDD	53	Power	Power supply pin for LVDS inputs.
LGND	58	Ground	Ground pin for LVDS inputs.
PVDD	64	Power	Power supply pin for PLL core.
PGND	63	Ground	Ground pin for PLL core.

●Function Description

PD	R/F	OE	Data output (Rxn) *1	Clock output
0	0	0	Hi-Z	Hi-Z
0	0	1	All fixed low	Fixed Low
0	1	0	Hi-Z	Hi-Z
0	1	1	All fixed low	Fixed Low
1	0	0	Hi-Z	Hi-Z
1	0	1	Data output	Output data is latched by falling edge of clock.
1	1	0	Hi-Z	Hi-Z
1	1	1	Data output	Output data is latched by rising edge of clock

*1 : Rxn
x = A,B,C,D,E
n = 0,1,2,3,4,5,6

●Electrical Characteristics

■DC Characteristics

○LVCMOS DC character (V_{DD}=2.3V～3.6V, Ta=-20℃～85℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
High Input voltage	V_{IH}	V_{DD}×0.8	-	V_{DD}	V	
Low Input voltage	V_{IL}	0.0	-	V_{DD}×0.2	V	
High Output voltage	V_{OH}	V_{DD}-0.5	-	V_{DD}	V	I_{OH}=-4mA (data) I_{OH}=-8mA (clock)
Low Output voltage	V_{OL}	0.0	-	0.4	V	I_{OL}=4mA (data) I_{OL}=8mA (clock)
Input current	I_{INC}	-	-	±10	μA	$0V \leqq V_{IN} \leqq V_{DD}$

○LVDS Receiver DC character (V_{DD}=2.3V～3.6V, Ta=-20℃～85℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Differential input High threshold	VTH	-	-	100	mV	V_{OC}*1=1.2V
Differential input Low threshold	VTL	-100	-	-	mV	V_{OC}*1=1.2V
Input current	IINL	-	-	±25	μA	V_{IN}=2.4V / 0V V_{DD}=3.6V

*1 Common Mode Voltage

■Supply Current

○Supply current

Parameter	Symbol	Limits		Unit	Conditions	
		Min.	Max.			
Receiver supply current (Gray Scale Pattern)	I_{RCCG}	52	-	mA	fCLKOUT=90MHz	C_L=8pF, V_{DD}=3.3V
Receiver supply current (Worst Case Pattern)	I_{RCCW}	95	-	mA	fCLKOUT=90MHz	C_L=8pF, V_{DD}=3.3V
Receiver power down supply current	I_{RCCS}	-	10	μA	PD=L, OE=L	

Gray Scale Pattern

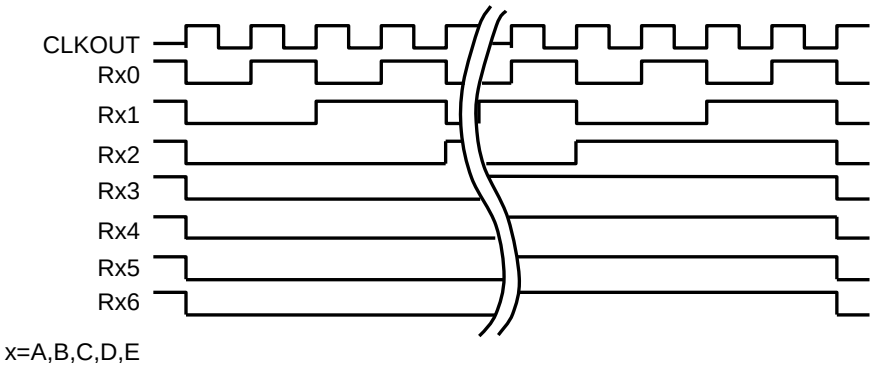


Fig.4 Gray Scale Pattern

Worst Case Pattern (Maximum power condition)

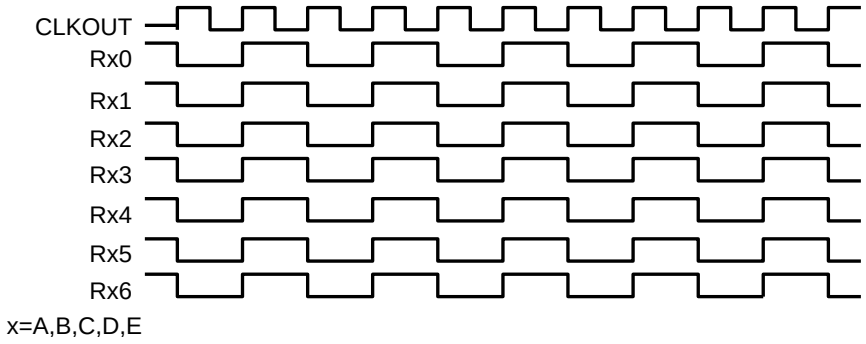


Fig.5 Worst Case Pattern

■AC Characteristics

○Switching characteristics

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
CLKOUT period	t_{RCP}	8.93	-	125	ns
CLKOUT "H" time	t_{RCH}	-	$0.5t_{RCP}$-1.0	-	ns
CLKOUT "L" time	t_{RCL}	-	$0.5t_{RCP}$-1.0	-	ns
LVCMOS data setup to CLKOUT	t_{RS}	$0.5t_{RCP}$-1.4	-	-	ns
LVCMOS data hold from CLKOUT	t_{RH}	$0.23t_{RCP}$-1.0	-	-	ns
LVCMOS data rise time	t_{TLH}	-	1.0	2.0	ns
LVCMOS data fall time	t_{THL}	-	1.0	2.0	ns
Input data position 0	t_{RIP1}	-0.25	0.0	+0.25	ns
Input data position 1	t_{RIP0}	$\frac{t_{RCIP}}{7}$ -0.25	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}$ +0.25	ns
Input data position 2	t_{RIP6}	$2\frac{t_{RCIP}}{7}$ -0.25	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}$ +0.25	ns
Input data position 3	t_{RIP5}	$3\frac{t_{RCIP}}{7}$ -0.25	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}$ +0.25	ns
Input data position 4	t_{RIP4}	$4\frac{t_{RCIP}}{7}$ -0.25	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}$ +0.25	ns
Input data position 5	t_{RIP3}	$5\frac{t_{RCIP}}{7}$ -0.25	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}$ +0.25	ns
Input data position 6	t_{RIP2}	$6\frac{t_{RCIP}}{7}$ -0.25	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}$ +0.25	ns
Phase Locked Loop set time	t_{RPLL}	-	-	10.0	ms
Clock input period	t_{RCIP}	8.93	-	125	ns

●AC Timing Diagrams

■LVCMOS

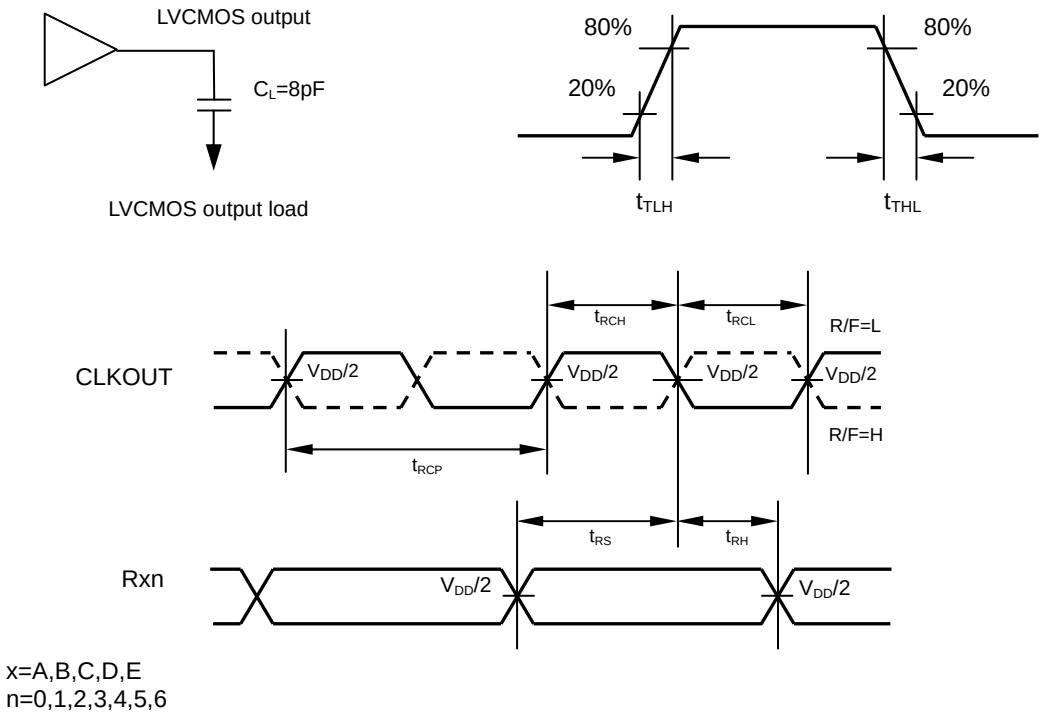


Fig.6 LVCMOS output timing

■Phase-Locked Loop set time

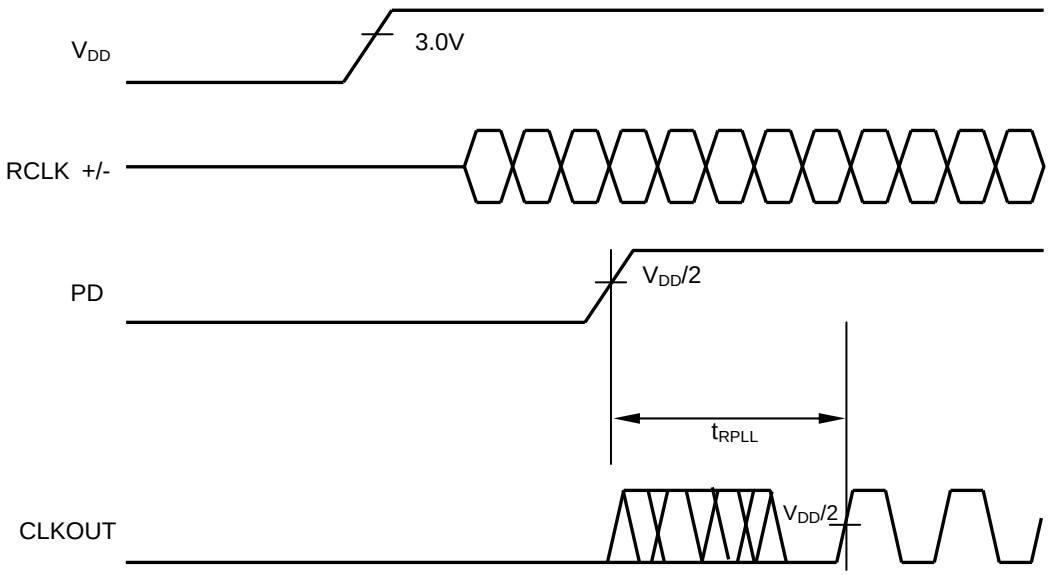


Fig.7 Phase-Locked Loop set time

●LVDS Data, Clock Input Timing

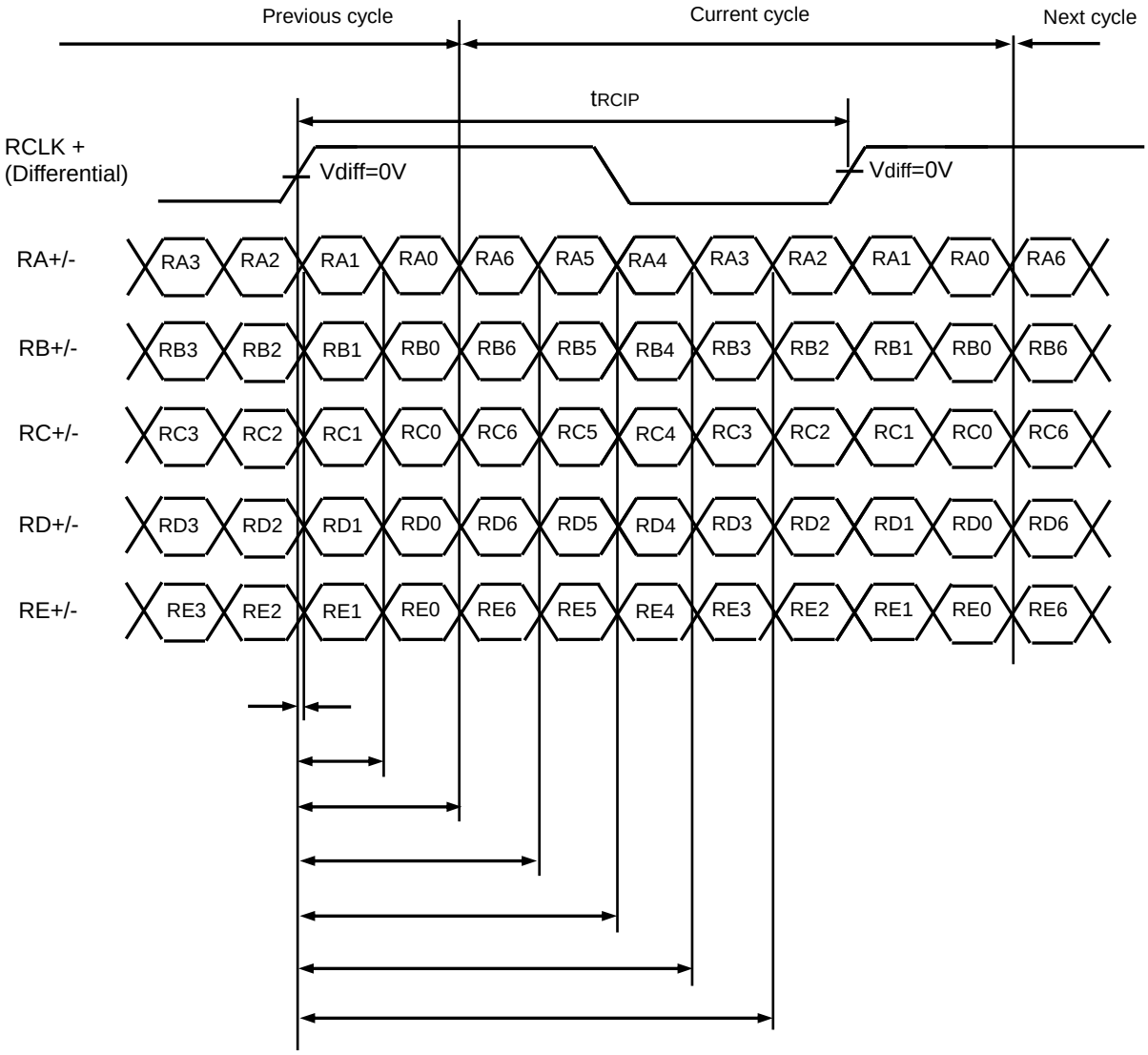


Fig.8 LVDS data and clock input timing

●LVDS Data, Clock Input and LVSMOS Output Timing

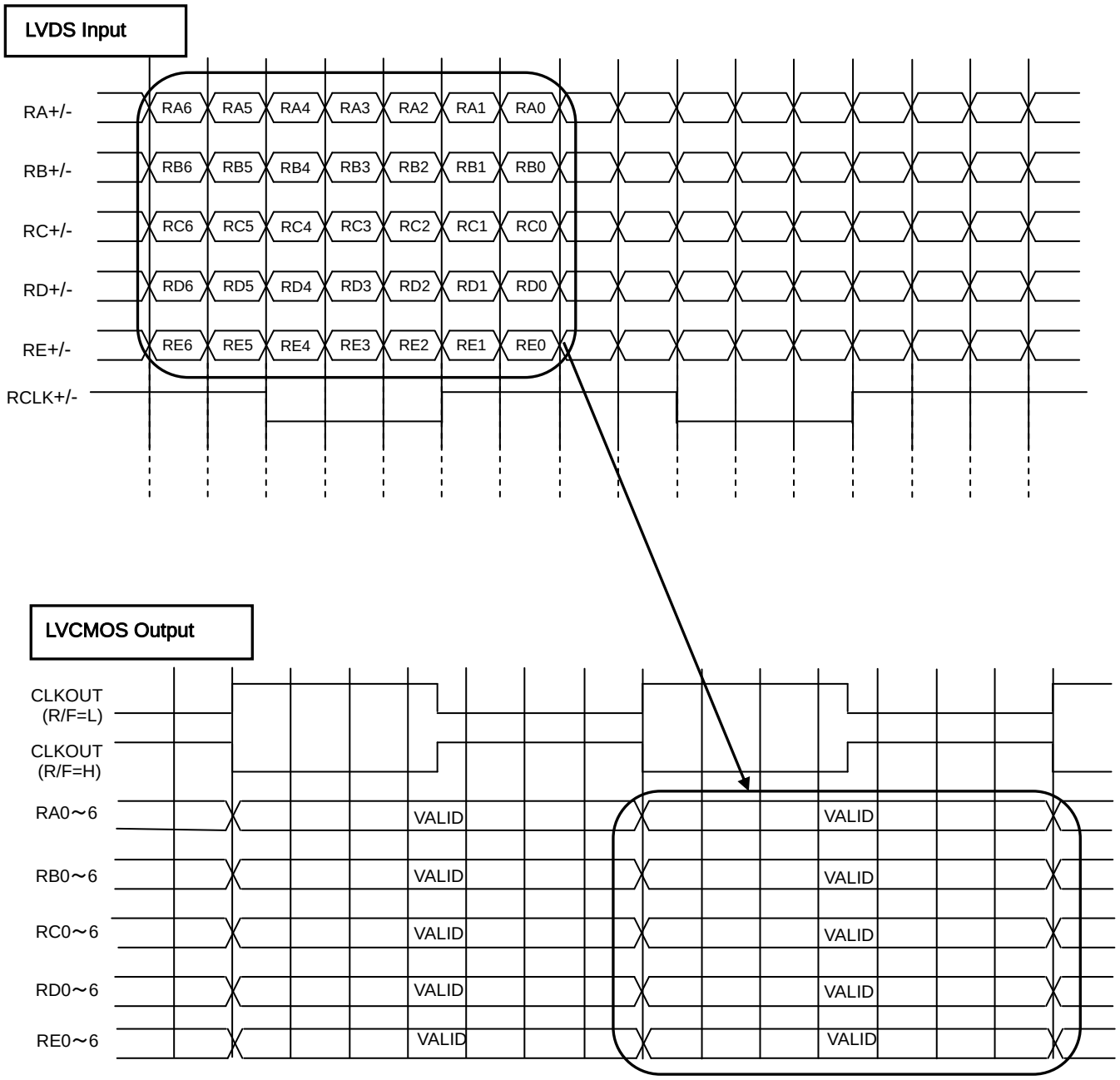


Fig.9 LVDS Data, Clock Input and LVCMOS Output Timing

●About the Power On Reset

Power on reset is not mandatory for this device.
(The PD pin should be set to high level when power on reset procedure is not used.)

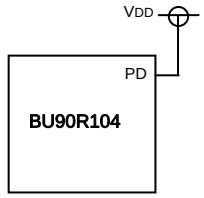
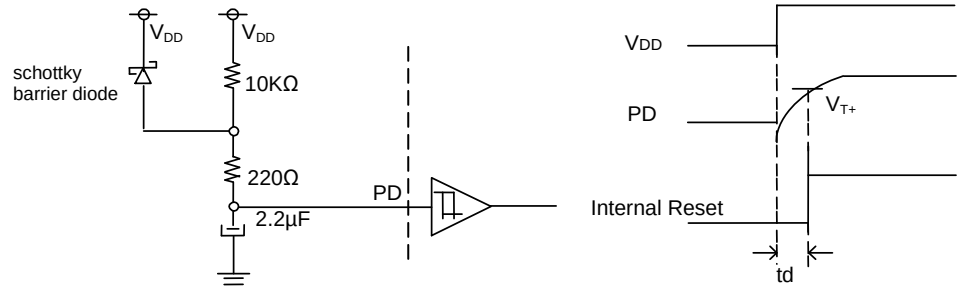


Fig.10 Terminal connection when power on reset is not used.

However, Power on reset procedure is strongly recommend for internal logic initialization by following two methods.
①The method of using CR circuit.
②The method of using external specific IC.

It is recommend to do enough examination for target application.



Be careful of temperature ofthe capacitor especially over and again.
B characteristic ceramics and function polymer aluminum electrolysis are recommended.

td is approximately equal to 20ms when the left RC coleus are applied.

Fig.11 Power on reset by external a CR circuit

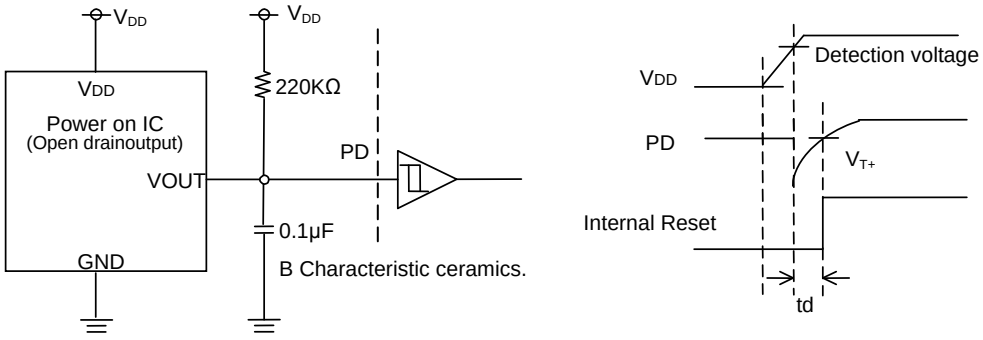
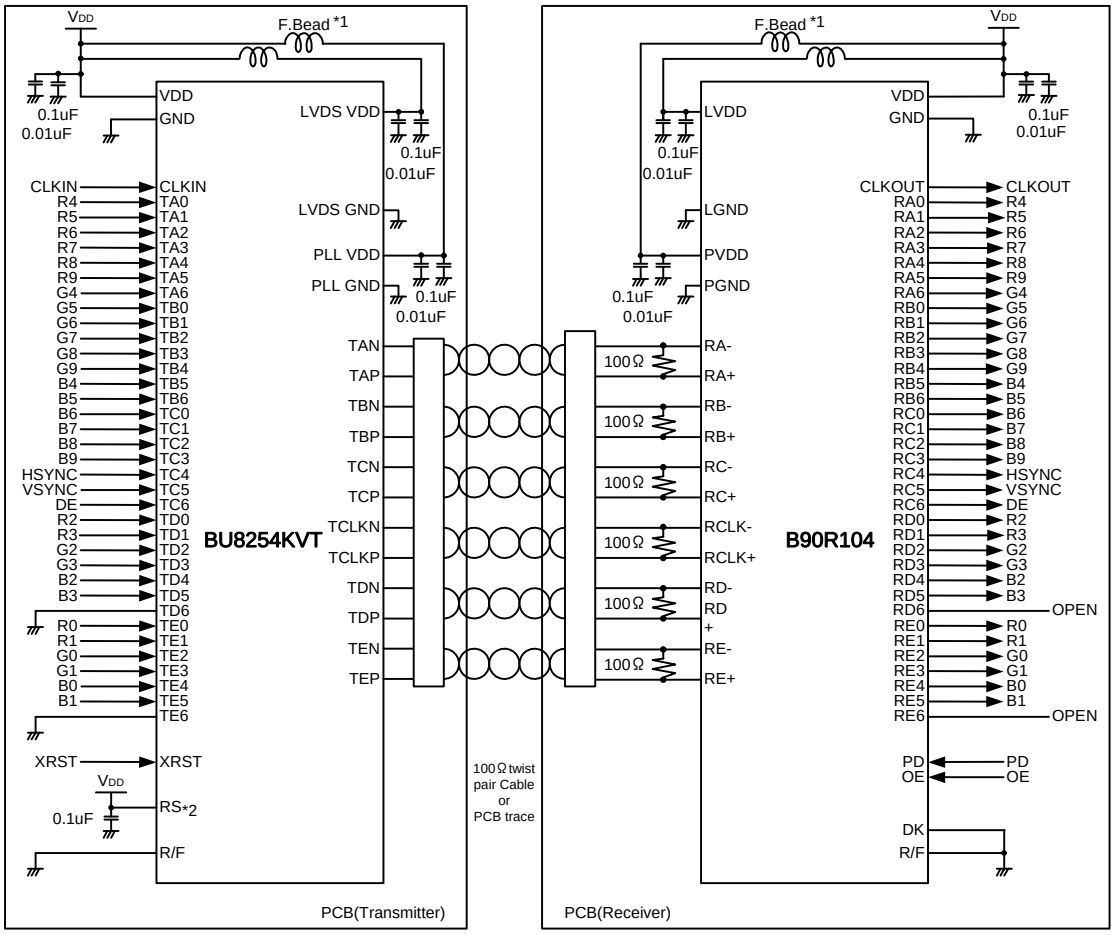


Fig.12 Power on reset by specific IC

●10 LVDS Level Input & Output

Example:
BU8254KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output
BU90R104 : LVCMOS level output/Falling edge

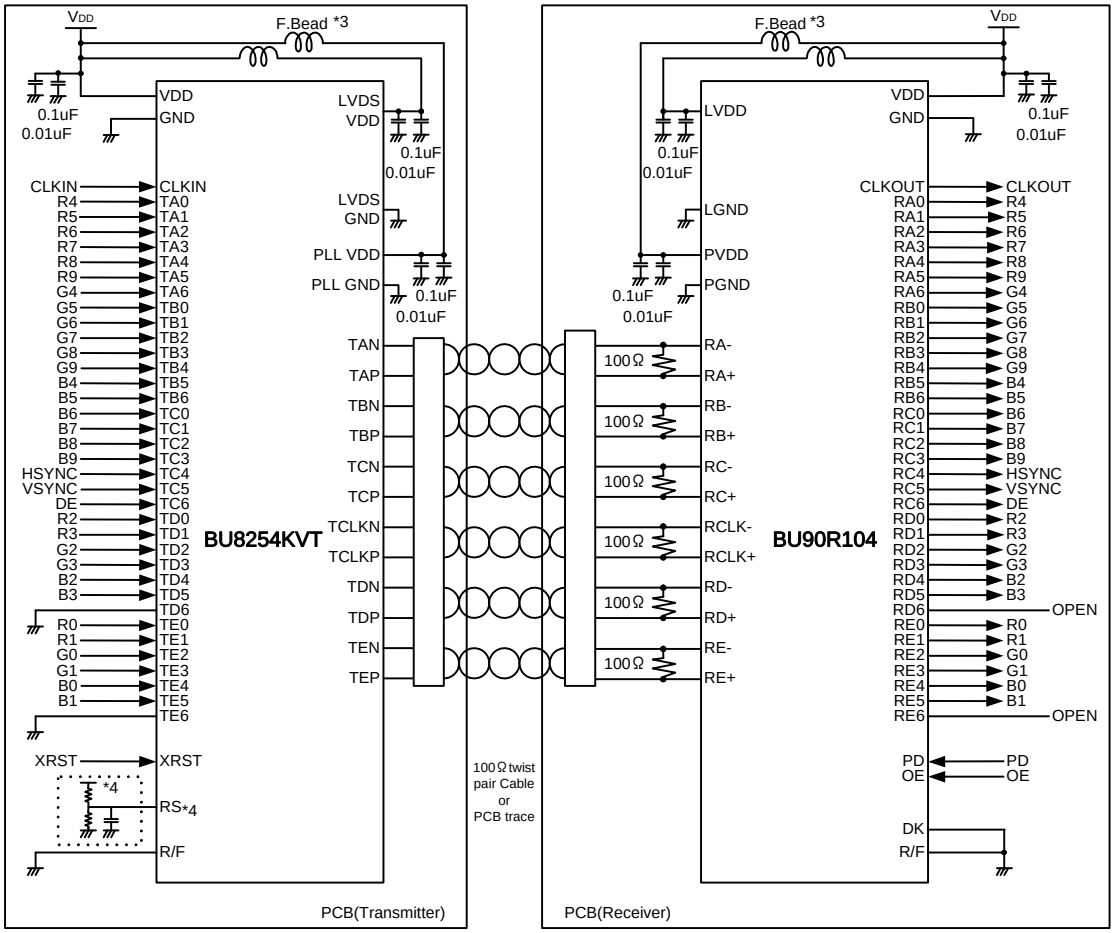


*1: Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing Co.)
*2 : If RS pin is tied to V_{DD}, LVDS swing is 350 mV.
If RS pin is tied to GND, LVDS swing is 200 mV.

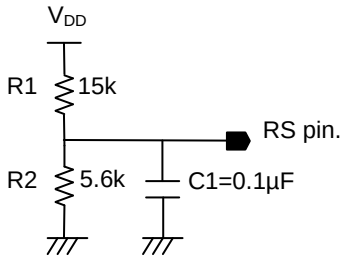
Fig.13

●10bit Small Swing Input & LVCMOS Level Output

Example:
BU8254KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output
BU90R104 : LVCMOS level output/Falling edge



*3 Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing Co.)
*4 : RS pin acts as VREF input pin when input voltage is set to half of high level signal input.
We recommend to locate by-pass condenser near the RS pin.



Example for LVTTL(1.8V input):(R1,R2)=(15kΩ,5.6kΩ)

Fig.14

●Notes for use

1) This chip is not designed to protect from radioactivity.

2) The chip is made strictly for the specific application or equipment.
Then it is necessary that the unit is measured as need.

3) This document may be used as strategic technical data which subjects to COCOM regulations.

●Ordering part number

B	U		9	0	R	1	0	4	-	E	2

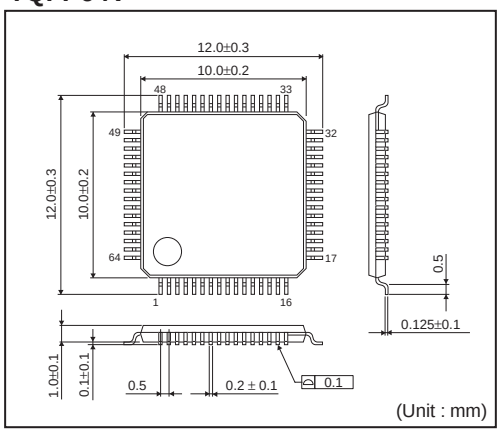
Part No.

Part No.
90R104

Package
TQFP64V

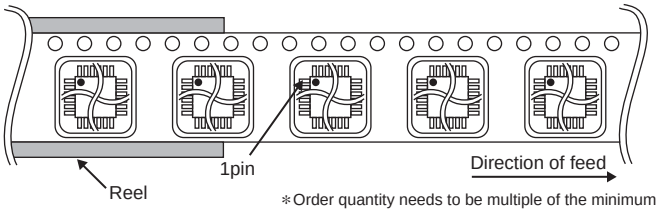
Packaging and forming specification
E2: Embossed tape and reel

TQFP64V



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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