National Semiconductor

PRELIMINARY
November 3, 2008

ADC10D1000
Low Power, 10-Bit, Dual 1.0 GSPS or Single 2.0 GSPS A/D Converter

1.0 General Description

The ADC10D1000 is the latest advance in National's Ultra-High-Speed ADC family. This low-power, high-performance CMOS analog-to-digital converter digitizes signals at 10-bit resolution for dual channels at sampling rates of up to 1.0 GSPS (Non-DES Mode) or for a single channel up to 2.0 GSPS (DES Mode). The ADC10D1000 achieves excellent accuracy and dynamic performance while dissipating less than 2.8 Watts. The product is packaged in a leaded or lead-free 292-ball thermally enhanced BGA package which does not require a heat sink over the rated industrial temperature range of -40°C to +85°C.

The ADC10D1000 builds upon the features, architecture and functionality of the 8-bit GHz family of ADCs. An expanded feature set includes AutoSync for multi-chip synchronization, 15-bit programmable gain and 12-bit plus sign programmable offset adjustment for each channel. The improved internal track-and-hold amplifier and the extended self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing 9.0 Effective Number of Bits (ENOB) with a 498 MHz input signal and a 1.0 GHz sample rate while providing a 10^{-18} Code Error Rate (CER) Dissipating a typical 2.8 Watts in Non-Demultiplex Mode at 1.0 GSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range.

Each channel has its own independent DDR Data Clock, DCLKI and DCLKQ, which are in phase when both channels are powered up, so that only one Data Clock could be used to capture all data, which is sent out at the same rate as the input sample clock. If the 1:2 Demux Mode is selected, a second 10-bit LVDS bus becomes active for each channel, such that the output data rate is sent out two times slower to relax data-capture timing requirements. The part can also be used as a single 2.0 GSPS ADC to sample one of the I or Q inputs. The output formatting can be programmed to be offset binary or two's complement and the Low Voltage Differential Signaling (LVDS) digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.2V to allow for power reduction for well-controlled back planes.

2.0 Features

- Excellent accuracy and dynamic performance
- Low power consumption
- Internally terminated, buffered, differential analog inputs
- R/W SPI Interface for Extended Control Mode
- Dual-Edge Sampling Mode, in which the I- and Q-channels sample one input at twice the sampling clock rate
- Test patterns at output for system debug
- Programmable 15-bit gain and 12-bit plus sign offset
- 1:1 non-demuxed or 1:2 demuxed LVDS outputs
- AutoSync feature for multi-chip systems
- Single 1.9V ± 0.1V power supply
- 292-ball BGA package (27mm x 27mm x 2.4mm with 1.27mm ball-pitch); no heat sink required
- LC sampling clock filter for jitter reduction

3.0 Key Specifications

(Non-Demux Non-DES Mode, Fs=1.0 GSPS, Fin = 248 MHz)

- Resolution — 10 Bits
- Conversion Rate
  - — Dual channels at 1.0 GSPS (typ)
  - — Single channel at 2.0 GSPS (typ)
- Code Error Rate — 10^{-18} (typ)
- ENOB — 9.1 bits (typ)
- SNR — 56.7 dBc (typ)
- SFDR — 66 dBc (typ)
- Full Power Bandwidth — 2.8 GHz (typ)
- DNL — ±0.2 LSB (typ)
- Power Consumption
  - — Single Channel Enabled — 1.61W (typ)
  - — Dual Channels Enabled — 2.77W (typ)
  - — Power Down Mode — 59 mW (typ)

4.0 Applications

- Wideband Communications
- Data Acquisition Systems
- Digital Oscilloscopes

5.0 Ordering Information

Industrial Temperature Range ($-40°C < T_A < +85°C$)	NS Package
ADC10D1000CIUT/NOPB	Lead-free 292-Ball BGA Thermally Enhanced Package
ADC10D1000CIUT	Leaded 292-Ball BGA Thermally Enhanced Package
ADC10D1000RB	Reference Board

If Military/Aerospace specified devices are required, please contract the National Semiconductor Sales Office/Distributors for availability and specifications. IBIS models are available at: http://www.national.com/analog/adc/ibis_models.

6.0 Block Diagram

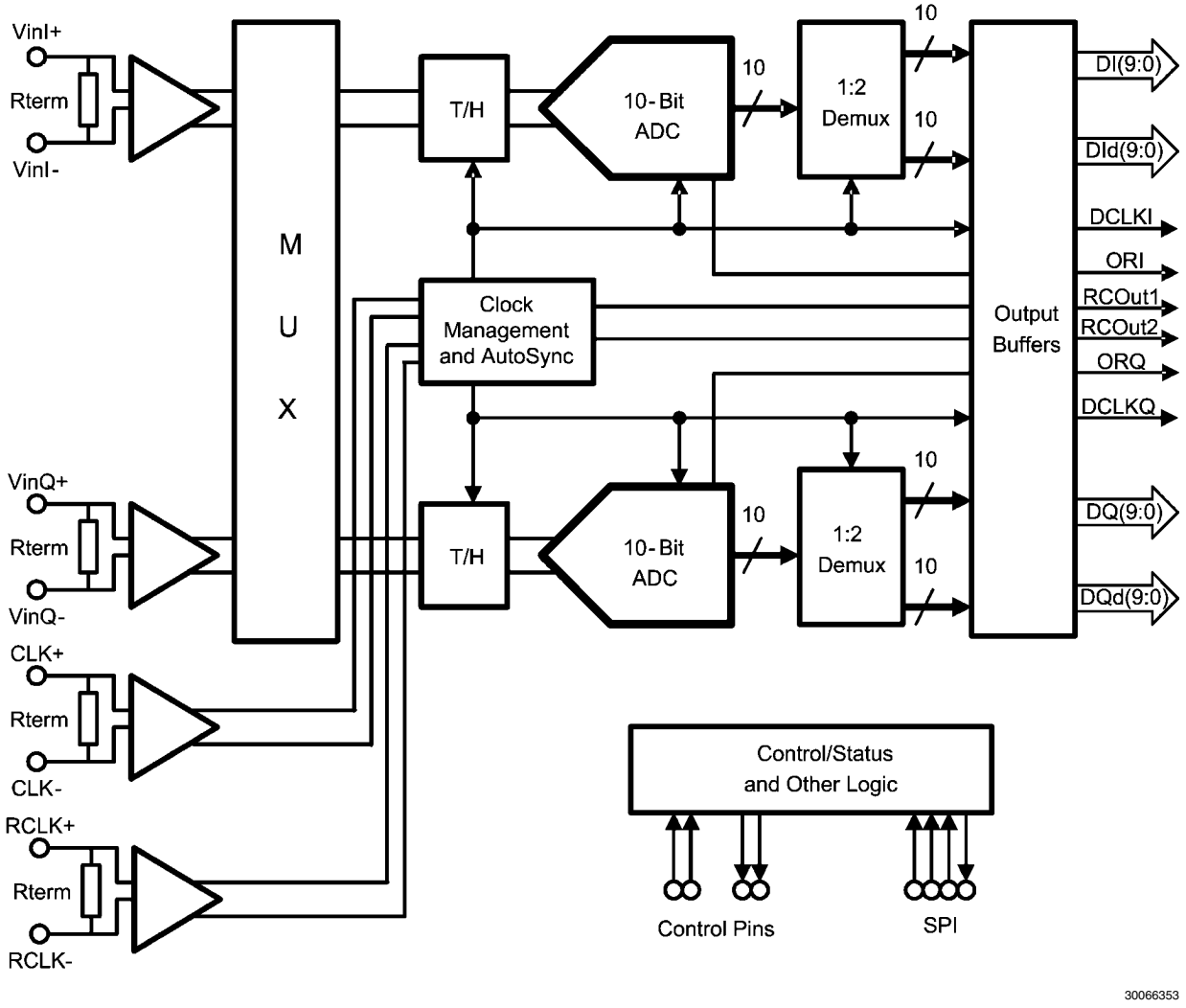

FIGURE 1. Simplified Block Diagram

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7.0 Connection Diagram

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A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	RSV	V_DR	DId1+	GND_DR	DId4+	V_DR	DId7+	GND_DR	DId9+	DId9-	GND_DR	A
B	Vbg	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	RSV	DId0+	DId1-	DId3+	DId4-	DId6+	DId7-	DId8+	RSV	RSV	RSV	B
C	Rtrim+	Vcmo	Rext+	SCSb	SCLK	V_A	V_A	V_E	GND_E	RSV	DId0-	DId2+	DId3-	DId5+	DId6-	DId8-	RSV	V_DR	DI0+	DI0-	C
D	DNC	Rtrim-	Rext-	GND	GND	CAL	DNC	V_A	V_A	RSV	V_DR	DId2-	GND_DR	DId5-	V_DR	GND_DR	V_DR	DI1+	DI2+	DI2-	D
E	V_A	Tdiode+	DNC	GND													GND_DR	DI1-	DI3+	DI3-	E
F	V_A	GND_TC	Tdiode-	DNC													GND_DR	DI4+	DI4-	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC													DI5+	DI5-	DI6+	DI6-	G
H	VinI+	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DI7+	DI7-	DI8+	DI8-	H
J	VinI-	GND_TC	V_TC	VbiasI				GND	GND	GND	GND	GND	GND				V_DR	DI9+	DI9-	V_DR	J
K	GND	VbiasI	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORI+	ORI-	DCLKI+	DCLKI-	K
L	GND	VbiasQ	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORQ+	ORQ-	DCLKQ+	DCLKQ-	L
M	VinQ-	GND_TC	V_TC	VbiasQ				GND	GND	GND	GND	GND	GND				GND_DR	DQ9+	DQ9-	GND_DR	M
N	VinQ+	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DQ7+	DQ7-	DQ8+	DQ8-	N
P	V_TC	GND_TC	V_TC	V_TC													DQ5+	DQ5-	DQ6+	DQ6-	P
R	V_A	GND_TC	V_TC	V_TC													V_DR	DQ4+	DQ4-	V_DR	R
T	V_A	GND_TC	GND_TC	GND													V_DR	DQ1-	DQ3+	DQ3-	T
U	GND_TC	CLK+	PDI	GND	GND	RCOut1-	DNC	V_A	V_A	RSV	V_DR	DQd2-	GND_DR	DQd5-	V_DR	V_DR	GND_DR	DQ1+	DQ2+	DQ2-	U
V	CLK-	DCLK _RST+	PDQ	CalDly	DES	RCOut2+	RCOut2-	V_E	GND_E	RSV	DQd0-	DQd2+	DQd3-	DQd5+	DQd6-	DQd8-	RSV	GND_DR	DQ0+	DQ0-	V
W	DCLK _RST-	GND	DNC	DDRPh	RCLK-	V_A	GND	GND_E	V_E	RSV	DQd0+	DQd1-	DQd3+	DQd4-	DQd6+	DQd7-	DQd8+	RSV	RSV	RSV	W
Y	GND	V_A	FSR	RCLK+	RCOut1+	V_A	GND	V_E	GND_E	RSV	V_DR	DQd1+	GND_DR	DQd4+	V_DR	DQd7+	GND_DR	DQd9+	DQd9-	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

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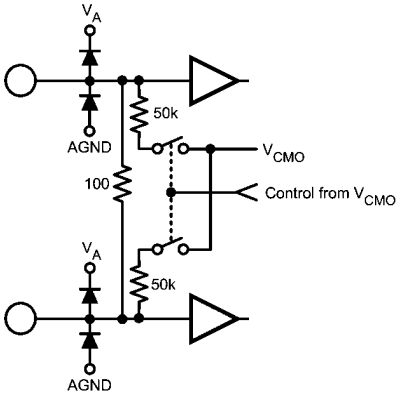
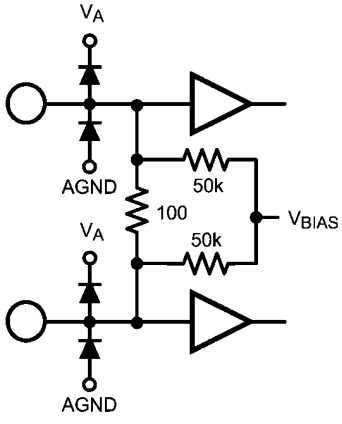
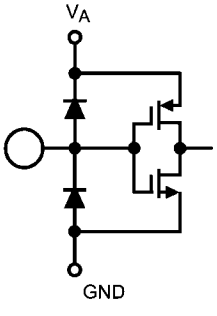
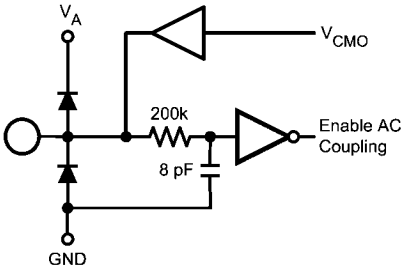
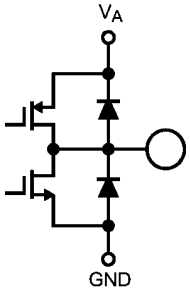
FIGURE 2. ADC10D1000 Connection Diagram

The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance. See *Section 16.5 Supply and Grounding Recommendations* for more information.

8.0 Ball Descriptions and Equivalent Circuits

TABLE 1. Analog Front-End and Clock Balls

Ball No.	Name	Equivalent Circuit	Description
H1/J1 N1/M1	VinI+/- VinQ+/-		Differential signal I- and Q-inputs. In the Non-Dual Edge Sampling (Non-DES) Mode, each I- and Q-input is sampled and converted by its respective channel with each positive transition of the CLK input. In Non-ECM (Non-Extended Control Mode) and DES Mode, both channels sample the I-input. In Extended Control Mode (ECM), the Q-input may optionally be selected for conversion in DES Mode by the DEQ Bit (Addr: 0**h**, Bit 6). Each I- and Q-channel input has an internal common mode bias that is disabled when DC-coupled Mode is selected. Both inputs must be either AC- or DC-coupled. The coupling mode is selected by the V_{CMO} Pin. In Non-ECM, the full-scale range of these inputs is determined by the FSR Pin; both I- and Q-channels have the same full-scale input range. In ECM, the full-scale input range of the I- and Q-channel inputs may be independently set via the Control Register (Addr: 3**h** and Addr: B**h**). Note that the high and low full-scale input range setting in Non-ECM corresponds to the mid and minimum full-scale input range in ECM. The input offset may also be adjusted in ECM.
U2/V1	CLK+/-		Differential Converter Sampling Clock. In the Non-DES Mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES Mode, the selected input is sampled on both transitions of this clock. This clock must be AC-coupled.
V2/W1	DCLK_RST+/-		Differential DCLK Reset. A positive pulse on this input is used to reset the DCLKI and DCLKQ outputs of two or more ADC10D1000s in order to synchronize them with other ADC10D1000s in the system. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK input. Although supported, this feature has been superseded by AutoSync.

Ball No.	Name	Equivalent Circuit	Description
C2	V_{CMO}		Common Mode Voltage Output or Signal Coupling Select. If AC-coupled operation at the analog inputs is desired, this pin should be held at logic-low level. This pin is capable of sourcing/ sinking up to 100 µA. For DC-coupled operation, this pin should be left floating or terminated into high-impedance. In DC-coupled Mode, this pin provides an output voltage which is the optimal common-mode voltage for the input signal and should be used to set the common-mode voltage of the driving buffer.
B1	V_{BG}		Bandgap Voltage Output or LVDS Common-mode Voltage Select. This pin provides a buffered version of the bandgap output voltage and is capable of sourcing/sinking 100 uA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the 1.2V LVDS common-mode voltage is selected; 0.8V is the default.
C3/D3	Rext+/-		External Reference Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rext+/-. The Rext resistor is used as a reference to trim internal circuits which affect the linearity of the converter; the value and precision of this resistor should not be compromised.
C1/D2	Rtrim+/-		Input Termination Trim Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rtrim+/-. The Rtrim resistor is used to establish the calibrated 100Ω input impedance of VinI, VinQ and CLK. These impedances may be fine tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not guaranteed for such an alternate value.
E2/F3	Tdiode+/-		Temperature Sensor Diode Positive (Anode) and Negative (Cathode) Terminals. This set of pins is used for die temperature measurements. It has not been fully characterized.

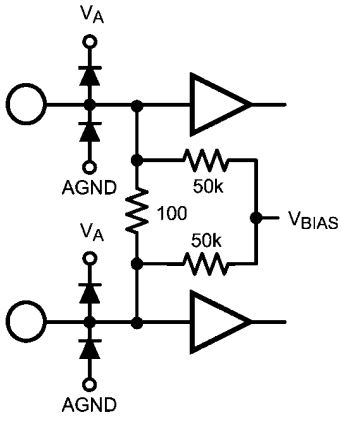
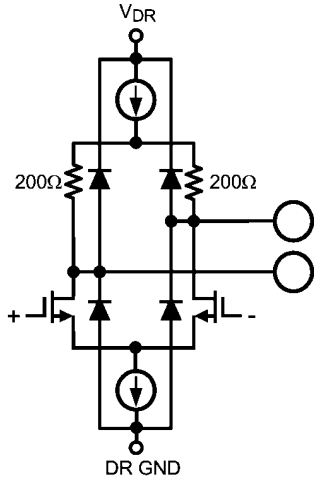
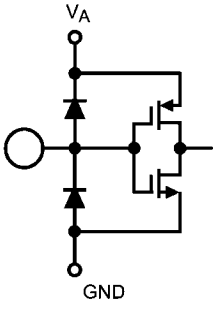
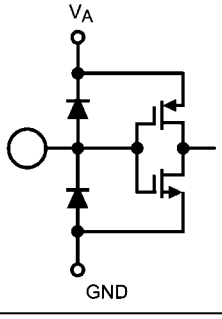
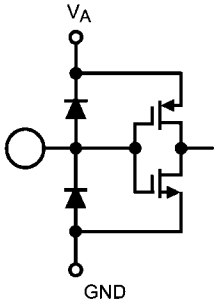
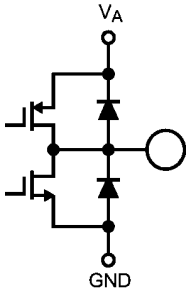
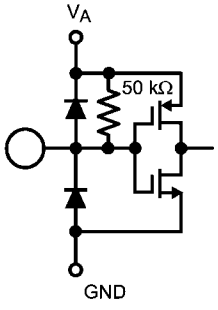
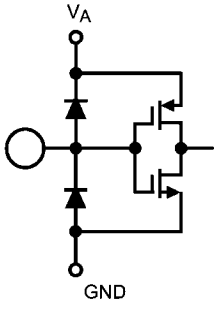
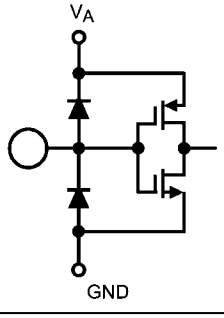
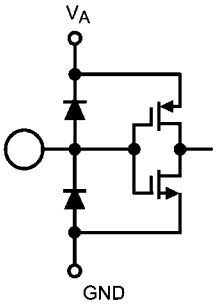
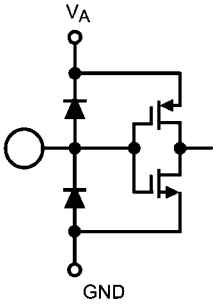
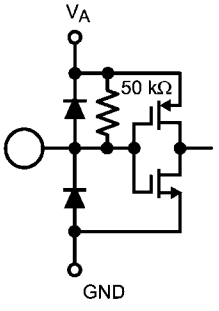
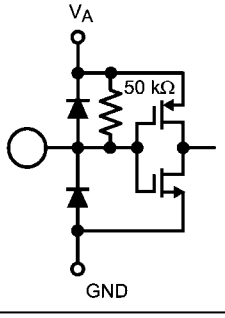
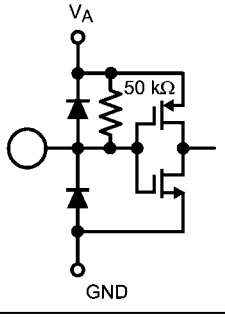
Ball No.	Name	Equivalent Circuit	Description
Y4/W5	RCLK+/-		Reference Clock Input. When the AutoSync feature is active, and the ADC10D1000 is in Slave Mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via Control Register (Addr: E**h**).
Y5/U6 V6/V7	RCOut1+/- RCOut2+/-		Reference Clock Output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in Master or Slave Mode. They are used to drive the RCLK of another ADC10D1000, to enable automatic synchronization for multiple ADCs (AutoSync feature). The impedance of each trace from RCOut1 and RCOut2 to the RCLK of another ADC10D1000 should be 100Ω differential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC Bit (Addr: E**h**, Bit 1) to enable/ disable this feature; default is disabled.

TABLE 2. Control and Status Balls

Ball No.	Name	Equivalent Circuit	Description
V5	DES		Dual Edge Sampling (DES) Mode select. In the Non-Extended Control Mode (Non-ECM), when this input is set to logic-high, the DES Mode of operation is selected, meaning that the VinI input is sampled by both channels in a time-interleaved manner. The VinQ input is ignored. When this input is set to logic-low, the device is in Non-DES Mode, i.e. the I- and Q-channels operate independently. In the Extended Control Mode (ECM), this input is ignored and DES Mode selection is controlled through the Control Register by the DES Bit (Addr: 0**h**, Bit 7); default is Non-DES Mode operation.
V4	CalDly		Calibration Delay select. By setting this input logic-high or logic-low, the user can select the device to wait a longer or shorter amount of time, respectively, before the automatic power-on self-calibration is initiated. This feature is pin-controlled only and is always active during ECM and Non-ECM.

Ball No.	Name	Equivalent Circuit	Description
D6	CAL		Calibration cycle initiate. The user can command the device to execute a self-calibration cycle by holding this input high a minimum of t_{CAL_H} after having held it low a minimum of t_{CAL_L}. If this input is held high at the time of power-on, the automatic power-on calibration cycle is inhibited until this input is cycled low-then-high. This pin is active in both ECM and Non-ECM. In ECM, this pin is logically OR'd with the CAL Bit (Addr: 0**h**, Bit 15) in the Control Register. Therefore, both pin and bit must be set low and then either can be set high to execute an on-command calibration.
B5	CalRun		Calibration Running indication. This output is logic-high while the calibration sequence is executing. This output is logic-low otherwise.
U3 V3	PDI PDQ		Power Down I- and Q-channel. Setting either input to logic-high powers down the respective I- or Q-channel. Setting either input to logic-low brings the respective I- or Q-channel to a operational state after a finite time delay. This pin is active in both ECM and Non-ECM. In ECM, each Pin is logically OR'd with its respective Bit. Therefore, either this pin or the PDI and PDQ Bit in the Control Register can be used to power-down the I- and Q-channel (Addr: 0**h**, Bit 11 and Bit 10), respectively.
A4	TPM		Test Pattern Mode select. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the Test Pattern Mode can only be activated through the Control Register by the TPM Bit (Addr: 0**h**, Bit 12).
A5	NDM		Non-Demuxed Mode select. Setting this input to logic-high causes the digital output bus to be in the 1:1 Non-Demuxed Mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 Demuxed Mode. This feature is pin-controlled only and remains active during ECM and Non-ECM.

Ball No.	Name	Equivalent Circuit	Description
Y3	FSR		Full-Scale input Range select. In Non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I- and Q-channel inputs is set to the lower or higher FSR value, respectively. In the ECM, this input is ignored and the full-scale range of the I- and Q-channel inputs is independently determined by the setting of Addr: 3**h** and Addr: B**h**, respectively. Note that the high (lower) FSR value in Non-ECM corresponds to the mid (min) available selection in ECM; the FSR range in ECM is greater.
W4	DDRPh		DDR Phase select. This input, when logic-low, selects the 0° Data-to-DCLK phase relationship. When logic-high, it selects the 90° Data-to-DCLK phase relationship, i.e. the DCLK transition indicates the middle of the valid data outputs. This pin only has an effect when the chip is in 1:2 Demuxed Mode, i.e. the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the Control Register by the DPS Bit (Addr: 0**h**, Bit 14); the default is 0° Mode.
B3	$\overline{\text{ECE}}$		Extended Control Enable bar. Extended feature control through the SPI interface is enabled when this signal is asserted (logic-low). In this case, most of the direct control pins have no effect. When this signal is de-asserted (logic-high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled via the control pins.
C4	$\overline{\text{SCS}}$		Serial Chip Select bar. In ECM, when this signal is asserted (logic-low), SCLK is used to clock in serial data which is present on SDI and to source serial data on SDO. When this signal is de-asserted (logic-high), SDI is ignored and SDO is in tri-stated.
C5	SCLK		Serial Clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, as long as timing specifications are not violated when the clock is enabled or disabled.

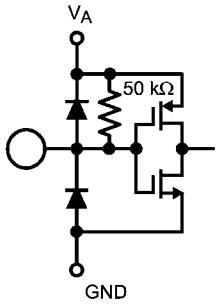
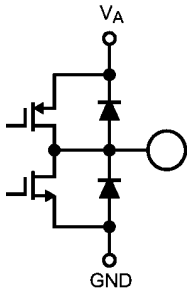
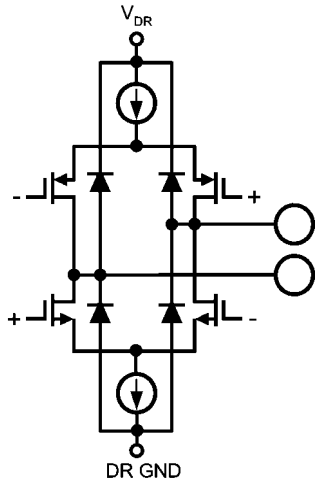
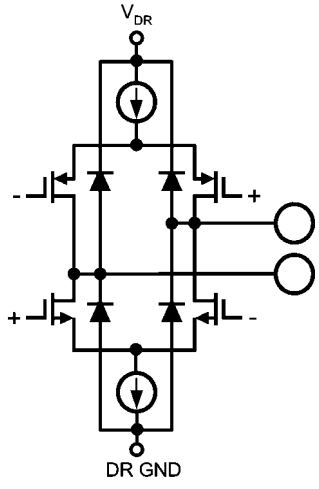
Ball No.	Name	Equivalent Circuit	Description
B4	SDI		Serial Data-In. In ECM, serial data is shifted into the device on this pin while $\overline{SCS}$ signal is asserted (logic-low).
A3	SDO		Serial Data-Out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is tri-stated when $\overline{SCS}$ is de-asserted.
D1, D7, E3, F4, W3, U7	DNC		Do Not Connect. These pins are used for internal purposes and should not be connected, i.e. left floating. Do not ground.
A10, B10, C10, D10, C17, B18, B19, B20, U10, V10, W10, Y10, V17, W18, W19, W20	RSV		Reserved. These pins are used for internal purposes. They may be left unconnected or grounded.

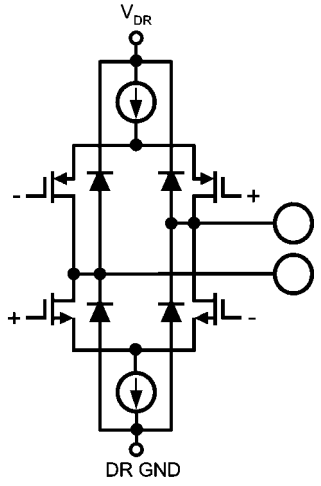
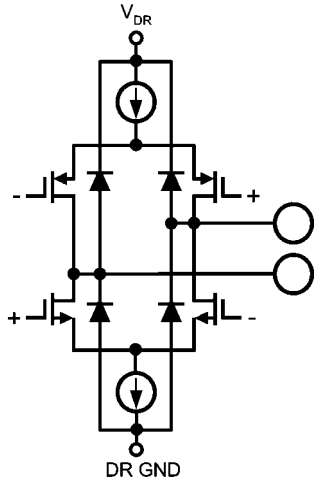
TABLE 3. Power and Ground Balls

Ball No.	Name	Equivalent Circuit	Description
A2, A6, B6, C6, C7, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A		Power Supply for the Analog circuitry. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply.
G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4	V_{TC}		Power Supply for the Track-and-Hold and Clock circuitry.
A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	V_{DR}		Power Supply for the Output Drivers.
A8, B9, C8, V8, W9, Y8	V_E		Power Supply for the Digital Encoder.
J4, K2	VbiasI		Bias Voltage I-channel. This is an externally decoupled bias voltage for the I-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.

Ball No.	Name	Equivalent Circuit	Description
L2, M4	VbiasQ		Bias Voltage Q-channel. This is an externally decoupled bias voltage for the Q-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
A1, A7, B2, B7, D4, D5, E4, K1, L1, T4, U4, U5, W2, W7, Y1, Y7, H8:N13	GND		Ground Return for the Analog circuitry.
F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	GND_{TC}		Ground Return for the Track-and-Hold and Clock circuitry.
A13, A17, A20, D13, D16, E17, F17, F20, M17, M20, U13, U17, V18, Y13, Y17, Y20	GND_{DR}		Ground Return for the Output Drivers.
A9, B8, C9, V9, W8, Y9	GND_{E}		Ground Return for the Digital Encoder.

TABLE 4. High-speed Digital Outputs

Ball No.	Name	Equivalent Circuit	Description
K19/K20 L19/L20	DCLKI+/- DCLKQ+/-		Data Clock Output for the I- and Q-channel data bus. These differential clock outputs are used to latch the output data and should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 Demux Mode or Non-Demux Mode, this signal is at ¼ or ½ the sampling clock rate, respectively. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized.
K17/K18 L17/L18	ORI+/- ORQ+/-		Out-of-Range Output for the I- and Q-channel. This differential output is asserted logic-high while the over- or under-range condition exists, i.e. the differential signal at each respective analog input exceeds the full-scale value. Each OR result refers to the current Data, with which it is clocked out. Each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.

Ball No.	Name	Equivalent Circuit	Description
J18/J19	DI9+/-		I- and Q-channel Digital Data Outputs. In Non-Demux Mode, this LVDS data is transmitted at the sampling clock rate. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, i.e. the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. Each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.
H19/H20	DI8+/-		
H17/H18	DI7+/-		
G19/G20	DI6+/-		
G17/G18	DI5+/-		
F18/F19	DI4+/-		
E19/E20	DI3+/-		
D19/D20	DI2+/-		
D18/E18	DI1+/-		
C19/C20	DI0+/-		
.	.		
M18/M19	DQ9+/-		
N19/N20	DQ8+/-		
N17/N18	DQ7+/-		
P19/P20	DQ6+/-		
P17/P18	DQ5+/-		
R18/R19	DQ4+/-		
T19/T20	DQ3+/-		
U19/U20	DQ2+/-		
U18/T18	DQ1+/-		
V19/V20	DQ0+/-		
A18/A19	DId9+/-		Delayed I- and Q-channel Digital Data Outputs. In Non-Demux Mode, these outputs are tri-stated. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, i.e. the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. Each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.
B17/C16	DId8+/-		
A16/B16	DId7+/-		
B15/C15	DId6+/-		
C14/D14	DId5+/-		
A14/B14	DId4+/-		
B13/C13	DId3+/-		
C12/D12	DId2+/-		
A12/B12	DId1+/-		
B11/C11	DId0+/-		
.	.		
Y18/Y19	DQd9+/-		
W17/V16	DQd8+/-		
Y16/W16	DQd7+/-		
W15/V15	DQd6+/-		
V14/U14	DQd5+/-		
Y14/W14	DQd4+/-		
W13/V13	DQd3+/-		
V12/U12	DQd2+/-		
Y12/W12	DQd1+/-		
W11/V11	DQd0+/-		

9.0 Absolute Maximum Ratings

(Notes 1, 2)

Supply Voltage (V_A, V_{TC}, V_{DR}, V_E)	2.2V
Supply Difference max($V_{A/TC/DR/E}$)- min($V_{A/TC/DR/E}$)	0V to 100 mV
Voltage on Any Input Pin (except V_{IN}+/-)	–0.15V to (V_A + 0.15V)
V_{IN}+/- Voltage Range	-0.15V to 2.2V
Ground Difference max($GND_{TC/DR/E}$) -min($GND_{TC/DR/E}$)	0V to 100 mV
Input Current at Any Pin (Note 3)	±50 mA
Power Dissipation at $T_A \leq 85°C$ (Note 3)	TBD W
ESD Susceptibility (Note 4)	
Human Body Model	2500V
Charged Device Model	750V
Machine Model	250V
Storage Temperature	–65°C to +150°C

10.0 Operating Ratings

(Notes 1, 2)

Ambient Temperature Range	$-40°C \leq T_A \leq +85°C$
Supply Voltage (V_A, V_{TC}, V_E)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	V_{CMO} ±75 mV
V_{IN}+/- Voltage Range (Maintaining Common Mode)	200mV to 2.0V
Ground Difference max($GND_{TC/DR/E}$) -min($GND_{TC/DR/E}$)	0V
CLK+/- Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$

TABLE 5. Package Thermal Resistance

Package	θ_{JA}	θ_{JC}
292-Ball BGA Thermally Enhanced Package	16°C / W	3°C / W

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 5)

11.0 Converter Electrical Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V_E = +1.9V$; I- and Q-channels, AC-coupled, unused channel terminated to AC ground, FSR Pin = High; C_L = 10 pF; Differential, AC coupled Sine Wave Sampling Clock, f_{CLK} = 1 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = Floating; Non-extended Control Mode; Rext = Rtrim = 3300Ω ± 0.1%; Analog Signal Source Impedance = 100Ω Differential; 1:2 Demultiplex Non-DES Mode; Duty Cycle Stabilizer on. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25°C, unless otherwise noted. (Notes 6, 7, 14)

TABLE 6. Static Converter Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
	Resolution with No Missing Codes			**10**	bits
INL	Integral Non-Linearity (Best fit)	1 MHz DC-coupled over-ranged sine wave	±0.7	**±1.4**	LSB (max)
DNL	Differential Non-Linearity	1 MHz DC-coupled over-ranged sine wave	±0.2	**±0.5**	LSB (max)
V_{OFF}	Offset Error		-2		LSB
V_{OFF_ADJ}	Input Offset Adjustment Range	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error	(Note 9)		**±25**	mV (max)
NFSE	Negative Full-Scale Error	(Note 9)		**±25**	mV (max)
	Out-of-Range Output Code	(V_{IN}+) – (V_{IN}–) > + Full Scale		**1023**	
		(V_{IN}+) – (V_{IN}–) < – Full Scale		**0**	

TABLE 7. Dynamic Converter Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
FPBW	Full Power Bandwidth	Non-DES Mode	2.8		GHz
		DES Mode	1.25		GHz
	Gain Flatness	D.C. to 498 MHz	±0.35		dBFS
		D.C. to 1.0 GHz	±0.5		dBFS
CER	Code Error Rate		10^{-18}		Error/Sample
NPR	Noise Power Ratio	$f_{c,notch}$ = 325 MHz, Notch width = 5% (25MHz)	45		dB
1:2 Demux Non-DES Mode					
ENOB	Effective Number of Bits	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	9.1		bits (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	9.0		bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	56.5		dB (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	56		dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	57		dB (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	56.5		dB (min)
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-66		dB (max)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-66		dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-71		dBc
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-71		dBc
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-70		dBc
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-70		dBc
SFDR	Spurious-Free Dynamic Range	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	66		dBc (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	66		dBc (min)
Non-Demux Non-DES Mode					
ENOB	Effective Number of Bits	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	9.1		bits (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	9.0		bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	56.5		dB (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	56		dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	57		dB (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	56.5		dB (min)
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-66		dB (max)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-66		dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-71		dBc
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-71		dBc
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-70		dBc
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-70		dBc
SFDR	Spurious-Free Dynamic Range	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	66		dBc (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	66		dBc (min)

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
DES Mode (Demux and Non-Demux Modes, Q-input only)					
ENOB	Effective Number of Bits	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	8.5		bits (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	8.3		bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	52.8		dB (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	51.4		dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	53.3		dB (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	51.8		dB (min)
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-63		dB (max)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-63		dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-67		dBc
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-69		dBc
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	-65		dBc
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	-64		dBc
SFDR	Spurious-Free Dynamic Range	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS	60.1		dBc (min)
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS	56.6		dBc (min)

TABLE 8. Analog Input/Output and Reference Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Analog Inputs					
V_{IN_FSR}	Analog Differential Input Full Scale Range	**Non-Extended Control Mode**			
		FSR Pin Low	600	**560**	mV_{P-P} (min)
				680	mV_{P-P} (max)
		FSR Pin High	790	**750**	mV_{P-P} (min)
				890	mV_{P-P} (max)
		Extended Control Mode			
		FM(14:0) = 0000**h**	600		mV_{P-P}
		FM(14:0) = 4000**h** (default)	790		mV_{P-P}
		FM(14:0) = 7FFF**h**	980		mV_{P-P}
V_{CMI}	Common Mode Input Voltage	DC-coupled Mode	V_{CMO}	**V_{CMO} – 75mV**	V (min)
				V_{CMO} + 75mV	V (max)
C_{IN}	Analog Input Capacitance, Non-DES Mode (Notes 10, 11)	Differential	0.02		pF
		Each input pin to ground	1.6		pF
	Analog Input Capacitance, DES Mode (Notes 10, 11)	Differential	0.08		pF
		Each input pin to ground	2.2		pF
R_{IN}	Differential Input Resistance		100	**105**	Ω (min)
				95	Ω (max)
Common Mode Output					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±100 µA	1.25	**1.15**	V (min)
				1.3	V (max)
TC_V_{CMO}	Common Mode Output Voltage Temperature Coefficient	I_{CMO} = ±100 µA	TBD		ppm/°C
V_{CMO_LVL}	V_{CMO} input threshold to set DC-coupling Mode		0.63		V
$C_{L\_}V_{CMO}$	Maximum V_{CMO} Load Capacitance			**TBD**	pF

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Bandgap Reference					
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.25	**1.15**	V (min)
				1.35	V (max)
TC_V_{BG}	Bandgap Reference Voltage Temperature Coefficient	I_{BG} = ±100 µA	TBD		ppm/°C
$C_{L\_}V_{BG}$	Maximum Bandgap Reference load Capacitance			**TBD**	pF

TABLE 9. I-channel to Q-channel Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
	Offset Match		2		LSB
	Positive Full-Scale Match	Zero offset selected in Control Register	2		LSB
	Negative Full-Scale Match	Zero offset selected in Control Register	2		LSB
	Phase Matching (I, Q)	f_{IN} = 1.0 GHz	< 1		Degree
X-TALK	Crosstalk from I-channel (Aggressor) to Q-channel (Victim)	Aggressor = 867 MHz F.S. Victim = 100 MHz F.S.	–65		dB
	Crosstalk from Q-channel (Aggressor) to I-channel (Victim)	Aggressor = 867 MHz F.S. Victim = 100 MHz F.S.	–65		dB

TABLE 10. Sampling Clock Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
V_{IN_CLK}	Differential Sampling Clock Input Level	Sine Wave Clock Differential Peak-to-Peak	0.6	**0.4**	V_{P-P} (min)
				2.0	V_{P-P} (max)
		Square Wave Clock Differential Peak-to-Peak	0.6	**0.4**	V_{P-P} (min)
				2.0	V_{P-P} (max)
C_{IN_CLK}	Sampling Clock Input Capacitance (Notes 10, 11)	Differential	TBD		pF
		Each input to ground	TBD		pF
R_{IN_CLK}	Sampling Clock Differential Input Resistance		100		Ω

TABLE 11. Digital Control and Output Pin Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Digital Control Pins (DES, CalDly, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$)					
V_{IH}	Logic High Input Voltage			**0.7 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage			**0.3 x V_A**	V (max)
C_{IN_DIG}	Digital Control Pin Input Capacitance (Notes 11, 13)	Measured from each control pin to GND	1.5		pF

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Digital Output Pins (Data, DCLKI, DCLKQ, ORI, ORQ)					
V_{OD}	LVDS Differential Output Voltage	V_{BG} = Floating, OVS = High	520		mV_{P-P} (min)
					mV_{P-P} (max)
		V_{BG} = Floating, OVS = Low	375		mV_{P-P} (min)
					mV_{P-P} (max)
		V_{BG} = V_A, OVS = High	570		mV_{P-P} (min)
					mV_{P-P} (max)
		V_{BG} = V_A, OVS = Low	400		mV_{P-P} (min)
					mV_{P-P} (max)
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	Output Offset Voltage	V_{BG} = Floating	800		mV
		V_{BG} = V_A	1200		mV
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	V_{BG} = Floating; D+ and D− connected to 0.8V	±4		mA
Z_O	Differential Output Impedance		100		Ω
V_{OH}	Logic High Output Level	CalRun, SDO I_{OH} = −400 µA (Note 12)	1.65	**1.5**	V
V_{OL}	Logic Low Output Level	CalRun, SDO I_{OH} = 400 µA (Note 12)	0.15	**0.3**	V

TABLE 12. Power Supply Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
PSRR1	D.C. Power Supply Rejection Ratio	Change in Full Scale Error with change in V_A from 1.8V to 2.0V	TBD		dB
I_A	Analog Supply Current	**1:2 Demux Mode**			
		PDI = PDQ = Low	900	**980**	mA (max)
		PDI = Low; PDQ = High	515		mA (max)
		PDI = High; PDQ = Low	515		mA (max)
		PDI = PDQ = High	30		mA
		Non-Demux Mode			
		PDI = PDQ = Low	900	**980**	mA (max)
		PDI = Low; PDQ = High	515		mA (max)
		PDI = High; PDQ = Low	515		mA (max)
		PDI = PDQ = High	30		mA
I_{TC}	Track-and-Hold and Clock Supply Current	**1:2 Demux Mode**			
		PDI = PDQ = Low	350	**390**	mA (max)
		PDI = Low; PDQ = High	220		mA (max)
		PDI = High; PDQ = Low	220		mA (max)
		PDI = PDQ = High	1		mA
		Non-Demux Mode			
		PDI = PDQ = Low	350	**390**	mA (max)
		PDI = Low; PDQ = High	220		mA (max)
		PDI = High; PDQ = Low	220		mA (max)
		PDI = PDQ = High	1		mA

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
I_{DR}	Output Driver Supply Current	**1:2 Demux Mode**			
		PDI = PDQ = Low	210	**260**	mA (max)
		PDI = Low; PDQ = High	110		mA (max)
		PDI = High; PDQ = Low	110		mA (max)
		PDI = PDQ = High	10		µA
		Non-Demux Mode			
		PDI = PDQ = Low	130	**200**	mA (max)
		PDI = Low; PDQ = High	80		mA (max)
		PDI = High; PDQ = Low	80		mA (max)
		PDI = PDQ = High	10		µA
I_E	Digital Encoder Supply Current	**1:2 Demux Mode**			
		PDI = PDQ = Low	60	**95**	mA (max)
		PDI = Low; PDQ = High	40		mA (max)
		PDI = High; PDQ = Low	40		mA (max)
		PDI = PDQ = High	0		mA
		Non-Demux Mode			
		PDI = PDQ = Low	67	**95**	mA (max)
		PDI = Low; PDQ = High	40		mA (max)
		PDI = High; PDQ = Low	40		mA (max)
		PDI = PDQ = High	0		mA
P_C	Power Consumption	**1:2 Demux Mode**			
		PDI = PDQ = Low	2.90	**3.25**	W (max)
		PDI = Low; PDQ = High	1.68		W (max)
		PDI = High; PDQ = Low	1.68		W (max)
		PDI = PDQ = High	58.9		mW
		Non-Demux Mode			
		PDI = PDQ = Low	2.77	**3.1**	W (max)
		PDI = Low; PDQ = High	1.61		W (max)
		PDI = High; PDQ = Low	1.61		W (max)
		PDI = PDQ = High	58.9		mW

TABLE 13. AC Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Sampling Clock (CLK)					
$f_{CLK\ (max)}$	Maximum Sampling Clock Frequency			**1.0**	GHz (min)
$f_{CLK\ (min)}$	Minimum Sampling Clock Frequency	Non-DES Mode	200		MHz
		DES Mode	500		MHz
	Sampling Clock Duty Cycle	$f_{CLK(min)} \le f_{CLK} \le f_{CLK(max)}$ (Note 12)	50	**20**	% (min)
				80	% (max)
t_{CL}	Sampling Clock Low Time	(Note 11)	TBD	**TBD**	ps (min)
t_{CH}	Sampling Clock High Time	(Note 11)	TBD	**TBD**	ps (min)
Data Clock (DCLKI, DCLKQ)					
	DCLK Duty Cycle	(Note 11)	50	**45**	% (min)
				55	% (max)
t_{SR}	Setup Time DCLK_RST±	(Note 12)	TBD		ps
t_{HR}	Hold Time DCLK_RST±	(Note 12)	TBD		ps

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
t_{PWR}	Pulse Width DCLK_RST±	(Note 11)		**TBD**	Sampling Clock Cycles (min)
t_{SYNC_DLY}	DCLK Synchronization Delay	90° Mode (Note 11)		**4**	Sampling Clock Cycles
		0° Mode (Note 11)		**5**	
t_{LHT}	Differential Low-to-High Transition Time	10%-to-90%, C_L = 2.5 pF	TBD		ps
t_{HLT}	Differential High-to-Low Transition Time	10%-to-90%, C_L = 2.5 pF	TBD		ps
t_{SU}	Data-to-DCLK Setup Time	90° Mode (Note 11)	TBD		ps
t_H	DCLK-to-Data Hold Time	90° Mode (Note 11)	TBD		ps
t_{OSK}	DCLK-to-Data Output Skew	50% of DCLK transition to 50% of Data transition (Note 11)	TBD		ps (max)
Data Input-to-Output					
t_{AD}	Aperture Delay	Sampling CLK+ Rise to Acquisition of Data	TBD		ns
t_{AJ}	Aperture Jitter		TBD		ps (rms)
t_{OD}	Sampling Clock-to Data Output Delay (in addition to Latency)	50% of Sampling Clock transition to 50% of Data transition	TBD		ns
t_{LAT}	Latency in 1:2 Demux Non-DES Mode (Note 11)	DI, DQ Outputs		**34**	Sampling Clock Cycles
		DId, DQd Outputs		**35**	
	Latency in 1:4 Demux DES Mode (Note 11)	DI Outputs		**34**	
		DQ Outputs		**34.5**	
		DId Outputs		**35**	
		DQd Outputs		**35.5**	
	Latency in Non-Demux Non-DES Mode (Note 11)	DI Outputs		**34**	
		DQ Outputs		**34**	
	Latency in Non-Demux DES Mode (Note 11)	DI Outputs		**34**	
		DQ Outputs		**34.5**	
t_{ORR}	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to accurate conversion	1		Sampling Clock Cycle
t_{WU}	Wake-Up Time (PDI/PDQ low to Rated Accuracy Conversion)	Non-DES Mode (Note 11)	500		ns
		DES Mode (Note 11)	1		µs
Serial Port Interface					
f_{SCLK}	Serial Clock Frequency	(Note 11)	15		MHz
	Serial Clock Low Time			**30**	ns (min)
	Serial Clock High Time			**30**	ns (min)
t_{SSU}	Serial Data-to-Serial Clock Rising Setup Time	(Note 11)	2.5		ns (min)
t_{SH}	Serial Data-to-Serial Clock Rising Hold Time	(Note 11)	1		ns (min)
t_{SCS}	$\overline{SCS}$-to-Serial Clock Rising Setup Time		2.5		ns
t_{HCS}	$\overline{SCS}$-to-Serial Clock Falling Hold Time		1.5		ns
t_{BSU}	Bus turn-around time		TBD		ns

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Calibration					
t_{CAL}	Calibration Cycle Time	Non-ECM	2.4×10^7		Sampling Clock Cycles
		ECM CSS = 0**b**	2.3×10^7		
		ECM; CSS = 1**b**			
		CMS(1:0) = 00**b**	0.8×10^7		Sampling Clock Cycles
		CMS(1:0) = 01**b**	1.5×10^7		
		CMS(1:0) = 10**b** (ECM default)	2.4×10^7		
t_{CAL_L}	CAL Pin Low Time	(Note 11)		**1280**	Clock Cycles (min)
t_{CAL_H}	CAL Pin High Time	(Note 11)		**1280**	Clock Cycles (min)
t_{CalDly}	Calibration delay determined by CalDly Pin	CalDly = Low		**TBD**	Clock Cycles (max)
		CalDly = High		**TBD**	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

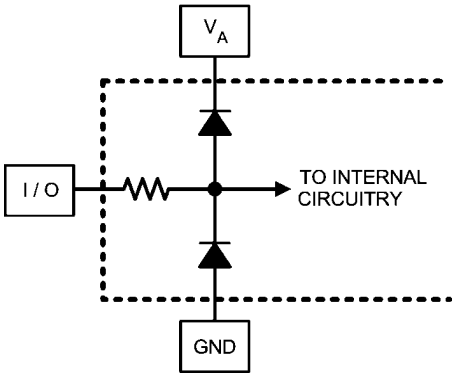
Note 2: All voltages are measured with respect to GND = GND_{TC} = GND_{DR} = GND_E = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply limits, i.e. less than GND or greater than V_A, the current at that pin should be limited to 50 mA. In addition, over-voltage at a pin must adhere to the maximum voltage limits. Simultaneous over-voltage at multiple pins requires adherence to the maximum package power dissipation limits.

Note 4: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω. Charged device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Note 5: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 6: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



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Note 7: To guarantee accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.

Note 8: Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See *Figure 4*. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Note 10: The analog and clock input capacitances are die capacitances only. Additional package capacitances of TBD pF differential and TBD pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 11: This parameter is guaranteed by design and is not tested in production.

Note 12: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 13: The digital control pin capacitances are die capacitances only. Additional package capacitance of TBD pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 14: The maximum clock frequency for Non-Demux Mode is 1 GHz.

12.0 Specification Definitions

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample-to-sample. Aperture jitter can be effectively considered as noise at the input.

CODE ERROR RATE (CER) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A CER of 10^{-18} corresponds to a statistical error in one word about every 31.7 years.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. It is measured at sample rate = 1 GSPS with a 1MHz input sine wave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this many (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops to 3 dB below its low frequency value for a full-scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors. The Positive Gain Error is the Offset Error minus the Positive Full-Scale Error. The Negative Gain Error is the Negative Full-Scale Error minus the Offset Error. The Gain Error is the Negative Full-Scale Error minus the Positive Full-Scale Error; it is also equal to the Positive Gain Error plus the Negative Gain Error.

INTEGRAL NON-LINEARITY (INL) is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dB.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N$$

where V_{FS} is the differential full-scale amplitude V_{IN_FSR} as set by the FSR input and "N" is the ADC resolution in bits, which is 10 for the ADC10D1000.

LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL OUTPUT VOLTAGE (V_{ID} and V_{OD}) is two times the absolute value of the difference between the V_D+ and V_D - signals; each measured with respect to Ground.

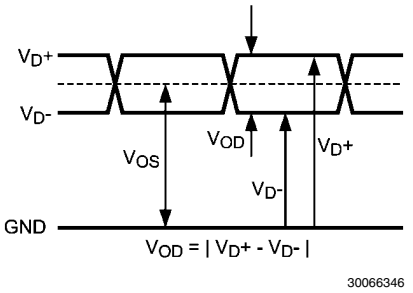


FIGURE 3. LVDS Output Signal Levels

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage with respect to ground; i.e., $[(V_D+) + (V_D-)]/2$. See *Figure 3*.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $-V_{IN}/2$ with the FSR pin low. For the ADC10D1000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

NOISE POWER RATIO (NPR) is the ratio of the sum of the power inside the notched bins to the sum of the power in an equal number of bins outside the notch, expressed in dB.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 511.5.

OUTPUT DELAY (t_{OD}) is the time delay (in addition to Latency) after the rising edge of CLK+ before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. The data lags the conversion by the Latency plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}/2$. For the ADC10D1000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) PSRR1 (D.C. PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the fundamental for a single-tone to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the fundamental for a single-tone to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding DC.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

13.0 Transfer Characteristic

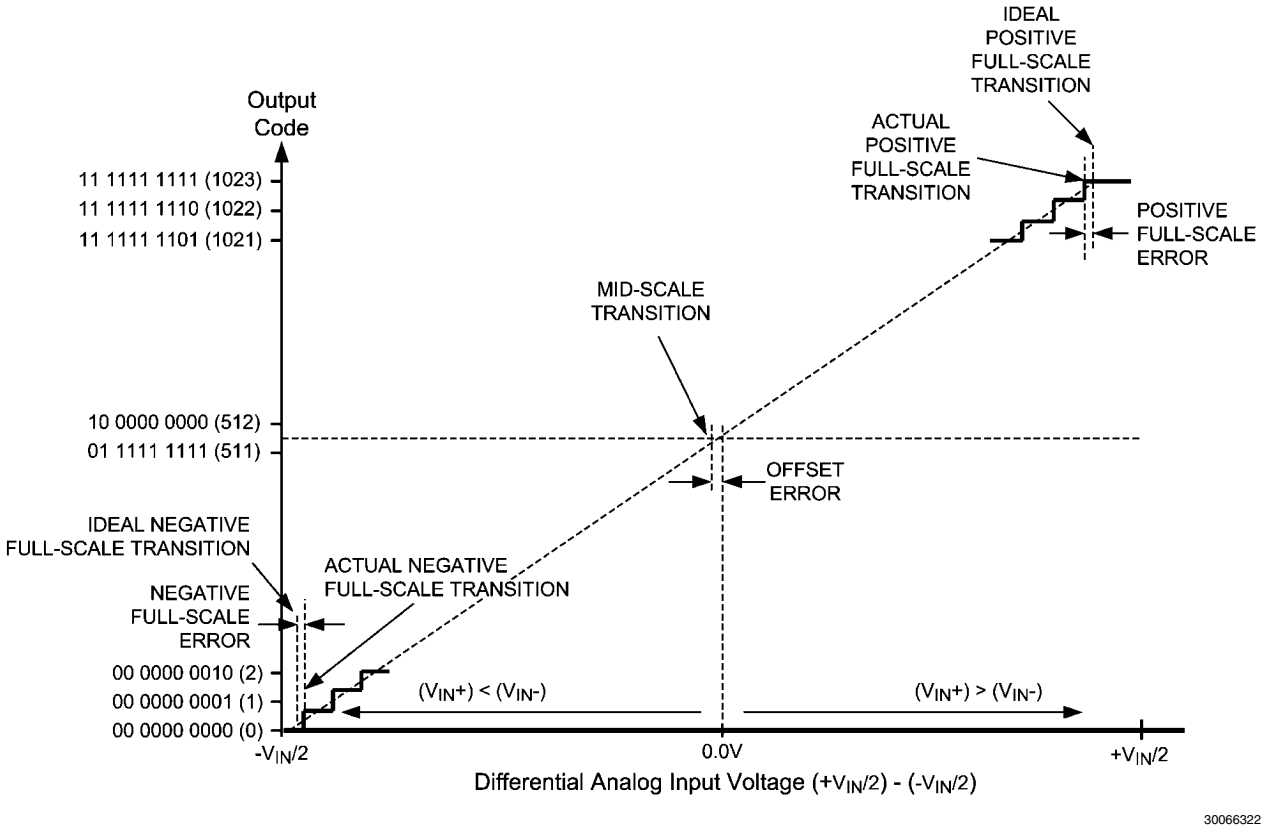


FIGURE 4. Input / Output Transfer Characteristic

14.0 Timing Diagrams

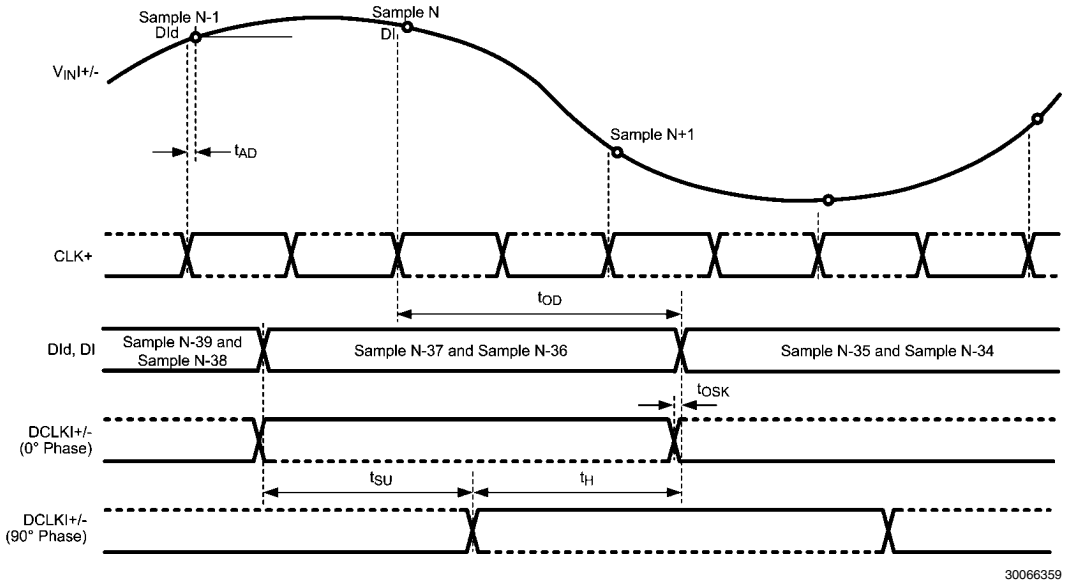


FIGURE 5. Clocking in 1:2 Demux Non-DES Mode*

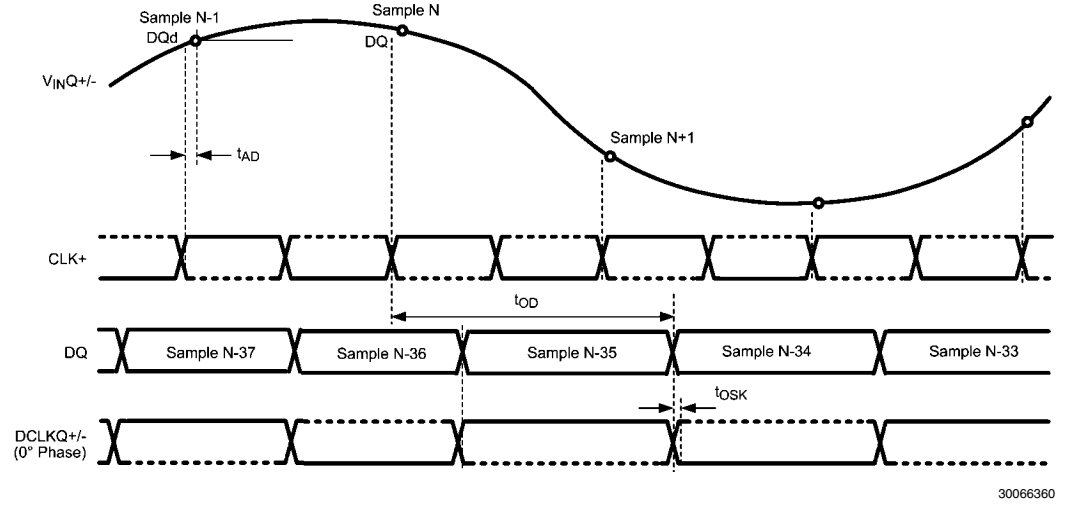


FIGURE 6. Clocking in Non-Demux Non-DES Mode*

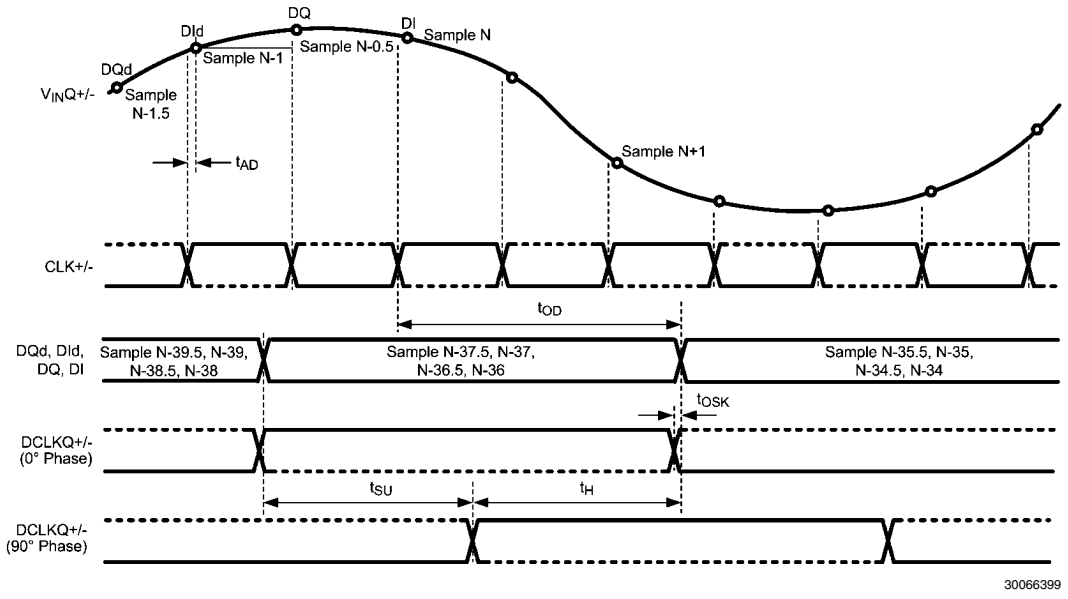


FIGURE 7. Clocking in 1:4 Demux DES Mode*

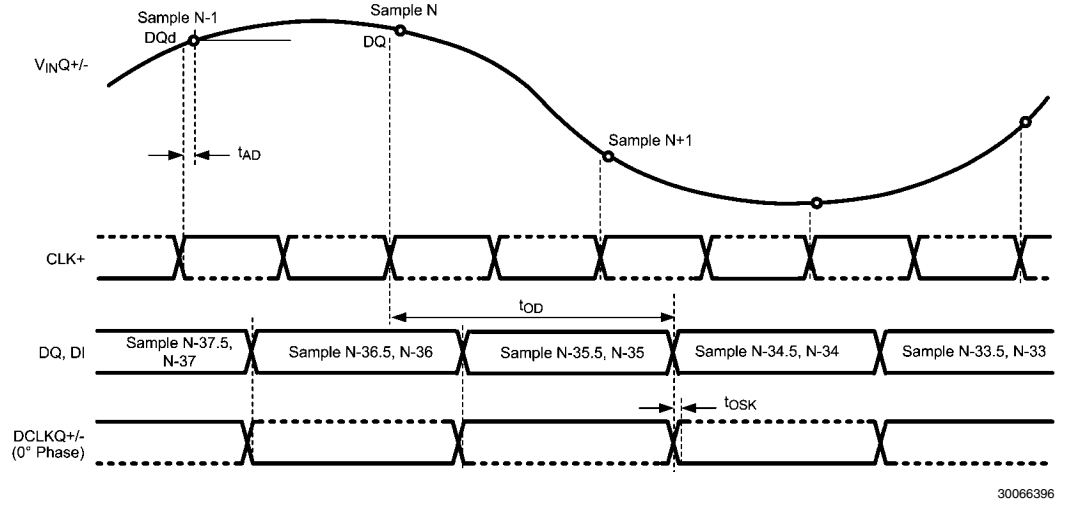


FIGURE 8. Clocking in Non-Demux Mode DES Mode*

* The timing for these figures is shown for the one input only (I or Q). However, both I- and Q-inputs may be used. For this case, the I-channel functions precisely the same as the Q-channel, with VinI, DCLKI, DId and DI instead of VinQ, DCLKQ, DQd and DQ. Both I- and Q-channel use the same CLK.

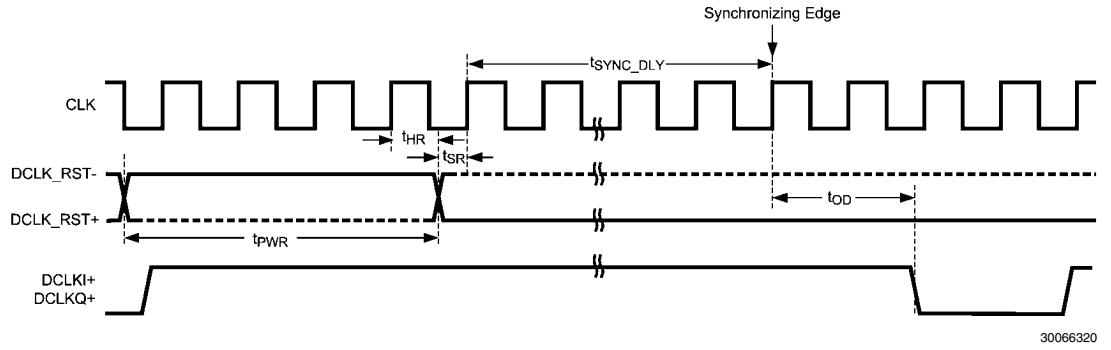


FIGURE 9. Data Clock Reset Timing (Demux Mode)

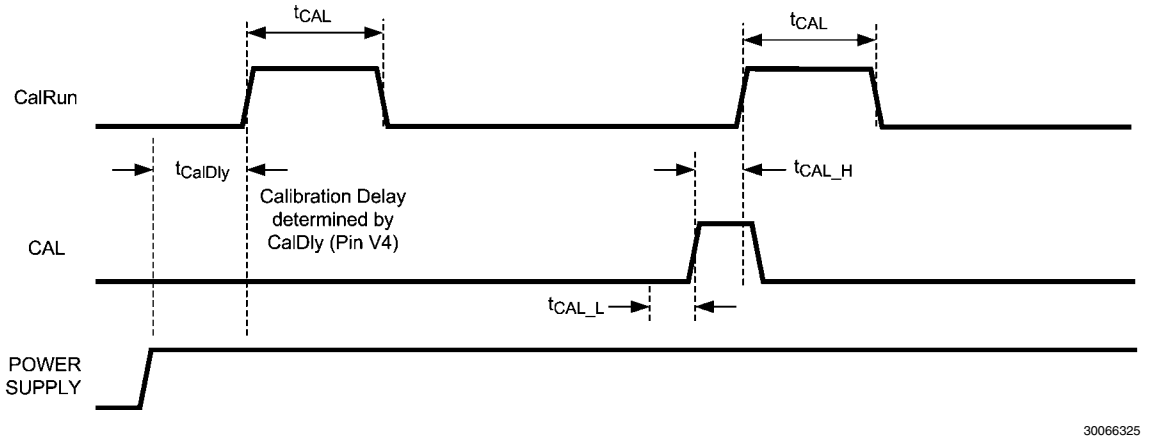


FIGURE 10. Power-on and On-Command Calibration Timing

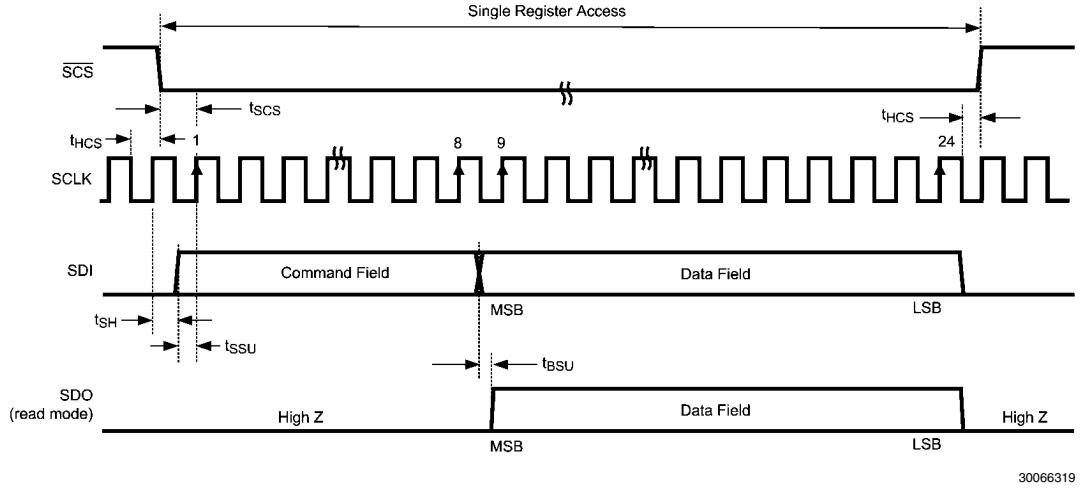


FIGURE 11. Serial Interface Timing

15.0 Functional Description

The ADC10D1000 is a versatile A/D converter with an innovative architecture which permits very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section. This section covers an overview, a description of control modes (Extended Control Mode and Non-Extended Control Mode), and features.

15.1 Overview

The ADC10D1000 uses a calibrated folding and interpolating architecture that achieves a high 9.1 Effective Number of Bits (ENOB). The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to correcting other non-idealities, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal (which is within the converter's input voltage range) is digitized to ten bits at speeds of 200 MSPS to 1.3 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the I- or Q-input will cause the Out-of-Range I-channel or Q-channel output (ORI or ORQ), respectively, to output a logic-high signal.

In ECM, an expanded feature set is available via the Serial Interface. The ADC10D1000 builds upon previous architectures, introducing a new AutoSync feature for multi-chip synchronization and increasing to 15-bit for gain and 12-bit plus sign for offset the independent programmable adjustment for each channel.

Each channel has a selectable output demultiplexer which feeds two LVDS buses. If the 1:2 Demux Mode is selected, the output data rate is reduced to half the input sample rate on each bus. When Non-Demux Mode is selected, the output data rate on each channel is at the same rate as the input sample clock and only one 10-bit bus per channel is active.

15.2 Control Modes

The ADC10D1000 may be operated in one of two control modes: Non-extended Control Mode (Non-ECM) or Extended Control Mode (ECM). In the simpler Non-ECM (also sometimes referred to as Pin Control Mode), the user affects available configuration and control of the device through the control pins. The ECM provides additional configuration and control options through a serial interface and a set of 16 registers, most of which are available to the customer.

15.2.1 Non-Extended Control Mode

In Non-extended Control Mode (Non-ECM), the Serial Interface is not active and all available functions are controlled via various pin settings. Non-ECM is selected by setting the $\overline{ECE}$ Pin to logic-high. Note that, for the control pins, "logic-high" and "logic-low" refer to V_A and GND, respectively. Nine dedicated control pins provide a wide range of control for the ADC10D1000 and facilitate its operation. These control pins provide DES Mode selection, Demux Mode selection, DDR Phase selection, execute Calibration, Calibration Delay setting, Power Down I-channel, Power Down Q-channel, Test Pattern Mode selection, and Full-Scale Input Range selection. In addition to this, two dual-purpose control pins provide for AC/DC-coupled Mode selection and LVDS output common-mode voltage selection. See *Table 14* for a summary.

TABLE 14. Non-ECM Pin Summary

Pin Name	Logic-Low	Logic-High	Floating
Dedicated Control Pins			
DES	Non-DES Mode	DES Mode	Not valid
NDM	Demux Mode	Non-Demux Mode	Not valid
DDRPh	0° Mode	90° Mode	Not valid
CAL	See *Section 15.2.1.4 Calibration Pin (CAL)*		Not valid
CalDly	Shorter delay	Longer delay	Not valid
PDI	I-channel active	Power Down I-channel	Power Down I-channel
PDQ	Q-channel active	Power Down Q-channel	Power Down Q-channel
TPM	Non-Test Pattern Mode	Test Pattern Mode	Not valid
FSR	Lower FS input Range	Higher FS input Range	Not valid
Dual-purpose Control Pins			
V_{CMO}	AC-coupled operation	Not allowed	DC-coupled operation
V_{BG}	Not allowed	Higher LVDS common-mode voltage	Lower LVDS common-mode voltage

15.2.1.1 Dual Edge Sampling Pin (DES)

The Dual Edge Sampling (DES) Pin selects whether the ADC10D1000 is in DES Mode (logic-high) or Non-DES Mode (logic-low). DES Mode means that a single input is sampled by both I- and Q-channels in a time-interleaved manner and the other input is deactivated. One of the ADCs samples the input signal on the rising sampling clock edge (duty cycle corrected); the other ADC samples the input signal on the falling sampling clock edge (duty cycle corrected). In Non-ECM, only the I-input may be used for DES Mode. In ECM, the Q-input may be selected via the DEQ Bit (Addr: 0**h**, Bit: 6).

To use this feature in ECM, use the DES bit in the Configuration Register (Addr: 0**h**; Bit: 7). See *Section 15.3.1.4 DES/Non-DES Mode* for more information.

15.2.1.2 Non-Demultiplexed Mode Pin (NDM)

The Non-Demultiplexed Mode (NDM) Pin selects whether the ADC10D1000 is in Demux Mode (logic-low) or Non-Demux Mode (logic-high). In Non-Demux Mode, the data from the input is produced at the sampled rate at a single 10-bit output bus. In Demux Mode, the data from the input is produced at half the sampled rate at twice the number of output buses. For Non-DES Mode, each I- or Q-channel will produce its data on one or two buses for Non-Demux or Demux Mode, respectively. For DES Mode, the Q-channel will produce its data on two or four buses for Non-Demux or Demux Mode, respectively.

This feature is pin-controlled only and remains active during both Non-ECM and ECM. See *Section 15.3.2.5 Demux/Non-demux Mode* for more information.

15.2.1.3 Dual Data Rate Phase Pin (DDRPh)

The Dual Data Rate Phase (DDRPh) Pin selects whether the ADC10D1000 is in 0° Mode (logic-low) or 90° Mode (logic-high). The Data is always produced in DDR Mode on the ADC10D1000. The Data may transition either with the DCLK transition (0° Mode) or halfway between DCLK transitions (90° Mode). The DDRPh Pin selects 0° Mode or 90° Mode for both the I-channel: DI- and DId-to-DCLKI phase relationship and for the Q-channel: DQ- and DQd-to-DCLKQ phase relationship.

To use this feature in ECM, use the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14). See *Section 15.3.2.1 DDR Clock Phase* for more information.

15.2.1.4 Calibration Pin (CAL)

The Calibration (CAL) Pin may be used to execute an on-command calibration or to disable the power-on calibration. The effect of calibration is to maximize the dynamic performance. To initiate an on-command calibration via the CAL pin, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles. Holding the CAL pin high upon power-on will prevent execution of the power-on calibration. In ECM, this pin remains active and is logically OR'd with the CAL bit.

To use this feature in ECM, use the CAL bit in the Configuration Register (Addr: 0**h**; Bit: 15). See *Section 15.3.3 Calibration Feature* for more information.

15.2.1.5 Calibration Delay Pin (CalDly)

The Calibration Delay (CalDly) Pin selects whether a shorter or longer delay time is present, after the application of power, until the start of the power-on calibration. The actual delay time is specified as t_{CalDly} and may be found in *Table 13*. This feature is pin-controlled only and remains active in ECM. It is recommended to select the desired delay time prior to power-on and not dynamically alter this selection.

See *Section 15.3.3 Calibration Feature* for more information.

15.2.1.6 Power Down I-channel Pin (PDI)

The Power Down I-channel (PDI) Pin selects whether the I-channel is powered down (logic-high) or active (logic-low). The digital data output pins, DI and DId, (both positive and negative) are put into a high impedance state when the I-channel is powered down. Upon return to the active state, the pipeline will contain meaningless information and must be flushed. The supply currents (typicals and limits) are available for the I-channel powered down or active and may be found in *Table 12*. The device should be recalibrated following a power-cycle of PDI (or PDQ).

This pin remains active in ECM. In ECM, either this pin or the PDI bit (Addr: 0**h**; Bit: 11) in the Control Register may be used to power-down the I-channel. See *Section 15.3.4 Power Down* for more information.

15.2.1.7 Power Down Q-channel Pin (PDQ)

The Power Down Q-channel (PDQ) Pin selects whether the Q-channel is powered down (logic-high) or active (logic-low). This pin functions similarly to the PDI pin, except that it applies to the Q-channel. The PDI and PDQ pins function independently of each other to control whether each I- or Q-channel is powered down or active.

This pin remains active in ECM. In ECM, either this pin or the PDQ bit (Addr: 0**h**; Bit: 10) in the Control Register may be used to power-down the Q-channel. See *Section 15.3.4 Power Down* for more information.

15.2.1.8 Test Pattern Mode Pin (TPM)

The Test Pattern Mode (TPM) Pin selects whether the output of the ADC10D1000 is a test pattern (logic-high) or the converted analog input (logic-low). The ADC10D1000 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In TPM, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. See *Section 15.3.2.6 Test Pattern Mode* for more information.

15.2.1.9 Full-Scale Input Range Pin (FSR)

The Full-Scale Input Range (FSR) Pin selects whether the full-scale input range for both the I- and Q-channel is higher (logic-high) or lower (logic-low). The input full-scale range is specified as V_{IN_FSR} in *Table 8*. In Non-ECM, the full-scale input range for each I- and Q-channel may not be set independently, but it is possible to do so in ECM. The device must be calibrated following a change in FSR to obtain optimal performance.

To use this feature in ECM, use the Configuration Registers (Addr: 3**h** and B**h**). See *Section 15.3.1 Input Control and Adjust* for more information.

15.2.1.10 AC/DC-Coupled Mode Pin (V_{CMO})

The V_{CMO} Pin serves a dual purpose. When functioning as an output, it provides the optimal common-mode voltage for the DC-coupled analog inputs. When functioning as an input, it selects whether the device is AC-coupled (logic-low) or DC-coupled (floating). This pin is always active, in both ECM and Non-ECM.

15.2.1.11 LVDS Output Common-mode Pin (V_{BG})

The V_{BG} Pin serves a dual purpose. When functioning as an output, it provides the bandgap reference. When functioning as an input, it selects whether the LVDS output common-mode voltage is higher (logic-high) or lower (floating). The LVDS output common-mode voltage is specified as V_{OS} and may be found in *Table 11*. This pin is always active, in both ECM and Non-ECM.

15.2.2 Extended Control Mode

In Extended Control Mode (ECM), most functions are controlled via the Serial Interface. In addition to this, several of the control pins remain active. See *Table 17* for details. ECM is selected by setting the $\overline{ECE}$ Pin to logic-low. If the $\overline{ECE}$ Pin is set to logic-high (Non-ECM), then the registers are reset to their default values. So, a simple way to reset the registers is by toggling the $\overline{ECE}$ pin. Four pins on the ADC10D1000 control the Serial Interface: $\overline{SCS}$, SCLK, SDI and SDO. This section covers the Serial Interface. The Register Definitions are located at the end of the datasheet so that they are easy to locate, see *Section 17.0 Register Definitions*.

15.2.2.1 The Serial Interface

The ADC10D1000 offers a Serial Interface that allows access to the sixteen control registers within the device. The Serial Interface is a generic 4-wire (optionally 3-wire) synchronous interface that is compatible with SPI type interfaces that are used on many micro-controllers and DSP controllers. Each serial interface access cycle is exactly 24 bits long. A register-read or register-write can be accomplished in one cycle. The signals are defined in such a way that the user can opt to simply join SDI and SDO signals in his system to accomplish a single, bidirectional SDI/O signal. A summary of the pins for this interface may be found in *Table 15*. See *Figure 11* for the timing diagram and *Table 13* for timing specification details. Control register contents are retained when the device is put into power-down mode.

TABLE 15. Serial Interface Pins

Pin	Name
C4	$\overline{SCS}$ (Serial Chip Select bar)
C5	SCLK (Serial Clock)
B4	SDI (Serial Data In)
A3	SDO (Serial Data Out)

$\overline{SCS}$: Each assertion (logic-low) of this signal starts a new register access, i.e. the SDI command field must be ready on the following SCLK rising edge. The user is required to de-assert this signal after the 24th clock. If the $\overline{SCS}$ is de-asserted before the 24th clock, no data read/write will occur. For a read operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, the SDO output will hold the D0 bit until $\overline{SCS}$ is de-asserted. For a write operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, data write will occur normally through the SDI input upon the 24th clock. Setup and hold times, t_{SCS} and t_{HCS}, with respect to the SCLK must be observed. $\overline{SCS}$ must be toggled in between register access cycles.

SCLK: This signal is used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. The user may disable the clock and hold it at logic-low. There is no minimum frequency requirement for SCLK; see f_{SCLK} in *Table 13* for more details.

SDI: Each register access requires a specific 24-bit pattern at this input, consisting of a command field and a data field. When in read mode, the data field is high impedance in case the bidirectional SDI/O option is used. Setup and hold times, t_{SH} and t_{SSU}, with respect to the SCLK must be observed.

SDO: This output is normally tri-stated and is driven only when $\overline{SCS}$ is asserted, the first 8 bits of command data have been received and it is a READ operation. The data is shifted out, MSB first, starting with the 8th clock's falling edge. At the end of the access, when $\overline{SCS}$ is de-asserted, this output is tri-stated once again. If an invalid address is accessed, the data sourced will consist of all zeroes. If it is a read operation, there will be a bus turnaround time, t_{BSU}, from when the last bit of the command field was read in until the first bit of the data field is written out.

Table 16 shows the Serial Interface bit definitions.

TABLE 16. Command and Data Field Definitions

Bit No.	Name	Comments
1	Read/Write (R/W)	1**b** indicates a read operation 0**b** indicates a write operation
2-3	Reserved	Bits must be set to 10**b**
4-7	A<3:0>	16 registers may be addressed. The order is MSB first
8	X	This is a "don't care" bit
9-24	D<15:0>	Data written to or read from addressed register

The serial data protocol is shown for a read and write operation in *Figure 12* and *Figure 13*, respectively.

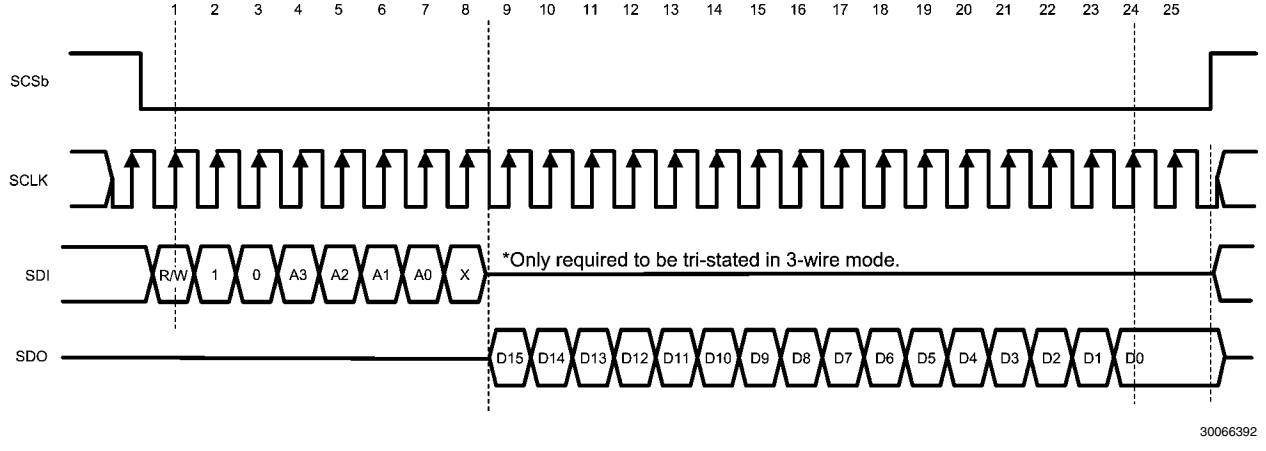


FIGURE 12. Serial Data Protocol - Read Operation

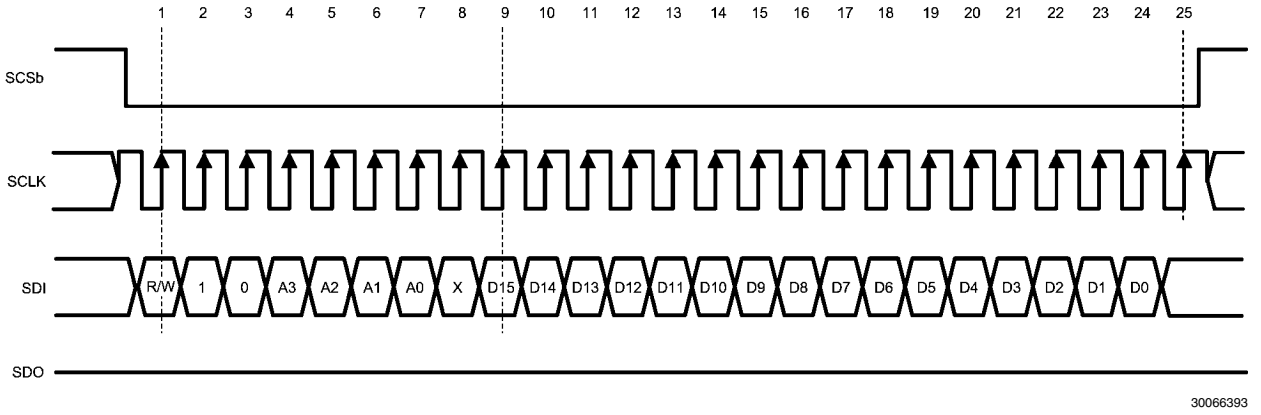


FIGURE 13. Serial Data Protocol - Write Operation

15.3 Features

The ADC10D1000 offers many features to make the device convenient to use in a wide variety of applications. *Table 17* is a summary of the features available, as well as details for the control mode chosen.

TABLE 17. Features and Modes

Feature	Non-ECM	Control Pin Active in ECM	ECM	Default ECM State
Input Control and Adjust				
AC/DC-coupled Mode Selection	Selected via V_{CMO} (Pin C2)	Yes	Not available	N/A
Input Full-scale Range Adjust	Selected via FSR (Pin Y3)	No	Selected via the Config Reg (Addr: 3**h** and B**h**)	Mid FSR value
Input Offset Adjust Setting	Not available	N/A	Selected via the Config Reg (Addr: 2**h** and A**h**)	Offset = 0 mV
LC Filter on Clock	Not available	N/A	Selected via the Config Reg (Addr: D**h**)	LC Filter off
DES/Non-DES Mode Selection	Selected via DES (Pin V5)	No	Selected via the DES Bit (Addr: 0**h**; Bit: 7)	Non-DES Mode
Sampling Clock Phase Adjust	Not available	N/A	Selected via the Config Reg (Addr: C**h** and D**h**)	t_{AD} adjust disabled
V_{CMO} Adjust	Not available	N/A	Selected via the Config Reg (Addr: 1**h**)	Default V_{CMO}
Output Control and Adjust				
DDR Clock Phase Selection	Selected via DDRPh (Pin W4)	No	Selected via the DPS Bit (Addr: 0**h**; Bit: 14)	0° Mode
LVDS Differential Output Voltage Amplitude Selection	Higher amplitude only	N/A	Selected via the OVS Bit (Addr: 0**h**; Bit: 13)	Higher amplitude
LVDS Common-Mode Output Voltage Amplitude Selection	Selected via V_{BG} (Pin B1)	Yes	Not available	N/A
Output Formatting Selection	Offset Binary only	N/A	Selected via the 2SC Bit (Addr: 0**h**; Bit: 4)	Offset Binary
Test Pattern Mode at Output	Selected via TPM (Pin A4)	No	Selected via the TPM Bit (Addr: 0**h**; Bit: 12)	TPM disabled
Demux/Non-Demux Mode Selection	Selected via NDM (Pin A5)	Yes	Not available	N/A
AutoSync	Not available	N/A	Selected via the Config Reg (Addr: E**h**)	Master Mode, RCOut1/2 disabled
DCLK Reset	Not available	N/A	Selected via the Config Reg (Addr: E**h**)	DCLK Reset disabled
Calibration				
On-command Calibration	Selected via CAL (Pin D6)	Yes	Selected via the CAL Bit (Addr: 0**h**; Bit: 15)	N/A (CAL = 0)
Power-on Calibration Delay Selection	Selected via CalDly (Pin V4)	Yes	Not available	N/A
Calibration Adjust	Not available	N/A	Selected via the Config Reg (Addr: 4**h**)	t_{CAL}
Power-Down				
Power down I-channel	Selected via PDI (Pin U3)	Yes	Selected via the PDI Bit (Addr: 0**h**; Bit: 11)	I-channel operational
Power down Q-channel	Selected via PDQ (Pin V3)	Yes	Selected via the PDQ Bit (Addr: 0**h**; Bit: 10)	Q-channel operational

15.3.1 Input Control and Adjust

There are several features and configurations for the input of the ADC10D1000 so that it may be used in many different applications. This section covers AC/DC-coupled Mode, input full-scale range adjust, input offset adjust, DES/Non-DES Mode, sampling clock phase adjust, an LC filter on the sampling clock, and V_{CMO} Adjust.

15.3.1.1 AC/DC-coupled Mode

The analog inputs may be AC or DC-coupled. See *Section 15.2.1.10 AC/DC-Coupled Mode Pin (V_{CMO})* for information on how to select the desired mode and *Section 16.1.5 DC-coupled Input Signals* and *Section 16.1.4 AC-coupled Input Signals* for applications information.

15.3.1.2 Input Full-Scale Range Adjust

The input full-scale range for the ADC10D1000 may be adjusted via Non-ECM or ECM. In Non-ECM, a control pin selects a higher or lower value; see *Section 15.2.1.9 Full-Scale Input Range Pin (FSR)* . In ECM, the input full-scale range may be adjusted with 15-bits of precision. See V_{IN_FSR} in *Table 8* for electrical specification details. Note that the higher and lower full-scale input range settings in Non-ECM correspond to the mid and min full-scale input range settings in ECM. It is necessary to execute an on-command calibration following a change of the input full-scale range. See *Section 17.0 Register Definitions* for information about the registers.

15.3.1.3 Input Offset Adjust

The input offset adjust for the ADC10D1000 may be adjusted with 12-bits of precision plus sign via ECM. See *Section 17.0 Register Definitions* for information about the registers.

15.3.1.4 DES/Non-DES Mode

The ADC10D1000 can operate in Dual-Edge Sampling (DES) or Non-DES Mode. The DES Mode allows for one of the ADC10D1000's inputs to be sampled by both channels' ADCs. One ADC samples the input on the rising edge of the sampling clock and the other ADC samples the same input on the falling edge of the sampling clock. A single input is thus sampled twice per clock cycle, resulting in an overall sample rate of twice the sampling clock frequency, e.g. 2.0 GSPS with a 1.0 GHz sampling clock. See *Section 15.2.1.1 Dual Edge Sampling Pin (DES)* for information on how to select the desired mode. Since DES Mode uses both I- and Q-channels to process the input signal, both channels must be powered up for the DES Mode to function properly.

In Non-ECM, only the I-input may be used for the DES Mode input. In ECM, either the I- or Q-input may be selected by first using the DES bit (Addr: 0**h**, Bit 7) to select the DES Mode. The DEQ Bit (Addr: 0**h**, Bit: 6) is used to select the Q-input, but the I-input is used by default.

In this mode, the outputs must be carefully interleaved in order to reconstruct the sampled signal. If the device is programmed into the 1:4 Demux DES Mode, the data is effectively demultiplexed by 1:4. If the sampling clock is 1.0 GHz, the effective sampling rate is doubled to 2.0 GSPS and each of the 4 output buses has an output rate of 500 MSPS. All data is available in parallel. To properly reconstruct the sampled waveform, the four bytes of parallel data that are output with each DCLK must be correctly interleaved. The sampling order is as follows, from the earliest to the latest: DQd, DId, DQ, DI. See *Figure 7*. If the device is programmed into the Non-Demux DES Mode, two bytes of parallel data are output with each edge of the DCLK in the following sampling order, from the earliest to the latest: DQ, DI. See *Figure 8*.

The performance of the ADC10D1000 in DES Mode depends on how well the two channels are interleaved, i.e. that the clock samples either channel with precisely a 50% duty-cycle, each channel has the same offset (nominally code 511/512), and each channel has the same full-scale range. The ADC10D1000 includes an automatic clock phase background adjustment in DES Mode to automatically and continuously adjust the clock phase of the I- and Q-channels, which also removes the need to adjust the clock phase setting manually. A difference exists in the typical offset between the I- and Q-channels, which can be removed via the offset adjust feature in ECM, to optimize DES Mode performance. If possible, it is recommended to use the Q-input for better DES Mode performance with no offset adjustment required. To adjust the I- or Q-channel offset, measure a histogram of the digital data and adjust the offset via the Control Register until the histogram is centered at code 511/512. Similarly, the full-scale range of each channel may be adjusted for optimal performance.

15.3.1.5 Sampling Clock Phase Adjust

The sampling clock (CLK) phase may be delayed internally to the ADC up to 825 ps in ECM. This feature is intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used, or to simplify complex system functions such as beam steering for phase array antennas.

Additional delay in the clock path also creates additional jitter, so a clock jitter-cleaner is made available when using the sampling clock phase adjust, see *Section 15.3.1.6 LC Filter on Sampling Clock*. Nevertheless, because the sampling clock phase adjust delays all clocks, including the DCLKs and output data, the user is strongly advised to use the minimal amount of adjustment and verify the net benefit of this feature in his system before relying on it.

15.3.1.6 LC Filter on Sampling Clock

A LC bandpass filter is available on the ADC10D1000 sampling clock to clean jitter on the incoming clock. This feature is only available when the CLK phase adjust feature is also used. This feature was designed to minimize the dynamic performance degradation resulting from additional clock jitter as much as possible. It is available in ECM via the LCF (LC Filter) bits in the Control Register (Addr: D**h**, Bits 7:0).

If the clock phase adjust feature is enabled, the sampling clock passes through additional gate delay, which adds jitter to the clock signal. The LC filter helps to remove this additional jitter, so it is only available when the clock phase adjust feature is also enabled. To enable both features, use SA (Addr: D**h**, Bit 8). The LCF bits are thermometer encoded and may be used to set a filter center frequency ranging from 0.8 GHz to 1.5 GHz; see *Table 18*.

TABLE 18. LC Filter Code vs. f_c

LCF(7:0)	LCF(7:0)	f_c (GHz)
0	0000 0000**b**	1.5
1	0000 0001**b**	1.4
2	0000 0011**b**	1.3
3	0000 0111**b**	1.2
4	0000 1111**b**	1.1
5	0001 1111**b**	1.0
6	0011 1111**b**	0.92
7	0111 1111**b**	0.85
8	1111 1111**b**	0.8

The LC filter is a second-order bandpass filter, which has the following simulated bandwidth for a center frequency at 1GHz, see *Table 19*.

TABLE 19. LC Filter Bandwidth vs. Level

Bandwidth at [dB]	-3	-6	-9	-12
Bandwidth [MHz]	±135	±235	±360	±525

15.3.1.7 V_{CMO} Adjust

The V_{CMO} of the ADC10D1000 is generated as a buffered version of the internal bandgap reference; see V_{CMO} in *Table 8*. This pin provides an output voltage which is the optimal common-mode voltage for the input signal and should be used to set the common-mode voltage of the driving buffer. However, in order to accomodate larger signals at the analog inputs, the V_{CMO} may be adjust to a lower value. From its typical default value, the V_{CMO} may be lowered by approximately 200 mV via the Control Register 1**h**. See *Section 17.0 Register Definitions* for more information. Adjusting the V_{CMO} away from its optimal value will also degrade the dynamic performance. The performance of the device, when using a V_{CMO} other than the default value, is not guaranteed.

15.3.2 Output Control and Adjust

There are several features and configurations for the output of the ADC10D1000 so that it may be used in many different applications. This section covers DDR clock phase, LVDS output differential and common-mode voltage, output formatting, Demux/Non-demux Mode, and Test Pattern Mode.

15.3.2.1 DDR Clock Phase

The ADC10D1000 output data is always delivered in Double Data Rate (DDR). With DDR, the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK; see *Figure 14*. The DCLK-to-Data phase relationship may be either 0° or 90°. For 0° Mode, the Data transitions on each edge of the DCLK. Any offset from this timing is t_{OSK}; see *Table 13* for details. For 90° Mode, the DCLK transitions in the middle of each Data cell. Setup and hold times for this transition, t_{SU} and t_H, may also be found in *Table 13*. The DCLK-to-Data phase relationship may be selected via the DDRPh Pin in Non-ECM (see *Section 15.2.1.3 Dual Data Rate Phase Pin (DDRPh)*) or the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14) in ECM.

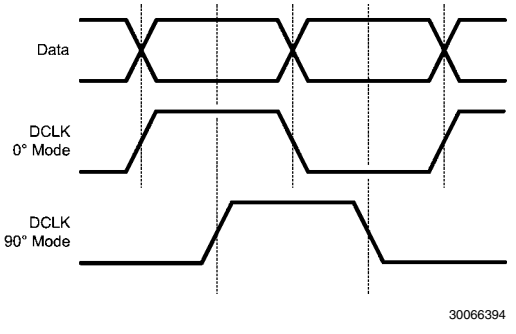


FIGURE 14. DDR DCLK-to-Data Phase Relationship

15.3.2.2 LVDS Output Differential Voltage

The ADC10D1000 is available with a selectable higher or lower LVDS output differential voltage. This parameter is V_{OD} and may be found in *Table 11*. The desired voltage may be selected via the OVS Bit (Addr: 0**h**, Bit 13); see *Section 17.0 Register Definitions* for more information.

15.3.2.3 LVDS Output Common-Mode Voltage

The ADC10D1000 is available with a selectable higher or lower LVDS output common-mode voltage. This parameter is V_{OS} and may be found in *Table 11*. See *Section 15.2.1.11 LVDS Output Common-mode Pin (V_{BG})* for information on how to select the desired voltage.

15.3.2.4 Output Formatting

The formatting at the digital data outputs may be either offset binary or two's complement. The default formatting is offset binary, but two's complement may be selected via the 2SC Bit (Addr: 0**h**, Bit 4); see *Section 17.0 Register Definitions* for more information.

15.3.2.5 Demux/Non-demux Mode

The ADC10D1000 may be in one of two demultiplex modes: Demux Mode or Non-Demux Mode (also sometimes referred to as 1:1 Demux Mode). In Non-Demux Mode, the data from the input is simply output at the sampling rate at which it was sampled on one 10-bit bus. In Demux Mode, the data from the input is output at half the sampling rate, on twice the number of buses. See *Figure 1*. Demux/Non-Demux Mode may only be selected by the NDM pin; see *Section 15.2.1.2 Non-Demultiplexed Mode Pin (NDM)*. In Non-DES Mode, the output data from each channel may be demultiplexed by a factor of 1:2 (1:2 Demux Non-DES Mode) or not demultiplexed (Non-Demux Non-DES Mode). In DES Mode, the output data from both channels interleaved may be demultiplexed (1:4 Demux DES Mode) or not demultiplexed (Non-Demux DES Mode).

15.3.2.6 Test Pattern Mode

The ADC10D1000 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In Test Pattern Mode, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. The test pattern output is the same in DES Mode or Non-DES Mode. Each port is given a unique 10-bit word, alternating between 1's and 0's. When the part is programmed into the Demux Mode, the test pattern's order is described in *Table 20*. If the I- or Q-channel is powered down, the test pattern will not be output for that channel.

TABLE 20. Test Pattern by Output Port in Demux Mode

Time	Qd	Id	Q	I	ORQ	ORI	Comments
T0	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	Pattern Sequence **n**
T1	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T2	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T3	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T4	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T5	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	Pattern Sequence **n+1**
T6	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T7	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T8	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T9	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T10	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	Pattern Sequence **n+2**
T11	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T12	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T13	...	...	...	...	...	...	

When the part is programmed into the Non-Demux Mode, the test pattern's order is described in *Table 21*.

TABLE 21. Test Pattern by Output Port in Non-Demux Mode

Time	I	Q	ORI	ORQ	Comments
T0	001**h**	000**h**	0**b**	0**b**	Pattern Sequence **n**
T1	001**h**	000**h**	0**b**	0**b**	
T2	3FE**h**	3FF**h**	1**b**	1**b**	
T3	3FE**h**	3FF**h**	1**b**	1**b**	
T4	001**h**	000**h**	0**b**	0**b**	
T5	3FE**h**	3FF**h**	1**b**	1**b**	
T6	001**h**	000**h**	0**b**	0**b**	
T7	3FE**h**	3FF**h**	1**b**	1**b**	
T8	3FE**h**	3FF**h**	1**b**	1**b**	
T9	3FE**h**	3FF**h**	1**b**	1**b**	
T10	001**h**	000**h**	0**b**	0**b**	Pattern Sequence **n+1**
T11	001**h**	000**h**	0**b**	0**b**	
T12	3FE**h**	3FF**h**	1**b**	1**b**	
T13	3FE**h**	3FF**h**	1**b**	1**b**	
T14	...	...	...	...	

15.3.3 Calibration Feature

The ADC10D1000 calibration must be run to achieve specified performance. The calibration procedure is exactly the same regardless of how it was initiated or when it is run. Calibration trims the analog input differential termination resistors, the CLK input resistor, and sets internal bias currents which affect the linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, resulting in maximizing the dynamic performance, as measured by: SNR, THD, SINAD (SNDR) and ENOB.

15.3.3.1 Calibration Control Pins and Bits

Table 22 is a summary of the pins and bits used for calibration. See *Section 8.0 Ball Descriptions and Equivalent Circuits* for complete pin information and *Figure 10* for the timing diagram.

TABLE 22. Calibration Pins

Pin/Bit	Name	Function
D6 (Addr: 0**h**; Bit 15)	CAL (Calibration)	Initiate calibration
V4	CalDly (Calibration Delay)	Select calibration delay
Addr: 4**h**	Calibration Adjust	Adjust calibration sequence and mode
B5	CalRun (Calibration Running)	Indicates while calibration is running
C1/D2	Rtrim+/- (Input termination trim resistor)	External resistor used to calibrate analog and CLK inputs
C3/D3	Rext+/- (External Reference resistor)	External resistor used to calibrate internal linearity

15.3.3.2 How to Execute a Calibration

Calibration may be initiated by holding the CAL pin low for at least t_{CAL_L} clock cycles, and then holding it high for at least another t_{CAL_H} clock cycles, as defined in *Table 13*. The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. The time taken by the calibration procedure is specified as t_{CAL}. The CAL Pin is active in both ECM and Non-ECM. However, in ECM, the CAL Pin is logically OR'd with the CAL Bit, so both the pin and bit are required to be set low before executing another calibration via either pin or bit.

15.3.3.3 Power-on Calibration

For standard operation, power-on calibration begins after a time delay following the application of power, as determined by the setting of the CalDly Pin and measured by t_{CalDly} (see *Table 13*). This delay allows the power supply to come up and stabilize before the power-on calibration takes place. The best setting (short or long) of the CalDly Pin depends upon the settling time of the power supply.

It is strongly recommended to set CalDly Pin (to either logic-high or logic-low) before powering the device on since this pin affects the power-on calibration timing. This may be accomplished by an external pull-up or pull-down resistor. If the CalDly Pin is toggled while the device is powered-on, it can execute a calibration even though the CAL Pin/Bit remains logic-low.

The power-on calibration will be not be performed if the CAL pin is logic-high at power-on. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC10D1000 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired.

If it is necessary to toggle the CalDly Pin during the system power up sequence, then the CAL Pin/Bit must be set to logic-high during the toggling and afterwards for 10^9 Sampling Clock cycles. This will prevent the power-on calibration, so an on-command calibration must be executed or the performance will be impaired.

15.3.3.4 On-command Calibration

In addition to the power-on calibration, it is recommended to execute an on-command calibration whenever the settings or conditions to the device are altered significantly, in order to obtain optimal parametric performance. Some examples include: changing the FSR via either ECM or Non-ECM, power-cycling either channel, and switching into or out of DES Mode. For best performance, it is also recommended that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, relative to the specific system performance requirements.

Due to the nature of the calibration feature, it is recommended to avoid unnecessary activities on the device while the calibration is taking place. For example, do not read or write to the Serial Interface or use the DCLK Reset feature while calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Also, it is recommended to not apply a strong narrow-band signal to the analog inputs during calibration because this may impair the accuracy of the calibration; broad spectrum noise is acceptable.

15.3.3.5 Calibration Adjust

The calibration event itself may be adjusted, for sequence and mode. This feature can be used if a shorter calibration time

than the default is required; see t_{CAL} in *Table 13*. However, the performance of the device, when using a shorter calibration time than the default setting, is not guaranteed.

The calibration sequence may be adjusted via CSS (Addr: 4**h**, Bit 14). The default setting of CSS = 1**b** executes both R_{IN} and R_{IN_CLK} Calibration (using Rtrim) and internal linearity Calibration (using Rext). Executing a calibration with CSS = 0**b** executes only the internal linearity Calibration. The first time that Calibration is executed, it must be with CSS = 1**b** to trim $R_{IN}$and R_{IN_CLK}. However, once the device is at its operating temperature and R_{IN} has been trimmed at least one time, it will not drift significantly. To save time in subsequent calibrations, trimming R_{IN} and R_{IN_CLK} may be skipped, i.e. by setting CSS = 0**b**.

The mode may be changed, to save calibration execution time for the internal linearity Calibration. See t_{CAL} in *Table 13*. Adjusting CMS(1:0) will select three different pre-defined calibration times. A larger amount of time will calibrate each channel more closely to the ideal values, but choosing shorter times will not significantly impact the performance. The fourth setting CMS(1:0) = 11**b** is not available.

15.3.3.6 Calibration and Power-Down

If PDI and PDQ are simultaenously asserted during a calibration cycle, the ADC10D1000 will immediately power down. The calibration cycle will continue when either or both channels are powered back up, but the calibration will be compromised due to the incomplete settling of bias currents directly after power up. Therefore, a new calibration should be executed upon powering the ADC10D1000 back up. In general, the ADC10D1000 should be recalibrated when either or both channels are powered back up, or after one channel is powered down. For best results, this should be done after the device has stabilized to its operating temperature.

15.3.4 Power Down

On the ADC10D1000, the I- and Q-channels may be powered down individually. This may be accomplished via the control pins, PDI and PDQ, or via ECM. In ECM, the PDI and PDQ pins are logically OR'd with the Control Register setting. See *Section 15.2.1.6 Power Down I-channel Pin (PDI)* and *Section 15.2.1.7 Power Down Q-channel Pin (PDQ)* for more information.

16.0 Applications Information

16.1 The Analog Inputs

The ADC10D1000 will continuously convert any signal which is present at the analog inputs, as long as a CLK signal is also provided to the device. This section covers important aspects related to the analog inputs including: acquiring the input, the reference voltage and FSR, out-of-range indication, AC/DC-coupled signals, and single-ended input signals.

16.1.1 Acquiring the Input

Data is acquired at the rising edge of CLK+ in Non-DES Mode and both the falling and rising edges of CLK+ in DES Mode. The digital equivalent of that data is available at the digital outputs a constant number of sampling clock cycles later for the DI, DQ, DId and DQd output buses, a.k.a. Latency, depending on the demultiplex mode which is selected. See t_{LAT} in *Table 13*. In addition to the Latency, there is a constant output delay, t_{OD}, before the data is available at the outputs. See t_{OD} in *Table 13* and the Timing Diagrams.

The output latency versus Demux/Non-Demux Mode is shown in *Table 23* and *Table 24*, respectively. For DES Mode, note that the I- and Q-channel inputs are available in ECM, but only the I-channel input is available in Non-ECM.

TABLE 23. Output Latency in Demux Mode

Data	Non-DES Mode	DES Mode	
		Q-input*	I-input
DI	I-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with rise of CLK, 34 cycles earlier	I-input sampled with rise of CLK, 34 cycles earlier
DQ	Q-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with fall of CLK, 34.5 cycles earlier	I-input sampled with fall of CLK, 34.5 cycles earlier
DId	I-input sampled with rise of CLK, 35 cycles earlier	Q-input sampled with rise of CLK, 35 cycles earlier	I-input sampled with rise of CLK, 35 cycles earlier
DQd	Q-input sampled with rise of CLK, 35 cycles earlier	Q-input sampled with fall of CLK, 35.5 cycles earlier	I-input sampled with fall of CLK, 35.5 cycles earlier

*Available in ECM only.

TABLE 24. Output Latency in Non-Demux Mode

Data	Non-DES Mode	DES Mode	
		Q-input*	I-input
DI	I-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with rise of CLK, 34 cycles earlier	I-input sampled with rise of CLK, 34 cycles earlier
DQ	Q-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with rise of CLK, 34.5 cycles earlier	I-input sampled with rise of CLK, 34.5 cycles earlier
DId	No output; high impedance.		
DQd	No output; high impedance.		

*Available in ECM only.

16.1.2 FSR and the Reference Voltage

The full-scale analog differential input range (V_{IN_FSR}) of the ADC10D1000 is derived from an internal 1.254V bandgap reference. In Non-ECM, this full-scale range has two settings controlled by the FSR Pin; see *Section 15.2.1.9 Full-Scale Input Range Pin (FSR)*. The FSR Pin operates on both I- and Q-channels. In ECM, the full-scale range may be independently set for each channel via Addr:3**h** and B**h** with 15 bits of precision; see *Section 17.0 Register Definitions*. The best SNR is obtained with a higher full-scale input range, but better distortion and SFDR are obtained with a lower full-scale input range. It is not possible to use an external analog reference voltage to modify the full-scale range, and this adjustment should only be done digitally, as described.

A buffered version of the internal 1.254V bandgap reference voltage is made available at the V_{BG} Pin for the user. The V_{BG} pin can drive a load of up to 80 pF and source or sink up to ±100 µA. It should be buffered if more current than this is required. This pin remains as a constant reference voltage regardless of what full-scale range is selected and may be used for a system reference. V_{BG} is a dual-purpose pin and it may also be used to select a higher LVDS output common-mode voltage; see *Section 15.2.1.11 LVDS Output Common-mode Pin (V_{BG})*.

16.1.3 Out-Of-Range Indication

Differential input signals are digitized to 10 bits, based on the full-scale range. Signal excursions beyond the full-scale range, i.e. greater than $+V_{IN\_FSR}/2$ or less than $-V_{IN\_FSR}/2$, will be clipped at the output. An input signal which is above the FSR will result in all 1's at the output and an input signal which is below the FSR will result in all 0's at the output. When the conversion result is clipped for the I-channel input, the Out-of-Range I-channel (ORI) output is activated such that ORI+ goes high and ORI- goes low while the signal is out of range. This output is active as long as accurate data on either or both of the buses would be outside the range of 000**h** to 3FF**h**. The Q-channel has a separate ORQ which functions similarly.

16.1.4 AC-coupled Input Signals

The ADC10D1000 analog inputs require a precise common-mode voltage. This voltage is generated on-chip when AC-coupling Mode is selected. See *Section 15.2.1.10 AC/DC-Coupled Mode Pin (V_{CMO})* for more information about how to select AC-coupled Mode.

In AC-coupled Mode, the analog inputs must of course be AC-coupled. For an ADC10D1000 used in a typical application, this may be accomplished by on-board capacitors, as shown in . For the ADC10D1000RB, the SMA inputs on the Reference Board are directly connected to the analog inputs on the ADC10D1000, so this may be accomplished by DC blocks (included with the hardware kit).

When the AC-coupled Mode is selected, an analog input channel that is not used (e.g. in DES Mode) should be connected to AC ground, e.g. through capacitors to ground . Do not connect an unused analog input directly to ground.

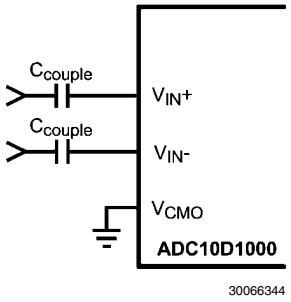


FIGURE 15. AC-coupled Differential Input

The analog inputs for the ADC10D1000 are internally buffered, which simplifies the task of driving these inputs and the RC pole which is generally used at sampling ADC inputs is not required. If the user desires to place an amplifier circuit before the ADC, care should be taken to choose an amplifier with adequate noise and distortion performance, and adequate gain at the frequencies used for the application.

16.1.5 DC-coupled Input Signals

In DC-coupled Mode, the ADC10D1000 differential inputs must have the correct common-mode voltage. This voltage is provided by the device itself at the V_{CMO} output pin. It is recommended to use this voltage because the V_{CMO} output potential will change with temperature and the common-mode voltage of the driving device should track this change. Full-scale distortion performance falls off as the input common mode voltage deviates from V_{CMO}. Therefore, it is recommended to keep the input common-mode voltage within TBD mV of V_{CMO}. Performance in AC- and DC-coupled Mode are similar, provided that the input common mode voltage at both analog inputs remains within TBD mV of V_{CMO}.

16.1.6 Single-Ended Input Signals

The analog inputs of the ADC10D1000 are not designed to accept single-ended signals. The best way to handle single-ended signals is to first convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-transformer, as shown in *Figure 16*.

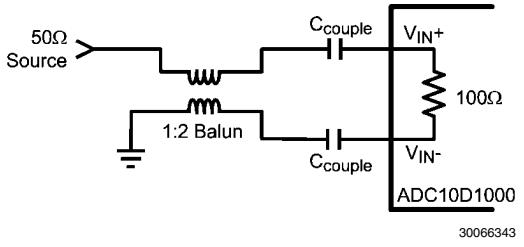


FIGURE 16. Single-Ended to Differential Conversion Using a Balun

When selecting a balun, it is important to understand the input architecture of the ADC. The impedance of the analog source should be matched to the ADC10D1000's on-chip 100Ω differential input termination resistor. The range of this termination resistor is specified as R_{IN} in *Table 8*.

16.1.7 Input Signal Layout

More information TBD.

16.2 The Clock Inputs

The ADC10D1000 has a differential clock input, CLK+ and CLK-, which must be driven with an AC-coupled, differential clock signal. This provides the level shifting to the clock to be driven with LVDS, PECL, LVPECL, or CML levels. The clock inputs are internally terminated to 100Ω differential and self-biased. This section covers coupling, frequency range, level, duty-cycle, jitter, and layout considerations.

16.2.1 CLK Coupling

The clock inputs of the ADC10D1000 must be capacitively coupled to the clock pins as indicated in *Figure 17*.

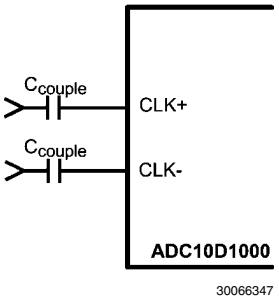


FIGURE 17. Differential Input Clock Connection

The choice of capacitor value will depend on the clock frequency, capacitor component characteristics and other system economic factors. For example, on the ADC10D1000RB, the capacitors have the value C_{couple} = 4.7 nF which yields a highpass cutoff frequency, f_c = 677.2 kHz.

16.2.2 CLK Frequency

Although the ADC10D1000 is tested and its performance is guaranteed with a differential 1.0 GHz sampling clock, it will typically function well over the input clock frequency range; see f_{CLK}(min) and f_{CLK}(max) in *Table 13*. Operation up to f_{CLK}(max) is possible if the maximum ambient temperatures indicated are not exceeded. Operating at sample rates above f_{CLK}(max) for the maximum ambient temperature may result in reduced device reliability and product lifetime. This is due to the fact that higher sample rates results in higher power consumption and die temperatures. If f_{CLK} < 300 MHz, enable LFS in the Control Register (Addr: 0**h**, Bit 8).

16.2.3 CLK Level

The input clock amplitude is specified as V_{IN_CLK} in *Table 10*. Input clock amplitudes above the max V_{IN_CLK} may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 511/512 when both input pins are at the same potential. Insufficient input clock levels will result in poor dynamic performance. Both of these results may be avoided by keeping the clock input amplitude within the specified limits of V_{IN_CLK}.

16.2.4 CLK Duty Cycle

The duty cycle of the input clock signal can affect the performance of any A/D converter. The ADC10D1000 features a duty cycle clock correction circuit which can maintain performance over the 20%-to-80% specified clock duty-cycle range. This feature is enabled by default and provides improved ADC clocking, especially in the Dual-Edge Sampling (DES) Mode.

16.2.5 CLK Jitter

High speed, high performance ADCs such as the ADC10D1000 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)}/ V_{FSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{FSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

$t_{J(MAX)}$ is the square root of the sum of the squares (RSS) sum of the jitter from all sources, including: the ADC input clock, system, input signals and the ADC itself. Since the effective jitter added by the ADC is beyond user control, it is recommended to keep the sum of all other externally added jitter to a minimum.

16.2.6 CLK Layout

The ADC10D1000 clock input is internally terminated with a trimmed 100Ω resistor. The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100Ω) characteristic impedance.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Otherwise, other signals can introduce jitter into the input clock signal. Also, the clock signal can introduce noise into the analog path if it is not properly isolated.

16.3 The LVDS Outputs

The Data, ORI, ORQ, DCLKI and DCLKQ outputs are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips; but they are not IEEE or ANSI communications standards compliant due to the low +1.9V supply used on this chip. These outputs should be terminated with a 100Ω differential resistor placed as closely to the receiver as possible. This section covers common-mode and differential voltage, and data rate.

16.3.1 Common-mode and Differential Voltage

The LVDS outputs have selectable common-mode and differential voltage, V_{OS} and V_{OD}; see *Table 11*. See *Section 15.3.2 Output Control and Adjust* for more information.

Selecting the higher V_{OS} will also increase V_{OD} slightly. The differential voltage, V_{OD}, may be selected for the higher or lower value. For short LVDS lines and low noise systems, satisfactory performance may be realized with the lower V_{OD}. This will also result in lower power consumption. If the LVDS lines are long and/or the system in which the ADC10D1000 is used is noisy, it may be necessary to select the higher V_{OD}.

16.3.2 Output Data Rate

The data is produced at the output at the same rate as it is sampled at the input. The minimum recommended input clock rate for this device is $f_{CLK(MIN)}$; see *Table 13*. However, it is possible to operate the device in 1:2 Demux Mode and capture data from just one 10-bit bus, e.g. just DI (or DId) although both DI and DId are fully operational. This will decimate the data by two and effectively halve the data rate.

16.4 Synchronizing Multiple ADC10D1000s in a System

The ADC10D1000 has two features to assist the user with synchronizing multiple ADCs in a system; AutoSync and DCLK Reset. The AutoSync feature is new and designates one ADC10D1000 as the Master ADC and other ADC10D1000s in the system as Slave ADCs. The DCLK Reset feature performs the same function as the AutoSync feature, but is the first generation solution to synchronizing multiple ADCs in a system; it is disabled by default. For the application in which there are multiple Master and Slave ADC10D1000s in a system, AutoSync may be used to synchronize the Slave ADC10D1000(s) to each respective Master ADC10D1000 and the DCLK Reset may be used to synchronize the Master ADC10D1000s with each other.

16.4.1 AutoSync Feature

AutoSync is a new feature which continuously synchronizes the outputs of multiple ADC10D1000s in a system. It may be used to synchronize the DCLK and data outputs of one or more Slave ADC10D1000s to one Master ADC10D1000. Several advantages of this feature include: no special synchronization pulse required, any upset in synchronization is recovered upon the next DCLK cycle, and the Master/Slave ADC10D1000s may be arranged as a binary tree so that any upset will quickly propagate out of the system.

More information TBD.

16.4.2 DCLK Reset Feature

The DCLK reset feature is available via ECM, but it is disabled by default. DCLKI and DCLKQ are always synchronized, by design, and do not require a pulse from DCLK_RST to become synchronized.

The DCLK_RST signal must observe certain timing requirements, which are shown in *Figure 9* of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{PWR}, t_{RS} and t_{RH} and may be found in *Table 13*.

The DCLK_RST signal can be asserted asynchronously to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state (logic-high) in Demux Mode; in Non-Demux Mode, the DCLK continues to function normally. Depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted, there are t_{SYNC_DLY} CLK cycles of systematic delay and the next CLK rising edge synchronizes the DCLK output with those of other ADC10D1000s in the system. For 90° Mode (DDRPh = logic-high), the synchronizing edge occurs on the rising edge of CLK, 4 cycles after the first rising edge of CLK after DCLK_RST is released. For 0° Mode (DDRPh = logic-low), this is 5 cycles instead. The DCLK output is enabled again after a constant delay of t_{OD}.

For both Demux and Non-Demux Modes, there is some uncertainty about how DCLK comes out of the reset state for the first DCLK_RST pulse. For the second (and subsequent) DCLK_RST pulses, the DCLK will come out of the reset state in a known way. Therefore, if using the DCLK Reset feature, it is recommended to apply one "dummy" DCLK_RST pulse before using the second DCLK_RST pulse to synchronize the outputs. This recommendation applies each time the device or channel is powered-on.

When using DCLK_RST to synchronize multiple ADC10D1000s, it is required that the Select Phase bits in the Control Register (Addr: E**h**, Bits 3,4) be the same for each Master ADC10D1000.

16.5 Supply and Grounding Recommendations

16.5.1 Power Planes

More info TBD.

16.5.2 Bypass Capacitors

More info TBD.

16.5.3 Linear Regulator Example

More info TBD.

16.5.4 Ground Planes

More info TBD.

16.5.5 Thermal Management

More info TBD.

16.6 System Power-on Considerations

There are a couple important topics to consider associated with system power-on event including configuration and calibration, and the Data Clock.

16.6.1 Power-on, Configuration, and Calibration

Following the application of power to the ADC10D1000, several events must take place before the output from the ADC10D1000 is valid and at full performance; at least one full calibration must be executed with the device configured in the desired mode.

Following the application of power to the ADC10D1000, there is a delay of t_{CalDly} and then the Power-on Calibration is executed. This is why it is recommended to set the CalDly Pin via an external pull-up or pull-down resistor. Then, the state of that input will be determined at the same time that power is applied to the ADC and t_{CalDly} will be a known quantity. For the purpose of this section, it is assumed that CalDly is set as recommended.

The Control Bits or Pins must be set or written to configure the ADC10D1000 in the desired mode. This must take place via either Extended Control Mode or Non-ECM (Pin Control Mode) before subsequent calibrations will yield an output at full performance in that mode. Some examples of modes include DES/Non-DES Mode, Demux/Non-demux Mode, and Full-Scale Range.

The simplest case is when device is in Non-ECM and the Control Pins are set by pull-up/down resistors, see *Figure 18*. For this case, the settings to the Control Pins ramp concurrently to the ADC voltage. Following the delay of t_{CalDly} and the calibration execution time, t_{CAL}, the output of the ADC10D1000 is valid and at full performance. If it takes longer than t_{CalDly} for the system to stabilize at its operating temperature, it is recommended to execute an on-command calibration at that time.

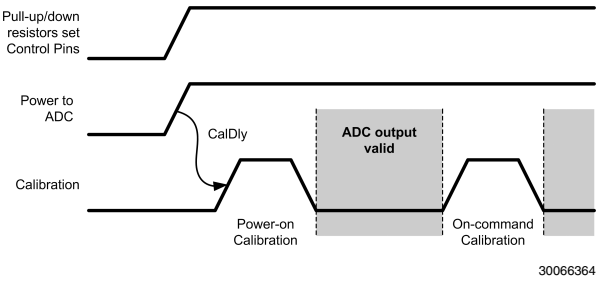


FIGURE 18. Power-on with Control Pins set by Pull-up/down Resistors

Another case is when the FPGA writes to the Control Pins (Non-ECM) or to the SPI (ECM), see *Figure 19*. It is always necessary to comply with the Operating Ratings and Absolute Maximum ratings, i.e. the Control Pins may not be driven below the ground or above the supply, regardless of what the voltage currently applied to the supply is. Therefore, it is not recommended to write to the Control Pins or SPI before power is applied to the ADC10D1000. As long as the FPGA has completed writing to the Control Pins or SPI, the Power-on Calibration will result in a valid output at full performance. Once again, if it takes longer than t_{CalDly} for the system to stabilize at its operating temperature, it is recommended to execute an on-command calibration at that time.

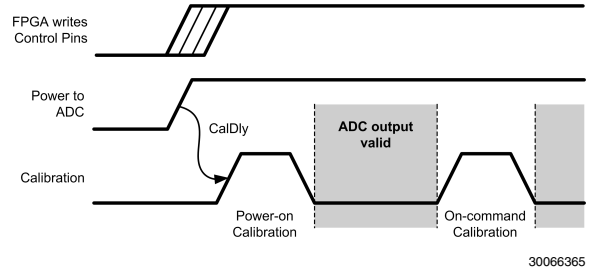


FIGURE 19. Power-on with Control Pins set by FPGA pre Power-on Cal

Due to system requirements, it may not be possible for the FPGA to write to the Control Pins or SPI before the Power-on Calibration takes place, see *Figure 20*. It is not critical to configure the device before the Power-on Calibration, but it is critical to realize that the output for such a case is not at its full performance. Following an On-command Calibration, the device will be at its full performance.

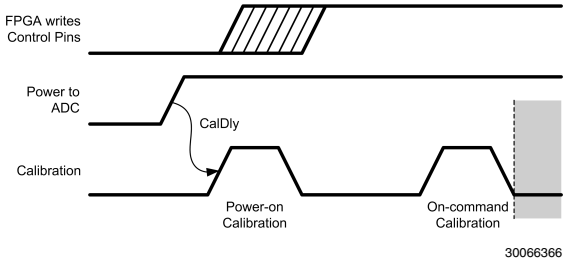


FIGURE 20. Power-on with Control Pins set by FPGA post Power-on Cal

16.6.2 Power-on and Data Clock (DCLK)

Many applications use the DCLK output for a system clock. For the ADC10D1000, each I- and Q-channel has its own

DCLKI and DCLKQ, respectively. The DCLK output is always active, unless that channel is powered-down or the DCLK Reset feature is used while the device is in Demux Mode. As the supply to the ADC10D1000 ramps, the DCLK also comes up, see this example from the ADC10D1000RB: *Figure 21*. While the supply is too low, there is no output at DCLK. As the supply continues to ramp, DCLK functions intermittently with irregular frequency, but the amplitude continues to track with the supply. Much below the low end of operating supply range of the ADC10D1000, the DCLK is already fully operational.

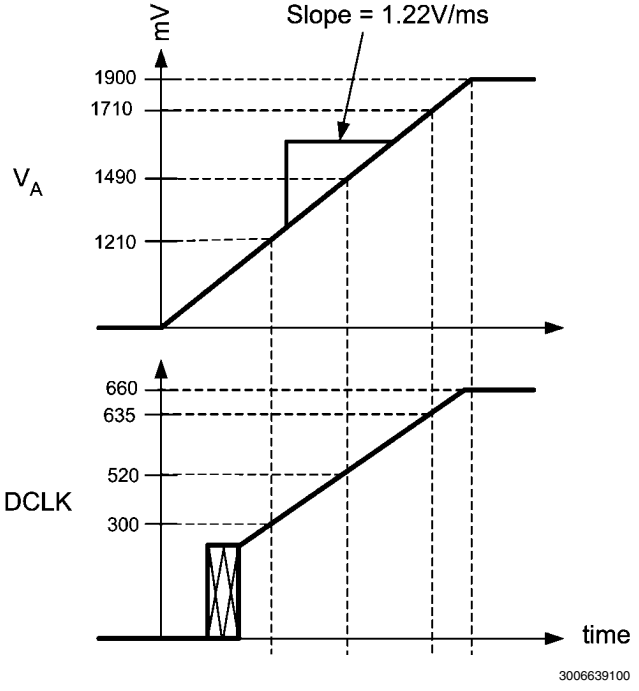


FIGURE 21. Supply and DCLK Ramping

16.7 Temperature Sensor Diode

The ADC10D1000 has an on-die temperature diode connected to pins Tdiode+/- which may be used to monitor the die temperature. National also provides a family of temperature sensors for this application which monitor different numbers of external devices, see *Table 25* .

TABLE 25. Temperature Sensor Recommendation

Number of External Devices Monitored	Recommended Temperature Sensor
1	LM95235
2	LM95213
4	LM95214

The temperature sensor (LM95235/13/14) is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can monitor the temperature of one, two, or four remote diodes as well as its own temperature. It can be used to accurately monitor the temperature of up to one, two, or four external devices such as the ADC10D1000, a FPGA, other system components, and the ambient temperature.

The temperature sensor reports temperature in two different formats for +127.875°C/-128°C range and 0°/255°C range. It has a Sigma-Delta ADC core which provides the first level of noise immunity. For improved performance in a noise environment, the temperature sensor includes programmable digital filters for Remote Diode temperature readings. When the digital filters are invoked, the resolution for the Remote Diode readings increases to 0.03125°C. For maximum flexibility and best accuracy, the temperature sensor includes offset registers that allow calibration of other diode types.

Diode fault detection circuitry in the temperature sensor can detect the absence or fault state of a remote diode: whether D+ is shorted to the power supply, D- or ground, or floating.

In the following of a typical application, the LM95213 is used to monitor the temperature of an ADC10D1000 as well as a FPGA, see *Figure 22*.

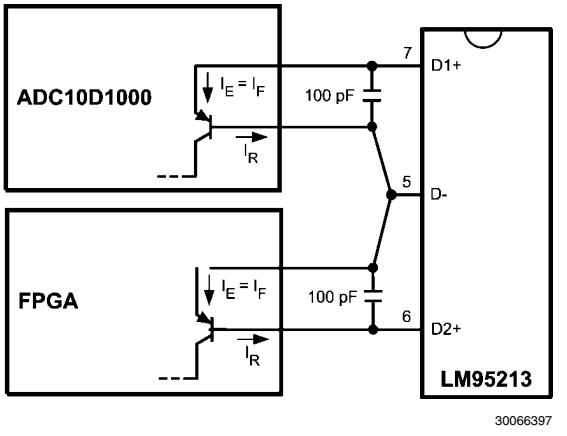


FIGURE 22. Typical Temperature Sensor Application

17.0 Register Definitions

Ten read/write registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Non-extended Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit. See *Table 26* for a summary.

TABLE 26. Register Addresses

A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0**h**	Configuration Register 1
0	0	0	1	1**h**	V_{CMO} Adjust
0	0	1	0	2**h**	I-channel Offset
0	0	1	1	3**h**	I-channel FSR
0	1	0	0	4**h**	Calibration Adjust
0	1	0	1	5**h**	Reserved
0	1	1	0	6**h**	Reserved
0	1	1	1	7**h**	Reserved
1	0	0	0	8**h**	Reserved
1	0	0	1	9**h**	Reserved
1	0	1	0	A**h**	Q-channel Offset
1	0	1	1	B**h**	Q-channel FSR
1	1	0	0	C**h**	Aperture Delay Coarse Adjust
1	1	0	1	D**h**	Aperture Delay Fine Adjust and LC Filter Adjust
1	1	1	0	E**h**	AutoSync
1	1	1	1	F**h**	Reserved

Configuration Register 1

Addr: 0**h** (0000**b**)																POR state: 2000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	LFS	DES	DEQ	DIQ	2SC	Res			
POR	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 CAL: Calibration Enable. When this bit is set to 1**b**, an on-command calibration is initiated. This bit is not reset automatically upon completion of the calibration. Therefore, the user must reset this bit to 0**b** and then set it to 1**b** again to execute another calibration. This bit is logically OR'd with the CAL Pin; both bit and pin must be set to 0**b** before either is used to execute a calibration.

Bit 14 DPS: DDR Phase Select. Set this bit to 0**b** to select the 0° Mode DDR Data-to-DCLK phase relationship and to 1**b** to select the 90° Mode. This bit has no effect when the device is in Non-Demux Mode.

Bit 13 OVS: Output Voltage Select. This bit sets the differential voltage level for the LVDS outputs including Data, OR, and DCLK. 0**b** selects the lower level and 1**b** selects the higher level. See V_{OD} in *Table 11* for details.

Bit 12 TPM: Test Pattern Mode. When this bit is set to 1**b**, the device will continually output a fixed digital pattern at the digital Data and OR outputs. When set to 0**b**, the device will continually output the converted signal, which was present at the analog inputs. See *Section 15.3.2.6 Test Pattern Mode* for details about the TPM pattern.

Bit 11 PDI: Power-down I-channel. When this bit is set to 0**b**, the I-channel is fully operational, but when it is set to 1**b**, the I-channel is powered-down. The I-channel may be powered-down via this bit or the PDI Pin, which is active, even in ECM.

Bit 10 PDQ: Power-down Q-channel. When this bit is set to 0**b**, the Q-channel is fully operational, but when it is set to 1**b**, the Q-channel is powered-down. The Q-channel may be powered-down via this bit or the PDQ Pin, which is active, even in ECM.

Bit 9 Reserved. Must be set to 0**b**.

Bit 8 LFS: Low-Frequency Select. If the sampling clock (CLK) is at or below 300 MHz, set this bit to 1**b**.

Bit 7 DES: Dual-Edge Sampling Mode select. When this bit is set to 0**b**, the device will operate in the Non-DES Mode; when it is set to 1**b**, the device will operate in the DES Mode. See *Section 15.3.1.4 DES/Non-DES Mode* for more information.

Bit 6 DEQ: DES Q-input select. When the device is in DES Mode, this bit can select the input that the device will operate on. The default setting of 0**b** selects the I-input and 1**b** selects the Q-input.

Bit 5 DIQ: DES I- and Q-input. When in DES Mode, setting this bit to 1**b** shorts the I- and Q-inputs. If the bit is left at its default 0**b**, the I- and Q-inputs remain electrically separate. For this bit to function correctly, DEQ (Bit 6) must also be set to 1**b**.

Bit 4 2SC: Two's Complement output. For the default setting of 0**b**, the data is output in Offset Binary format; when set to 1**b**, the data is output in Two's Complement format.

Bits 3:0 Reserved. Must be set to 0**b**.

V_{CMO} Adjust

Addr: 1**h** (0001**b**)																POR state: 2A00**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res								VCA(2:0)			Res				
POR	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bits 15:8 Reserved. Must be set as shown.

Bits 7:5 VCA(2:0): V_{CMO} Adjust. Adjusting from the default VCA(2:0) = 0**d** to VCA(2:0) = 7**d** decreases V_{CMO} from it's typical value (see V_{CMO} in *Table 8*) to 1.05V by increments of ~28.6 mV.

Code	**V_{CMO}**
000 (default)	V_{CMO}
100	V_{CMO}- 114 mV
111	V_{CMO}- 200 mV

Bits 4:0 Reserved. Must be set as shown.

I-channel Offset Adjust

Addr: 2**h** (0010**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM(11:0)											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13 Reserved. Must be set to 0**b**.

Bit 12 OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1**b** incurs a negative offset of the set magnitude.

Bits 11:0 OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is guaranteed by design only for the 9 MSBs.

Code	**Offset [mV]**
0000 0000 0000 (default)	0
1000 0000 0000	22.5
1111 1111 1111	45

I-channel Full Scale Range Adjust

Addr: 3**h** (0011**b**)																POR state: 4000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
POR	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 Reserved. Must be set to 0**b**.

Bits 14:0 FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0**d**) to 980 mV (32767**d**) with the default setting at 790 mV (16384**d**). Monotonicity is guaranteed by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 790 mV. See V_{IN_FSR} in *Table 8* for characterization details.

Code	**FSR [mV]**
000 0000 0000 0000	600
100 0000 0000 0000 (default)	790
111 1111 1111 1111	980

Calibration Adjust

Addr: 4**h** (0100**b**)																POR state: DA7F**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	CSS	Res				CMS(1:0)		Res							
POR	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	1

Bit 15 Reserved. Must be set as shown.

Bit 14 CSS: Calibration Sequence Select. The default 1**b** selects the following calibration sequence: reset all previously calibrated elements to nominal values, do R_{IN} Calibration, do internal linearity Calibration. Setting CSS = 0**b** selects the following calibration sequence: do not reset R_{IN} to its nominal value, skip R_{IN} calibration, do internal linearity Calibration. The calibration must be completed at least one time with CSS = 1**b** to calibrate R_{IN}. Subsequent calibrations may be run with CSS = 0**b** (skip R_{IN} calibration) or 1**b** (full R_{IN} and internal linearity Calibration).

Bits 13:10 Reserved. Must be set as shown.

Bits 9:8 CMS(1:0): Calibration Mode Select. These bits affect the length of time taken to calibrate the internal linearity. See t_{CAL} in *Table 13*.

Bits 7:0 Reserved. Must be set as shown.

Reserved

Addr: 5**h** (0101**b**)																POR state: XXXX**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bits 15:0 Reserved. Do not write.

Reserved

Addr: 6**h** (0110**b**)																POR state: 1C70**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Reserved

Addr: 7**h** (0111**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Reserved

Addr: 8**h** (1000**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Reserved

Addr: 9**h** (1001**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Q-channel Offset Adjust

Addr: A**h** (0110**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM(11:0)											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13 Reserved. Must be set to 0**b**.

Bit 12 OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1**b** incurs a negative offset of the set magnitude.

Bits 11:0 OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is guaranteed by design only for the 9 MSBs.

Code	**Offset [mV]**
0000 0000 0000 (default)	0
1000 0000 0000	22.5
1111 1111 1111	45

Q-channel Full-Scale Range Adjust

Addr: B**h** (0111**b**)																POR state: 4000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
POR	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 Reserved. Must be set to 0**b**.

Bits 14:0 FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0**d**) to 980 mV (32767**d**) with the default setting at 790 mV (16384**d**). Monotonicity is guaranteed by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 790 mV. See V_{IN_FSR} in *Table 8* for characterization details.

Code	**FSR [mV]**
000 0000 0000 0000	600
100 0000 0000 0000 (default)	790
111 1111 1111 1111	980

Aperture Delay Coarse Adjust

Addr: C**h** (1100**b**)																POR state: 0004**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM(11:0)												STA	DCC	Res	
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 15:4 CAM(11:0): Coarse Adjust Magnitude. This 12-bit value determines the amount of delay that will be applied to the input CLK signal. The range is 0 ps delay for CAM(11:0) = 0**d** to a maximum delay of 825 ps for CAM(11:0) = 2431**d** (±95 ps due to PVT variation) in steps of ~340 fs. For code CAM(11:0) = 2432**d** and above, the delay saturates and the maximum delay applies. Additional, finer delay steps are available in register D**h**. Either STA (Bit 3) or SA (Addr: D**h**, Bit 8) must be selected to enable this function.

Bit 3 STA: Select t_{AD} Adjust. Set this bit to 1**b** to enable the t_{AD} adjust feature. When using this feature, make sure that SA (Addr: D**h**, Bit 8) is set to 0**b**.

Bit 2 DCC: Duty Cycle Correct. This bit can be set to 0**b** to disable the automatic duty-cycle stabilizer feature of the chip. This feature is enabled by default.

Bits 1:0 Reserved. Must be set to 0**b**.

Aperture Delay Fine Adjust and LC Filter Adjust

Addr: D**h** (1101**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAM(5:0)						Res	SA	LCF(7:0)							
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:10 FAM(5:0): Fine Aperture Adjust Magnitude. This 6-bit value determines the amount of additional delay that will be applied to the input CLK when the Clock Phase Adjust feature is enabled via STA (Addr: C**h**, Bit 3) or SA (Addr: D**h**, Bit 8). The range is straight binary from 0 ps delay for FAM(5:0) = 0**d** to 2.3 ps delay for FAM(5:0) = 63**d** (±300 fs due to PVT variation) in steps of ~36 fs.

Bit 9 Reserved. Must be set to 0**b**.

Bit 8 SA: Select t_{AD} and LC filter Adjust. Set this bit to 1**b** to enable the t_{AD} and LC filter adjust features. Using this bit is the same as enabling STA (Addr: C**h**, Bit 3), but also enables the LC filter to clean the clock jitter.

Bits 7:0 LCF(7:0): LC tank select Frequency. Use these bits to select the center frequency of the LC filter on the clock input. The range is from 0.8 GHz (255**d**) to 1.5 GHz (0**d**). Note that the tuning range is not binary encoded, and the eight bits are thermometer encoded, i.e. the mid value of 1.1 GHz tuning is achieved with LCF(7:0) = 0000 1111**b**.

AutoSync

Addr: E**h** (1110**b**)																POR state: 0003**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRC(9:0)										Res	SP(1:0)		ES	DOC	DR
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits 15:6 DRC(9:0): Delay Reference Clock (9:0). These bits may be used to increase the delay on the input reference clock when synchronizing multiple ADCs. The minimum delay is 0s (0**d**) to 1000 ps (639**d**). The delay remains the maximum of 1000 ps for any codes above or equal to 639**d**.

Bit 5 Reserved. Must be set to 0**b**.

Bits 4:3 SP(1:0): Select Phase. These bits select the phase of the reference clock which is latched. The codes correspond to the following phase shift:
00 = 0°
01 = 90°
10 = 180°
11 = 270°

Bit 2 ES: Enable Slave. Set this bit to 1**b** to enable the Slave Mode of operation. In this mode, the internal divided clocks are synchronized with the reference clock coming from the master ADC. The master clock is applied on the input pins RCLK. If this bit is set to 0**b**, then the device is in Master Mode.

Bit 1 DOC: Disable Output reference Clocks. Setting this bit to 0**b** sends a CLK/4 signal on RCOut1 and RCOut2. The default setting of 1**b** disables these output drivers. This bit functions as described, regardless of whether the device is operating in Master or Slave Mode, as determined by ES (Bit 2).

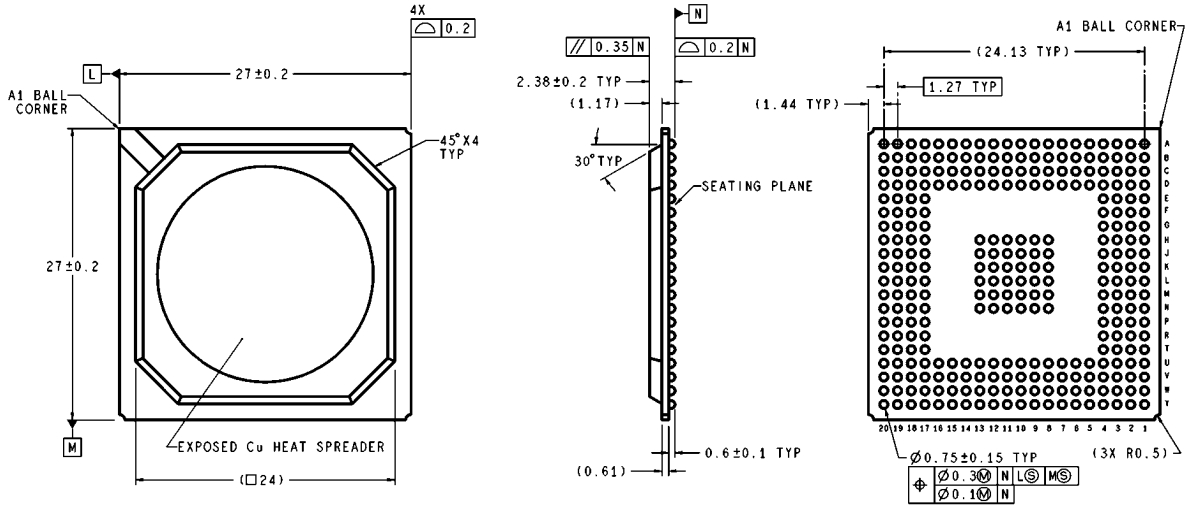
Bit 0 DR: Disable Reset. The default setting of 1**b** leaves the DCLK_RST functionality disabled. Set this bit to 0**b** to enable DCLK_RST functionality.

Reserved

Addr: F**h** (1111**b**)															POR state: 000C**h**	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits 15:0 Reserved. This address is read only.

18.0 Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

UFH292A (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-034, VARIATION BAL-2.

292-Ball BGA Thermally Enhanced Package
Order Number ADC10D1000CUIT
NS Package Number UFH292A

Notes

Notes

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