14 BIT, 80 MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **14 Bit Resolution**
- **80 MSPS Maximum Sample Rate**
- **Typical SNR = 74.4 dBc at 80 MSPS and 30 MHz IF**
- **Typical SFDR = 96.5 dBc at 80 MSPS and 30 MHz IF**
- **Assured SFDR = 91 dBc at 80 MSPS and 30 MHz IF**
- **2.2 V_{pp} Differential Input Range**
- **5 V Supply Operation**
- **3.3 V CMOS Compatible Outputs**
- **1.85 W Total Power Dissipation**
- **2s Complement Output Format**
- **On-Chip Input Analog Buffer, Track and Hold, and Reference Circuit**
- **52 Pin HTQFP Package With Exposed Heatsink**
- **Pin Compatible to the ADS5423, ADS5424, and AD6644/45**
- **Industrial Temperature Range = –40°C to 85°C**

APPLICATIONS

- **Single and Multichannel Digital Receivers**
- **Base Station Infrastructure**
- **Instrumentation**
- **Video and Imaging**

RELATED DEVICES

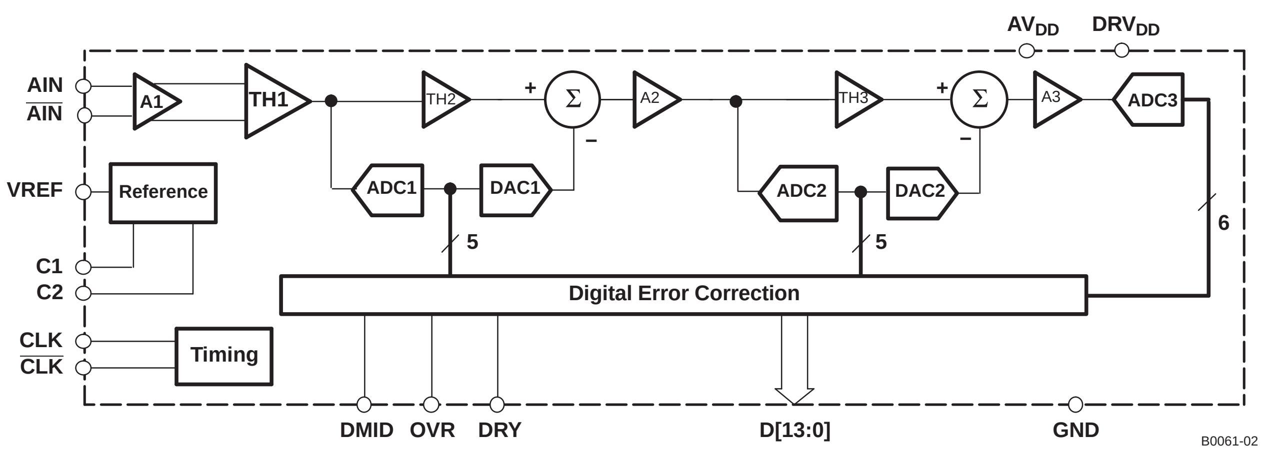
- **Clocking: CDC7005**
- **Amplifiers: OPA695, THS4509**

DESCRIPTION

The ADS5433 is a 14 bit 80 MSPS analog-to-digital converter (ADC) that operates from 5 V and 3.3 V supplies while providing 3.3 V CMOS compatible digital outputs. The ADS5433 is optimized for spurious-free dynamic range (SFDR). Pin-compatible to the ADS5423, ADS5424, and AD6644/45, the ADS5433 provides enhanced SFDR for input frequencies up to 100 MHz. At 80 MSPS, SFDR is typically 96.5 dBc and is guaranteed to 91 dBc over the industrial temperature range (-40°C to 85°C) with a -1 dBFS 30 MHz input signal.

The ADS5433 input buffer isolates the internal switching of the on-chip Track and Hold (T&H) from disturbing the signal source. A 2.2 V_{PP} input range and internal reference generator simplify system design. The ADS5433 is available in a 52 pin HTQFP package and is built on Texas Instrument's complementary bipolar process (BiCom3).

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS5433	HTQFP-52 (1) PowerPAD™	PJY	-40°C to 85°C	ADS5433I	ADS5433IPJY	Tray, 160
					ADS5433IPJYR	Tape and Reel, 1000

(1) Thermal pad size: Octagonal 2,5 mm side

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		ADS5433	UNIT
Supply voltage	AV_{DD} to GND	6	V
	DRV_{DD} to GND	5	
Analog input to GND		–0.3 to AV_{DD} + 0.3	V
Clock input to GND		–0.3 to AV_{DD} + 0.3	V
CLK to $\overline{CLK}$		±2.5	V
Digital data output to GND		–0.3 to DRV_{DD} + 0.3	V
Operating temperature range		–40 to 85	°C
Maximum junction temperature		150	°C
Storage temperature range		–65 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL CHARACTERISTICS(1)

PARAMETER	TEST CONDITIONS	TYP	UNIT
θ_{JA}	Soldered slug, no airflow	22.5	°C/W
θ_{JA}	Soldered slug, 200-LPFM airflow	15.8	°C/W
θ_{JA}	Unsoldered slug, no airflow	33.3	°C/W
θ_{JA}	Unsoldered slug, 200-LPFM airflow	25.9	°C/W
θ_{JC}	Bottom of package (heatslug)	2	°C/W

(1) Using 25 thermal vias (5 × 5 array). See the Application Section.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
SUPPLIES					
AV_{DD}	Analog supply voltage	4.75	5	5.25	V
DRV_{DD}	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
V_{CM}	Input common-mode voltage		2.4		V
DIGITAL OUTPUT					
	Maximum output load		10		pF
CLOCK INPUT					
	ADCLK input sample rate (sine wave) $1/t_C$	30		80	MSPS
	Clock amplitude, sine wave, differential (1)		3		V_{PP}
	Clock duty cycle (2)		50%		
	Open free-air temperature range	–40		85	°C

(1) See Figure 12 and Figure 13 for more information.
(2) See Figure 11 for more information.

ELECTRICAL CHARACTERISTICS

Over full temperature range (T_{MIN} = –40°C to T_{MAX} = 85°C), sampling rate = 80 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential sinusoidal clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				14		Bits
ANALOG INPUTS						
	Differential input range			2.2		V_{PP}
	Differential input resistance	See Figure 27		1		kΩ
	Differential input capacitance	See Figure 27		1.5		pF
	Analog input bandwidth			570		MHz
INTERNAL REFERENCE VOLTAGES						
V_{REF}	Reference voltage			2.4		V
DYNAMIC ACCURACY						
	No missing codes			Tested		
DNL	Differential linearity error	f_{IN} = 10 MHz	–0.95	±0.5	1.5	LSB
INL	Integral linearity error	f_{IN} = 10 MHz		±1.5		LSB
	Offset error		–5	0	5	mV
	Offset temperature coefficient			1.7		ppm/°C
	Gain error		–5	0.9	5	%FS
	PSRR			1		mV/V
	Gain temperature coefficient			77		ppm/°C
POWER SUPPLY						
I_{AVDD}	Analog supply current	V_{IN} = full scale, f_{IN} = 30 MHz		355	410	mA
I_{DRVDD}	Output buffer supply current	V_{IN} = full scale, f_{IN} = 30 MHz		35	47	mA
	Power dissipation	Total power with 10-pF load on each digital output to ground, f_{IN} = 70 MHz		1.85	2.2	W
	Power-up time			20	100	ms
DYNAMIC AC CHARACTERISTICS						
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		74.6		dBc
		f_{IN} = 30 MHz	73	74.4		
		f_{IN} = 50 MHz		74.3		
		f_{IN} = 70 MHz	73	74		
		f_{IN} = 100 MHz		73.4		
		f_{IN} = 170 MHz		71.9		
		f_{IN} = 230 MHz		70.5		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		95.3		dBc
		f_{IN} = 30 MHz	91	96.5		
		f_{IN} = 50 MHz		95.7		
		f_{IN} = 70 MHz		90.8		
		f_{IN} = 100 MHz		84		
		f_{IN} = 170 MHz		70		
		f_{IN} = 230 MHz		61.3		

ELECTRICAL CHARACTERISTICS (Continued)

Over full temperature range (T_{MIN} = –40°C to T_{MAX} = 85°C), sampling rate = 80 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential sinusoidal clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS (Continued)						
SINAD	Signal-to-noise + distortion	f_{IN} = 10 MHz	72.8	74.5		dBc
		f_{IN} = 30 MHz		74.4		
		f_{IN} = 50 MHz		74.2		
		f_{IN} = 70 MHz		73.8		
		f_{IN} = 100 MHz		73		
		f_{IN} = 170 MHz		67.4		
		f_{IN} = 230 MHz		59.9		
HD2	Second harmonic	f_{IN} = 10 MHz		105		dBc
		f_{IN} = 30 MHz		103		
		f_{IN} = 50 MHz		103		
		f_{IN} = 70 MHz		94		
		f_{IN} = 100 MHz		96		
		f_{IN} = 170 MHz		77		
		f_{IN} = 230 MHz		67		
HD3	Third harmonic	f_{IN} = 10 MHz		97		dBc
		f_{IN} = 30 MHz		101		
		f_{IN} = 50 MHz		97		
		f_{IN} = 70 MHz		91		
		f_{IN} = 100 MHz		84		
		f_{IN} = 170 MHz		70		
		f_{IN} = 230 MHz		61		
	Worst-harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz		99		dBc
		f_{IN} = 30 MHz		98		
		f_{IN} = 50 MHz		99		
		f_{IN} = 70 MHz		98		
		f_{IN} = 100 MHz		98		
		f_{IN} = 170 MHz		94		
		f_{IN} = 230 MHz		92		
	RMS idle channel noise	Input pins tied together		0.9		LSB

DIGITAL CHARACTERISTICS

Over full temperature range (T_{MIN} = –40°C to T_{MAX} = 85°C), AV_{DD} = 5 V, DRV_{DD} = 3.3 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUTS					
Low-level output voltage	C_{LOAD} = 10 pF(1)		0.1	0.6	V
High-level output voltage	C_{LOAD} = 10 pF(1)	2.6	3.2		V
Output capacitance			3		pF
DMID			DRV_{DD}/2		V

(1) Equivalent capacitance to ground of (load + parasitics of transmission lines).

TIMING REQUIREMENTS(1)

Over full temperature range, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, sampling rate = 80 MSPS

PARAMETER		MIN	TYP	MAX	UNIT
APERTURE TIME					
t_A	Aperture delay		500		ps
t_J	Clock slope independent aperture uncertainity (jitter)		150		fs
k_J	Clock slope dependent jitter factor		50		µV
CLOCK INPUT					
t_{CLK}	Clock period	12.5			ns
t_{CLKH} (2)	Clock pulsewidth high	6.25			ns
t_{CLKL} (2)	Clock pulsewidth low	6.25			ns
CLOCK TO DATAREADY (DRY)					
t_{DR}	Clock rising 50% to DRY falling 50%	2.8	3.9	4.7	ns
t_{C_DR}	Clock rising 50% to DRY rising 50%		$t_{DR} + t_{CLKH}$		ns
$t_{C\_DR\_50\%}$	Clock rising 50% to DRY rising 50% with 50% duty cycle clock	9	10.1	11	ns
CLOCK TO DATA, OVR(4)					
t_r	Data V_{OL} to data V_{OH} (rise time)		2		ns
t_f	Data V_{OH} to data V_{OL} (fall time)		2		ns
L	Latency		3		Cycles
$t_{su(C)}$	Valid DATA(3) to clock 50% with 50% duty cycle clock (setup time)	4.8(4)	6.3		ns
$t_{H(C)}$	Clock 50% to invalid DATA(3) (hold time)	2.6	3.6		ns
DATAREADY (DRY) to DATA, OVR(5)					
$t_{su(DR)\_50\%}$	Valid DATA(3) to DRY 50% with 50% duty cycle clock (setup time)	3.3(6)	4		ns
$t_{h(DR)\_50\%}$	DRY 50% to invalid DATA(3) with 50% duty cycle clock (hold time)	5.4	5.9		ns

(1) All values obtained from design and characterization.
(2) See Figure 1 for more information.
(3) See V_{OH} and V_{OL} levels.
(4) $t_{SU(C)} = t_{CLK} - t_{CLK}(min) + t_{SU(C)}(min)$, where $t_{CLK}(min)$ = 12.5 ns and $t_{SU(C)}(min)$ = 4.8 ns for all sample rates equal to or below 80MSPS.
(5) Data is updated with clock rising edge or DRY falling edge.
(6) $t_{SU(DR)50\%} = (t_{CLK} / 2) - (t_{CLK}(min) / 2) + t_{SU(DR)}(min)$, where $t_{CLK}(min)$ = 12.5 ns and $t_{SU(DR)}(min)$ = 3.3 ns for all sample rates equal to or below 80MSPS.

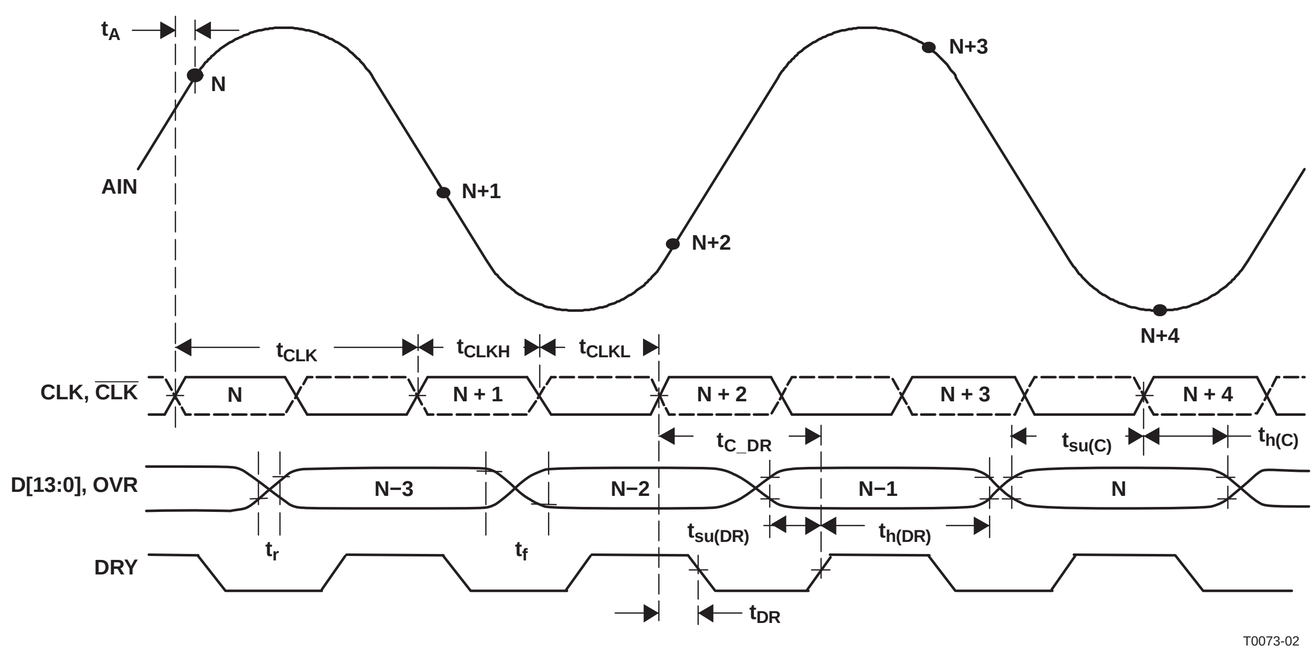
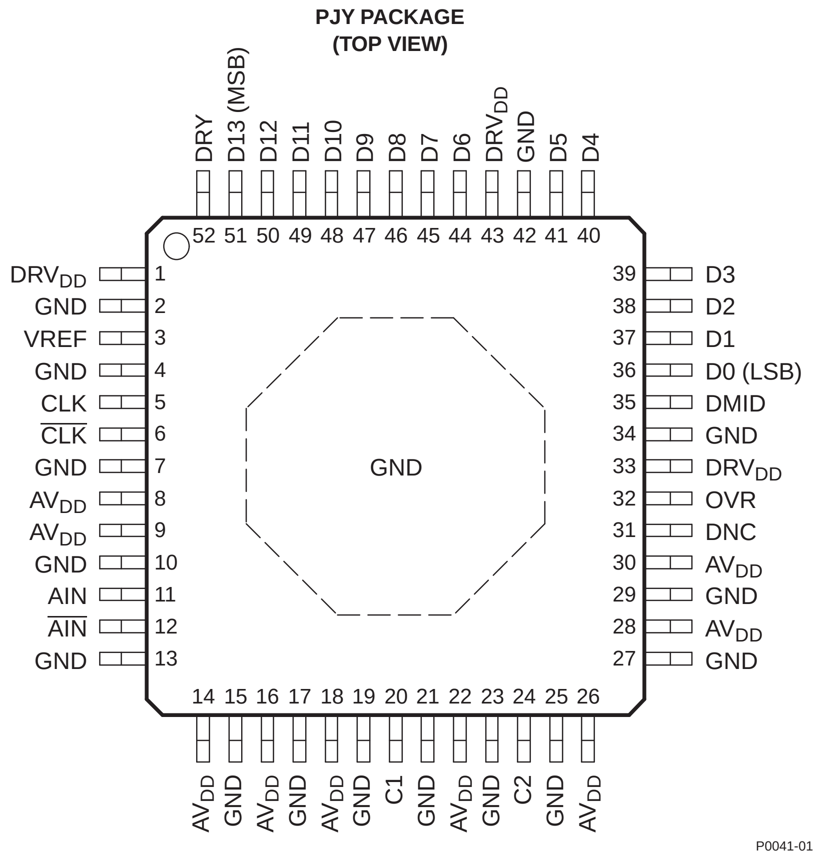


Figure 1. Timing Diagram

PIN CONFIGURATION



PIN ASSIGNMENTS

TERMINAL		DESCRIPTION
NAME	NO.	
DRV_{DD}	1, 33, 43	3.3 V power supply, digital output stage only
GND	2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	Ground
VREF	3	2.4 V reference. Bypass to ground with a 0.1-µF microwave chip capacitor.
CLK	5	Clock input. Conversion initiated on rising edge.
$\overline{CLK}$	6	Complement of CLK, differential input
AV_{DD}	8, 9, 14, 16, 18, 22, 26, 28, 30	5 V analog power supply
AIN	11	Analog input
$\overline{AIN}$	12	Complement of AIN, differential analog input
C1	20	Internal voltage reference. Bypass to ground with a 0.1-µF chip capacitor.
C2	24	Internal voltage reference. Bypass to ground with a 0.1-µF chip capacitor.
DNC	31	Do not connect
OVR	32	Overrange bit. A logic level high indicates the analog input exceeds full scale.
DMID	35	Output data voltage midpoint. Approximately equal to $(DV_{CC})/2$
D0 (LSB)	36	Digital output bit (least significant bit); two's complement
D1–D5, D6–D12	37–41, 44–50	Digital output bits in two's complement
D13 (MSB)	51	Digital output bit (most significant bit); 2s complement
DRY	52	Data ready output

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSB.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual value average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

PSRR

The maximum change in offset voltage divided by the total change in supply voltage, in units of mV/V.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree celcius of the paramter from T_{MIN} or T_{MAX}. It is computed as the maximum variation of that parameter over the whole temperature range divided by $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first five harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N} \tag{1}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D} \tag{2}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Total Harmonic Distortion (THD)

THD is the ratio of the fundamental power (P_S) to the power of the first five harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D} \quad (3)$$

THD is typically given in units of dBc (dB to carrier).

Power Up Time

The difference in time from the point where the supplies are stable at ±5% of the final value, to the time the ac test is past.

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequiencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when it is referred to the full-scale range.

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 80 MSPS, 3.3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

SPECTRAL PERFORMANCE

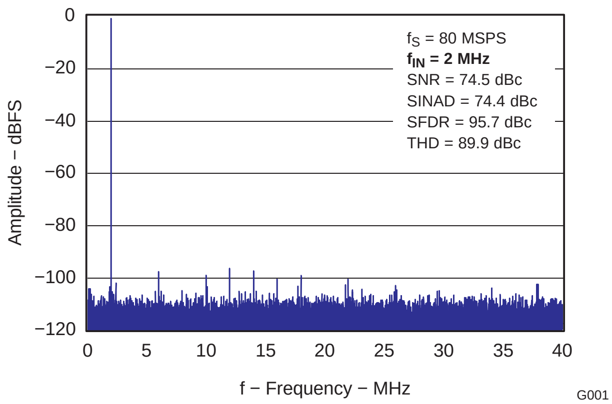


Figure 2.

SPECTRAL PERFORMANCE

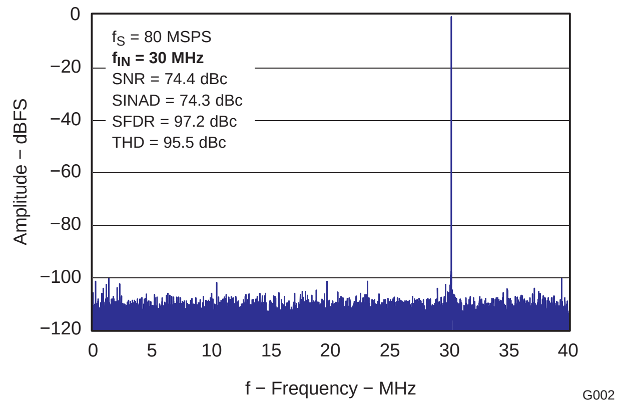


Figure 3.

SPECTRAL PERFORMANCE

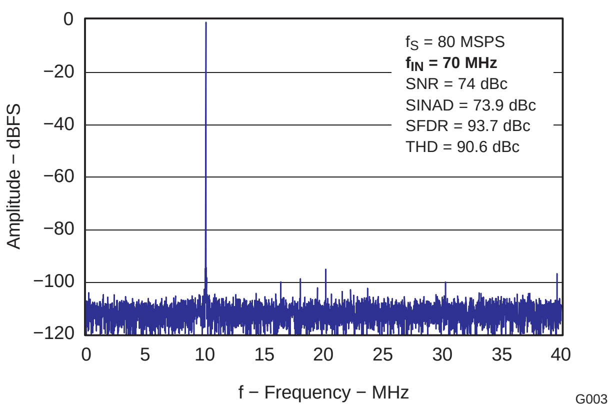


Figure 4.

TWO-TONE INTERMODULATION DISTORTION

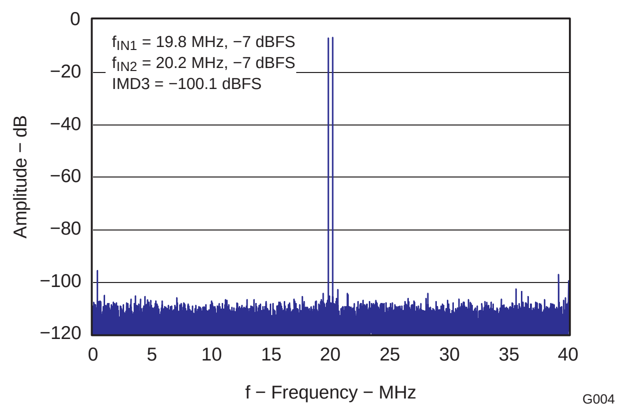


Figure 5.

TWO-TONE INTERMODULATION DISTORTION

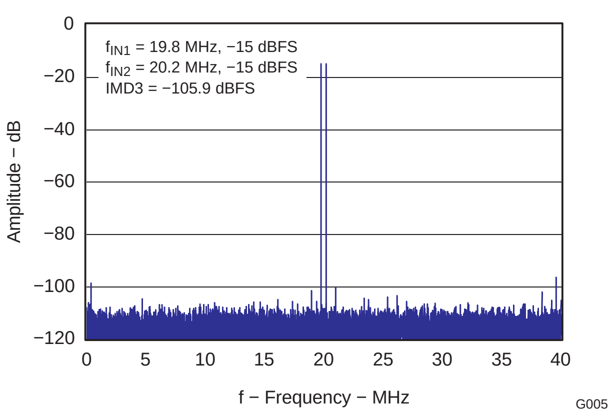


Figure 6.

TWO-TONE INTERMODULATION DISTORTION

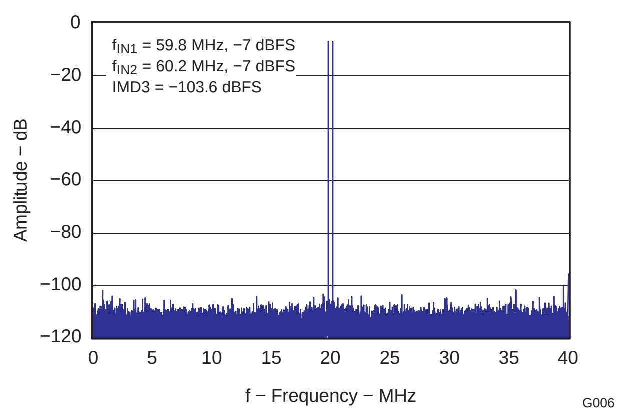


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 80 MSPS, 3.3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

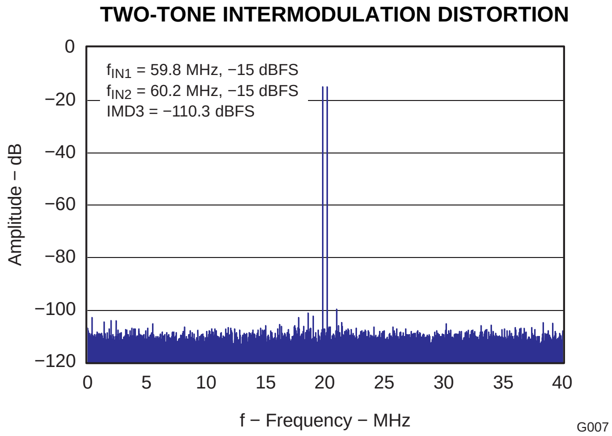


Figure 8.

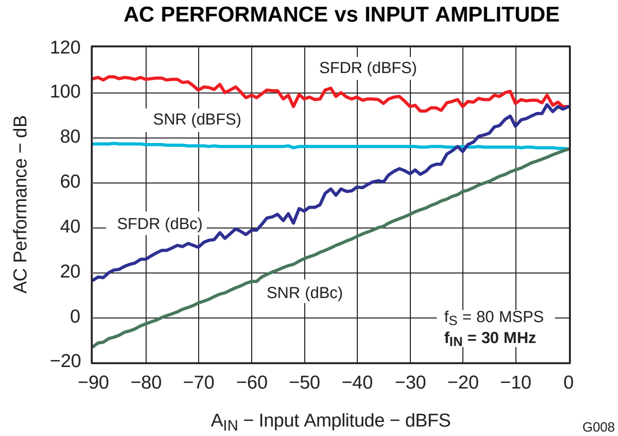


Figure 9.

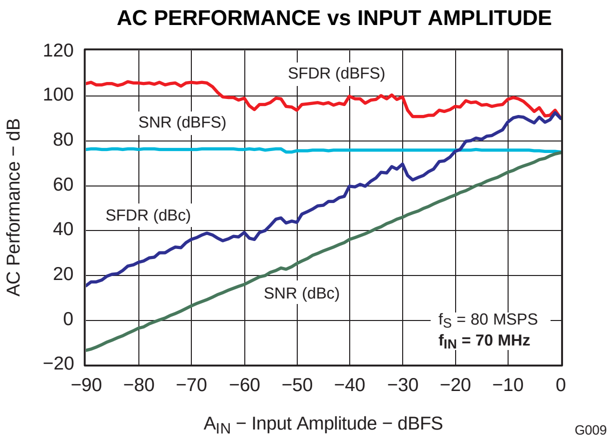


Figure 10.

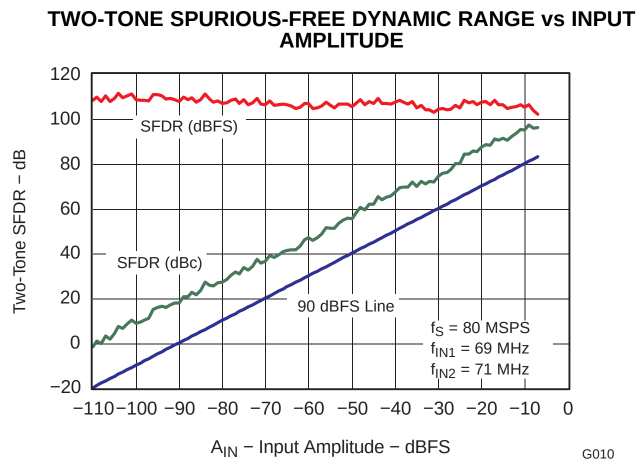


Figure 11.

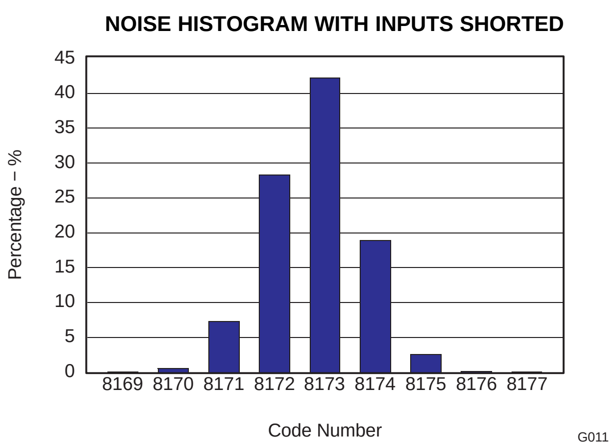


Figure 12.

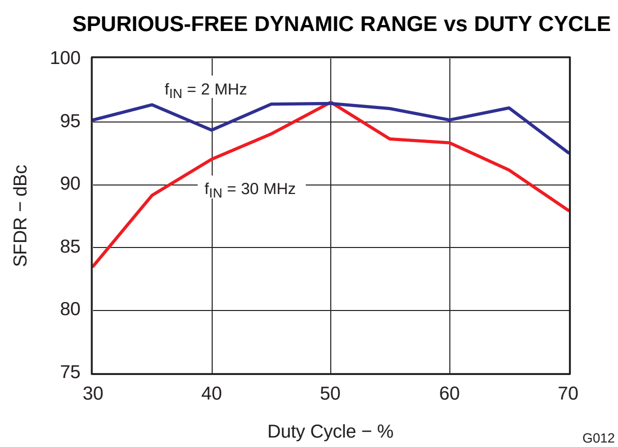


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 80 MSPS, 3.3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

AC PERFORMANCE vs CLOCK LEVEL

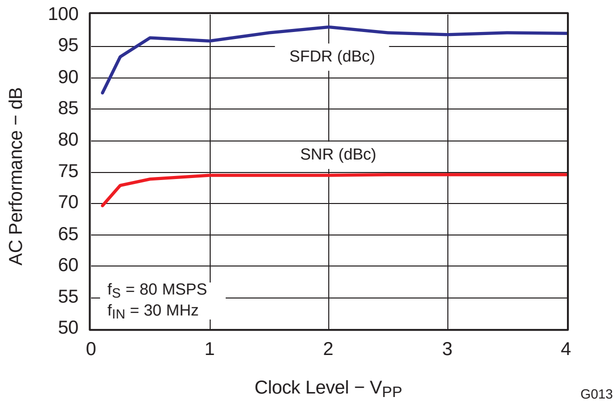


Figure 14.

AC PERFORMANCE vs CLOCK LEVEL

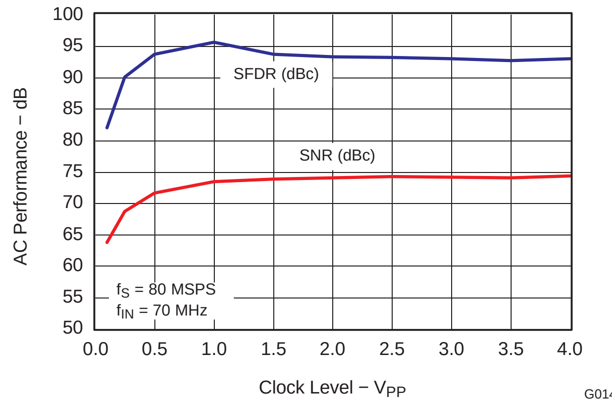


Figure 15.

AC PERFORMANCE vs CLOCK COMMON MODE

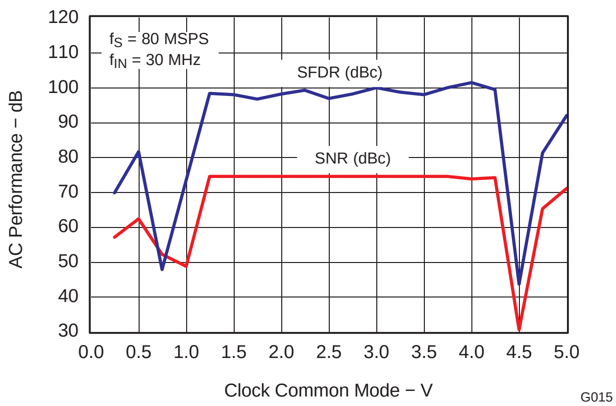


Figure 16.

SPURIOUS-FREE DYNAMIC RANGE vs ANALOG SUPPLY VOLTAGE

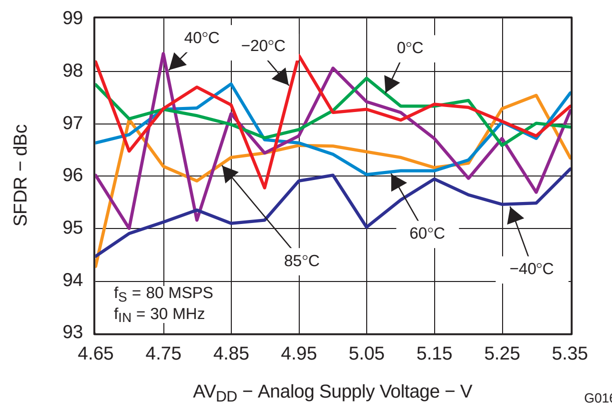


Figure 17.

SIGNAL-TO-NOISE RATIO vs ANALOG SUPPLY VOLTAGE

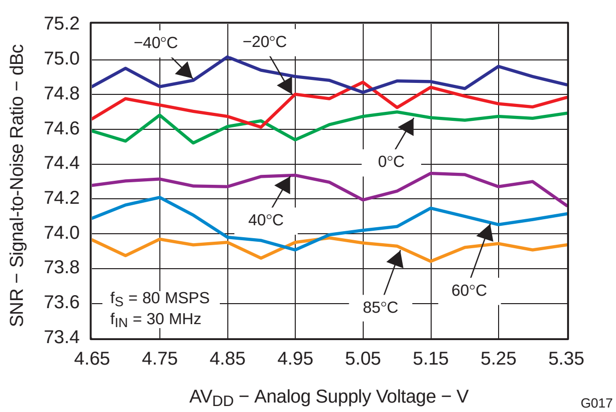


Figure 18.

SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL SUPPLY VOLTAGE

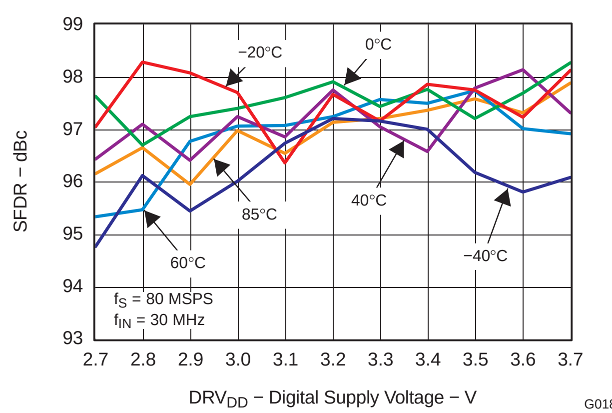


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 80 MSPS, 3.3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

SIGNAL-TO-NOISE RATIO vs DIGITAL SUPPLY VOLTAGE

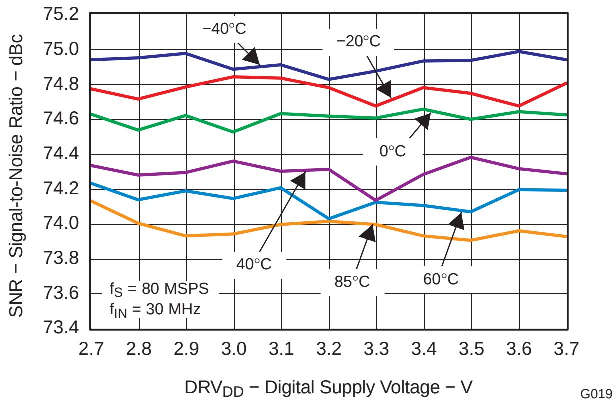


Figure 20.

DIFFERENTIAL NONLINEARITY

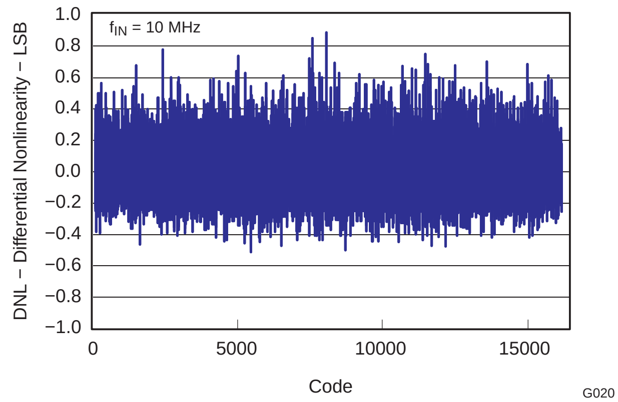


Figure 21.

INTEGRAL NONLINEARITY

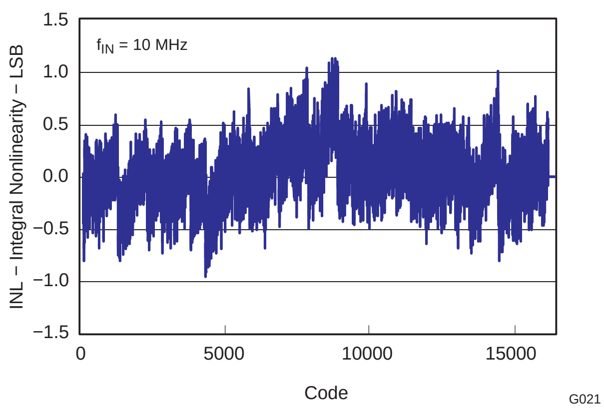


Figure 22.

DIFFERENTIAL NONLINEARITY

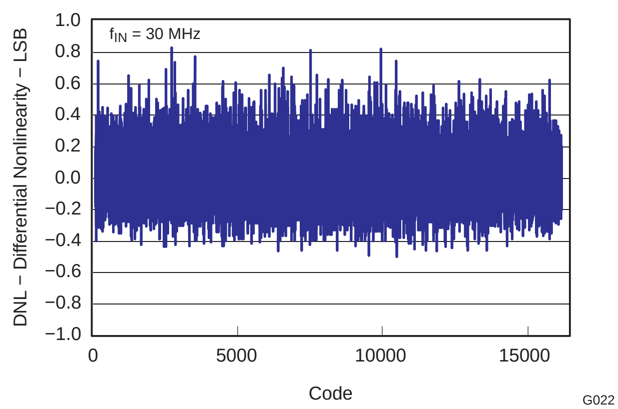


Figure 23.

INTEGRAL NONLINEARITY

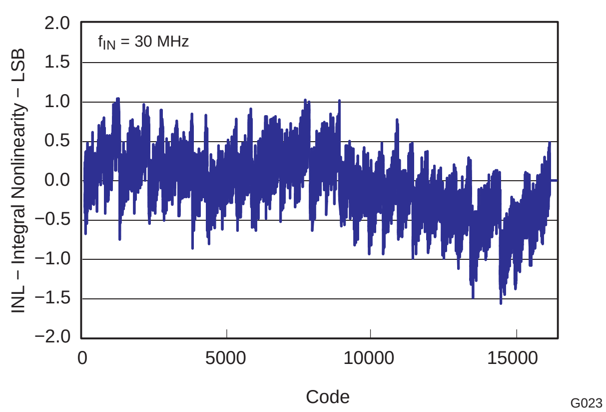


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 80 MSPS, 3.3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY AND SAMPLING FREQUENCY

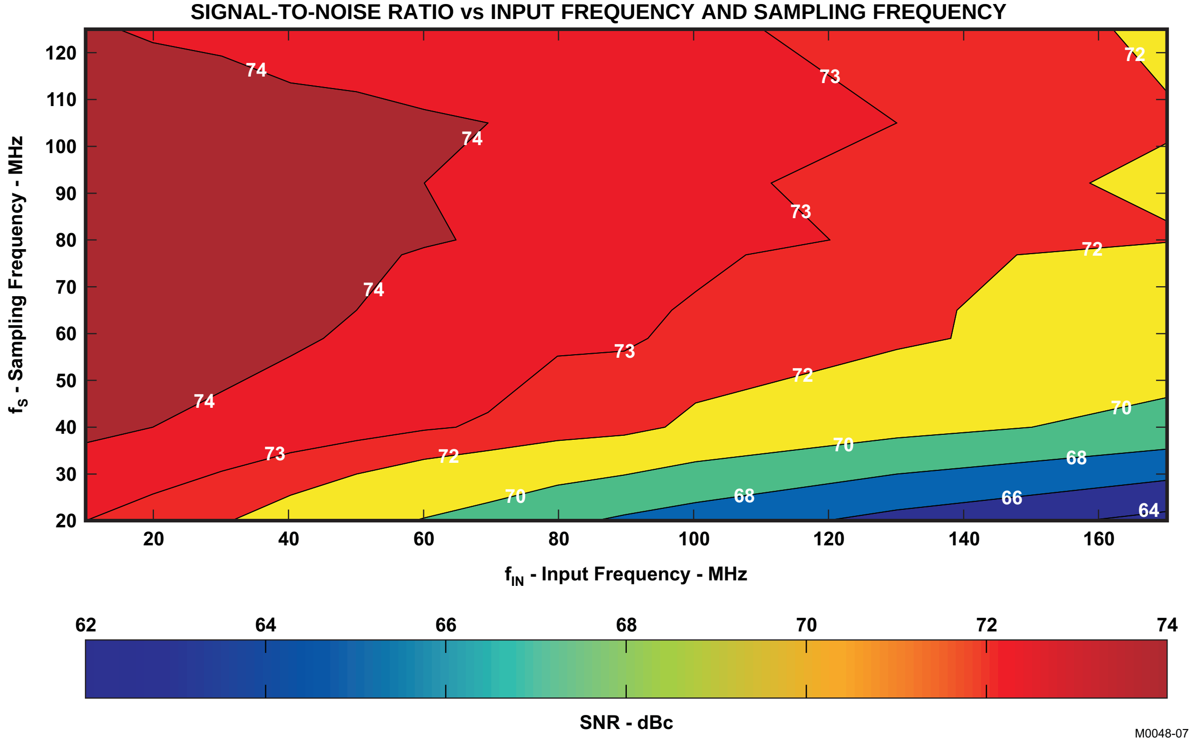


Figure 25.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY AND SAMPLING FREQUENCY

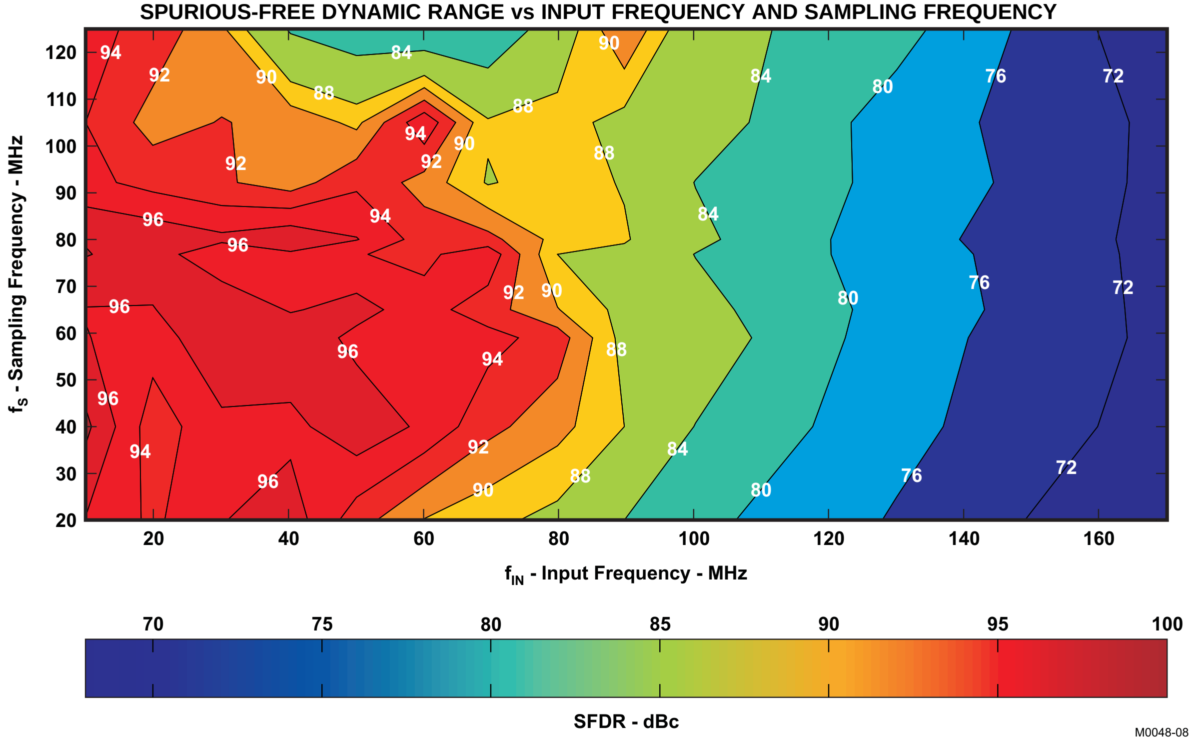


Figure 26.

EQUIVALENT CIRCUITS

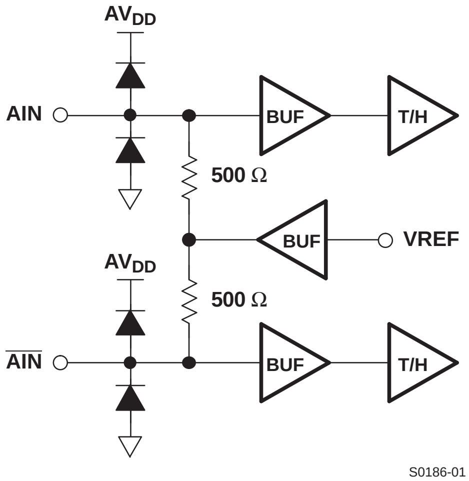


Figure 27. Analog Input

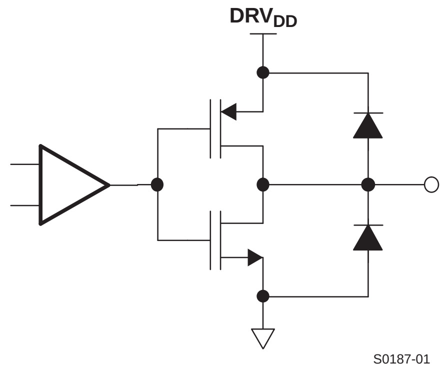


Figure 28. Digital Output

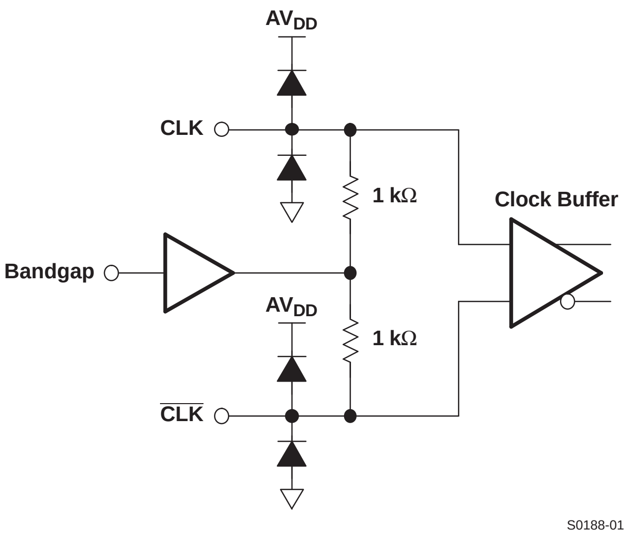


Figure 29. Clock Input

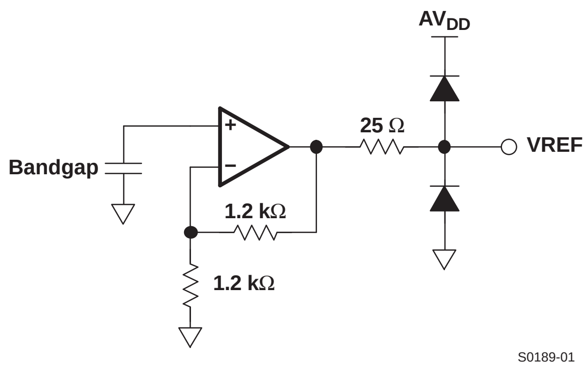


Figure 30. Reference

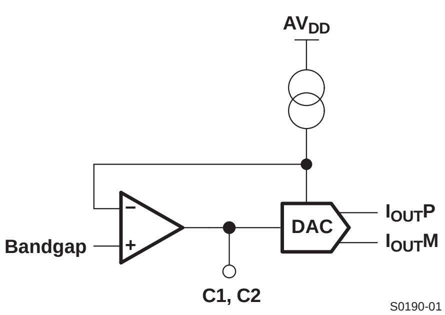


Figure 31. Decoupling Pin

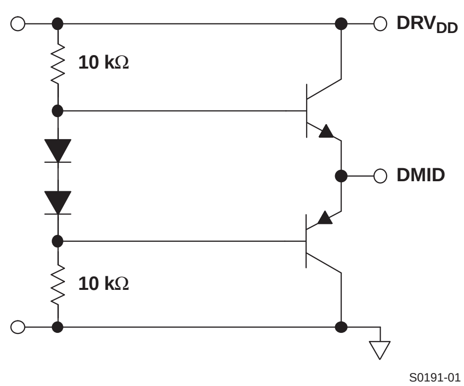


Figure 32. DMID Generation

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5433 is a 14 bit, 80 MSPS, monolithic pipeline analog to digital converter. Its bipolar analog core operates from a 5 V supply, while the output uses 3.3 V supply for compatibility with the CMOS family. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of three clock cycles, after which the output data is available as a 14 bit parallel word, coded in binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5433 (see Figure 27) consists of an analog differential buffer followed by a bipolar track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500 Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 11 and 12) swings symmetrically between 2.4 +0.55 V and 2.4 –0.55 V. This means that each input is driven with a signal of up to 2.4 ±0.55 V, so that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. The maximum swing is determined by the internal reference voltage generator eliminating any external circuitry for this purpose.

The ADS5433 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 33 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required a step up transformer can be used. For higher gains that would require impractical higher turn ratios on the transformer, a single-ended amplifier driving the transformer can be used (see Figure 34). Another circuit optimized for performance would be the one on Figure 35, using the THS4304 or the OPA695. Texas Instruments has shown excellent performance on this configuration up to 10 dB gain with the THS4304 and at 14 dB gain with the OPA695. For the best performance, they need to be configured differentially after the transformer (as shown) or in inverting mode for the OPA695 (see SBAA113); otherwise, HD2 from the op amps limits the useful frequency.

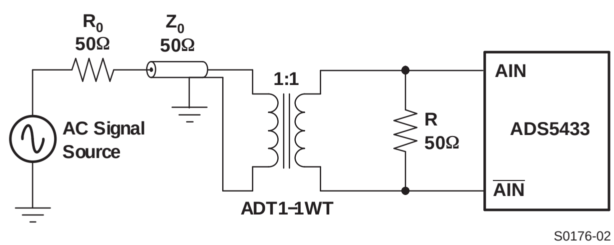


Figure 33. Converting a Single-Ended Input to a Differential Signal Using RF Transformers

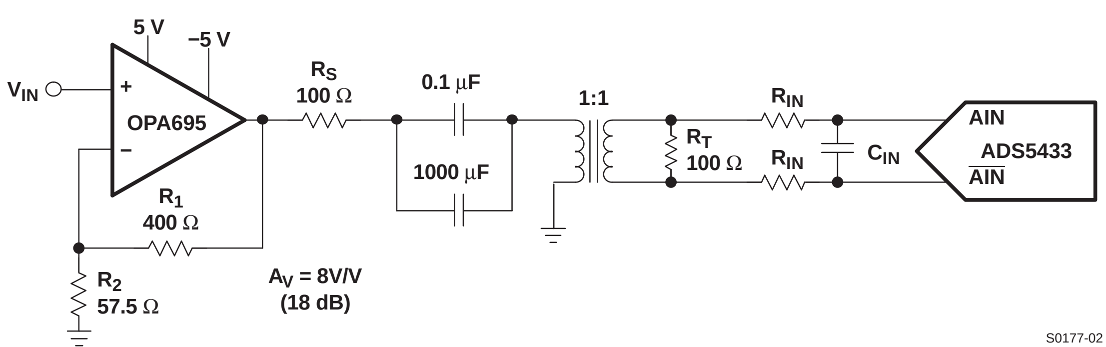


Figure 34. Using the OPA695 With the ADS5433

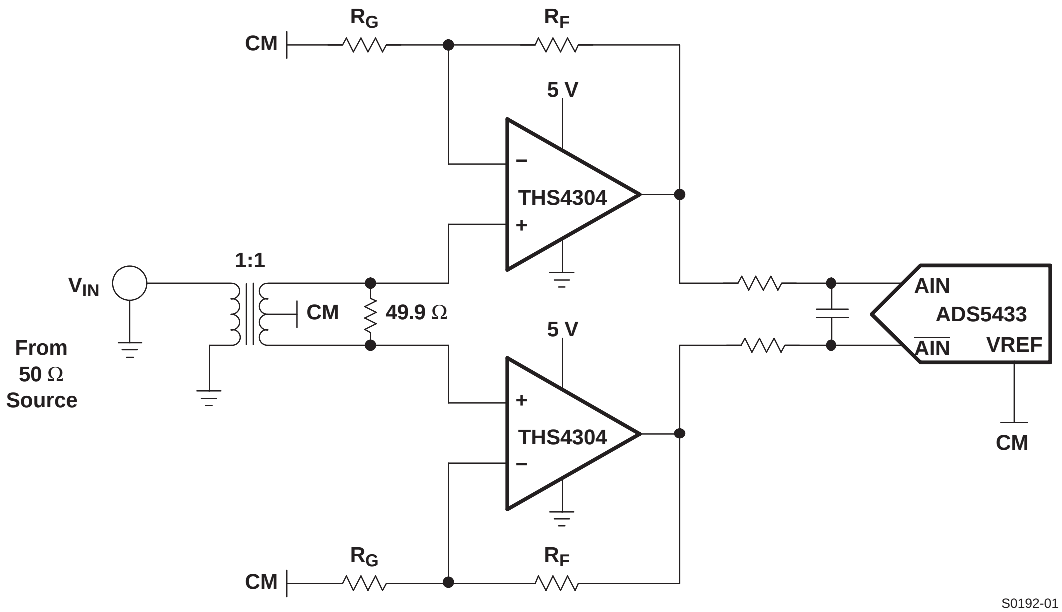


Figure 35. Using the THS4304 With the ADS5433

Besides these, Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, and OPA847) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instrument's THS9001, can also be used with an RF transformer for high input frequency applications. For applications requiring dc-coupling with the signal source, instead of using a topology with three single ended amplifiers, a differential input/differential output amplifier like the THS4509 (see Figure 36) can be used, which minimizes board space and reduce number of components.

Figure 38 shows their combined SNR and SFDR performance versus frequency with –1 dBFS input signal level and sampling at 80 MSPS.

On this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5433.

The 225 Ω resistors and 2.7 pF capacitor between the THS4509 outputs and ADS5433 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (–3 dB).

For this test, an Agilent signal generator is used for the signal source. The generator is an ac-coupled 50 Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source.

Input termination is accomplished via the 69.8 Ω resistor and 0.22 mF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22 µF capacitor and 49.9 Ω resistor is inserted to ground across the 69.8 W resistor and 0.22 µF capacitor on the alternate input to balance the circuit.

Gain is a function of the source impedance, termination, and 348 Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50 Ω termination for other common gains.

Since the ADS5433 recommended input common-mode voltage is +2.4 V, the THS4509 is operated from a single power supply input with V_{S+} = +5 V and V_{S-} = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

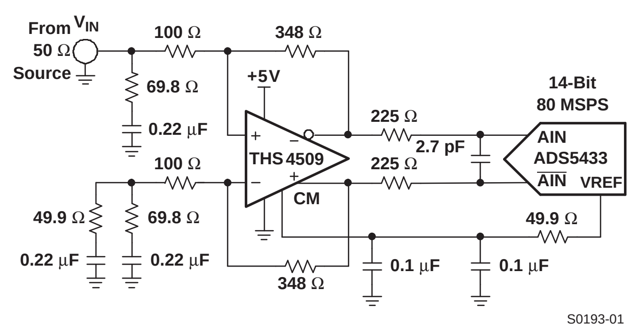


Figure 36. Using the THS4509 With the ADS5433

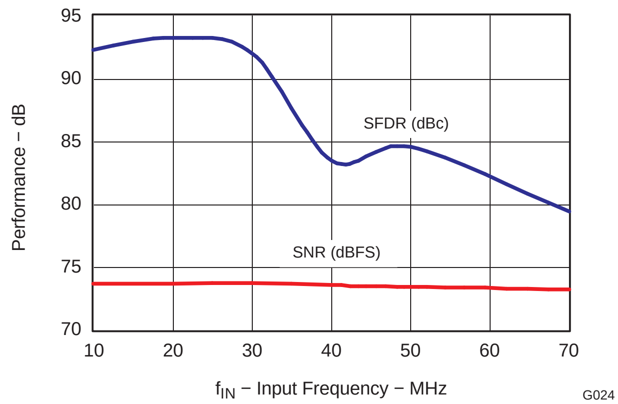


Figure 37. Performance vs Input Frequency for the THS4509 + ADS5433 Configuration

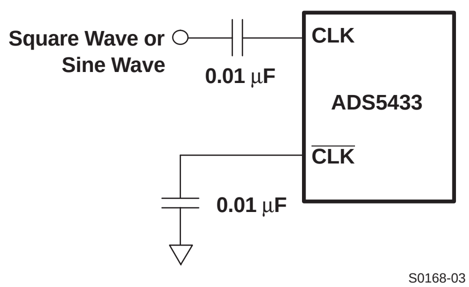


Figure 38. Single-Ended Clock

CLOCK INPUTS

The ADS5433 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low input frequency applications, where jitter may not be a big concern, the use of single ended clock (see Figure 38) could save some cost and board space without any trade-off in performance. When driven on this configuration, it is best to connect CLKM (pin 11) to ground with a 0.01 µF capacitor, while CLKP is ac-coupled with a 0.01 µF capacitor to the clock source, as shown in Figure 35.

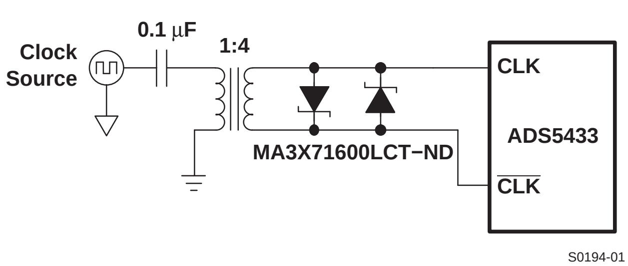


Figure 39. Differential Clock

Nevertheless, for jitter sensitive applications, the use of a differential clock will have some advantages (as with any other ADCs) at the system level. The first advantage is that it allows for common-mode noise rejection at the PCB level. A further analysis (see *Clocking High Speed Data Converters*, SLYT075) reveals one more advantage. The following formula describes the different contributions to clock jitter:

$$(\text{Jittertotal})^2 = (\text{EXT\_jitter})^2 + (\text{ADC\_jitter})^2 = (\text{EXT\_jitter})^2 + (\text{ADC\_int})^2 + (\text{K/clock\_slope})^2$$

The first term would represent the external jitter, coming from the clock source, plus noise added by the system on the clock distribution, up to the ADC. The second term is the ADC contribution, which can be divided in two portions. The first does not depend directly on any external factor. That is the best we can get out of our ADC. The second contribution is a term inversely proportional to the clock slope. The faster the slope, the smaller this term will be. As an example, we could compute the ADC jitter contribution from a sinusoidal input clock of 3 V_{PP} amplitude and Fs = 80 MSPS:

$$\text{ADC\_jitter} = \text{sqrt}\ ((150\text{fs})^2 + (5 \times 10^{-5}/(1.5 \times 2 \times \text{PI} \times 80 \times 10^6))^2) = 164\text{fs}$$

The use of differential clock allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. This, on the case of sinusoidal clock, results on higher slew rates which minimizes the impact of the jitter factor inversely proportional to the clock slope.

Figure 39 shows this approach. The back-to-back Schottky can be added to limit the clock amplitude in cases where this would exceed the absolute maximum ratings, even when using a differential clock. Figure 12 and Figure 13 show the performance versus input clock amplitude for a sinusoidal clock.

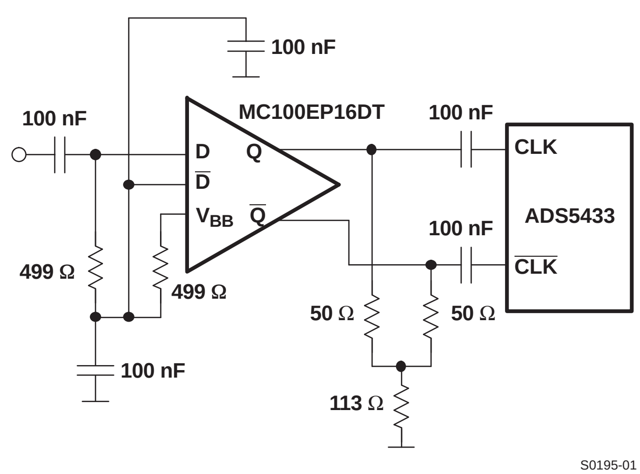


Figure 40. Differential Clock Using PECL Logic

Another possibility is the use of a logic based clock, as PECL. In this case, the slew rate of the edges will most likely be much higher than the one obtained for the same clock amplitude based on a sinusoidal clock. This solution would minimize the effect of the slope dependent ADC jitter. Nevertheless, observe that for the ADS5433, this term is small and has been optimized. Using logic gates to square a sinusoidal clock may not produce the best results as logic gates may not have been optimized to act as comparators, adding too much jitter while squaring the inputs.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1 kΩ resistors. It is recommended using an ac coupling, but if for any reason, this scheme is not possible, due to, for instance, asynchronous clocking, the ADS5433 presents a good tolerance to clock common-mode variation (see Figure 14).

Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 11 shows the performance variation of the ADC versus clock duty cycle.

DIGITAL OUTPUTS

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (DRY, pin 52), and an out-of-range indicator (OVR, pin 32) that equals 1 when the output reaches the full-scale limits.

The output format is two's complement. When the input voltage is at negative full scale (around –1.1 V differential), the output will be, from MSB to LSB, 10 0000 0000 0000. Then, as the input voltage is increased, the output switches to 10 0000 0000 0001, 10 0000 0000 0010 and so on until 11 1111 1111 1111 right before mid-scale (when both inputs are tied together if we neglect offset errors). Further increase on input voltages, outputs the word 00 0000 0000 0000, to be followed by 00 0000 0000 0001, 00 0000 0000 0010 and so on until reaching 01 1111 1111 1111 at full-scale input (1.1 V differential).

Although the output circuitry of the ADS5433 has been designed to minimize the noise produced by the transients of the data switching, care must be taken when designing the circuitry reading the ADS5433 outputs. Output load capacitance should be minimized by minimizing the load on the output traces, reducing their length and the number of gates connected to them, and by the use of a series resistor with each pin. Typical numbers on the data sheet tables and graphs are obtained with 100 Ω series resistor on each digital output pin, followed by a 74AVC16244 digital buffer as the one used in the evaluation board.

POWER SUPPLIES

The use of low noise power supplies with adequate decoupling is recommended, being the linear supplies the first choice vs switched ones, which tend to generate more noise components that can be coupled to the ADS5433.

The ADS5433 uses two power supplies. For the analog portion of the design, a 5 V AV_{DD} is used, while for the digital outputs supply (DRV_{DD}), we recommend the use of 3.3 V. All the ground pins are marked as GND, although AGND pins and DRGND pins are not tied together inside the package. Customers willing to experiment with different grounding schemes should know that AGND pins are 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, and 29, while DRGND pins are 2, 34, and 42. Nevertheless, we recommend that both grounds are tied together externally, using a common ground plane. That is the case on the production test boards and modules provided to customer for evaluation. In order to obtain the best performance, the user should layout the board to assure that the digital return currents do not flow under the analog portion of the board. This can be achieved without the need to split the board and just with careful component placing and increasing the number of vias and ground planes.

Finally, notice that the metallic heat sink under the package is also connected to analog ground.

LAYOUT INFORMATION

The evaluation board represents a good guideline of how to layout the board to obtain the maximum performance out of the ADS5433. General design rules as the use of multilayer boards, single ground plane for both, analog and digital ADC ground connections and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock should also be isolated from other signals, especially on applications where low jitter is required, as high IF sampling.

Besides performance oriented rules, special care has to be taken when considering the heat dissipation out of the device. The thermal heat sink (octagonal, with 2,5 mm on each side) should be soldered to the board, and provision for more than 16 ground vias should be made. The thermal package information describes the T_{JA} values obtained on the different configurations.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS5433IPJY	NRND	QFP	PJY	52	160	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
ADS5433IPJYG3	NRND	QFP	PJY	52	160	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
ADS5433IPJYR	NRND	QFP	PJY	52	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
ADS5433IPJYRG3	NRND	QFP	PJY	52	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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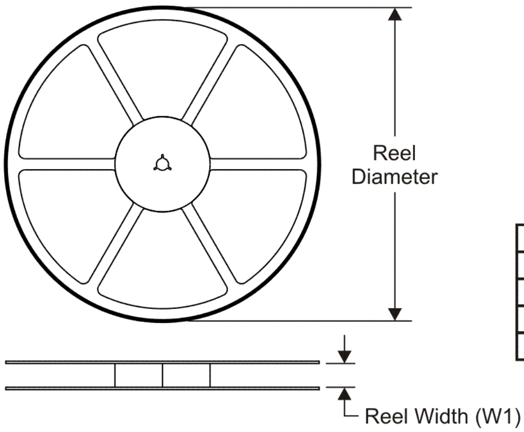
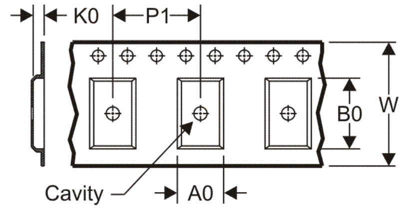
TAPE AND REEL INFORMATION

REEL DIMENSIONS

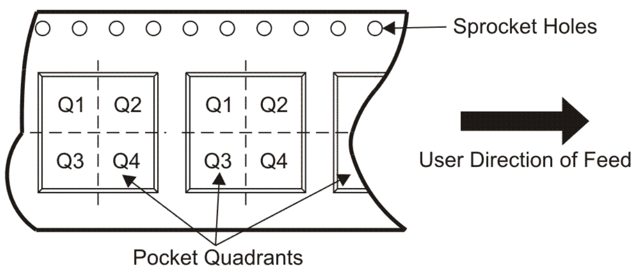


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

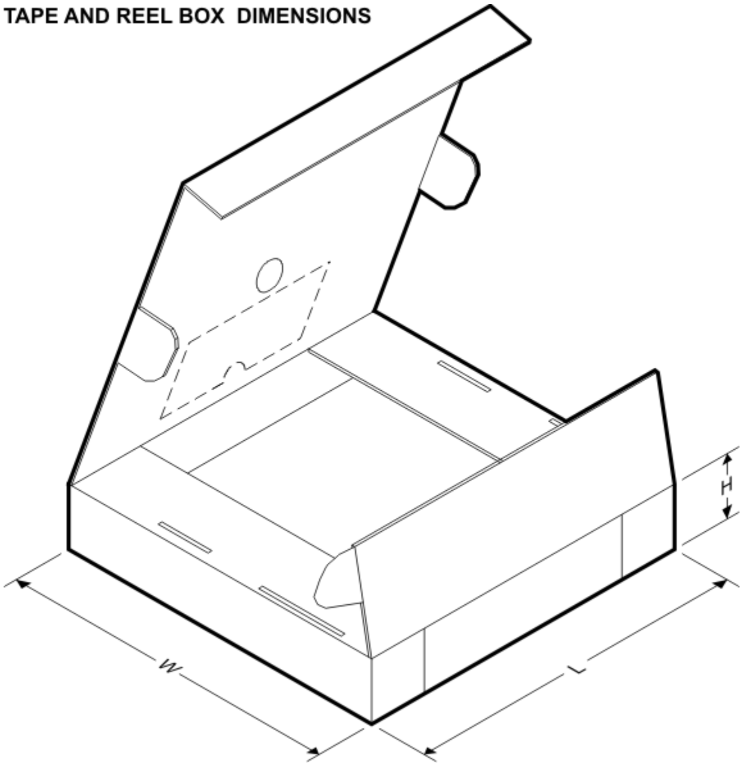
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5433IPJYR	QFP	PJY	52	1000	330.0	24.4	12.35	12.35	2.2	16.0	24.0	Q2

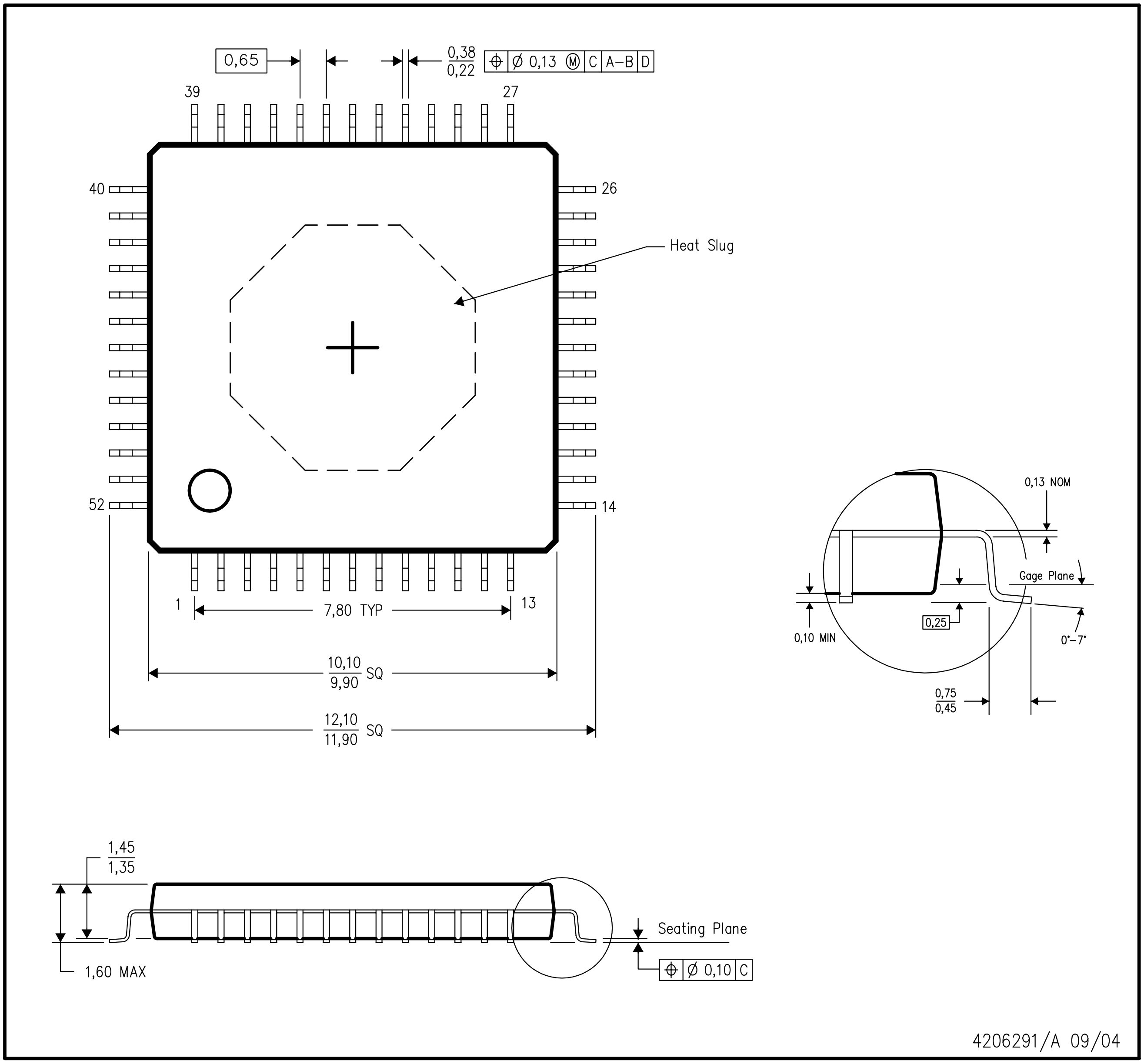
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5433IPJYR	QFP	PJY	52	1000	333.2	345.9	31.8

PJY (S-PQFP-G52) PLASTIC QUAD FLATPACK



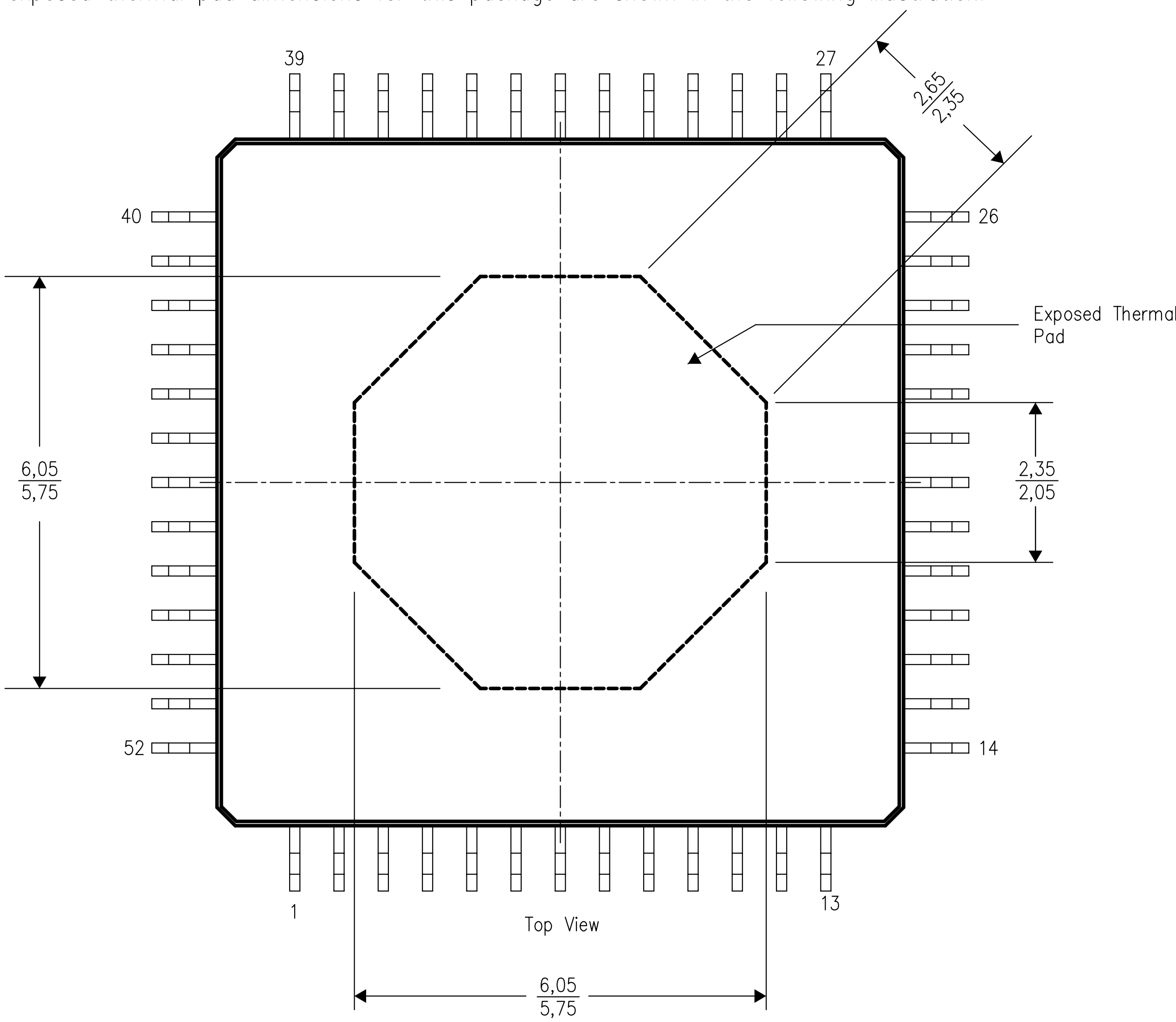
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com.

THERMAL INFORMATION

This PowerQuad 4™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerQuad 4 package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions