10-/8-BIT, 3-MSPS, MICRO-POWER, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **3-MHz Sample Rate Serial Device**
- **10-Bit Resolution – ADS7884**
- **8-Bit Resolution – ADS7885**
- **Zero Latency**
- **48-MHz Serial Interface**
- **Supply Range: 2.7 V to 5.5 V**
- **Low Power Dissipation:**
  - **6.8 mW at 3-V V_{DD}, 2.5 MSPS**
  - **15 mw at 5-V V_{DD}, 3 MSPS**
- **±0.3 LSB INL, ±0.3 LSB DNL – ADS7884**
- **±0.15 LSB INL, ±0.1 LSB DNL – ADS7885**
- **61.7 dB SINAD, –81 dB THD – ADS7884**
- **49.8 dB SINAD, –68 dB THD – ADS7885**
- **Unipolar Input Range: 0 V to V_{DD}**
- **Powerdown Current: 1 µA**
- **Wide Input Bandwidth: 30 MHz at 3 dB**
- **6-Pin SOT23 Package**

APPLICATIONS

- **Base Band Converters in Radio Communication**
- **Motor Current/Bus Voltage Sensors in Digital Drives**
- **Optical Networking (DWDM, MEMS Based Switching)**
- **Optical Sensors**
- **Battery Powered Systems**
- **Medical Instrumentations**
- **High-Speed Data Acquisition Systems**
- **High-Speed Closed-Loop Systems**

DESCRIPTION

The ADS7884 is a 10-bit, 3-MSPS analog-to-digital converter (ADC), and the ADS7885 is a 8-bit, 3-MSPS ADC. The devices include a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in each device is controlled by the $\overline{CS}$ and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output.

The devices operate from a wide supply range from 2.7 V to 5.5 V. The low power consumption of the devices make them suitable for battery-powered applications. The devices also include a power saving powerdown feature for when the devices are operated at lower conversion speeds.

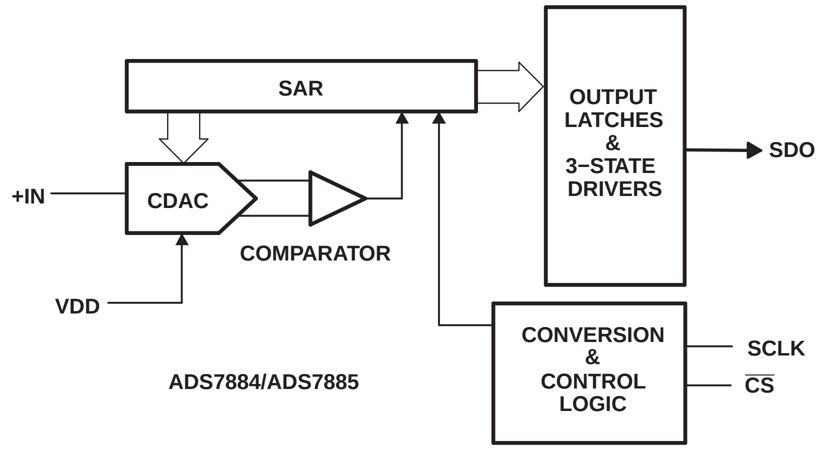
The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.5 V when device supply is 2.7 V. This feature is useful when digital signals are coming from other circuit with different supply levels. Also this relaxes restriction on power up sequencing.

The ADS7884 and ADS7885 are available in a 6-pin SOT23 package and are specified for operation from –40°C to 125°C.

Micro-Power Miniature SAR Converter Family

BIT	< 300 KSPS	300 KSPS – 1.25 MSPS	3 MSPS
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})	—
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})	ADS7884 (2.7 V_{DD} to 5.5 V_{DD})
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})	ADS7885 (2.7 V_{DD} to 5.5 V_{DD})

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



PACKAGE/ORDERING INFORMATION(1)

DEVICE	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS7884	±0.8	±0.8	10	6-Pin SOT23	DBV	–40°C to 125°C	7884	ADS7884SDBVT	Tape and reel 250
							7884	ADS7884SDBVR	Tape and reel 3000
ADS7885	±0.4	±0.4	8	6-Pin SOT23	DBV	–40°C to 125°C	7885	ADS7885SDBVT	Tape and reel 250
							7885	ADS7885SDBVR	Tape and reel 3000

(1) For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
+IN to AGND		–0.3 V to $+V_{DD}$ +0.3 V
$+V_{DD}$ to AGND		–0.3 V to 7.0 V
Digital input voltage to GND		–0.3V to (7.0 V)
Digital output to GND		–0.3 V to ($+V_{DD}$ + 0.3 V)
Operating temperature range		–40°C to 125°C
Storage temperature range		–65°C to 150°C
Junction temperature (T_J Max)		150°C
Power dissipation, SOT23 package		(T_J Max–T_A)/θ_{JA}
Thermal impedance, θ_{JA}	SOT23	295.2°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ADS7884 SPECIFICATIONS

+V_{DD} = 2.7 V to 5.5 V, T_A = –40°C to 125°C, f_{sample} = 2.5 MSPS for V_{DD} = 2.7 V to 3.6 V, f_{sample} = 3 MSPS for V_{DD} = 3.6 V to 5.5 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span(1)		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.20		V_{DD}+0.20	V
C_i	Input capacitance(2)			27		pF
I_{llkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			10		Bits
	No missing codes		10			Bits
INL	Integral nonlinearity		–0.8	±0.3	0.8	LSB(3)
DNL	Differential nonlinearity		–0.8	±0.3	0.8	LSB
E_O	Offset error(4)(5)(6)		–1	±0.2	1	LSB
E_G	Gain error(5)		–1	±0.2	1	LSB
SAMPLING DYNAMICS						
	Conversion time	48-MHz SCLK, V_{DD} = 5 V	224	240		ns
	Acquisition time			93.3		ns
	Maximum throughput rate	48-MHz SCLK, V_{DD} = 5 V			3	MHz
	Aperture delay			10		ns
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion(7)	100 kHz		–81		dB
SINAD	Signal-to-noise and distortion	100 kHz	60	61.7		dB
SFDR	Spurious free dynamic range	100 kHz		81		dB
	Full power bandwidth	At –3 dB	30			MHz
DIGITAL INPUT/OUTPUT						
Logic family — CMOS						
V_{IH}	High-level input voltage	V_{DD} = 2.7 V to 3.6 V	1.5		5.5	V
		V_{DD} = 3.6 V to 5.5 V	2.2		5.5	
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	At I_{source} = 200 µA	V_{DD}–0.2			V
V_{OL}	Low-level output voltage	At I_{sink} = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS						
+V_{DD}	Supply voltage		2.7	3.3	5.5	V
	Supply current (normal mode)	At V_{DD} = 3.0 V, 2.5-MSPS throughput		2.25	3	mA
		At V_{DD} = 3.0 V, static state		1.8		
		At V_{DD} = 5.0 V, 3-MSPS throughput		3	4	
		At V_{DD} = 5.0 V, static state		2		
	Power down state supply current	SCLK off			1	µA
		SCLK on (48 MHz)		90	200	
	Power dissipation	V_{DD} = 5 V, 3 MSPS		15	20	mW
		V_{DD} = 3 V, 2.5 MSPS		6.8		

(1) Ideal input span; does not include gain or offset error.
(2) Refer to Figure 43 for details on sampling circuit
(3) LSB means least significant bit
(4) Measured relative to an ideal full-scale input
(5) Offset error and gain error ensured by characterization.
(6) First transition of 000H to 001H at ($V_{ref}/2^{10}$)
(7) Calculated on the first nine harmonics of the input frequency

ADS7884 SPECIFICATIONS (continued)

$+V_{DD}$ = 2.7 V to 5.5 V, T_A = –40°C to 125°C, f_{sample} = 2.5 MSPS for V_{DD} = 2.7 V to 3.6 V, f_{sample} = 3 MSPS for V_{DD} = 3.6 V to 5.5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation in static state	V_{DD} = 5 V		10		mW
	V_{DD} = 3 V		5.4		
Powerdown time				0.1	µs
Powerup time				0.8	µs
TEMPERATURE RANGE					
Specified performance		–40		125	°C

ADS7885 SPECIFICATIONS

+V_{DD} = 2.7 V to 5.5 V, T_A = –40°C to 125°C, f_{sample} = 2.5 MSPS for V_{DD} = 2.7 V to 3.6 V, f_{sample} = 3 MSPS for V_{DD} = 3.6 V to 5.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span (1)		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.20		V_{DD}+0.20	V
C_i	Input capacitance (2)			27		pF
I_{lkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			8		Bits
	No missing codes		8			Bits
INL	Integral nonlinearity		–0.4	±0.15	0.4	LSB (3)
DNL	Differential nonlinearity		–0.4	±0.1	0.4	LSB
E_O	Offset error (4)(5)(6)		–0.4	±0.1	0.4	LSB
E_G	Gain error (5)		–0.5	±0.1	0.5	LSB
SAMPLING DYNAMICS						
	Conversion time	48-MHz SCLK, V_{DD} = 5 V	182	198		ns
	Acquisition time	3 MSPS mode		135		ns
	Maximum throughput rate	48-MHz SCLK, V_{DD} = 5 V			3	MHz
	Aperture delay			10		ns
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion (7)	100 kHz		–68		dB
SINAD	Signal-to-noise and distortion	100 kHz	49	49.8		dB
SFDR	Spurious free dynamic range	100 kHz		74		dB
	Full power bandwidth	At –3 dB	30			MHz
DIGITAL INPUT/OUTPUT						
Logic family — CMOS						
V_{IH}	High-level input voltage	V_{DD} = 2.7 V to 3.6 V	1.5		5.5	V
		V_{DD} = 3.6 V to 5.5 V	2.2		5.5	
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	At I_{source} = 200 µA	V_{DD}–0.2			V
V_{OL}	Low-level output voltage	At I_{sink} = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS						
+V_{DD}	Supply voltage		2.7	3.3	5.5	V
	Supply current (normal mode)	At V_{DD} = 3.0 V, 2.5-MSPS throughput		2.25	3	mA
		At V_{DD} = 3.0 V, static state		1.8		
		At V_{DD} = 5.0 V, 3-MSPS throughput		3	4	
		At V_{DD} = 5.0 V, static state		2		
	Power down state supply current	SCLK off			1	µA
		SCLK on (48 MHz)		90	200	
	Power dissipation	V_{DD} = 5 V, 3 MSPS		15	20	mW
		V_{DD} = 3 V, 2.5 MSPS		6.8		

(1) Ideal input span; does not include gain or offset error.
(2) Refer to Figure 43 for details on sampling circuit
(3) LSB means least significant bit
(4) Measured relative to an ideal full-scale input
(5) Offset error and gain error ensured by characterization.
(6) First transition of 000H to 001H at ($V_{ref}/2^8$)
(7) Calculated on the first nine harmonics of the input frequency

ADS7885 SPECIFICATIONS (continued)

+V_{DD} = 2.7 V to 5.5 V, T_A = –40°C to 125°C, f_{sample} = 2.5 MSPS for V_{DD} = 2.7 V to 3.6 V, f_{sample} = 3 MSPS for V_{DD} = 3.6 V to 5.5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation in static state	V_{DD} = 5 V		10		mW
	V_{DD} = 3 V		5.4		
Powerdown time				0.1	µs
Powerup time				0.8	µs
TEMPERATURE RANGE					
Specified performance		–40		125	°C

TIMING REQUIREMENTS (see Figure 1)

All specifications typical at T_A = –40°C to 125°C, V_{DD} = 2.7 V to 5.5 V, unless otherwise specified.

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	ADS7884	V_{DD} = 3 V			11.5 × t_{SCLK}	ns
			V_{DD} = 5 V			11.5 × t_{SCLK}	
		ADS7885	V_{DD} = 3 V			9.5 × t_{SCLK}	
			V_{DD} = 5 V			9.5 × t_{SCLK}	
t_{acq}	Aquisition time		V_{DD} = 3 V	62.5			ns
			V_{DD} = 5 V	52			
t_q	Minimum quiet time needed from bus 3-state to start of next conversion		V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d1}	Delay time, $\overline{CS}$ low to first data (0) out		V_{DD} = 3 V		9	15	ns
			V_{DD} = 5 V		8	11	
t_{su1}	Setup time, $\overline{CS}$ low to SCLK low		V_{DD} = 3 V	7			ns
			V_{DD} = 5 V	5			
t_{d2}	Delay time, SCLK falling to SDO		V_{DD} = 3 V		11	20	ns
			V_{DD} = 5 V		9	12	
t_{h1}	Hold time, SCLK falling to data valid(2)		V_{DD} < 3 V	5.5			ns
			V_{DD} > 5 V	4			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state		V_{DD} = 3 V		9	15	ns
			V_{DD} = 5 V		8	11	
t_{w1}	Pulse duration, $\overline{CS}$		V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d4}	Delay time, $\overline{CS}$ high to SDO 3-state,		V_{DD} = 3 V		9	15	ns
			V_{DD} = 5 V		8	11	
t_{wH}	Pulse duration, SCLK high		V_{DD} = 3 V	0.45 × t_{SCLK}			ns
			V_{DD} = 5 V	0.45 × t_{SCLK}			
t_{wL}	Pulse duration, SCLK low		V_{DD} = 3 V	0.45 × t_{SCLK}			ns
			V_{DD} = 5 V	0.45 × t_{SCLK}			
	Frequency, SCLK		V_{DD} = 3 V			40	MHz
			V_{DD} = 5 V			48	
t_{d5}	Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use min spec not to accidently enter in powerdown) Figure 3		V_{DD} = 3 V	–2		4	ns
			V_{DD} = 5 V	–2		3	

(1) 3-V Specifications apply from 2.7 V to 3.6 V, and 5-V specifications apply from 4.5 V to 5.5 V.
(2) With 10-pf load.

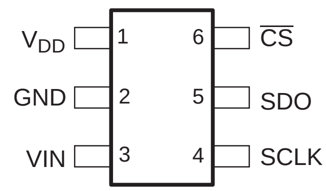
TIMING REQUIREMENTS (see Figure 1) (continued)

All specifications typical at T_A = –40°C to 125°C, V_{DD} = 2.7 V to 5.5 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_{d6}	Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in powerdown (use max spec not to accidently enter in powerdown) Figure 3	V_{DD} = 3 V	–2		4	ns
		V_{DD} = 5 V	–2		3	

DEVICE INFORMATION

SOT23 PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	–	Power supply input also acts like a reference voltage to ADC.
GND	2	–	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	I	Analog signal input
SCLK	4	I	Serial clock
SDO	5	O	Serial data out
$\overline{CS}$	6	I	Chip select signal, active low

ADS7884 NORMAL OPERATION

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as **a** in Figure 1. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 2 leading zeros, followed by 10-bit data in MSB first format and padded by 4 lagging zeros.

The falling edge of $\overline{CS}$ clocks out the first zero, and a second zero is clocked out on FIRST falling edge of the clock. Data is in MSB first format with the MSB being clocked out on the 2nd falling edge. Data is padded with four lagging zeros as shown in Figure 1. The conversion ends on the first rising edge of SCLK after the 11th falling edge. At this point the device enters the acquisition phase. This point is indicated by **b** in Figure 1.

Figure 1 shows device data is read in a sixteen clock frame. However, $\overline{CS}$ can be asserted (pulled high) any time after 11 clocks have elapsed. SDO goes to 3-state with the $\overline{CS}$ high level. The next conversion should not be started (by pulling $\overline{CS}$ low) until the end of the quiet sampling time (t_q) after SDO goes to 3-state or until the minimum acquisition time (t_{acq}) has elapsed. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to the Powerdown Mode section for more details.) $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on powerup sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the Specifications table.

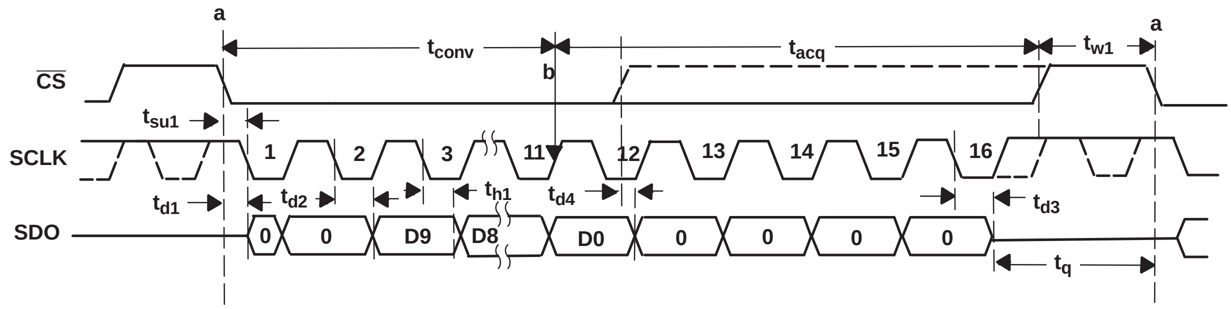


Figure 1. ADS7884 Interface Timing Diagram

ADS7885 NORMAL OPERATION

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as **a** in Figure 2. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 2 leading zeros, followed by 8-bit data in MSB first format and padded by 6 lagging zeros.

The falling edge of $\overline{CS}$ clocks out the first zero, and a second zero is clocked out on FIRST falling edge of the clock. Data is in MSB first format with the MSB being clocked out on the 3rd falling edge. Data is padded with six lagging zeros as shown in Figure 2. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the first rising edge of SCLK after the 9th falling edge. At this point the device enters the acquisition phase. This point is indicated by **b** in Figure 2.

Figure 2 shows device data is read in a sixteen clock frame. However, $\overline{CS}$ can be asserted (pulled high) any time after 9 clocks have elapsed (after the 10th falling edge of SCLK). SDO goes to 3-state with the $\overline{CS}$ high level. The next conversion should not be started (by pulling $\overline{CS}$ low) until the end of the quiet sampling time (t_q) after SDO goes to 3-state or until the minimum acquisition time (t_{acq}) has elapsed. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to the Powerdown Mode section for more details.) $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on powerup sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the Specifications section.

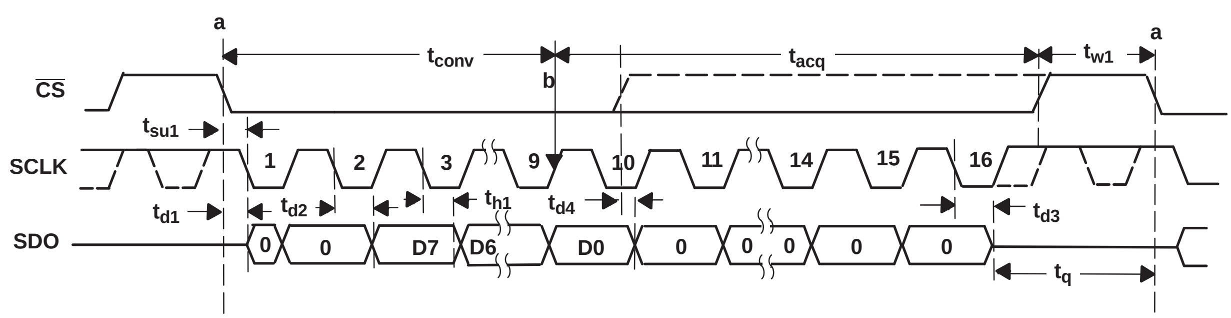


Figure 2. ADS7885 Interface Timing Diagram

POWER DOWN MODE

The device enters powerdown mode if $\overline{CS}$ goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this powerdown condition as shown in Figure 3.

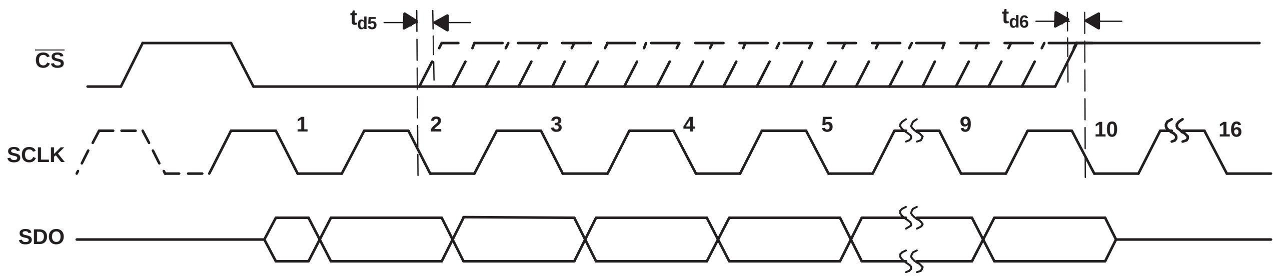


Figure 3. Entering Power Down Mode

A dummy cycle with $\overline{CS}$ low for more than 10 SCLK falling edges brings the device out of powerdown mode. For the device to come to the fully powered up condition it takes 0.8 µs. $\overline{CS}$ can be pulled high any time after the 10th falling edge as shown in Figure 4. Note that the powerup time of 0.8 µsec is more than a single conversion cycle at 3 MSPS speed. This means the device requires three dummy conversion frames at 3 MSPS speed or one elongated dummy conversion frame. The data during dummy conversion frames is invalid.

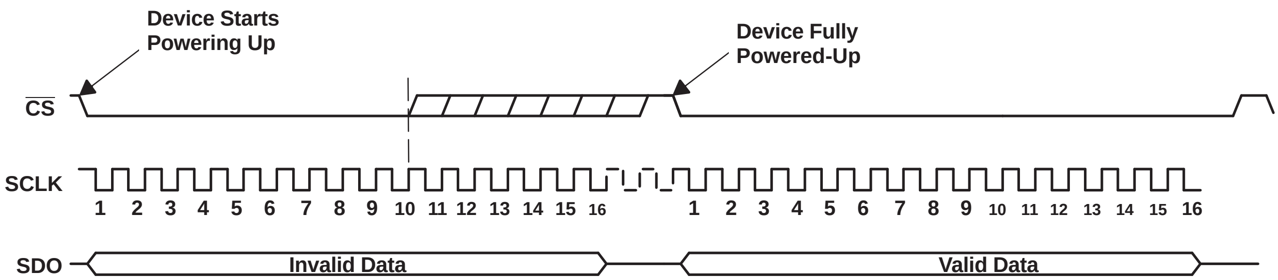


Figure 4. Exiting Power Down Mode

TYPICAL CHARACTERISTICS ADS7884

SUPPLY CURRENT vs SUPPLY VOLTAGE

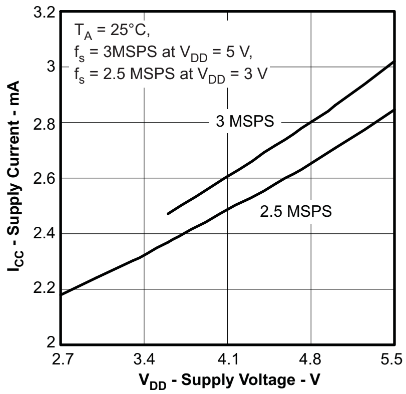


Figure 5.

SUPPLY CURRENT vs SCLK FREQUENCY

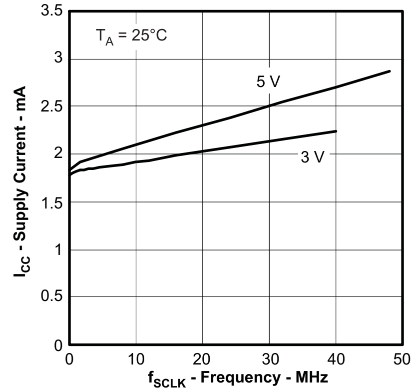


Figure 6.

SUPPLY CURRENT vs SAMPLE RATE

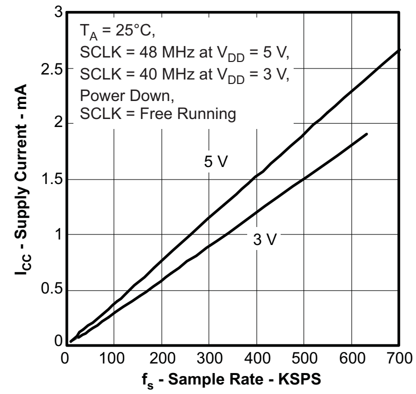


Figure 7.

INPUT LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

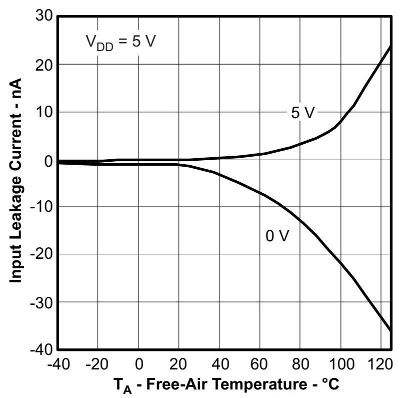


Figure 8.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

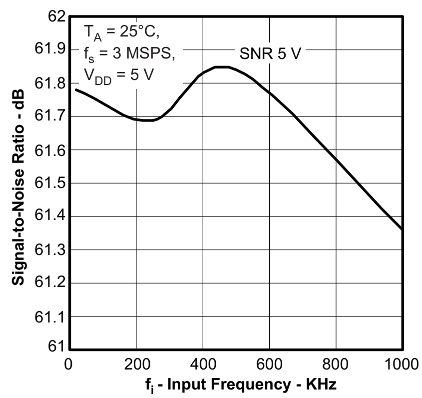


Figure 9.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

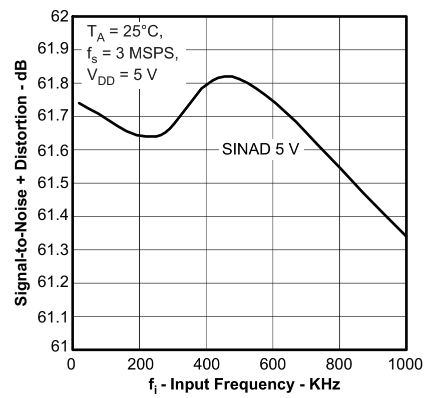


Figure 10.

SIGNAL-TO-NOISE + DISTORTION vs SUPPLY VOLTAGE

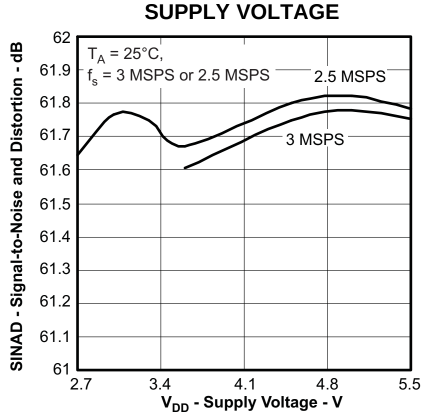


Figure 11.

SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE

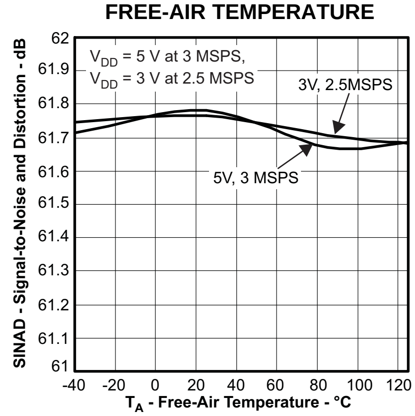


Figure 12.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

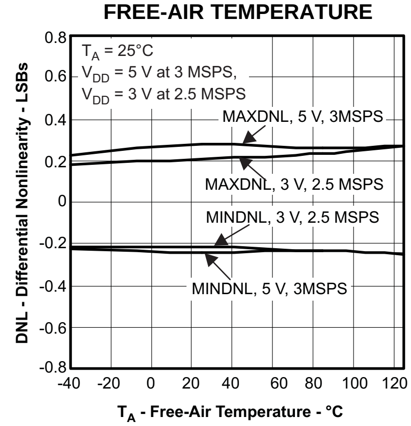


Figure 13.

TYPICAL CHARACTERISTICS ADS7884 (continued)

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

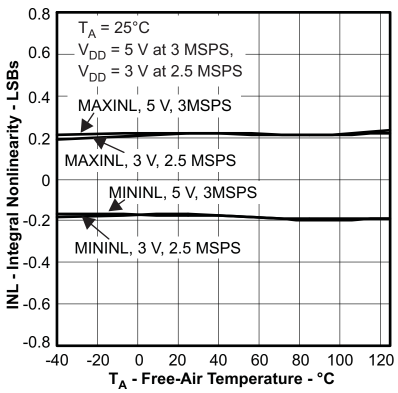


Figure 14.

DIFFERENTIAL NONLINEARITY vs SUPPLY VOLTAGE

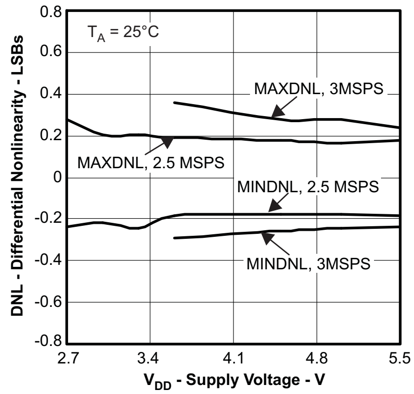


Figure 15.

INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE

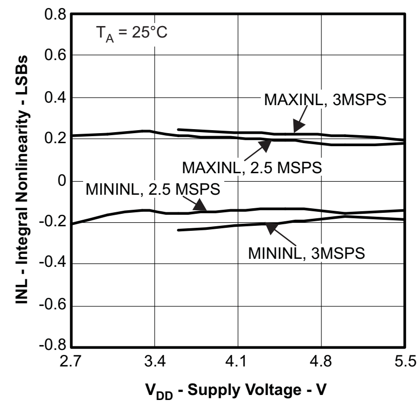


Figure 16.

OFFSET ERROR vs SUPPLY VOLTAGE

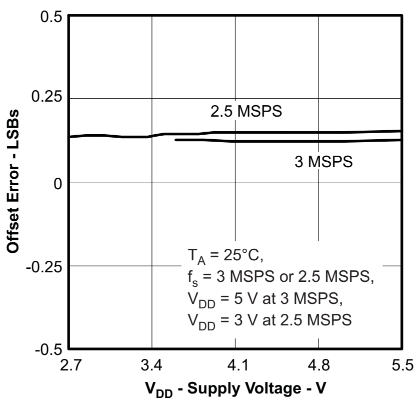


Figure 17.

OFFSET ERROR vs FREE-AIR TEMPERATURE

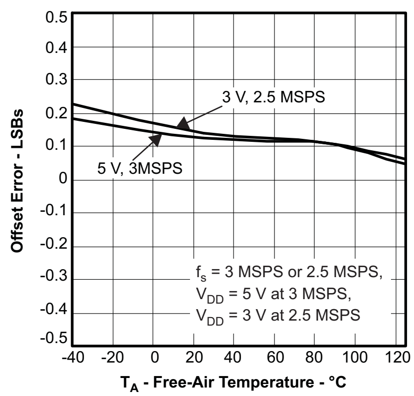


Figure 18.

GAIN ERROR vs SUPPLY VOLTAGE

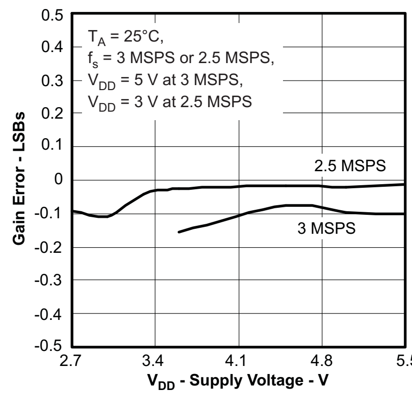


Figure 19.

GAIN ERROR vs FREE-AIR TEMPERATURE

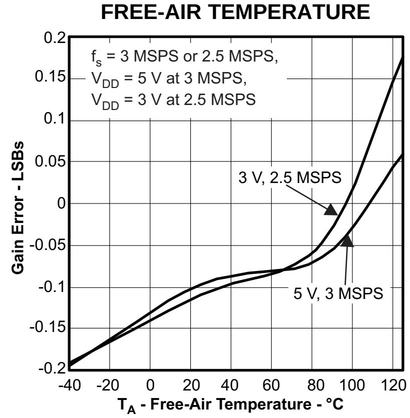


Figure 20.

TYPICAL CHARACTERISTICS ADS7884 (continued)

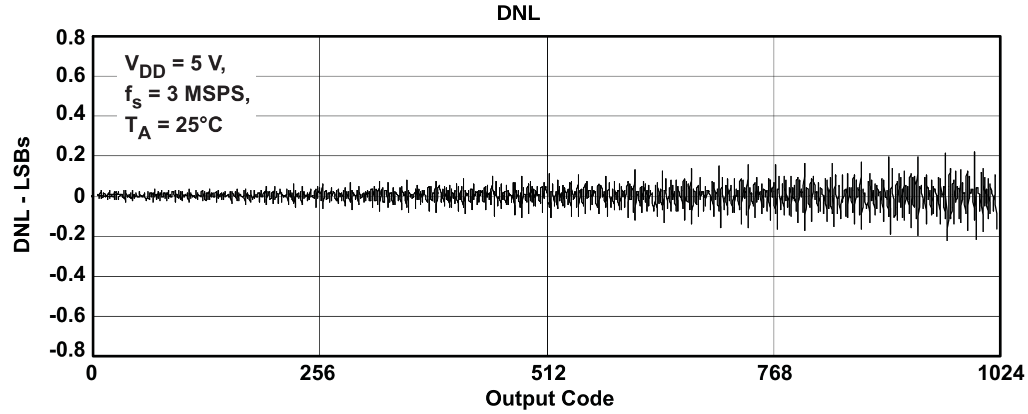


Figure 21.

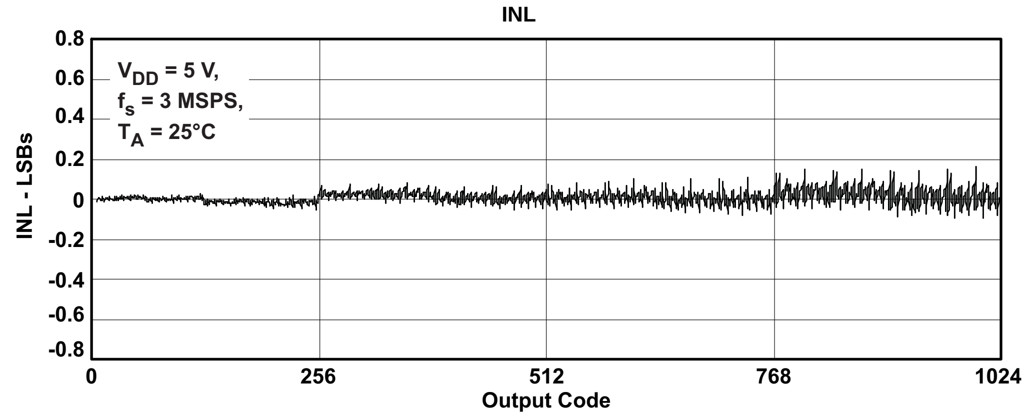


Figure 22.

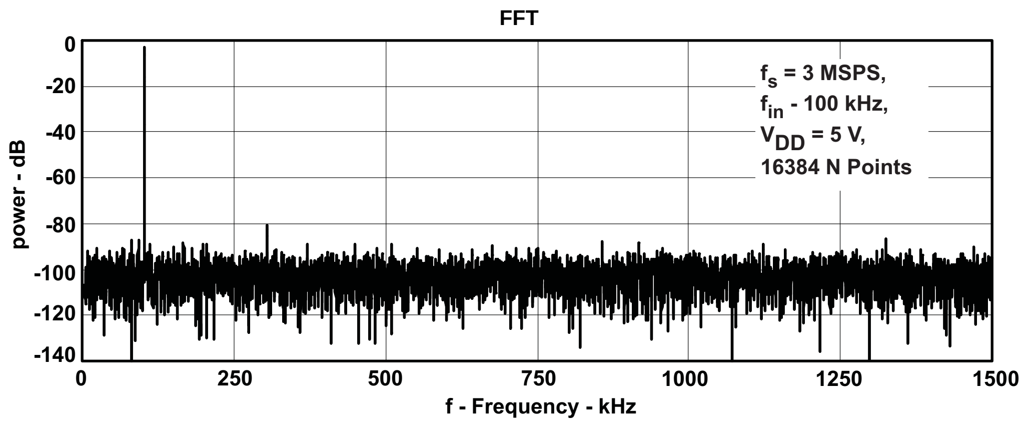


Figure 23.

TYPICAL CHARACTERISTICS ADS7885

SUPPLY CURRENT vs SUPPLY VOLTAGE

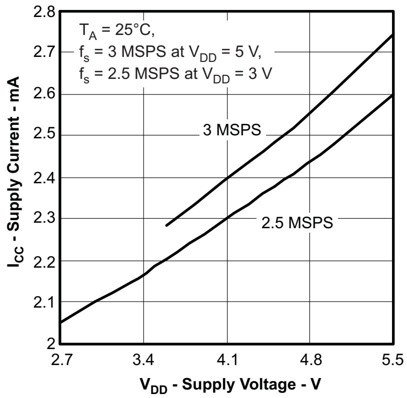


Figure 24.

SUPPLY CURRENT vs SCLK FREQUENCY

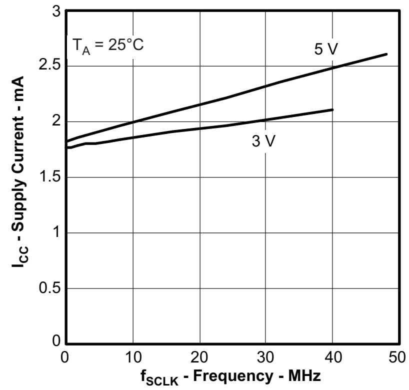


Figure 25.

SUPPLY CURRENT vs SAMPLE RATE

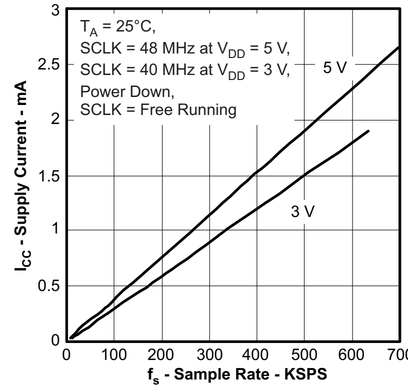


Figure 26.

INPUT LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

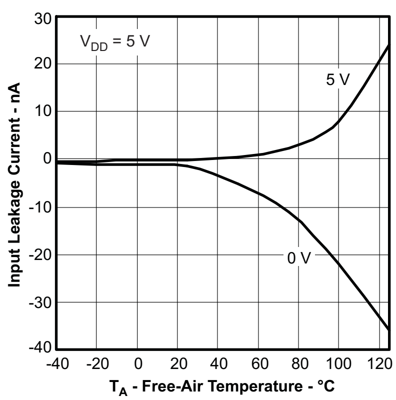


Figure 27.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

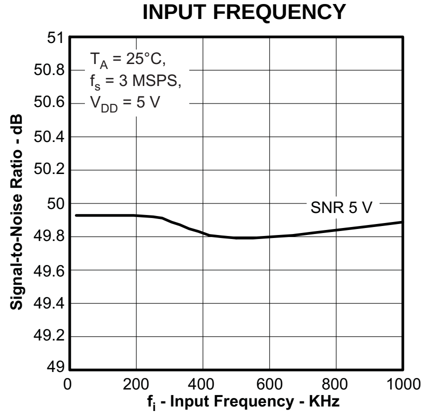


Figure 28.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

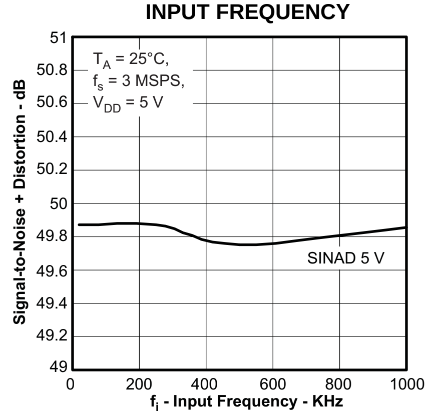


Figure 29.

SIGNAL-TO-NOISE + DISTORTION vs SUPPLY VOLTAGE

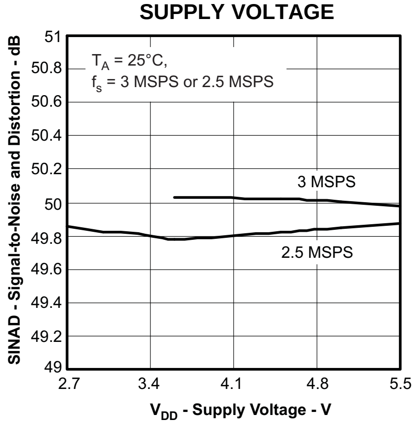


Figure 30.

SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE

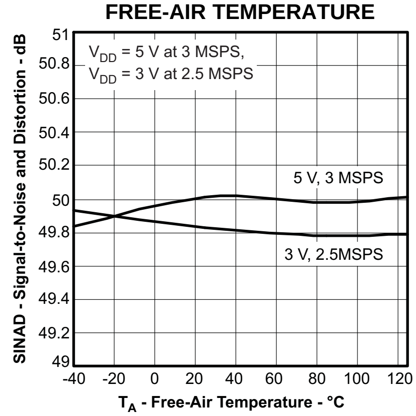


Figure 31.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

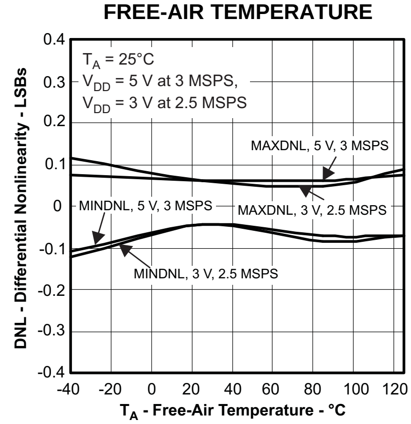


Figure 32.

TYPICAL CHARACTERISTICS ADS7885 (continued)

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

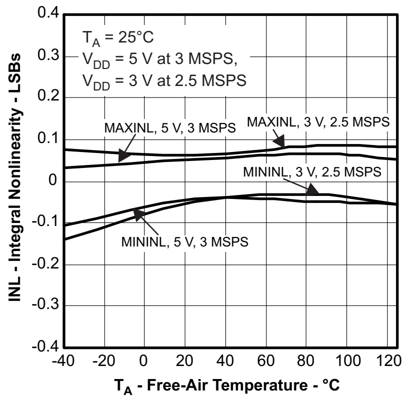


Figure 33.

DIFFERENTIAL NONLINEARITY vs SUPPLY VOLTAGE

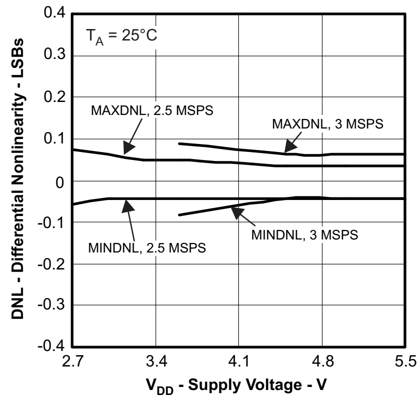


Figure 34.

INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE

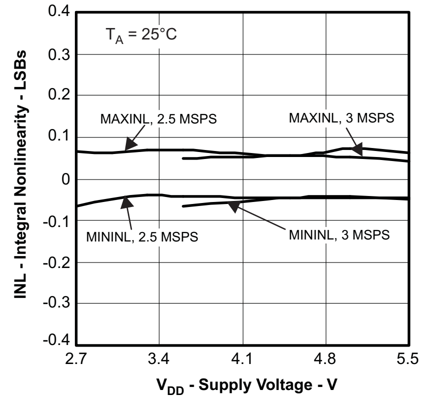


Figure 35.

OFFSET ERROR vs SUPPLY VOLTAGE

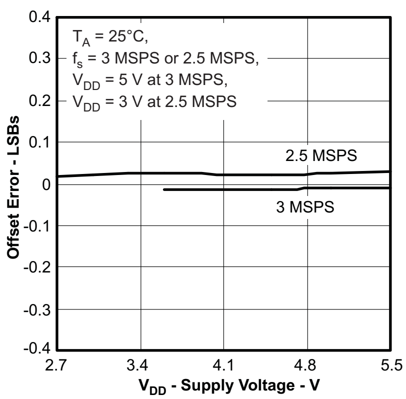


Figure 36.

OFFSET ERROR vs FREE-AIR TEMPERATURE

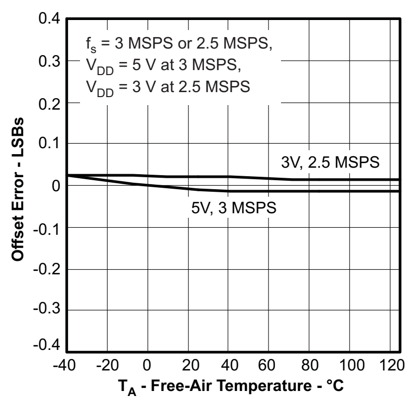


Figure 37.

GAIN ERROR vs SUPPLY VOLTAGE

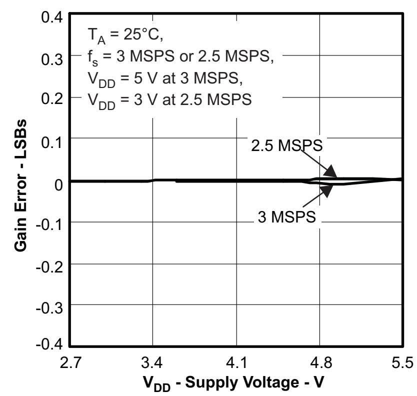


Figure 38.

GAIN ERROR vs FREE-AIR TEMPERATURE

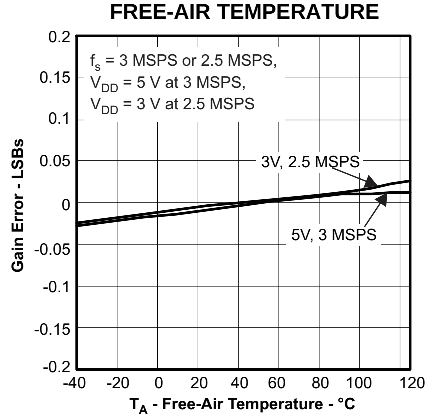


Figure 39.

TYPICAL CHARACTERISTICS ADS7885 (continued)

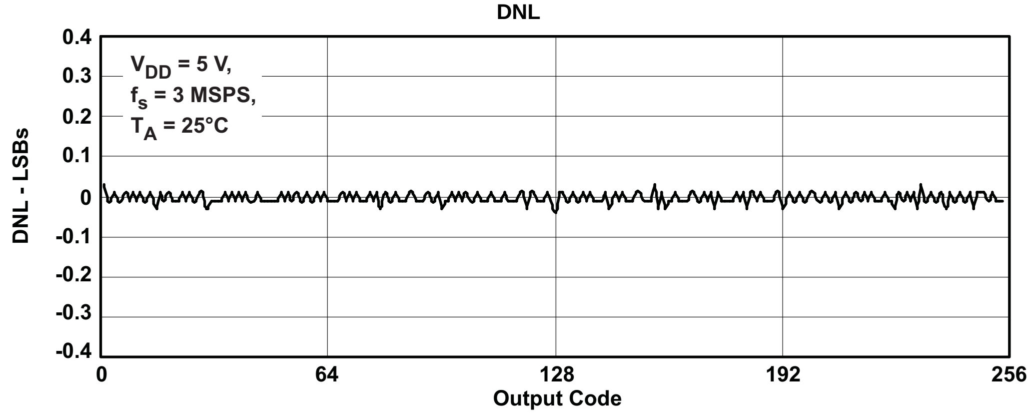


Figure 40.

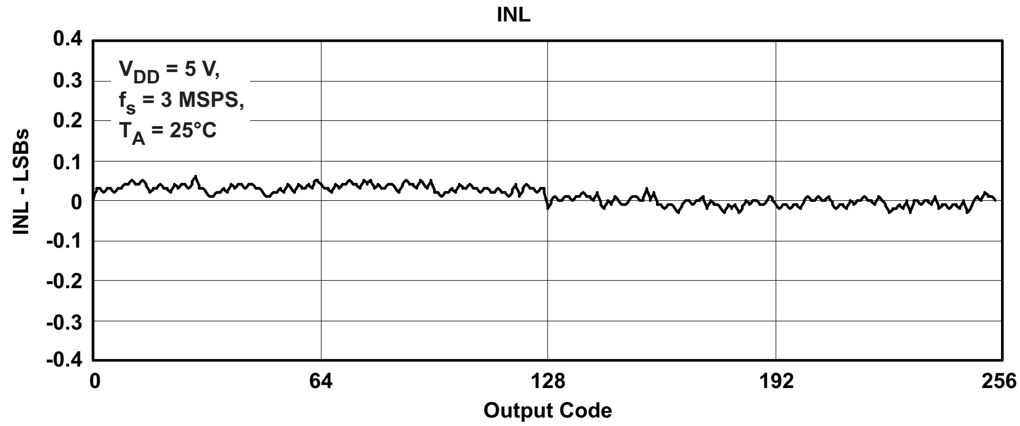


Figure 41.

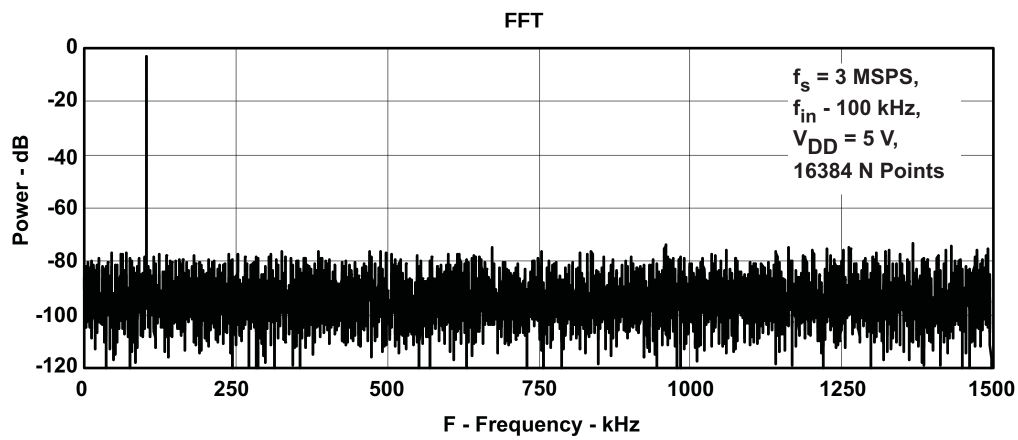


Figure 42.

APPLICATION INFORMATION

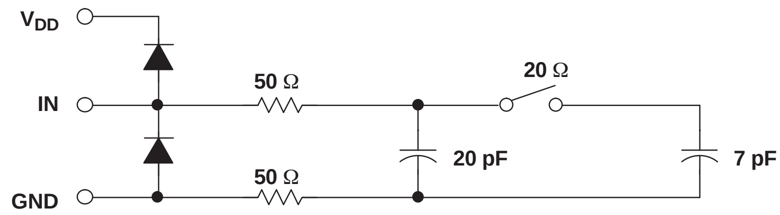


Figure 43. Typical Equivalent Sampling Circuit

Driving the VIN and V_{DD} Pins of the ADS7884 and ADS7885

The VIN input to the ADS7884 and ADS7885 should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7884 and ADS7885 A/D converters are derived from the supply voltage internally. The devices offer limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7884 and ADS7885 draw very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like REF3030 or REF3130. The ADS7884 and ADS7885 can operate off a wide range of supply voltages. The actual choice of the reference voltage generator would depend upon the system. Figure 45 shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer like the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the V_{DD} input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. Figure 46 shows one possible application circuit.

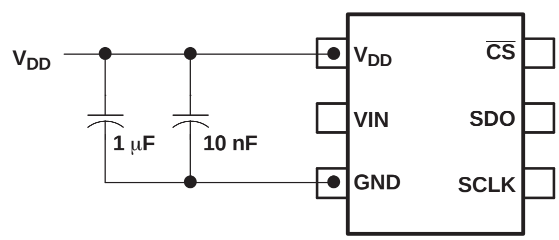


Figure 44. Supply/Reference Decoupling Capacitors

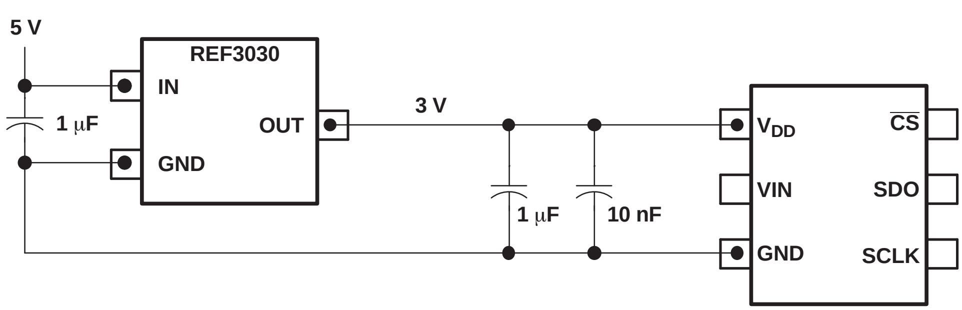


Figure 45. Using the REF3030 Reference

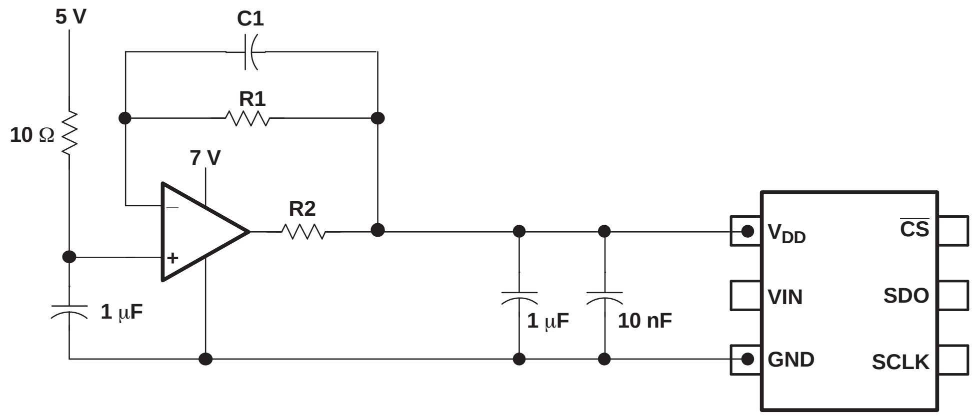


Figure 46. Buffering with the OPA735

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7884SDBVR	ACTIVE	SOT-23	DBV	6	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR		7884	Samples
ADS7884SDBVT	ACTIVE	SOT-23	DBV	6	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR		7884	Samples
ADS7885SDBVR	ACTIVE	SOT-23	DBV	6	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR		7885	Samples
ADS7885SDBVT	ACTIVE	SOT-23	DBV	6	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR		7885	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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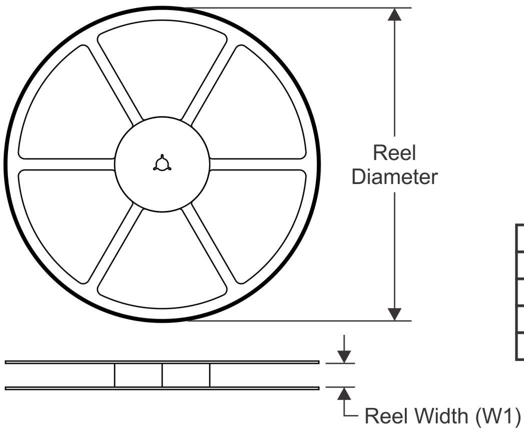
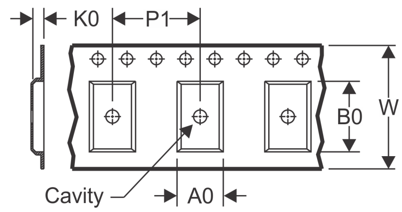
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

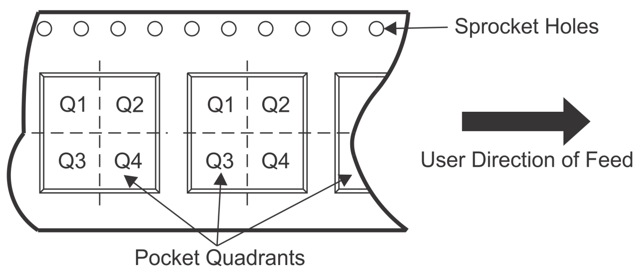


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

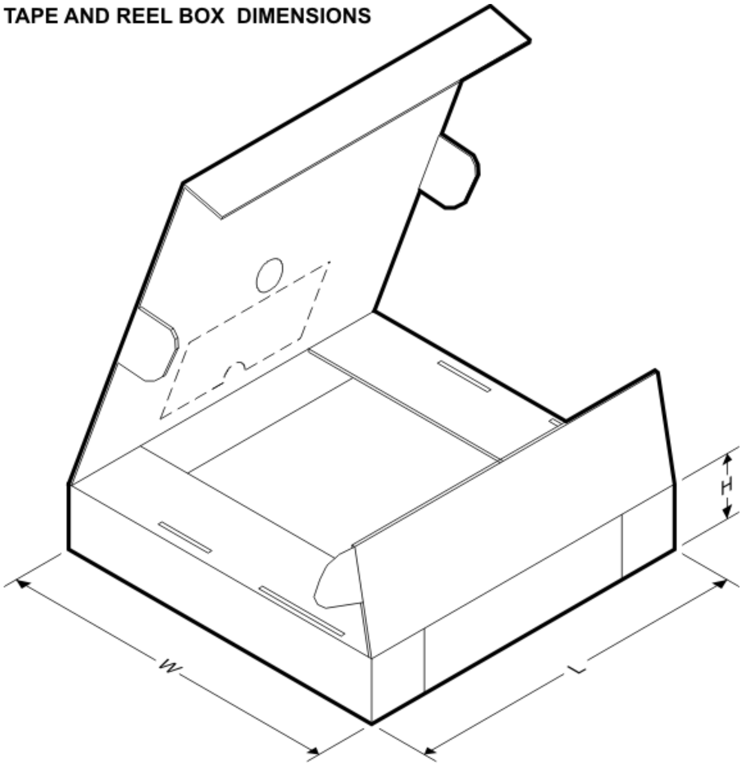
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7884SDBVR	SOT-23	DBV	6	3000	177.8	9.7	3.2	3.1	1.39	4.0	8.0	Q3
ADS7884SDBVT	SOT-23	DBV	6	250	177.8	9.7	3.2	3.1	1.39	4.0	8.0	Q3
ADS7885SDBVR	SOT-23	DBV	6	3000	177.8	9.7	3.2	3.1	1.39	4.0	8.0	Q3
ADS7885SDBVT	SOT-23	DBV	6	250	177.8	9.7	3.2	3.1	1.39	4.0	8.0	Q3

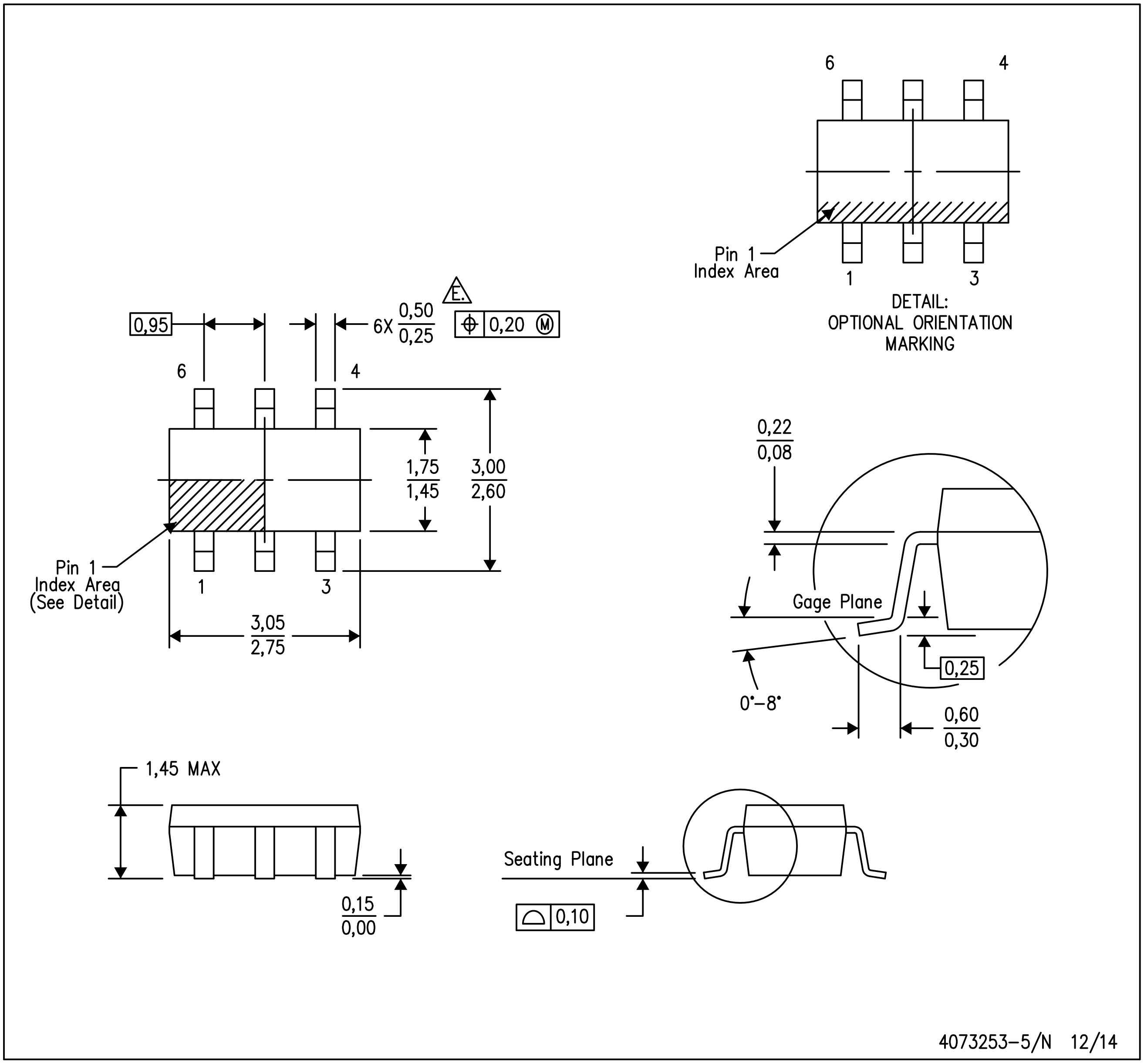
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

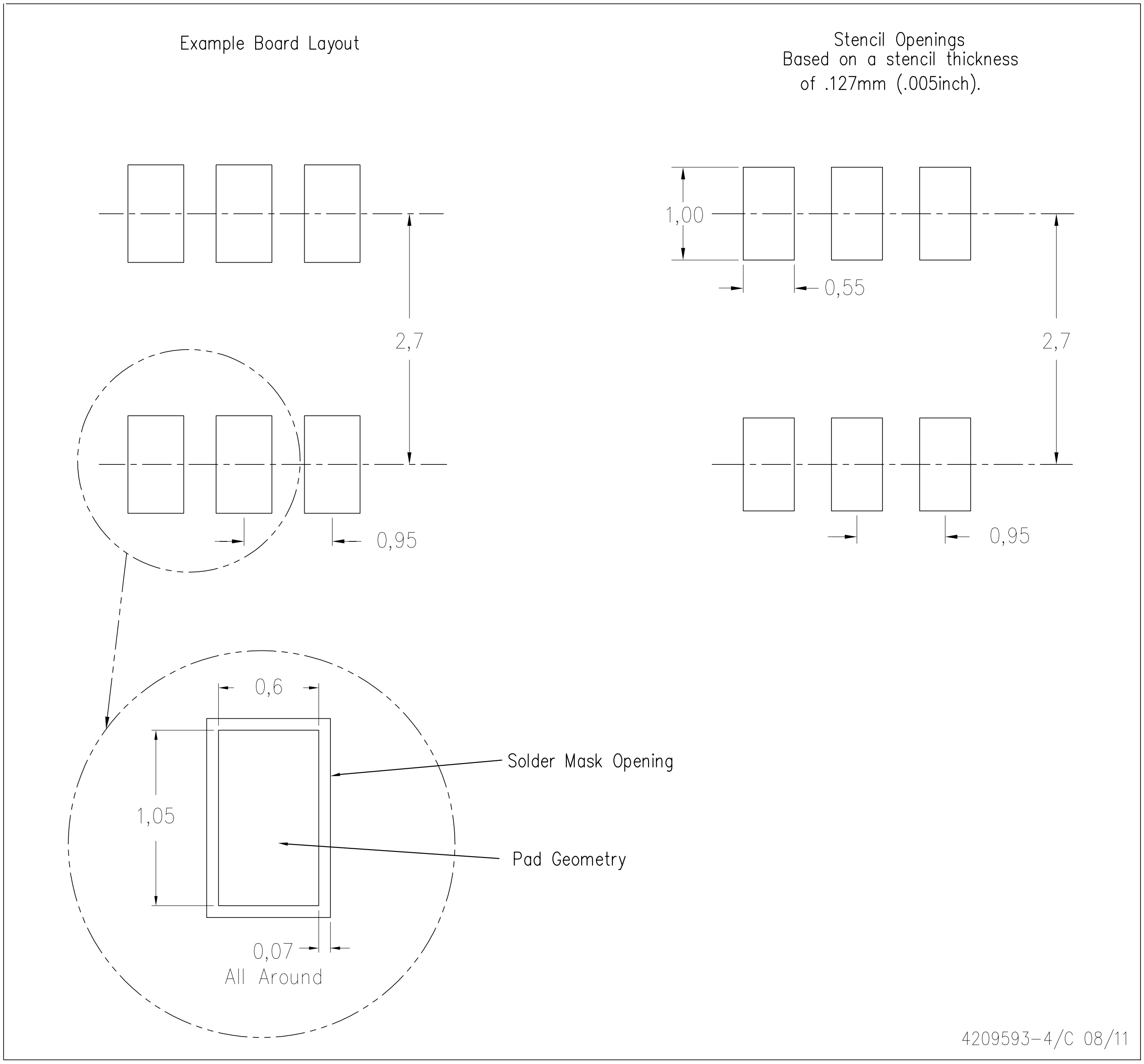
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7884SDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADS7884SDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
ADS7885SDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADS7885SDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.