TPS659037 User's Guide to Power AM572x and AM571x

This User's Guide can be used as a guide for integrating the TPS659037 power-management integrated circuit (PMIC) into a system using AM572x or AM571x.

1 Introduction

This user's guide can be used as a guide for connectivity between the TPS659037 PMIC and a processor. This guide describes the platform connections as well as the power-up, power-down, and sleep entry and exit sequences along with the OTP configurations. In addition, this user's guide describes the initialization software and advises how to get started with the TPS659037 PMIC. For more information on creating a board-compatible power solution for the AM572x and AM571x family of devices, refer to the *AM572x/AM571x Compatibility Guide* (SPRABX8). This user's guide does not provide details about the power resources, external components, or the functionality of the device. For such information, see the TPS659037 data sheet, *TPS659037 Power Management Unit (PMU) for Processor* (SLIS165).

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source.

2 Device Versions

Two different versions of the TPS659037 device are available and the OTP settings for each version are described in this document. Both versions of the device can be used to power the AM572x or AM571x processor. The OTP version can be read from the SW_REVISION register. In this user's guide, each device version is distinguished either by the part number or the SW_REVISION value which are both listed in Table 1.

Table 1. TPS659037 OTP Settings Differentiation

PART NUMBER	CONTENT OF SW_REVISION REGISTER
TPS6590376ZWSR	0x8A
TPS6590377ZWSR	0x8B

3 Platform Connection

Figure 1 shows the detailed connections between the processor and TPS6590376ZWSR. This configuration combines DSPEVE, GPU, and IVAHD domains of the processor to one PMIC supply SMPS45. The configuration allows selecting between 1.35-V output on SMPS3 supporting DDR3L and 1.5-V output supporting DDR3. If VIO_IN of the PMIC should be 3.3-V, it can be supplied by the switched 3.3-V rail enabled by REGEN1. If VIO_IN of the PMIC should be 1.8 V, it can be supplied by SMPS8.

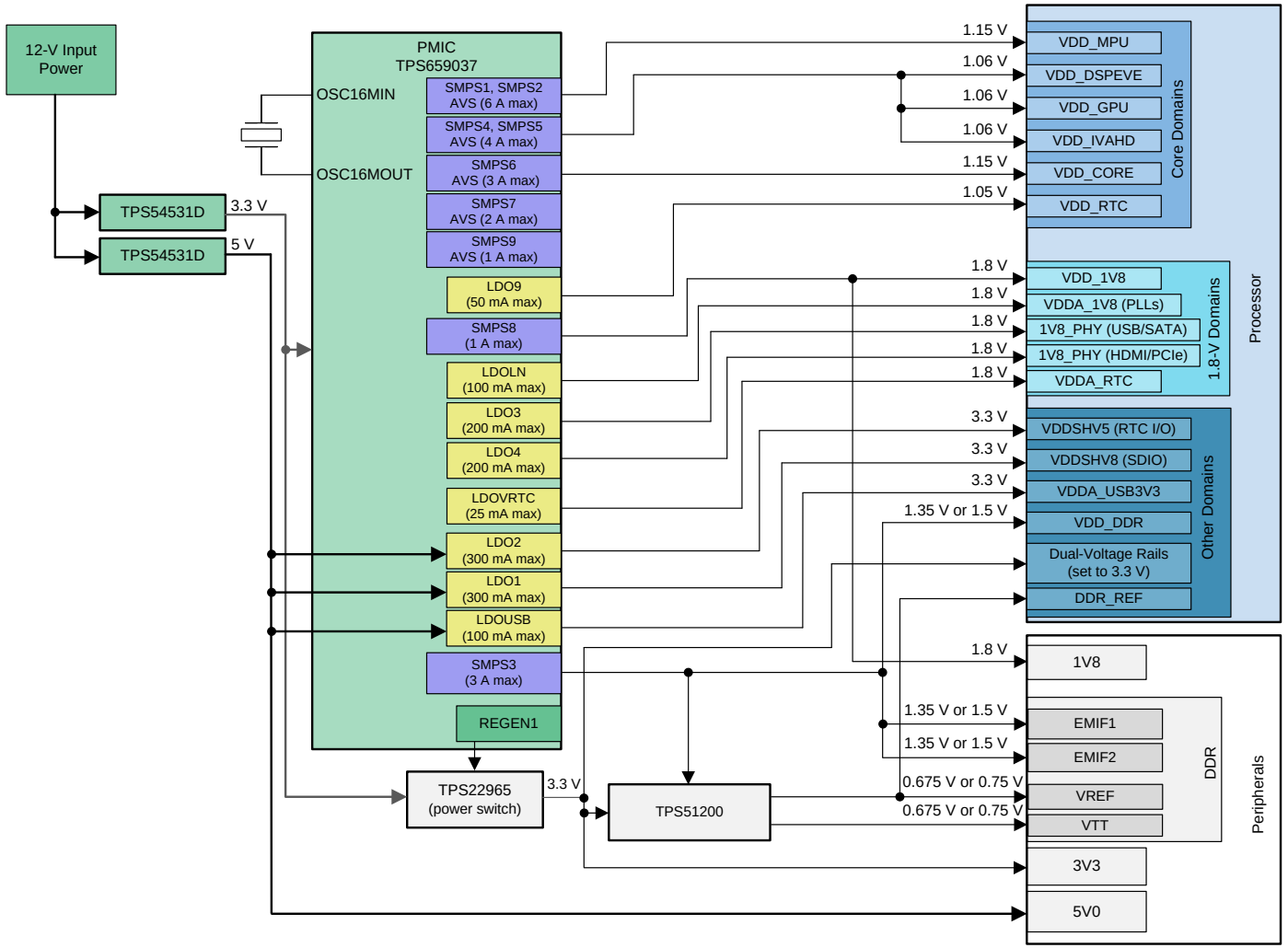

Figure 1. Processor Connection With TPS6590376ZWSR

Figure 2 shows the detailed connections between the processor and the TPS6590377ZWSR. This configuration uses an independent supply for each of the core rails. It also uses LDO2 for the 1.8-V I/O supply and SMPS9 for the 3.3-V I/O supply. The configuration allows selecting between 1.35-V output on SMPS3 supporting DDR3L and 1.5-V output supporting DDR3.

TPS6590377ZWSR allows two options to power VIO of the PMIC and processor at 3.3V, as shown by the dotted lines. If less than 1-A of current is required, SMPS9 can be used to power VIO. If more than 1-A of current is required, REGEN1 can be used to enable a load switch which will sequence an external 3.3V supply. In the case that VIO_IN of the PMIC should be 1.8V, it can be supplied by LDO2.

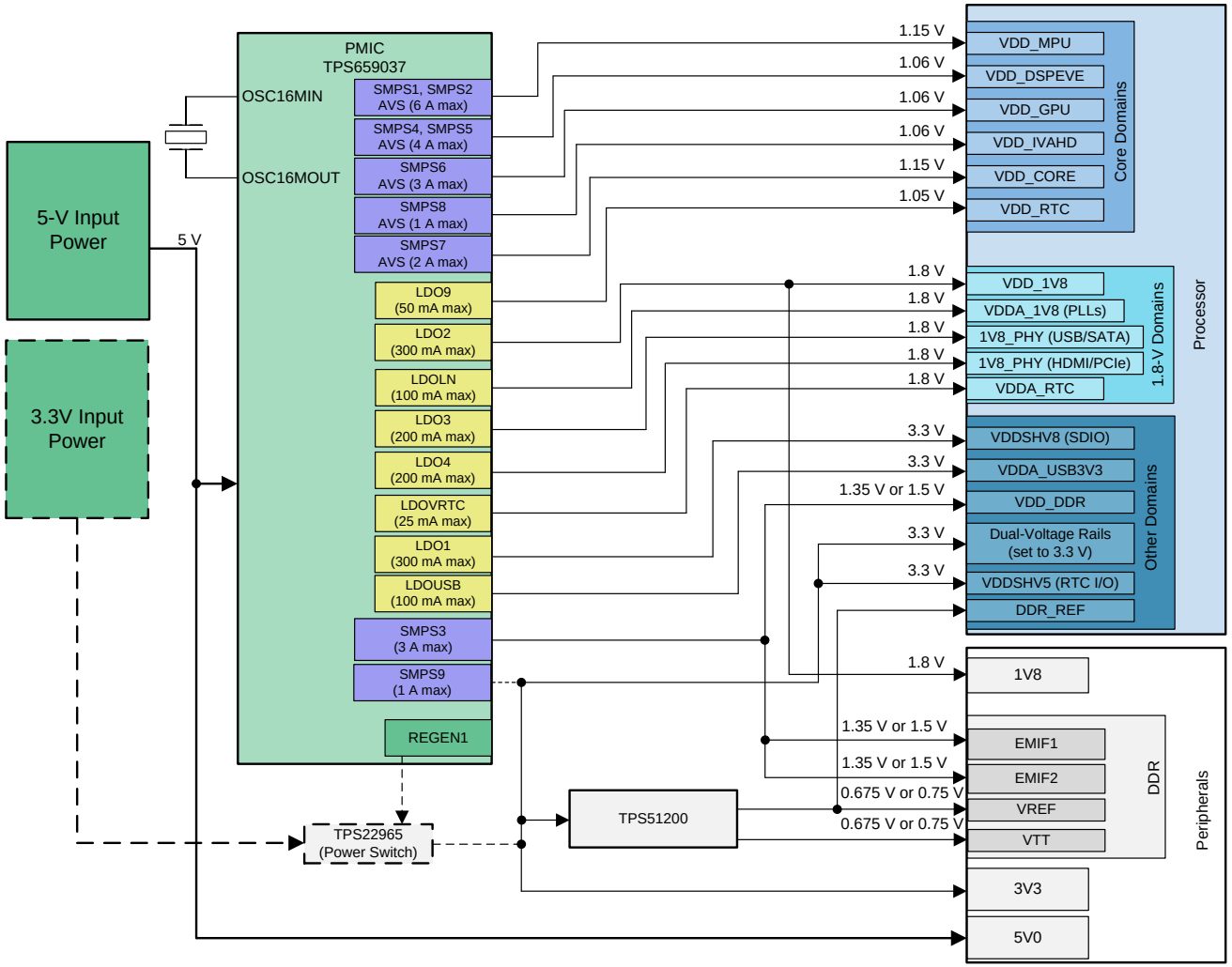

Figure 2. Processor Connection With TPS6590377ZWSR

In both configurations, LDO3 and LDO4 are used to supply the PHY domains. Table 2 describes how the PHY domains should be split between the two LDOs.

Table 2. LDO3 and LDO4 Mapping to PHY Domains

TPS659037 LDO	PROCESSOR BALL	VOLTAGE RAIL (AM572x)	VOLTAGE RAIL (AM571x)
LDO3 (300 mA)	AA13	VDDA_USB1	VDDA_USB1
	AB12	VDDA_USB2	VDDA_USB2
	W12	VDDA_USB3	VDDA_CSI2
	V13	VDDA_SATA	VDDA_SATA
LDO4 (300 mA)	Y17	VDDA_HDMI	VDDA_HDMI
	W14	VDDA_PCIE	VDDA_USB3
	AA17	VDDA_PCIE0	VDDA_PCIE
	AA16	VDDA_PCIE1	VDDA_PCIE0

4 BOOT OTP Configuration

All TPS659037 resource settings are stored in the form of registers. Therefore, all platform-related settings are linked to an action altering these registers. This action can be a static update (register initialization value) or a dynamic update of the register (either from the user or from a power sequence).

Resources and platform settings are stored in nonvolatile memory (OTP). These settings are defined as follows:

Static platform settings — These settings define, for example, SMPS or LDO default voltages, and GPIO functionality. Most static platform settings can be overwritten by a power sequence or by the user.

Sequence platform settings — These settings define the TPS659037 power sequences between state transitions, such as the OFF2ACT sequence when transitioning from OFF state to ACTIVE state. The power sequence is composed of several register accesses that define which resources (and the corresponding registers) must be updated during the respective state transition. The state of these resources can be overwritten by the user when the power sequence completes execution.

5 Static Platform Settings

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device, distinguished by the SW_REVISION.

5.1 System Voltage Monitoring

Table 3. System Voltage Monitoring OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE	UNIT
VSYS_MON	VSYS_HI	System voltage rising-edge threshold	3.1		V
VSYS_LO	VSYS_LO	System voltage falling-edge threshold	2.75		V

The power state-machine of the TPS659037 device is controlled by comparators monitoring the voltage on the VCC_SENSE and VCCx pins. For electrical parameters refer to the data sheet.

VSYS_LO — When the voltage on the VCC1 pin rises above VSYS_LO, the device enters from the BACKUP to the OFF state. When the device is in the ACTIVE, SLEEP, or OFF state and the voltage on the VCC1 pin decreases below VSYS_LO, the device enters BACKUP mode. The VSYS_LO level is OTP programmable.

VSYS_HI — During power up, the VSYS_HI OTP value is used as a threshold for the VSYS_MON comparator which is gating the PMIC startup (as a threshold for transition from the OFF to ACTIVE state). The VSYS_MON comparator monitors the VCC_SENSE pin. After power up, the user can use software to configure the comparator threshold in the VSYS_MON register.

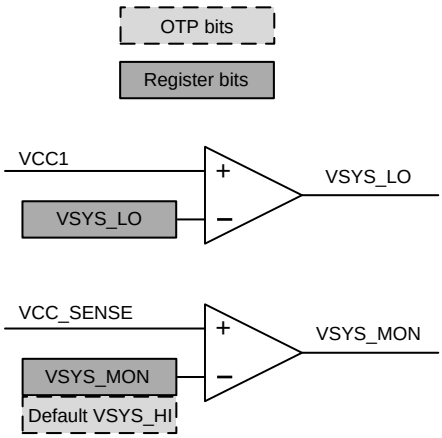

Figure 3. PMIC Comparators

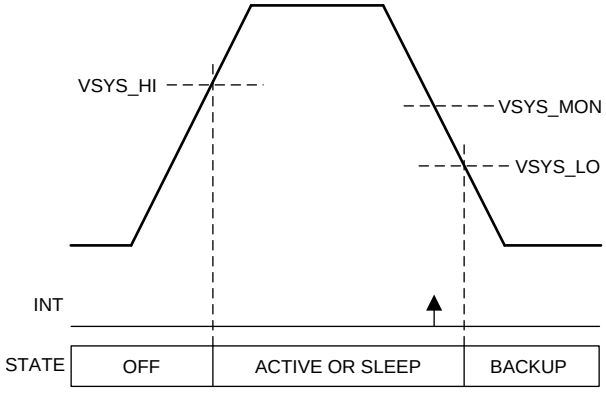

Figure 4. State Transitions

NOTE: The maximum input voltage of the VCC_SENSE and VCC_SENSE2 pins depend on the OTP setting of PMU_CONFIG [HIGH_VCC_SENSE] as listed in the *Recommended Operating Conditions* table of the TPS659037 data sheet. This configuration is set as HIGH_VCC_SENSE = 0 with the VCC_SENSE and VCC_SENSE2 pins are connected to VCC1.

For the recommended operating conditions of the electrical parameters, see *TPS659037-Q1 Automotive Power Management Unit (PMU) for Processor*, (SLIS165).

5.2 SMPS

This section describes the default voltage for each SMPS. Each device has two default voltages for SMPS3 based on the connection of the BOOT0 pin. If the BOOT0 pin is connected to 0 V, then SMPS3 defaults to 1.35 V. If the BOOT0 pin is connected to 1.8 V, then SMPS3 outputs 1.5 V.

By default, SMPS7 and SMPS9 remain off in OTP 0x8A. SMPS7 and SMPS9 can be enabled after startup through I^2C by setting the appropriate SMPSx_CTRL and SMPSx_VOLTAGE registers.

Table 4. SMPS OTP Settings

BIT	DESCRIPTION[1]	0x8A VALUE		0x8B VALUE		UNIT
		BOOT0 = 0	BOOT0 = 1	BOOT0 = 0	BOOT0 = 1	
SMPS12_VOLTAGE	Default output voltage for the regulator	1.15				V
SMPS3_VOLTAGE	Default output voltage for the regulator	1.35	1.5	1.35	1.5	V
SMPS45_VOLTAGE	Default output voltage for the regulator	1.06				V
SMPS6_VOLTAGE	Default output voltage for the regulator	1.15		1.06		V
SMPS7_VOLTAGE	Default output voltage for the regulator	0		1.15		V
SMPS8_VOLTAGE	Default output voltage for the regulator	1.8		1.06		V
SMPS9_VOLTAGE	Default output voltage for the regulator	0		3.3		V
SMPS12_SMPS123_EN	SMPS3 configuration	SMPS3 single phase				

(1) The regulator output voltage cannot be modified while active from one (0.7 to 1.65 V) voltage range to the other (1 to 3.3 V) voltage range or the other way around. The regulator must be turned off to do so.

5.3 LDO

This section describes the default output voltage for each LDO.

Table 5. LDO OTP Settings

BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE	UNIT
LDO1_VOLTAGE	Default output voltage for the regulator	3.3		V
LDO2_VOLTAGE	Default output voltage for the regulator	3.3	1.8	V
LDO3_VOLTAGE	Default output voltage for the regulator	1.8		V
LDO4_VOLTAGE	Default output voltage for the regulator	1.8		V
LDO9_VOLTAGE	Default output voltage for the regulator	1.05		V
LDOLN_VOLTAGE	Default output voltage for the regulator	1.8		V
LDOUSB_VOLTAGE	Default output voltage for the regulator	3.3		V

NOTE: LDO1 and LDO2 share a single input LDO12_IN and must by supplied by the same voltage. Refer to the input voltage parameter in the data sheet.

5.4 Interrupts

The interrupts are split into four register groups (INT1, INT2, INT3, and INT4). All interrupts are logically combined on a single output line, INT (default active-low). This line is used as an external interrupt line to warn the host processor of any interrupt event that has occurred within the device. The OTP settings in this section show whether each interrupt is enabled or disabled by default.

Table 6. INT1 OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
INT1_MASK	VSYS_MON	Enable and disable interrupt from the VSYS_MON comparator	1: Interrupt generation disabled	
	PWRDOWN	Enable and disable interrupt from the PWRDOWN pin	0: Interrupt generated	
	PWRON	Enable and disable interrupt from PWRON pin. A PWRON event is always an ON request.	1: Interrupt generation disabled	
	LONG_PRESS_KEY	Enable and disable interrupt from long key press on the PWRON pin	1: Interrupt generation disabled	
	RPWRON	Enable and disable interrupt from RPWRON pin. A RPWRON event is always an ON request.	0: Interrupt generated	
	HOTDIE	Enable and disable interrupt from device hot-die detection. The interrupt can be used as a pre-warning for processor to limit the PMIC load, before increasing die temperature forces shutdown.	0: Interrupt generated	

Table 7. INT2 OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
INT2_MASK	SHORT	Triggered from internal event of SMPS or LDO outputs failing. If an interrupt is enabled, it is an ON request.	0: Interrupt generated	
	WDT	Enable and disable interrupt from watchdog expiration	0: Interrupt generated	
	RTC_TIMER	Enable and disable RTC timer interrupt. Timer period preprogrammed. If an interrupt is enabled, it is an ON request.	1: Interrupt generation disabled	
	RTC_ALARM	Enable and disable RTC alarm interrupt. The alarm is preprogrammed for certain date or time. If an interrupt is enabled, it is an ON request.	0: Interrupt generated	
	RESET_IN	Enable and disable interrupt from the RESET_IN pin	0: Interrupt generated	

Table 8. INT3 OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
INT3_MASK	GPADC_EOC_SW	GPADC result ready from software-initiated conversion	1: Interrupt generation disabled	
	GPADC_AUTO_1	GPADC automatic conversion result 1 above or below the reference threshold	0: Interrupt generated	
	GPADC_AUTO_0	GPADC automatic conversion result 0 above or below the reference threshold	0: Interrupt generated	

Table 9. INT4 OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
INT4_MASK	GPIO_7	Enable and disable interrupt from the GPIO7 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_6	Enable and disable interrupt from the GPIO6 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_5	Enable and disable interrupt from the GPIO5 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_4	Enable and disable interrupt from the GPIO4 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_3	Enable and disable interrupt from the GPIO3 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_2	Enable and disable interrupt from the GPIO2 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_1	Enable and disable interrupt from the GPIO1 pin rising or falling edge	1: Interrupt generation disabled	
	GPIO_0	Enable and disable interrupt from the GPIO0 pin rising or falling edge	1: Interrupt generation disabled	

5.5 GPIO

TPS659037 integrates eight configurable general-purpose I/Os (GPIOs) that are multiplexed with alternative features. This section describes the default configuration of each GPIO, as well as the configuration of internal pullup or pulldown resistors on the GPIOs.

Table 10. GPIO OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
PRIMARY_SECONDARY_PAD2	GPIO_7	Select pin function	10: POWERHOLD	
	GPIO_6	Select pin function	1: SYSEN2	
	GPIO_5	Select pin function	00: GPIO_5	
	GPIO_4	Select pin function	1: SYSEN1	
PRIMARY_SECONDARY_PAD1	GPIO_2	Select pin function	00: GPIO_2	
	GPIO_1	Select pin function	00: GPIO_1	
PU_PD_GPIO_CTRL2	GPIO_7_PD	Enable and disable pulldown for GPIO_7. Applies if GPIO mode is selected	0: Pulldown not enabled	
PU_PD_GPIO_CTRL1	GPIO_3_PD	Enable and disable pulldown for GPIO_3. Applies if GPIO mode is selected	1: Pulldown enabled	
	GPIO_2_PU	Enable and disable pullup for GPIO_2. Applies if GPIO mode is selected	0: Pullup not enabled	
	GPIO_2_PD	Enable and disable pulldown for GPIO_2. Applies if GPIO mode is selected	1: Pulldown enabled	
	GPIO_1_PU	Enable and disable pullup for GPIO_1. Applies if GPIO mode is selected	0: Pullup not enabled	
	GPIO_1_PD	Enable and disable pulldown for GPIO_1. Applies if GPIO mode is selected	1: Pulldown enabled	
	GPIO_0_PD	Enable and disable pulldown for GPIO_0. Applies if GPIO mode is selected	0: Pulldown not enabled	

5.6 MISC

This section describes miscellaneous device configuration settings including pulldowns, polarity of signals, communication settings, and other functionality.

Table 11. MISC1 OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
PRIMARY_SECONDARY_PAD2	RESET_IN_PD	Enable and disable internal pulldown for the RESET_IN pin	1: Pulldown enabled	
	PWRDOWN_PD	Enable and disable internal pulldown for the PWRDOWN pin	1: Pulldown enabled	
POLARITY_CTRL	PWRGOOD_USB_PSELPOLARITY_	Select polarity, applies to PWRGOOD and USB_PSEL selection	0: Active high	
	PWRDOWN_POLARITY	Select PWRDOWN pin polarity: 0: Device is switched off when PWRDOWN is high. 1: Device is switched off when PWRDOWN is low.	0: Active high	
	RESET_IN_POLARITY	Select RESET_IN pin polarity: 0: Device is switched off when RESET_IN is low. 1: Device is switched off when RESET_IN is high.	0: Active low	
	GPIO_3_POLARITY	Select polarity for GPIO3 pin:	0: Active high	

Table 12. MISC2 OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
LONG_PRESS_KEY	PWRON_DEBOUNCE	Debounce time selection for PWRON pin	00: 15 ms	
I2C_SPI	I2C_SPI	Selection of control interface, I^2C, or SPI	0: I^2C	
	ID_I2C2	I2C_2 address for page access versus initial address (0H12)	0: Address is 0x12	
	ID_I2C1	I2C_1 address for I^2C register access	I2C_1[0] = 1: 0x58 I2C_1[1] = 1: 0x59 I2C_1[2] = 1: 0x5A I2C_1[3] = 1: 0x5B	
PMU_CONFIG	HIGH_VCC_SENSE	Enable internal buffers on VCC_SENSE to allow voltage sensing above 5.25 V	0: High VCC sense not enabled	
	GATE_RESET_OUT	Gating of RESET_OUT until crystal oscillator is stable.	0: Not gated	
	AUTODEVON	Automatically set DEV_ON bit after startup sequence completes	0: AUTODEVON disabled	
	SWOFF_DLY	Delay before switch-off to allow host processor to save context. Device is maintained as ACTIVE until delay expiration then switches off.	00: No delay	
SPARE	REGEN2_OD	Configures REGEN2 to be open drain or push-pull.	0: Push-pull mode	
	REGEN1_OD	Configures REGEN1 to be open drain or push-pull.	0: Push-pull mode	
	OSC16M_CFG(1)	Configures the 16-Mhz oscillator to be enabled or disabled.	0: 16-MHz oscillator enabled	

(1) The 16-MHz oscillator is enabled in both devices, and therefore a 16.384-MHz crystal must be populated between OSC16MIN and OSC16MOUT.

5.7 SWOFF_HWRST

This section describes whether each reset type is configured to generate a HWRST or SWORST.

Hardware reset (HWRST) — A hardware reset occurs when any OFF request is configured to generate a hardware reset. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state (execute either the ACT2OFF or SLP2OFF sequence).

Switch-off reset (SWORST) — A switch-off reset occurs when any OFF request is configured to not generate a hardware reset. This reset acts as the HWRST, except only the SWO registers are reset. The device enters the OFF state, from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence.
The power resource control registers for SMPS and LDO voltage levels and operating mode control are in SWORST domain. Additionally some registers control the 32-kHz, REGENx and SYSENx, watchdog, external charger control, and VSYS_MON comparator. This list is indicative only.

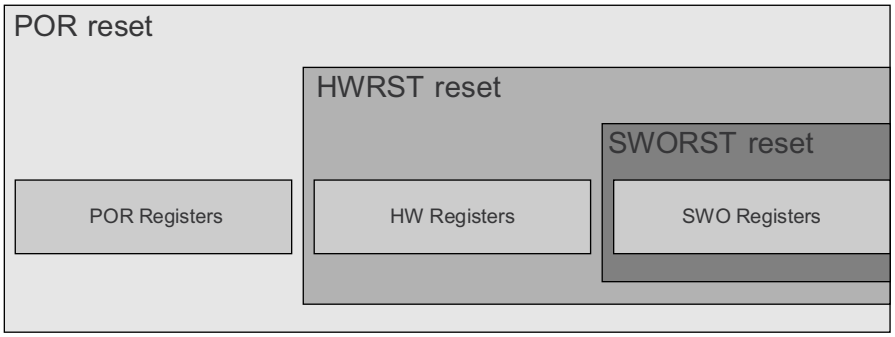

Figure 5. Reset Levels versus Registers

Table 13. SWOFF_HWRST OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
SWOFF_HWRST	PWRON_LPK	Define if PWRON long key press is causing HWRST or SWORST	1: HWRST	
	PWRDOWN	Define if PWRDOWN pin is causing HWRST or SWORST	0: SWORST	
	WTD	Define if watchdog expiration is causing HWRST or SWORST	1: HWRST	
	TSHUT	Define if thermal shutdown is causing HWRST or SWORST	1: HWRST	
	RESET_IN	Define if RESET_IN pin is causing HWRST or SWORST	1: HWRST	
	SW_RST	Define if register bit is causing HWRST or SWORST	1: HWRST	
	VSYS_LO	Define if VSYS_LO is causing HWRST or SWORST	1: HWRST	
	GPADC_SHUTDOWN	Define if GPADC event is causing HWRST or SWORST	0: SWORST	

5.8 Shutdown_ColdReset

These OTP settings show whether each OFF request is configured to generate a shutdown request (SD) or cold reset request (CR).

- When configured to generate an SD, the embedded power controller (EPC) executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
- When configured to generate a CR, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.

Table 14. Shutdown_ColdReset OTP Settings

REGISTER	BIT	DESCRIPTION	0x8A VALUE	0x8B VALUE
SWOFF_COLDRST	PWRON_LPK	Define if PWRON long key press causes shutdown or cold reset	0: Shutdown	
	PWRDOWN	Define if PWRDOWN pin causes shutdown or cold reset	1: Cold reset	
	WTD	Define if watchdog timer expiration causes shutdown or cold reset	1: Cold reset	
	TSHUT	Define if thermal shutdown causes shutdown or cold reset	0: Shutdown	
	RESET_IN	Define if RESET_IN pin causes shutdown or cold reset	1: Cold reset	
	SW_RST	Define if SW_RST register bit causes shutdown or cold reset	1: Cold reset	
	VSYS_LO	Define if VSYS_LO causes shutdown or cold reset	0: Shutdown	
	GPADC_SHUTDOWN	Define if GPADC shutdown causes shutdown or cold reset	0: Shutdown	

6 Sequence Platform Settings

A power sequence is an automatic preprogrammed sequence handled by the TPS659037 device to configure the device resources: SMPSs, LDOs, part of GPIOs, and REGEN signals into ON, OFF, or SLEEP state.

6.1 OFF2ACT Sequences

When an ON request occurs in the OFF state, the device is switched on and each resource is enabled based on the programmed OFF2ACT sequence.

Figure 6 shows the OFF2ACT sequence of the TPS6590376ZWSR.

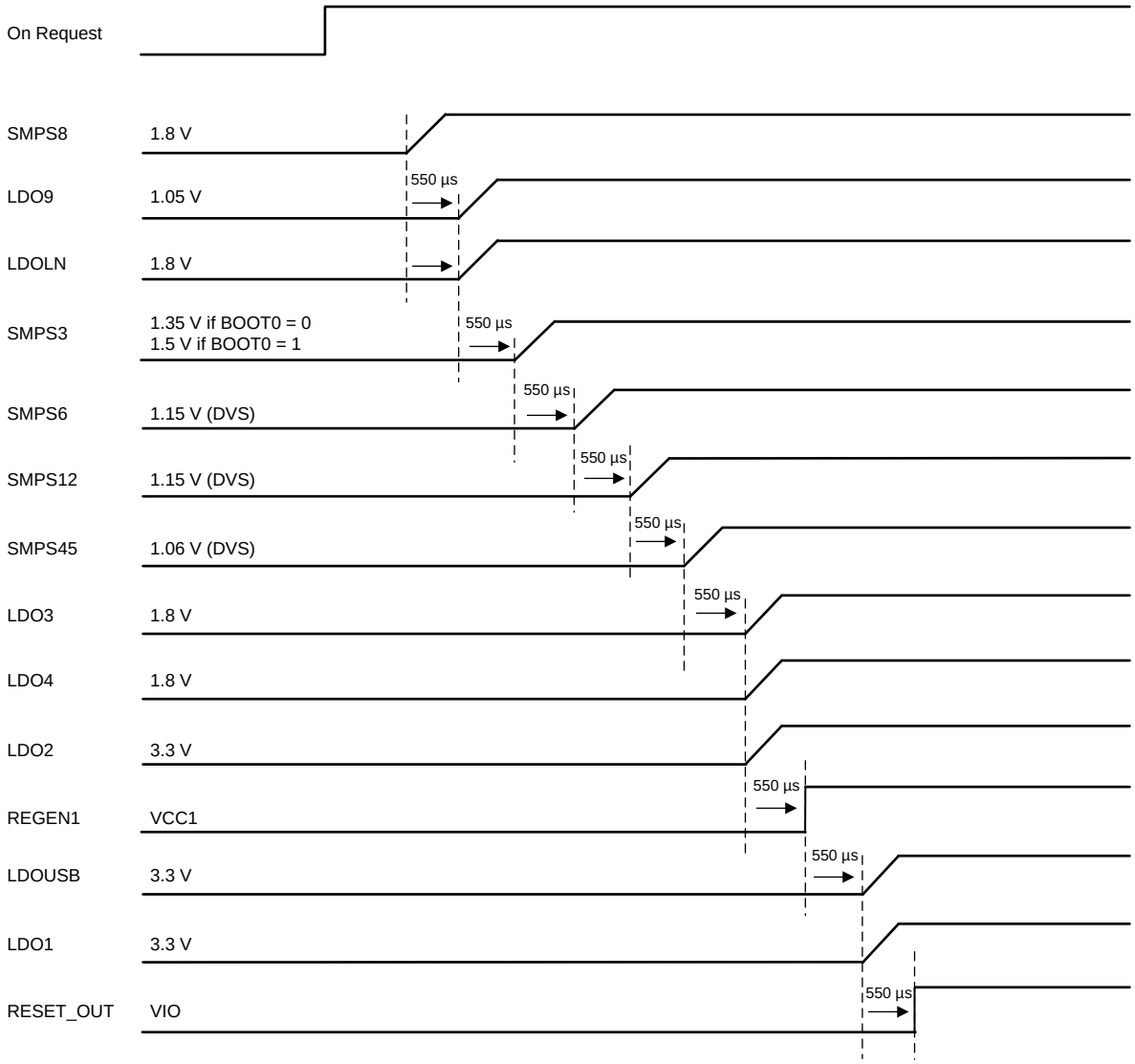

Figure 6. OFF2ACT Sequence of TPS6590376ZWSR

Figure 7 shows the OFF2ACT sequence of TPS6590377ZWSR.

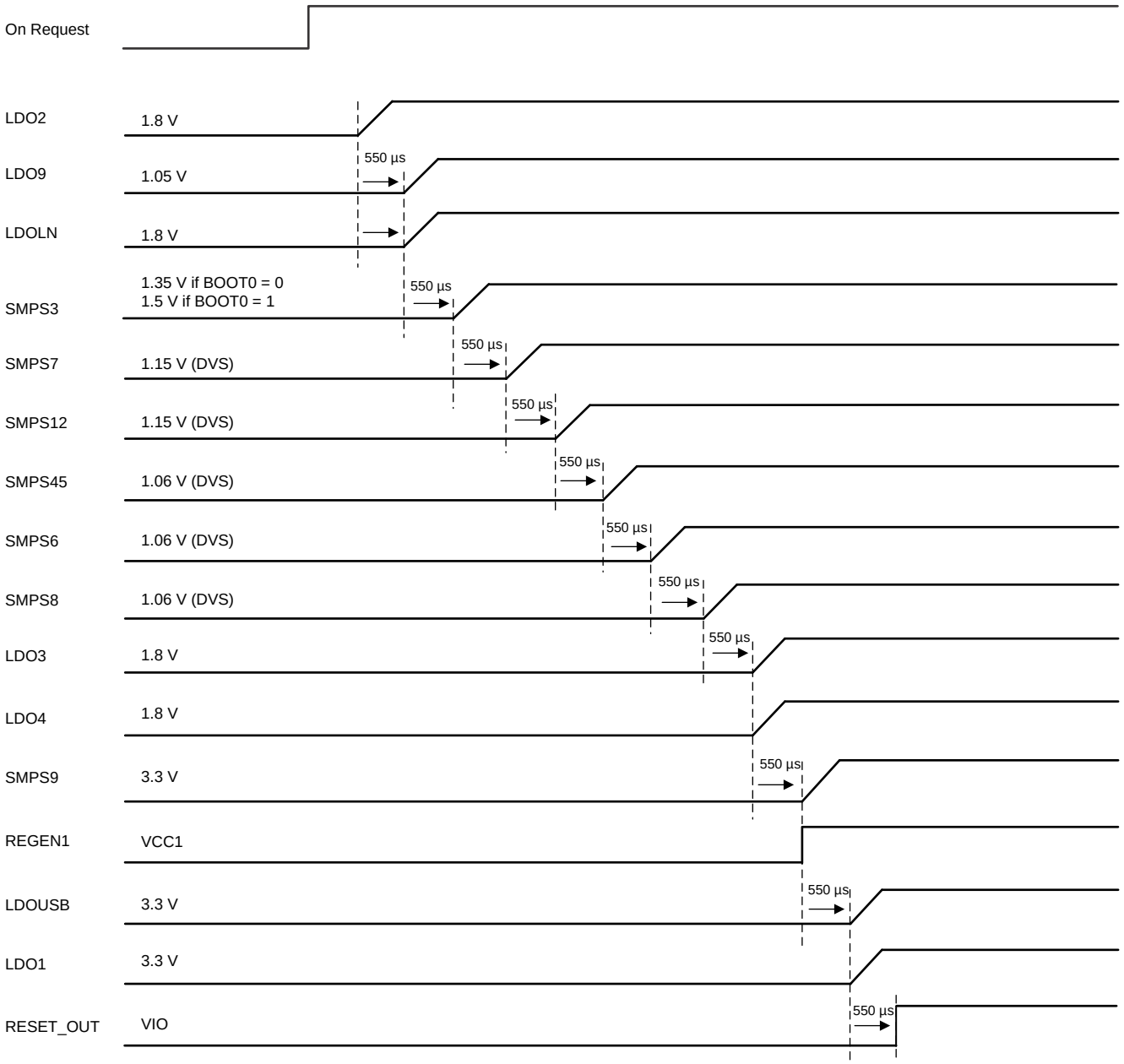

Figure 7. OFF2ACT Sequence of TPS6590377ZWSR

6.2 ACT2OFF Sequences

When an OFF request occurs during the ACTIVE state, each resource is disabled based on the programmed ACT2OFF sequence. Figure 8 shows the ACT2OFF sequence of TPS6590376ZWSR.

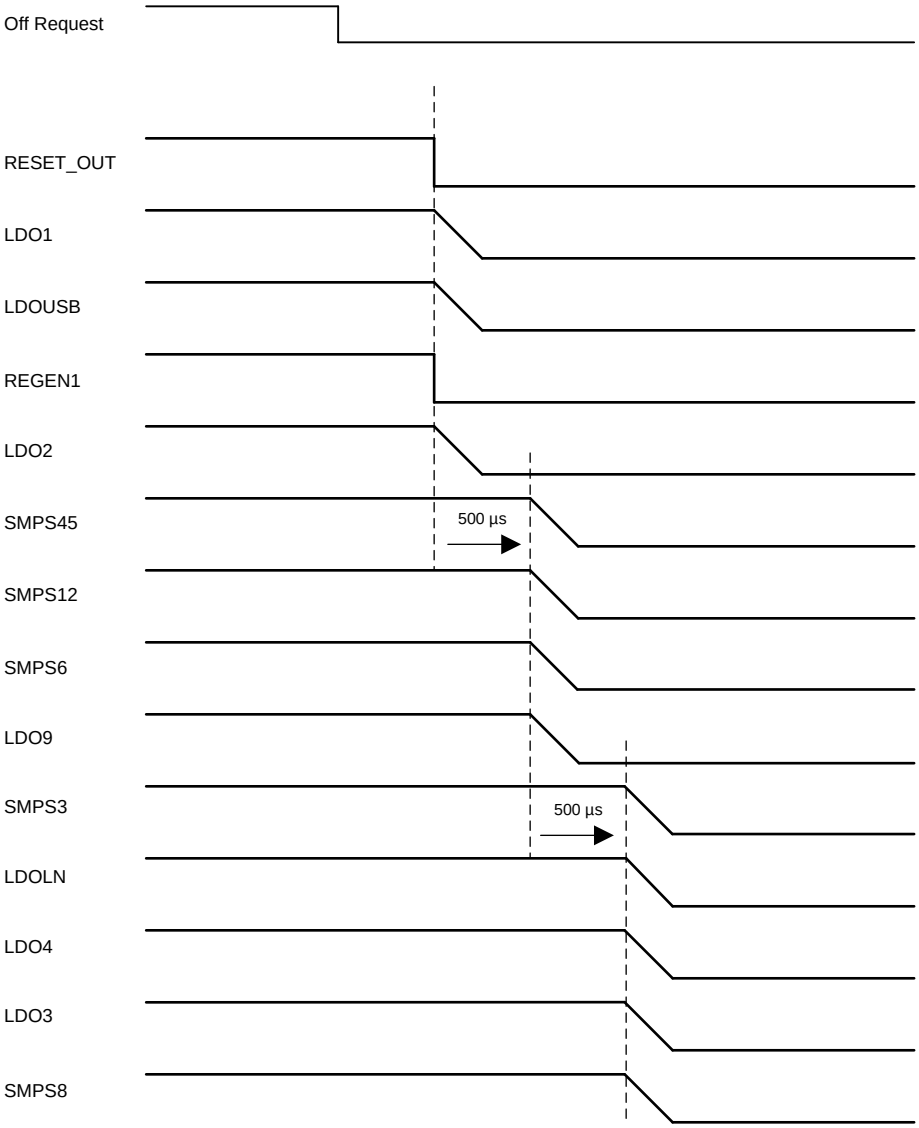

Figure 8. Power Down Sequence of TPS6590376ZWSR

Figure 9 shows the ACT2OFF sequence of TPS6590377ZWSR.

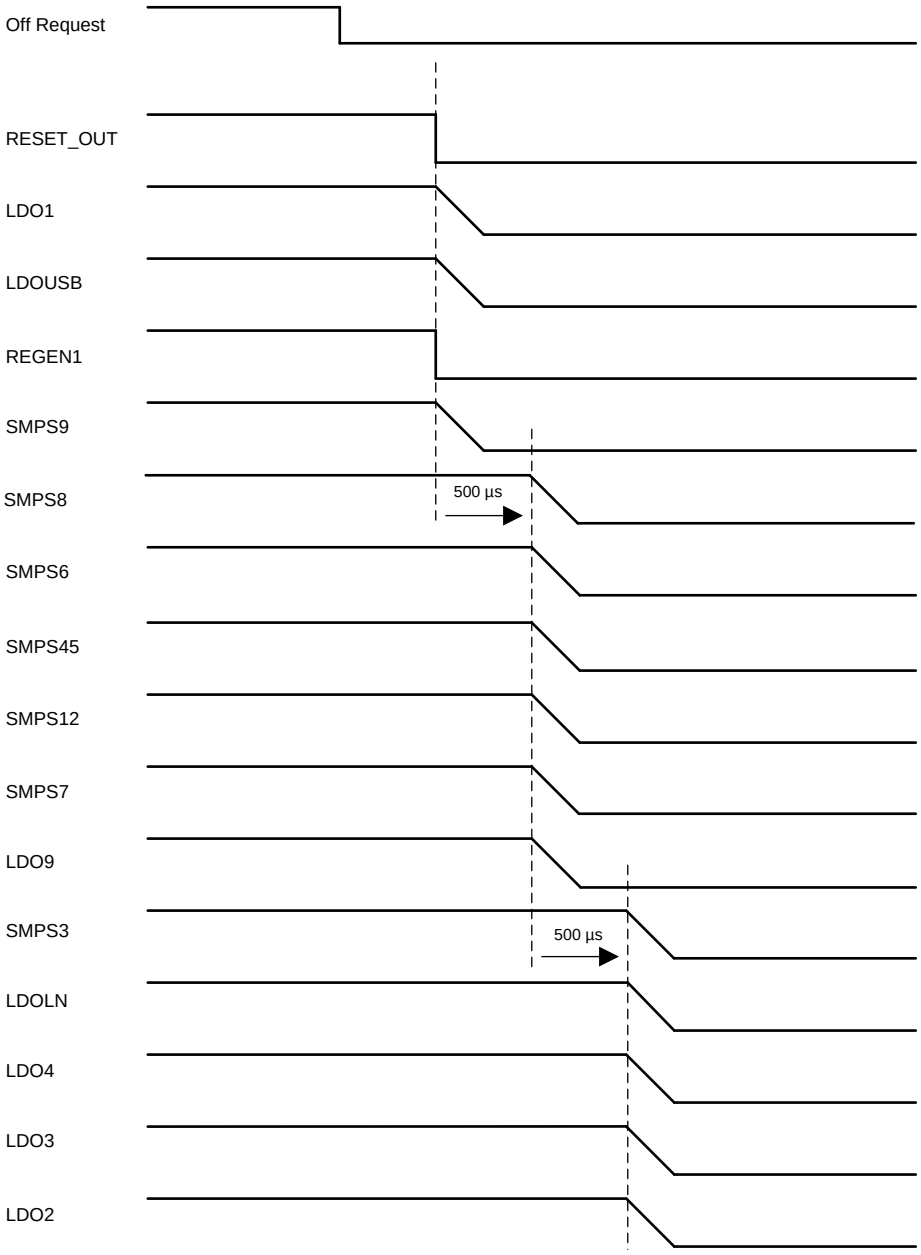

Figure 9. Power Down Sequence of TPS6590377ZWSR

6.3 ACT2SLP and SLP2ACT Sequences

The AM572x processor does not support RTC mode. Therefore keeping the PMIC out of the SLEEP state by always keeping the NSLEEP pin connected to 1.8 V during operation is recommended. Although the processor does not support RTC mode, this section is provided to describe the behavior of the PMIC in case the PMIC enters the SLEEP state.

When a SLEEP request occurs during active mode, each resource transitions to the sleep operating mode (MODE_SLEEP bits of the corresponding CTRL register) based on the programmed ACT2SLP sequence. When a WAKE request occurs during sleep mode, each resource transitions to the active operating mode (MODE_ACTIVE bits of the corresponding CTRL register) based on the programmed SLP2ACT sequence.

The following five steps must occur before a resource shuts off in sleep mode.

Step 1. NSLEEP must be unmasked through the POWER_CTRL.NSLEEP_MASK register bit.

Step 2. Each resource must be assigned to NSLEEP through the appropriate NSLEEP_xxxx_ASSIGN registers. For example, the NSLEEP_SMPS_ASSIGN register.

Step 3. Each resource must be set to be OFF in sleep mode by setting the MODE_SLEEP bits of the appropriate xxxx_CTRL register. For example, SMPS12_CTRL register.

Step 4. All interrupts must be cleared, because any pending interrupt prevents the PMIC from going to sleep mode.

Step 5. A SLEEP request is generated through the NSLEEP pin.

Note that RESET_OUT is in the VIO domain, and therefore outputs the same voltage as VIO_IN. When VIO_IN is connected to SMPS9 or a switched 3.3V rail, then RESET_OUT will be shut off during sleep mode at the same time as VIO_IN of the PMIC. If VIO_IN remains supplied during sleep mode, then RESET_OUT will remain on.

Figure 10 shows the ACT2SLP and SLP2ACT sequences of TPS6590376ZWSR.

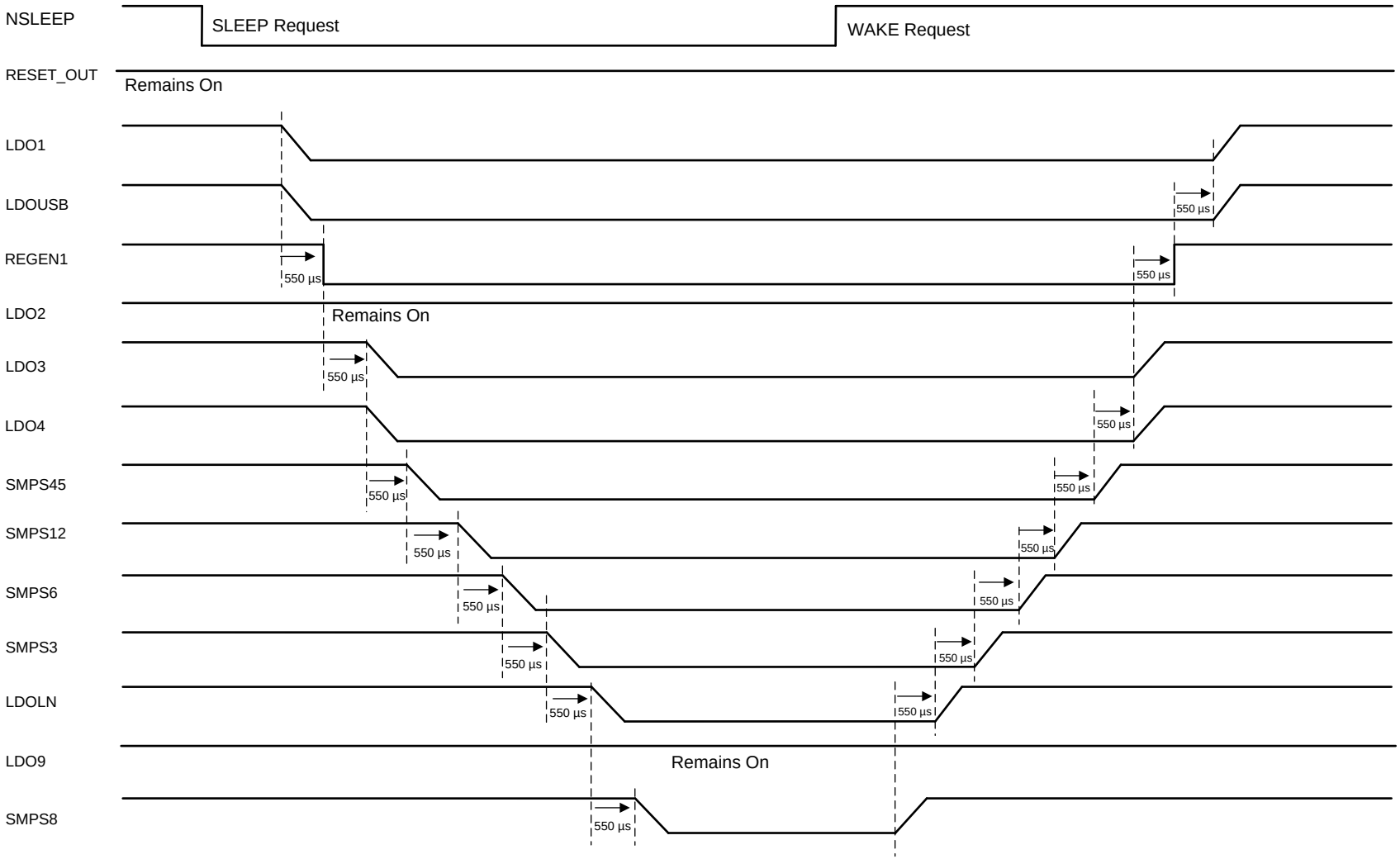

Figure 10. ACT2SLP and SLP2ACT Sequences of TPS6590376ZWSR

Figure 11 shows the ACT2SLP and SLP2ACT sequences of TPS6590377ZWSR.

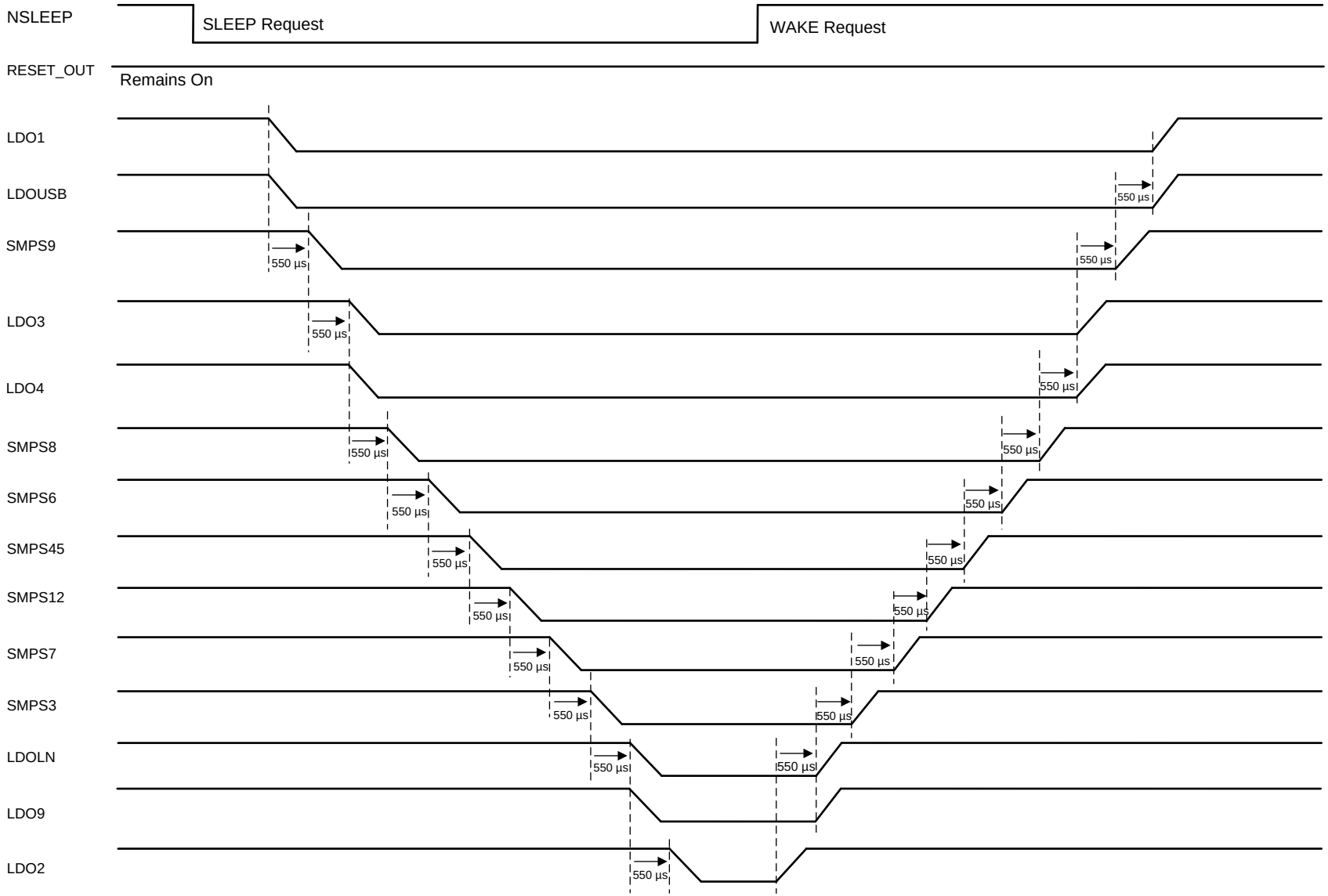

Figure 11. ACT2SLP and SLP2ACT Sequences of TPS6590377ZWSR

7 Warm Reset Sequences

A warm reset is triggered by the NRESWARM pin. During a warm reset, the OFF2ACT sequence is executed regardless of the actual state (ACTIVE, SLEEP) and the device returns to or remains in the ACTIVE state. Resources that are part of power-up sequence go to ACTIVE mode and the output voltage level is reloaded from OTP or kept in the previous value depending on the WR_S bit in the SMPSx_CTRL register or the LDOx_CTRL register. Resources that are not part of the OFF2ACT sequence are not impacted by a warm reset and maintain the previous state. Additionally, if BOOT1 = 1, then RESET_OUT is asserted low during the warm reset sequence. If BOOT1 = 0, RESET_OUT is not asserted low.

If BOOT1 = 1 is used, then the PMIC must be enabled by the POWERHOLD (GPIO_7) pin. If the PMIC will be enabled by the PWRON pin and kept on using the DEV_ON bit, then BOOT1 = 0 must be used. If POWERHOLD is set to GND while BOOT1 = 1, the PMIC will shut off during the warm reset sequence.

Figure 12 shows the warm reset sequence of TPS6590376ZWSR in the case that all resources are turned off. If any resource is on when NRESWARM is asserted, the resource remains on.

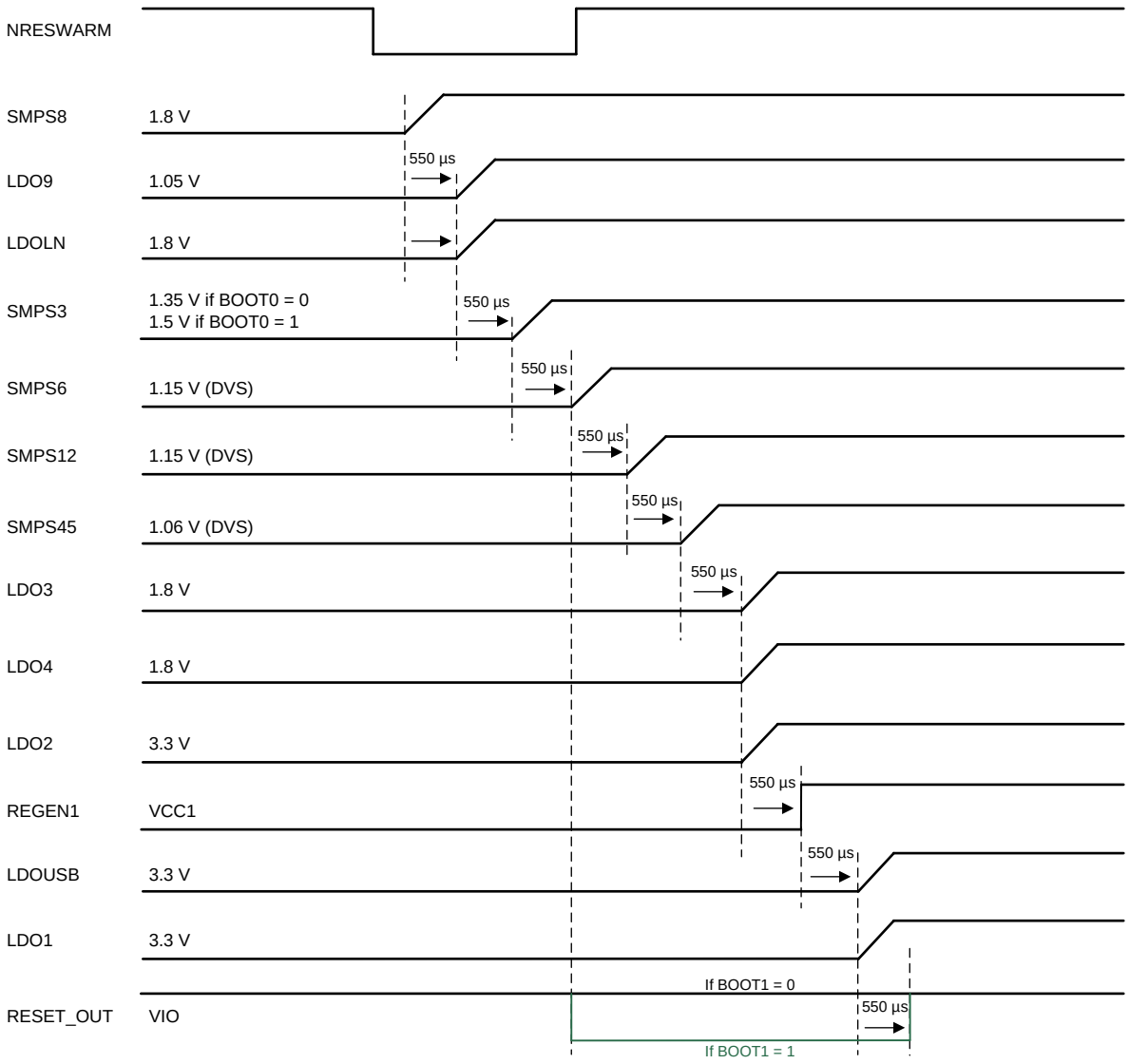

Figure 12. Warm Reset Sequence of TPS6590376ZWSR

Figure 13 shows the warm reset sequence of TPS6590377ZWSR in the case that all resources are turned off. If any resource is on when NRESWARM is asserted, the resource remains on.

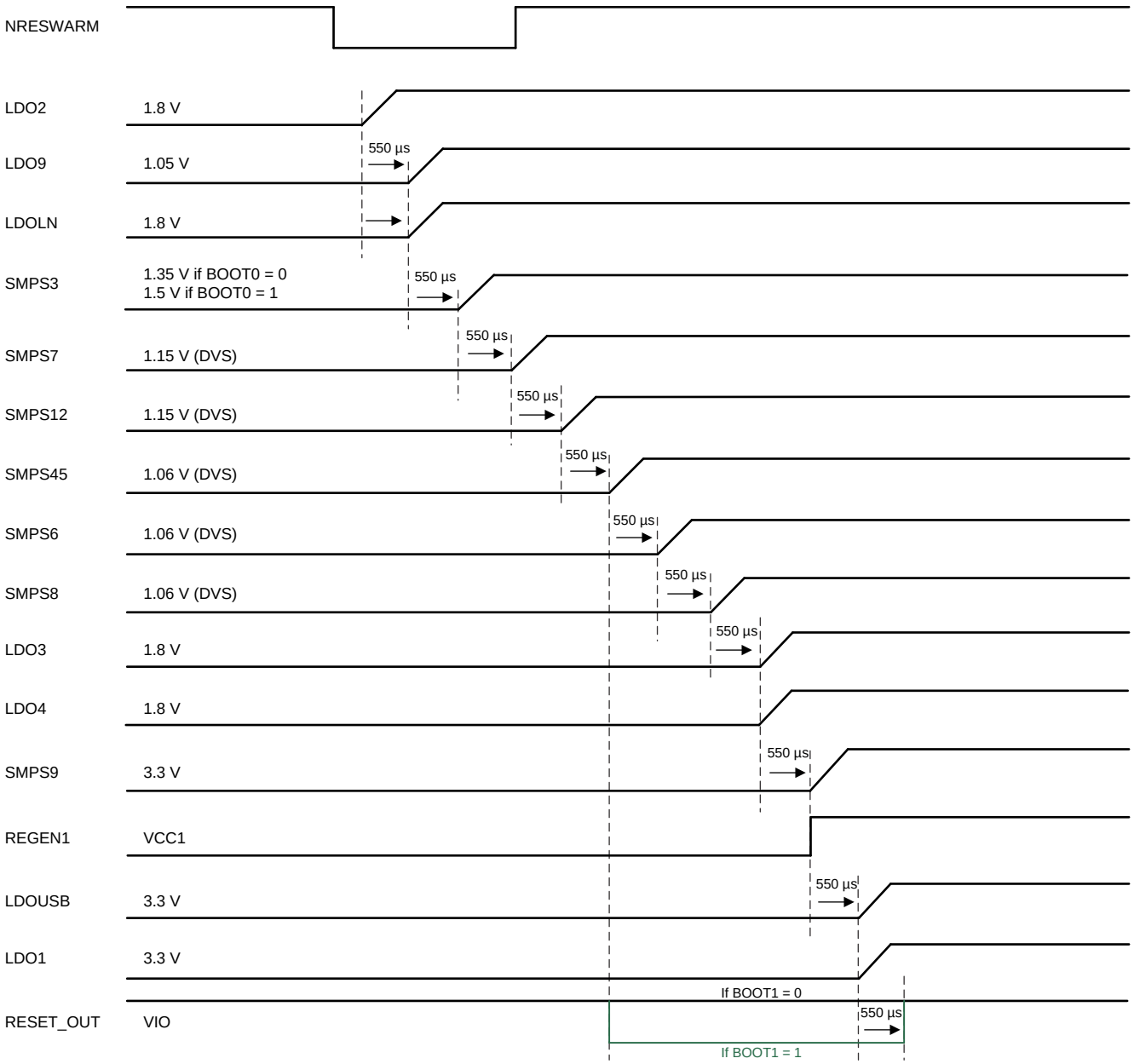

Figure 13. Warm Reset Sequence of TPS6590377ZWSR

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from C Revision (November 2015) to D Revision **Page**

- Changed REGEN1 voltage to VCC1 12

Changes from B Revision (September 2015) to C Revision **Page**

- Updated the document to describe TPS6590376 (0x8A) instead of TPS6590374 (0x80), and TPS6590377 (0x8B) instead of TPS6590375 (0x81) 1

Changes from B Revision (September 2015) to C Revision **Page**

- Updated the document to describe TPS6590376 (0x8A) instead of TPS6590374 (0x80), and TPS6590377 (0x8B) instead of TPS6590375 (0x81) 1

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