Stand-Alone USB-Friendly Synchronous Switch-Mode Li-Ion or Li-Polymer Battery Charger with System Power Selector and Low I_q

Check for Samples: bq24618

FEATURES

- **USB Friendly 4.7V–28V Input Operating Range**
- **Stand-Alone Charge Controller to Support 1–6 Li-Ion or Li-Polymer Battery Cells**
- **Up to 10A Charge Current and Adapter Current**
- **600-kHz NMOS-NMOS Synchronous Buck Converter**
- **High-Accuracy Voltage and Current Regulation**
  - **±0.5% Charge Voltage Accuracy**
  - **±3% Charge Current Accuracy**
  - **±3% Adapter Current Accuracy**
- **Integration**
  - **Automatic System Power Selection From Adapter or Battery**
  - **Internal Loop Compensation**
  - **Internal Soft Start**
  - **Dynamic Power Management**
- **Safety Protection**
  - **Input Overvoltage Protection**
  - **Battery Thermistor Sense Hot/Cold Charge Suspend**
  - **Battery Detection**
  - **Reverse-Protection Input FET**
  - **Programmable Safety Timer**
  - **Charge Overcurrent Protection**
  - **Battery Short Protection**
  - **Battery Overvoltage Protection**
  - **Thermal Shutdown**
- **Status Outputs**
  - **Adapter Present**
  - **Charger Operation Status**
- **Charge Enable Pin**
- **6-V Gate Drive for Synchronous Buck Converter**
- **30-ns Driver Dead-Time and 99.5% Max. Effective Duty Cycle**
- **24-pin, 4-mm × 4-mm QFN Package**
- **Energy Star Low Quiescent Current I_q**
  - **< 15-μA Off-State Battery Discharge Current**
  - **< 1.5-mA Off-State Input Quiescent Current**

APPLICATIONS

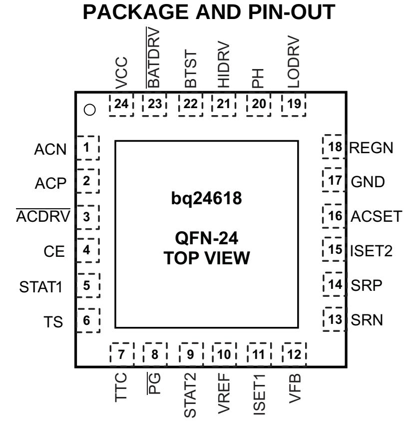
- **Tablet PC**
- **Smart Phones**
- **Portable Media Players, Navigation Devices, Notebook and Ultra-Mobile PC**
- **Personal Digital Assistants**
- **Handheld Terminals**
- **Industrial and Medical Equipment**

DESCRIPTION

The bq24618 is highly integrated Li-ion or Li-polymer switch-mode battery-charge controller. It offers a constant-frequency synchronous switching PWM controller with high-accuracy charge current and voltage regulation, charge preconditioning, termination, adapter-current regulation and charge-status monitoring.

The bq24618 operates from either a USB port or ac adapter and supports charge currents up to 10 A. The device charges the battery in three phases: preconditioning, constant current, and constant voltage. Charge is terminated when the current reaches a minimum user-selectable level. A programmable charge timer provides a safety backup for charge termination. The bq24618 automatically restarts the charge cycle if the battery voltage falls below an internal threshold, and enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage.

PACKAGE AND PIN-OUT



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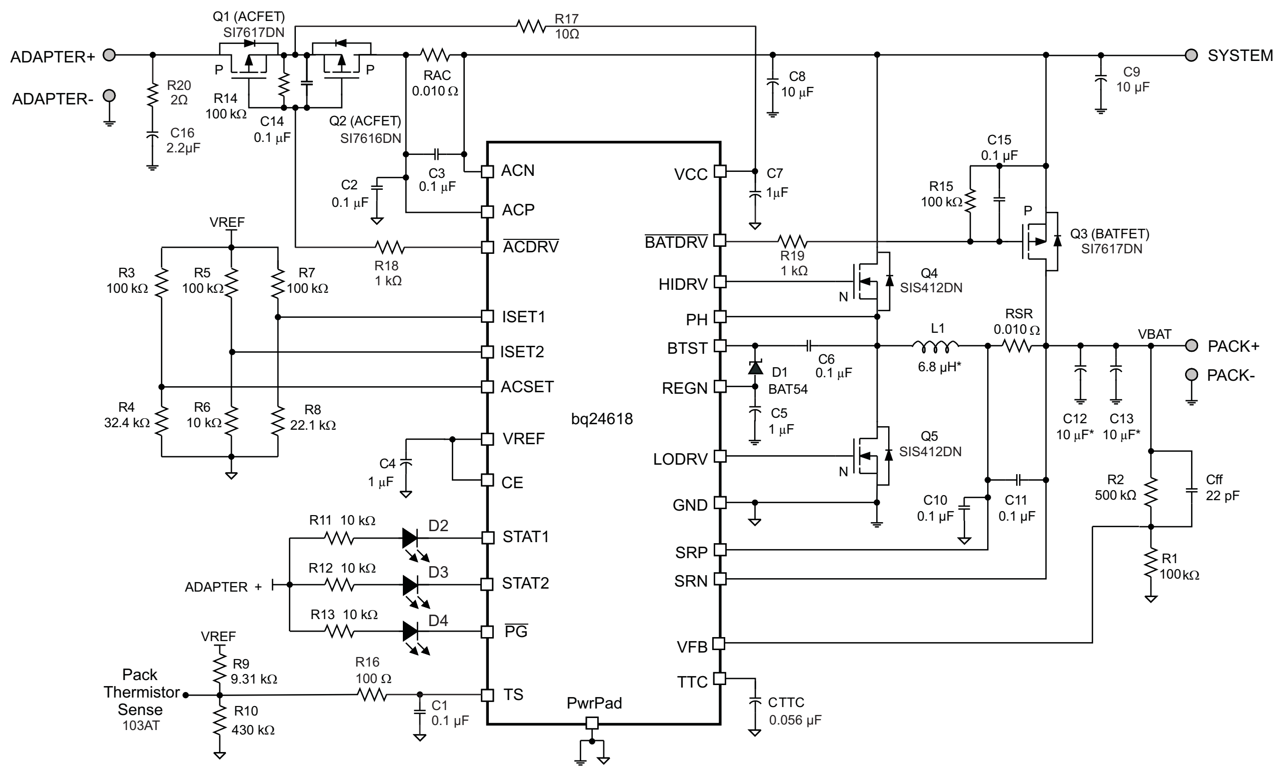
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

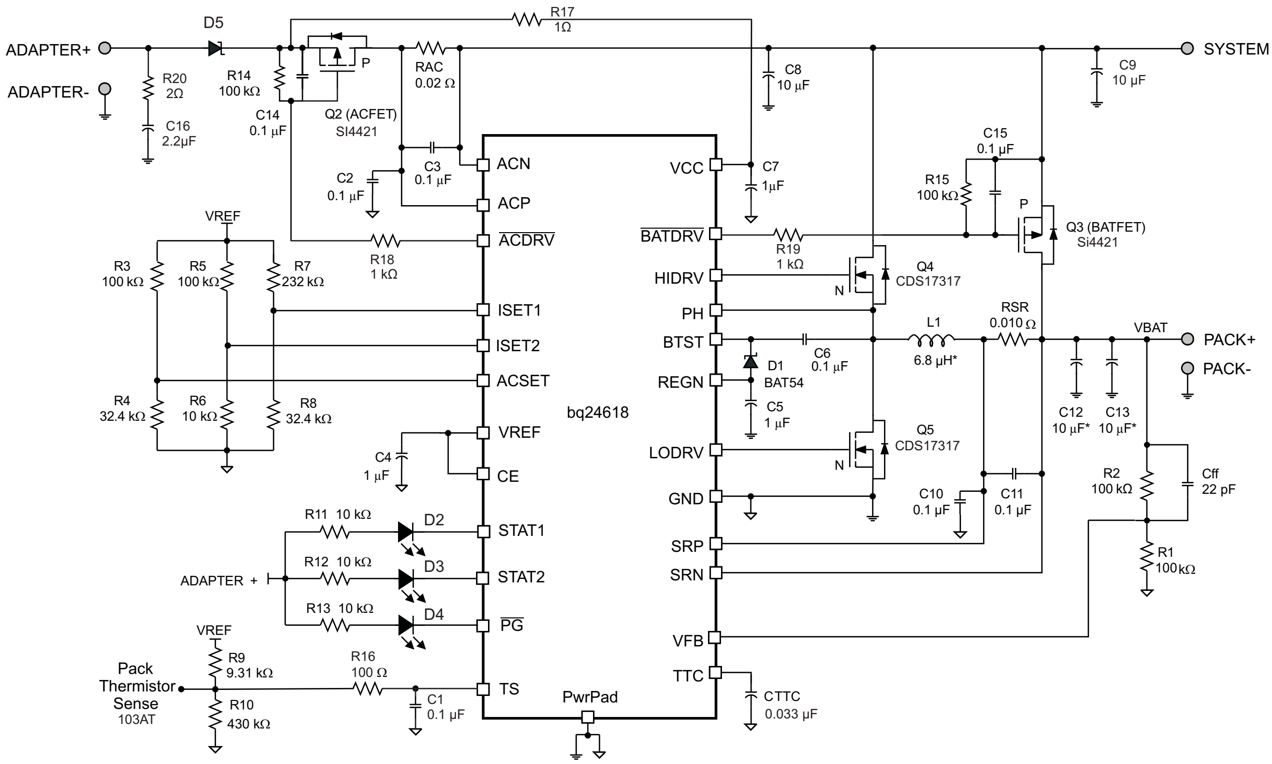
The bq24618 controls external switches to prevent battery discharge back to the input, to connect the adapter to the system, and to connect the battery to the system using 6-V gate drives for better system efficiency. The bq24618 features dynamic power management (DPM). These features reduce battery charge current when the input power limit is reached to avoid overloading the ac adapter when supplying the load and the battery charger simultaneously. A highly accurate current-sense amplifier enables precise measurement of input current from the ac adapter to monitor the overall system power.

TYPICAL APPLICATIONS



VIN = 19 V, 3-cell, $I_{adapter\_limit}$ = 4 A, I_{charge} = 3 A, $I_{pre\text{-}charge}$ = I_{term} = 0.3 A, 5-hour safety timer

Figure 1. Typical System Schematic



VIN = 5 V, 1-cell, $I_{adapter\_limit}$ = 2 A, I_{charge} = 2 A, $I_{pre\text{-}charge}$ = I_{term} = 0.3 A, 3-hour safety timer

Figure 2. Typical System Schematic

ORDERING INFORMATION

PART NUMBER	IC MARKING	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24618	QWG	24-pin 4-mm × 4-mm QFN	bq24618RGER	3000
			bq24618RGET	250

THERMAL INFORMATION

THERMAL METRIC[1]		bq24616 RGE 24 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[2]	43	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	54.3	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	19	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1] [2] [3]

			VALUE	UNIT
	Voltage range	VCC, ACP, ACN, SRP, SRN, $\overline{BATDRV}$, $\overline{ACDRV}$, CE, STAT1, STAT2, $\overline{PG}$	–0.3 to 33	V
		PH	–2 to 36	V
		VFB	–0.3 to 16	V
		REGN, LODRV, ACSET, TS, TTC	–0.3 to 7	V
		BTST, HIDRV with respect to GND	–0.3 to 39	V
		VREF, ISET1, ISET2	–0.3 to 3.6	V
	Maximum difference voltage	ACP–ACN, SRP–SRN	–0.5 to 0.5	V
T_J	Junction temperature range		–40 to 155	°C
T_{stg}	Storage temperature range		–55 to 155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.
(3) Must have a series resistor between battery pack to VFB if battery pack voltage is expected to be greater than 16 V. Usually, the resistor-divider top resistor takes care of this.

RECOMMENDED OPERATING CONDITIONS

			VALUE	UNIT
	Voltage range	VCC, ACP, ACN, SRP, SRN, $\overline{BATDRV}$, $\overline{ACDRV}$, CE, STAT1, STAT2, $\overline{PG}$	–0.3 to 28	V
		PH	–2 to 30	V
		VFB	–0.3 to 14	V
		REGN, LODRV, ACSET, TS, TTC	–0.3 to 6.5	V
		BTST, HIDRV with respect to GND	–0.3 to 34	V
		ISET1, ISET2	–0.3 to 3.3	V
		VREF	3.3	V
	Maximum difference voltage	ACP–ACN, SRP–SRN	–0.2 to 0.2	V
T_J	Junction temperature range		0 to 125	°C
T_{stg}	Storage temperature range		–55 to 155	°C

ELECTRICAL CHARACTERISTICS

4.7 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{VCC_OP}	VCC input voltage operating range		4.7		28	V
QUIESCENT CURRENTS						
I_{BAT}	Total battery discharge current (sum of currents into VCC, BTST, PH, ACP, ACN, SRP, SRN, VFB), VFB ≤ 2.1 V	V_{VCC} < V_{SRN}, V_{VCC} > V_{UVLO} (SLEEP)			15	μA
	Battery discharge current (sum of currents into BTST, PH, SRP, SRN, VFB), VFB ≤ 2.1 V	V_{VCC} > V_{SRN}, V_{VCC} > V_{UVLO} CE = LOW			5	μA
		V_{VCC} > V_{SRN}, V_{VCC} > V_{VCCLOW} CE = HIGH, charge done			5	μA
I_{AC}	Adapter supply current (current into VCC, ACP, ACN pin)	V_{VCC} > V_{SRN}, V_{VCC} > V_{UVLO} CE = LOW (IC quiescent current)		1	1.5	mA
		V_{VCC} > V_{SRN}, V_{VCC} > V_{VCCLOW}, CE = HIGH, charge done		2	5	mA
		V_{VCC} > V_{SRN}, V_{VCC} > V_{VCCLOW}, CE = HIGH, charging, Qg_total = 20 nC		25		mA
CHARGE VOLTAGE REGULATION						
V_{FB}	Feedback regulation voltage			2.1		V
	Charge-voltage regulation accuracy	T_J = 0°C to 85°C	–0.5%		0.5%	
		T_J = –40°C to 125°C	–0.7%		0.7%	
I_{VFB}	Leakage current into VFB pin	VFB = 2.1 V			100	nA
CURRENT REGULATION – FAST CHARGE						
V_{ISET1}	ISET1 voltage range				2	V
V_{IREG_CHG}	SRP-SRN current sense voltage range	V_{IREG_CHG} = V_{SRP} – V_{SRN}			100	mV
K_{ISET1}	Charge-current set factor (amps of charge current per volt on ISET1 pin)	R_{SENSE} = 10 mΩ		5		A/V
	Charge-current regulation accuracy	V_{IREG_CHG} = 40 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–4%		4%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 1.5 mV (V_{SRN} > 3.1 V)	–40%		40%	
I_{ISET1}	Leakage current into ISET1 pin	V_{ISET1} = 2 V			100	nA
CURRENT REGULATION – PRECHARGE						
V_{ISET2}	ISET2 voltage range				2	V
K_{ISET2}	Precharge-current set factor (amps of precharge current per volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V
	Precharge-current regulation accuracy	V_{IREG_PRECH} = 20 mV	–4%		4%	
		V_{IREG_PRECH} = 5 mV	–25%		25%	
		V_{IREG_PRECH} = 1.5 mV (V_{SRN} < 3.1 V)	–55%		55%	
I_{ISET2}	Leakage current into ISET2 pin	V_{ISET2} = 2 V			100	nA

ELECTRICAL CHARACTERISTICS (continued)

4.7 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE TERMINATION						
K_{TERM}	Termination current set factor (amps of termination current per volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V
	Termination current accuracy	V_{ITERM} = 20 mV	–4%		4%	
		V_{ITERM} = 5 mV	–25%		25%	
		V_{ITERM} = 1.5 mV	–45%		45%	
	Deglitch time for termination (both edges)			100		ms
t_{QUAL}	Termination qualification time	$V_{BAT} > V_{RECH}$ and $I_{CHG} < I_{TERM}$		250		ms
I_{QUAL}	Termination qualification current	Discharge current once termination is detected		2		mA
INPUT CURRENT REGULATION						
V_{ACSET}	ACSET voltage range				2	V
V_{IREG_DPM}	ACP-ACN current-sense voltage range	$V_{IREG\_DPM} = V_{ACP} – V_{ACN}$			100	mV
K_{ACSET}	Input-current set factor (amps of input current per volt on ACSET pin)	R_{SENSE} = 10 mΩ		5		A/V
I_{ACSET}	Input-current regulation-accuracy leakage current into ACSET pin	V_{IREG_DPM} = 40 mV	–3%		3%	
		V_{IREG_DPM} = 20 mV	–4%		4%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
I_{ISET1}	Leakage current into ACSET pin	V_{ACSET} = 2 V			100	nA
INPUT UNDERVOLTAGE LOCKOUT COMPARATOR (UVLO)						
V_{UVLO}	AC undervoltage rising threshold	Measure on VCC	3.65	3.85	4	V
V_{UVLO_HYS}	AC undervoltage hysteresis, falling			350		mV
VCC LOWV COMPARATOR						
	Falling threshold, disable charge	Measure on VCC		4.1		V
	Rising threshold, resume charge			4.35	4.5	V
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
V_{SLEEP_FALL}	SLEEP falling threshold	$V_{VCC} – V_{SRN}$ to enter SLEEP	40	100	150	mV
V_{SLEEP_HYS}	SLEEP rising threshold				600	mV
	SLEEP rising delay	VCC falling below SRN, delay to turn off ACFET		1		µs
	SLEEP falling delay	VCC rising above SRN, delay to turn on ACFET		30		µs
	SLEEP rising shutdown deglitch	VCC falling below SRN, delay to enter SLEEP mode		100		ms
	SLEEP falling power up deglitch	VCC rising above SRN, delay to exit SLEEP mode		30		ms
ACN / SRN COMPARATOR						
$V_{ACN-SRN\_FALL}$	ACN to SRN falling threshold	$V_{ACN} – V_{SRN}$ to turn on BATFET	100	200	310	mV
$V_{ACN-SRN\_HYS}$	ACN to SRN rising hysteresis			100		mV
	ACN to SRN rising deglitch	$V_{ACN} – V_{SRN} > V_{ACN-SRN\_RISE}$		2		ms
	ACN to SRN falling deglitch	$V_{ACN} – V_{SRN} < V_{ACN-SRN\_FALL}$		50		µs
BAT LOWV COMPARATOR						
V_{LOWV}	Precharge to fast-charge transition (LOWV threshold)	Measured on VFB pin, Rising	1.534	1.55	1.566	V
V_{LOWV_HYS}	LOWV hysteresis			100		mV
	LOWV rising deglitch	VFB falling below V_{LOWV}		25		ms
	LOWV falling deglitch	VFB rising above $V_{LOWV} + V_{LOWV\_HYS}$		25		ms
RECHARGE COMPARATOR						
V_{RECHG}	Recharge threshold (with respect to V_{REG})	Measured on VFB pin, falling	35	50	65	mV
	Recharge rising deglitch	VFB decreasing below V_{RECHG}		10		ms
	Recharge falling deglitch	VFB decreasing above V_{RECHG}		10		ms

ELECTRICAL CHARACTERISTICS (continued)

4.7 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BAT OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Overvoltage rising threshold	As percentage of V_{FB}		104%		
V_{OV_FALL}	Overvoltage falling threshold	As percentage of V_{FB}		102%		
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC overvoltage rising threshold on VCC		31.04	32	32.96	V
V_{ACOV_HYS}	AC overvoltage falling hysteresis			1		V
	AC overvoltage deglitch (both edge)	Delay to changing the STAT pins		1		ms
	AC overvoltage rising deglitch	Delay to disable charge		1		ms
	AC overvoltage falling deglitch	Delay to resume charge		20		ms
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		145		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			15		°C
	Thermal shutdown rising deglitch	Temperature increasing		100		μs
	Thermal shutdown falling deglitch	Temperature decreasing		10		ms
THERMISTOR COMPARATOR						
V_{LTF}	Cold temperature rising threshold	As percentage of V_{VREF}	72.5%	73.5%	74.5%	
V_{LTF_HYS}	Rising hysteresis	As percentage of V_{VREF}	0.2%	0.4%	0.6%	
V_{HTF}	Hot temperature rising threshold	As percentage of V_{VREF}	36.2%	37%	37.8%	
V_{TCO}	Cut-off temperature rising threshold	As percentage of V_{VREF}	33.7%	34.4%	35.1%	
	Deglitch time for temperature out-of-range detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		400		ms
	Deglitch time for temperature in-valid-range detection	$V_{TS} < V_{LTF} – V_{LTF\_HYS}$ or $V_{TS} > V_{TCO}$, or $V_{TS} > V_{HTF}$		20		ms
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{OC}	Charge overcurrent falling threshold	Current rising, in non-synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} < 2 V		45.5		mV
		Current rising, as percentage of $V_{(IREG\_CHG)}$, in synchronous mode, V_{SRP} > 2.2 V		160%		
	Charge overcurrent threshold floor	Minimum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2 V		50		mV
	Charge overcurrent threshold ceiling	Maximum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2 V		180		mV
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{ISYNSET}$	Charge undercurrent falling threshold	Switch from SYNCH to NON-SYNCH, V_{SRP} > 2.2 V	1	5	9	mV
BATTERY SHORTED COMPARATOR (BATSHORT)						
V_{BATSHT}	BAT short falling threshold, forced non-syn mode	V_{SRP} falling		2		V
V_{BATSHT_HYS}	BAT short rising hysteresis			200		mV
V_{BATSHT_DEG}	Deglitch on both edge			1		μs
LOW CHARGE CURRENT COMPARATOR						
V_{LC}	Low charge current (average) falling threshold to force into non-synchronous mode	Measure on $V_{(SRP-SRN)}$		1.25		mV
V_{LC_HYS}	Low charge current rising hysteresis			1.25		mV
V_{LC_DEG}	Deglitch on both edge			1		μs
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	$V_{VCC} > V_{UVLO}$, (0–35 mA load)	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, $V_{VCC} > V_{UVLO}$	35			mA

ELECTRICAL CHARACTERISTICS (continued)

4.7 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 10V, CE = HIGH, (0–40 mA load)	5.7	6.0	6.3	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, V_{VCC} > V_{UVLO}, CE = HIGH	40			mA
TTC INPUT AND SAFETY TIMER						
T_{PRECHG}	Precharge safety timer range(1)	Precharge time before fault occurs	1440	1800	2160	sec
T_{CHARGE}	Fast-charge safety timer range, with ±10% accuracy(1)	Tchg = C_{TTC} × K_{TTC}	1		10	Hr
	Fast-charge timer accuracy(1)	0.01 µF ≤ C_{TTC} ≤ 0.11 µF	–10%		10%	
K_{TTC}	Timer multiplier			5.6		min/nF
	TTC low threshold	V_{TTC} below this threshold disables the safety timer and termination			0.4	V
	TTC oscillator high threshold			1.5		V
	TTC oscillator low threshold			1		V
	TTC source/sink current		45	50	55	µA
BATTERY SWITCH (BATFET) DRIVER						
$R_{DS\_BAT\_OFF}$	BATFET turnoff resistance	V_{ACN} > 5V			150	Ω
$R_{DS\_BAT\_ON}$	BATFET turnon resistance	V_{ACN} > 5V			20	kΩ
V_{BATDRV_REG}	BATFET drive voltage	V_{BATDRV_REG} = V_{ACN} – V_{BATDRV} when V_{ACN} > 5 V and BATFET is on	4.2		7	V
V_{BATFET_ACN}	ACN voltage to keep BATFET on	BATFET on	2.6			V
AC SWITCH (ACFET) DRIVER						
$R_{DS\_AC\_OFF}$	ACFET turnoff resistance	V_{VCC} > 5 V			30	Ω
$R_{DS\_AC\_ON}$	ACFET turnon resistance	V_{VCC} > 5 V			20	kΩ
V_{ACDRV_REG}	ACFET drive voltage	V_{ACDRV_REG} = V_{VCC} – V_{ACDRV} when V_{VCC} > 5 V and ACFET is on	4.2		7	V
AC / BAT MOSFET DRIVERS TIMING						
	Driver dead time	Dead time when switching between AC and BAT		10		µs
BATTERY DETECTION						
t_{WAKE}	Wake time	Maximum time charge is enabled		500		ms
I_{WAKE}	Wake current	R_{SENSE} = 10 mΩ	50	125	200	mA
$t_{DISCHARGE}$	Discharge time	Maximum time discharge current is applied		1		s
$I_{DISCHARGE}$	Discharge current			8		mA
I_{FAULT}	Fault current after a time-out fault			2		mA
V_{WAKE}	Wake threshold (with respect to V_{REG})	Voltage on VFB to detect battery absent during wake		50		mV
V_{DISCH}	Discharge threshold	Voltage on VFB to detect battery absent during discharge		1.55		V
PWM HIGH-SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High-side driver (HSD) turnon resistance	V_{BTST} – V_{PH} = 5.5 V		3.3	6	Ω
$R_{DS\_HI\_OFF}$	High-side driver turnoff resistance	V_{BTST} – V_{PH} = 5.5 V		1	1.3	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BTST} – V_{PH} when low side refresh pulse is requested	4.0	4.2		V
PWM LOW-SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low-side driver (LSD) turnon resistance			4.1	7	Ω
$R_{DS\_LO\_OFF}$	Low-side driver turnoff resistance			1	1.4	Ω

(1) Verified by design

ELECTRICAL CHARACTERISTICS (continued)

4.7 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM DRIVERS TIMING						
	Driver dead time	Dead time when switching between LSD and HSD, no load at LSD and HSD		30		ns
PWM OSCILLATOR						
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of VCC		7		%
	PWM switching frequency(2)		510	600	690	kHz
INTERNAL SOFT START (8 steps to regulation current ICHG)						
	Soft-start steps			8		step
	Soft-start step time			1.6		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power up	Delay from CE = 1 until charger is allowed to turn on		1.5		s
LOGIC IO PIN CHARACTERISTICS (CE, STAT1, STAT2, $\overline{PG}$)						
V_{IN_LO}	CE input-low threshold voltage				0.8	V
V_{IN_HI}	CE input-high threshold voltage		2.1			
V_{BIAS_CE}	CE input bias current	V = 3.3 V (CE has internal 1-MΩ pulldown resistor)			6	μA
V_{OUT_LO}	STAT1, STAT2, $\overline{PG}$ output low saturation voltage	Sink current = 5 mA			0.5	V
I_{OUT_HI}	Leakage current	V = 32 V			1.2	μA

(2) Verified by design

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

	Figure
REF, REGN, and $\overline{PG}$ Power Up (CE = 1)	Figure 3
Charge Enable	Figure 4
Current Soft-Start (CE = 1)	Figure 5
Charge Disable	Figure 6
Continuous-Conduction Mode Switching Waveforms	Figure 7
Cycle-by-Cycle Synchronous to Nonsynchronous	Figure 8
100% Duty and Refresh Pulse	Figure 9
Transient System Load (DPM)	Figure 10
Battery Insertion	Figure 11
Battery-to-Ground Short Protection	Figure 12
Battery-to-Ground Short Transition	Figure 13
Efficiency vs Output Current	Figure 14

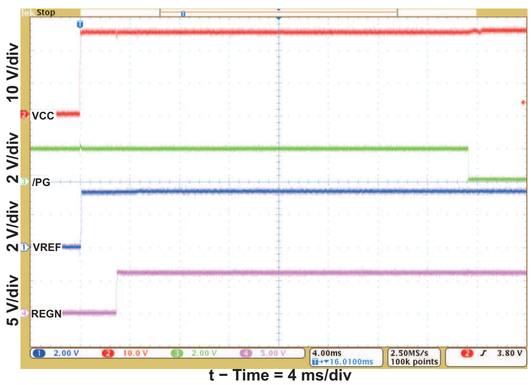


Figure 3. REF, REGN, and $\overline{PG}$ Power Up (CE = 1)

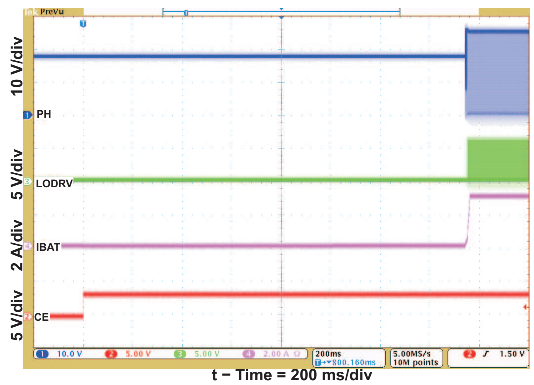


Figure 4. Charge Enable

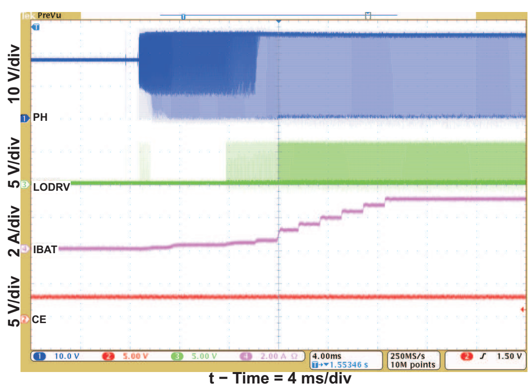


Figure 5. Current Soft-Start (CE = 1)

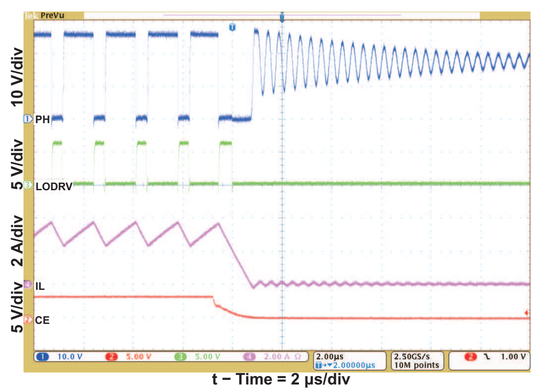


Figure 6. Charge Disable

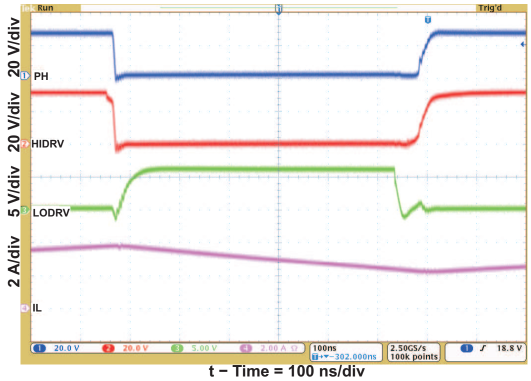


Figure 7. Continuous-Conduction Mode Switching Waveform

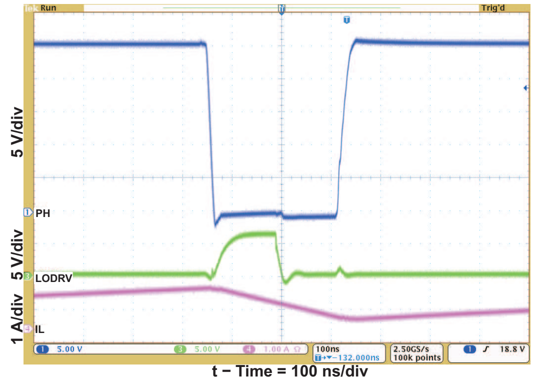


Figure 8. Cycle-by-Cycle Synchronous to Nonsynchronous

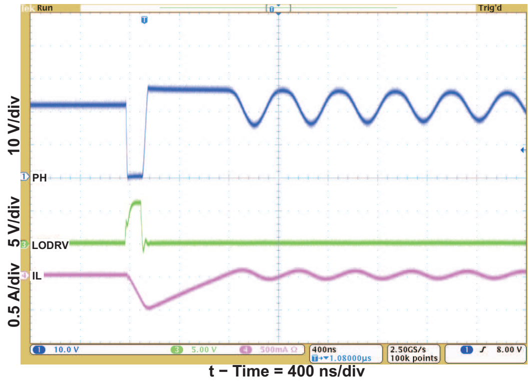


Figure 9. 100% Duty and Refresh Pulse

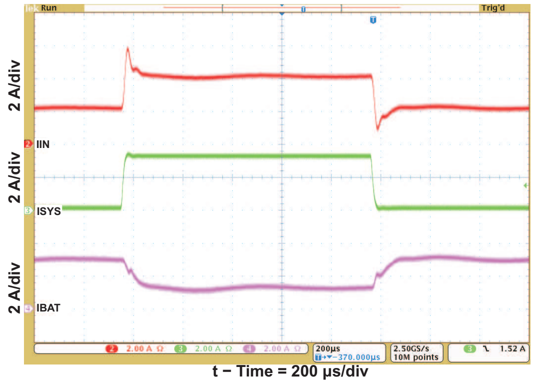


Figure 10. Transient System Load (DPM)

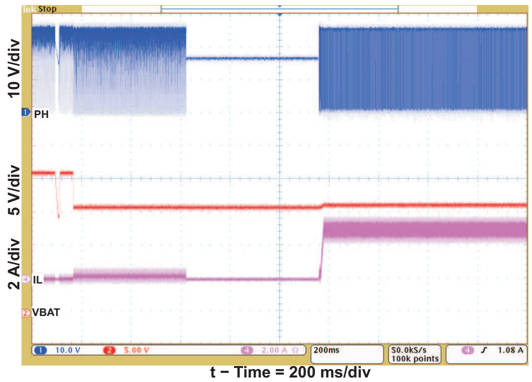


Figure 11. Battery Insertion

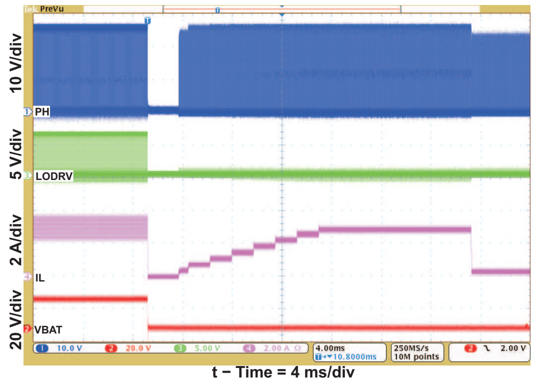


Figure 12. Battery-to-GND Short Protection

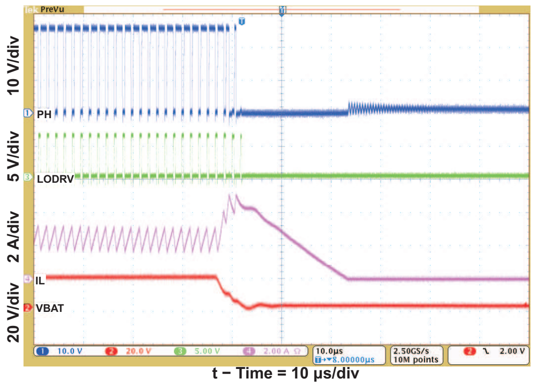


Figure 13. Battery-to-GND Short Transition

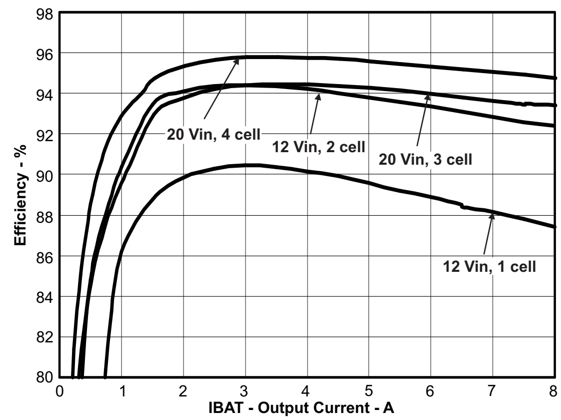


Figure 14. Efficiency vs Output Current

Pin Functions – 24-Pin QFN

PIN NO.	PIN NAME	FUNCTION DESCRIPTION
1	ACN	Adapter current-sense resistor, negative input. A 0.1-μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from the ACN pin to GND for common-mode filtering.
2	ACP	Adapter current-sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from the ACP pin to GND for common-mode filtering.
3	$\overline{\text{ACDRV}}$	AC adapter to system MOSFET driver output. Connect through a 1-kΩ resistor to the gate of the ACFET P-channel power MOSFET and the reverse conduction blocking P-channel power MOSFET. The internal gate drive is asymmetrical, allowing a quick turnoff and slow turnon, in addition to the internal break-before-make logic with respect to $\overline{\text{BATDRV}}$. If needed, an optional capacitor from gate to source of the ACFET is used to slow down the ON and OFF times.
4	CE	Charge-enable active-HIGH logic input. HI enables charge. LO disables charge. It has an internal 1-MΩ pulldown resistor.
5	STAT1	Open-drain charge-status pin to indicate various charger operations (See Table 3)
6	TS	Temperature qualification voltage input for battery-pack negative-temperature-coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to GND. (See Figure 19)
7	TTC	SafetyTimer and termination control. Connect a capacitor from this node to GND to set the timer. When this input is LOW, the timer and termination are disabled. When this input is HIGH, the timer is disabled but termination is allowed.
8	$\overline{\text{PG}}$	Open-drain power-good status output. Active-LOW when IC has a valid VCC (not in UVLO or ACOV or SLEEP mode). Active-HIGH when IC has an invalid VCC. $\overline{\text{PG}}$ can be used to drive an LED or communicate with a host processor.
9	STAT2	Open-drain charge-status pin to indicate various charger operations (See Table 3)
10	VREF	3.3-V regulated voltage output. Place a 1-μF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for programming of voltage and current regulation and for programming the TS threshold.
11	ISET1	Fast-charge current-set input. The voltage on the ISET1 pin programs the fast-charge current-regulation set point.
12	VFB	Output-voltage analog-feedback adjustment. Connect the output of a resistive voltage divider from the battery terminals to this node to adjust the output battery-regulation voltage.
13	SRN	Charge-current sense resistor, negative input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from the SRN pin to GND for common-mode filtering.
14	SRP	Charge-current sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from the SRP pin to GND for common-mode filtering.
15	ISET2	Pre-charge and termination current-set input. The voltage on the ISET2 pin programs the pre-charge current regulation set-point and termination-current trigger point.
16	ACSET	Adapter-current set input. The voltage on the ACSET pin programs the input-current regulation set-point during dynamic power management (DPM).
17	GND	Low-current sensitive analog/digital ground. On PCB layout, connect with thermal pad underneath the IC.
18	REGN	PWM low-side driver positive 6-V supply output. Connect a 1-μF ceramic capacitor from REGN to the GND pin, close to the IC. Use for low-side driver and high-side driver bootstrap voltage by connecting a small-signal Schottky diode from REGN to BTST.
19	LODRV	PWM low-side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
20	PH	PWM high-side driver negative supply. Connect to the phase-switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor).
21	HIDRV	PWM high-side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
22	BTST	PWM high-side driver positive supply. Connect to the phase-switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-μF bootstrap capacitor from PH to BTST, and a bootstrap Schottky diode from REGN to BTST.
23	$\overline{\text{BATDRV}}$	Battery-to-system MOSFET driver output. Gate drive for the battery-to-system load BAT PMOS power FET to isolate the system from the battery to prevent current flow from the system to the battery, while allowing a low-impedance path from battery to system. Connect this pin through a 1-kΩ resistor to the gate of the input BAT P-channel MOSFET. Connect the source of the FET to the system load voltage node. Connect the drain of the FET to the battery pack positive terminal. The internal gate drive is asymmetrical to allow a quick turnoff and slow turnon, in addition to the internal break-before-make logic with respect to $\overline{\text{ACDRV}}$. If needed, an optional capacitor from gate to source of the BATFET is used to slow down the ON and OFF times.
24	VCC	IC power positive supply. Connect through a 10-Ω to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse-blocking power P-channel MOSFET. Place a 1-μF ceramic capacitor from VCC to the GND pin close to the IC.
	Thermal pad	Exposed pad beneath the IC. Always solder the thermal pad to the board, and have vias on the thermal-pad plane star-connecting to GND and to the ground plane for a high-current power converter. It also serves as a thermal pad to dissipate the heat.

BLOCK DIAGRAM

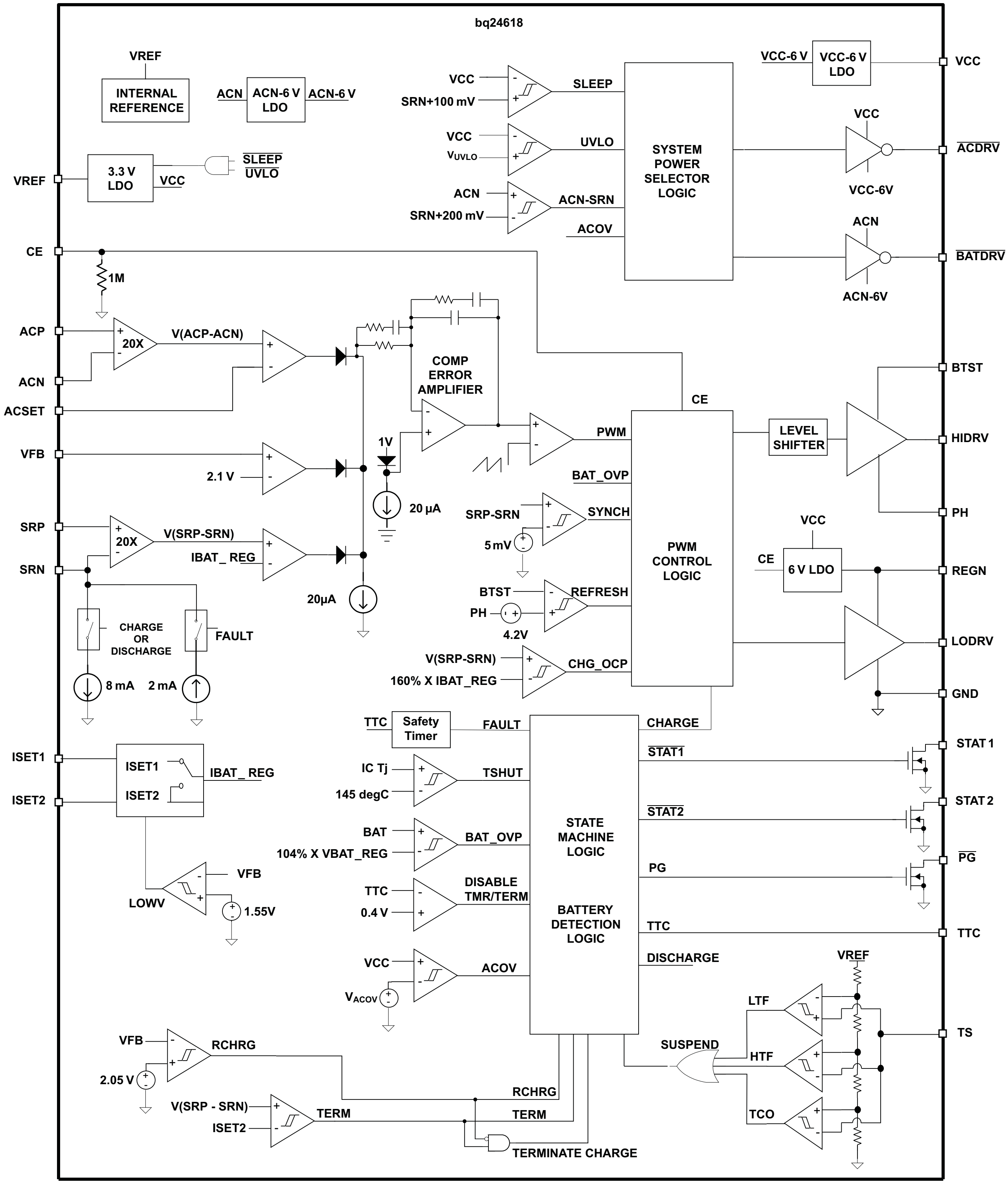


Figure 15. Functional Block Diagram for bq24618

OPERATIONAL FLOWCHART

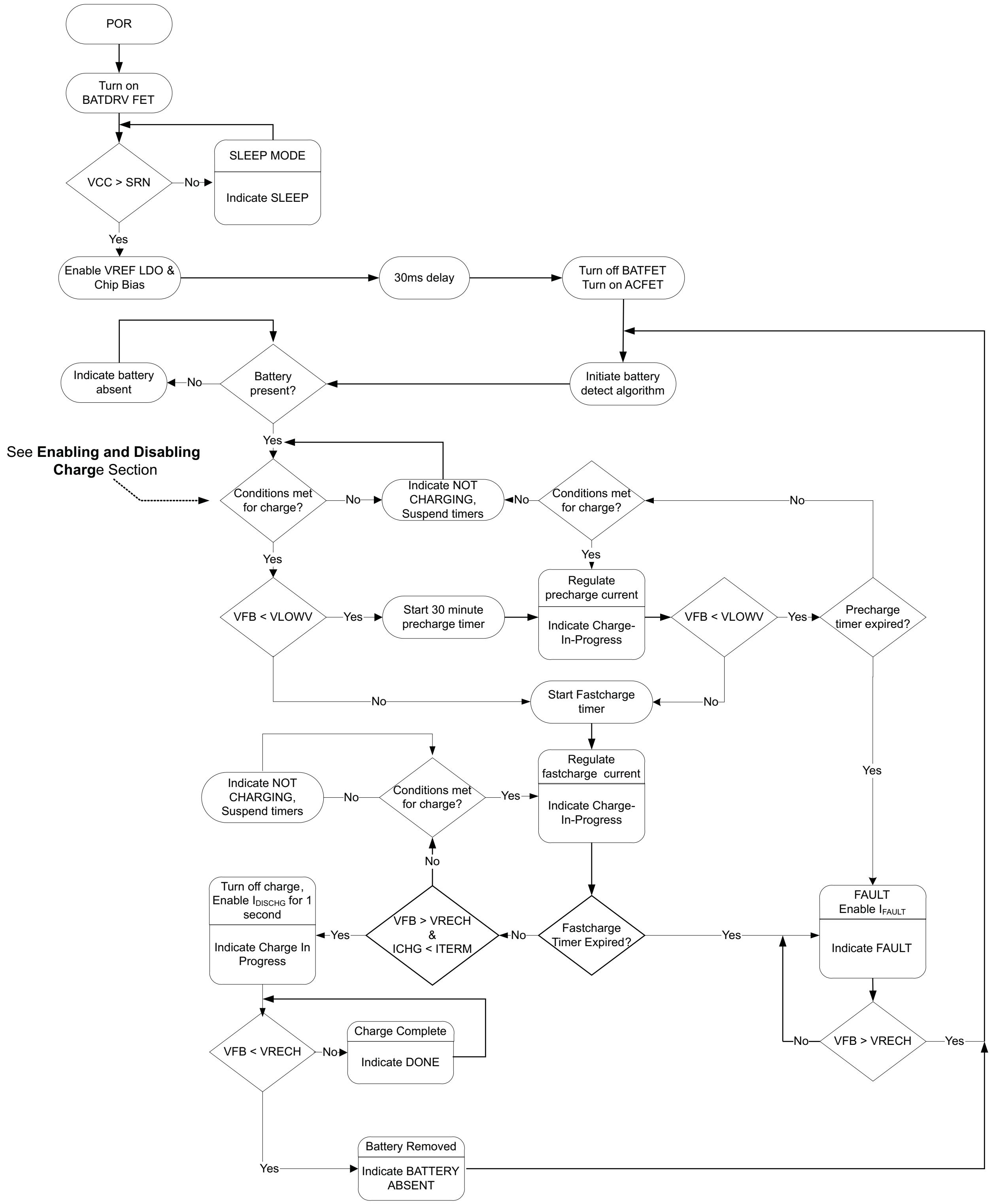


Figure 16. Operational Flowchart

DETAILED DESCRIPTION

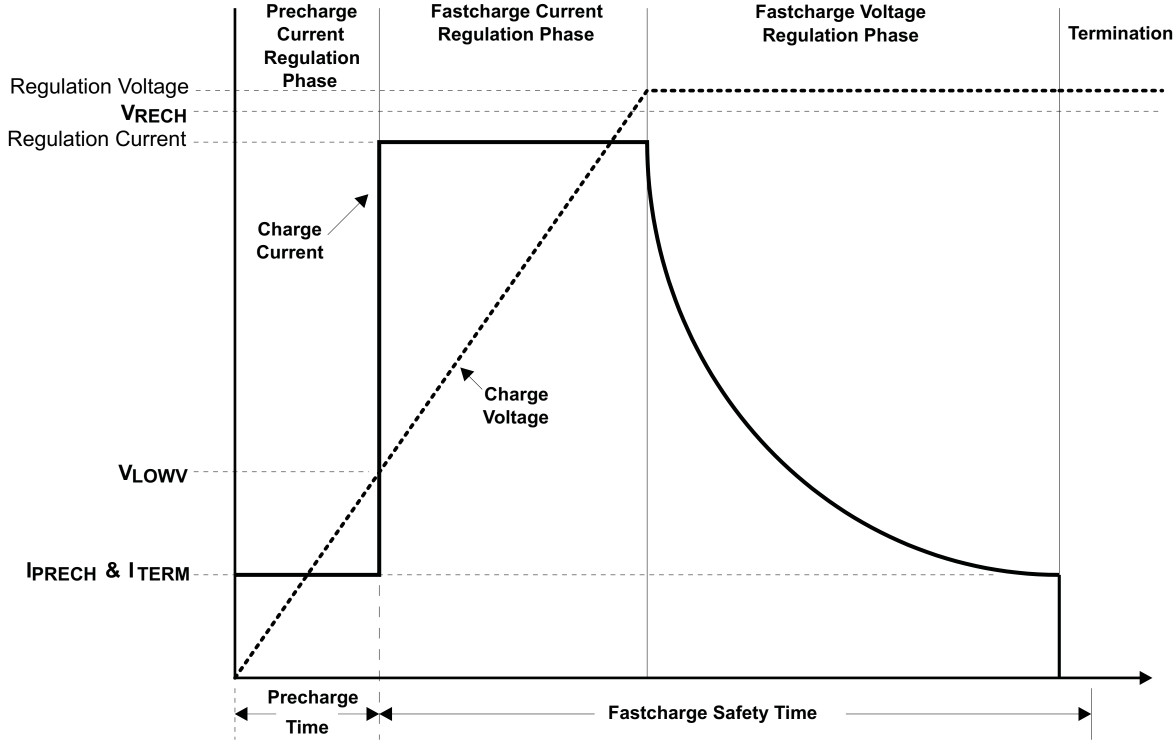


Figure 17. Typical Charging Profile

Battery Voltage Regulation

The bq24618 uses a high-accuracy voltage band gap and regulator for the high charging-voltage accuracy. The charge voltage is programmed via a resistor divider from the battery to ground, with the midpoint tied to the VFB pin. The voltage at the VFB pin is regulated to 2.1 V, giving the following equation for the regulation voltage:

$$V_{BAT} = 2.1\ V \times \left[1 + \frac{R2}{R1}\right], \quad (1)$$

where R2 is connected from VFB to the battery and R1 is connected from VFB to GND.

Battery Current Regulation

The ISET1 input sets the maximum fast-charging current. Battery-charge current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100 mV. Thus, for a 10-mΩ sense resistor, the maximum charging current is 10 A. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET1}}{20 \times R_{SR}} \quad (2)$$

V_{ISET1}, the input voltage range of ISET1, is between 0 V and 2 V. The SRP and SRN pins are used to sense voltage across R_{SR} using the default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor gives a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

Input Adapter Current Regulation

The total input from an ac adapter or other dc source is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without dynamic power management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the battery charger reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capability of the ac adaptor can be lowered, reducing system cost.

Similar to sensing battery regulation current, adaptor current is sensed by resistor R_{AC} connected between ACP and ACN. Its maximum value is set by ACSET using Equation 3:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \tag{3}$$

V_{ACSET}, the input voltage range of ACSET, is between 0 V and 2 V. The ACP and ACN pins are used to sense voltage across R_{AC} using the default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor gives a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

Precharge

On power up, if the battery voltage is below the V_{LOWV} threshold, the bq24618 applies the precharge current to the battery. This feature is intended to revive deeply discharged cells. If the V_{LOWV} threshold is not reached within 30 minutes of initiating precharge, the charger turns off and a FAULT is indicated on the status pins.

The precharge current is determined by the voltage on the ISET2 pin, V_{ISET2}, according to Equation 4.

$$I_{PRECHARGE} = \frac{V_{ISET2}}{100 \times R_{SR}} \tag{4}$$

Charge Termination, Recharge, and Safety Timer

The bq24618 monitors the charging current during the voltage regulation phase. When V_{TTC} is valid, termination is detected while the voltage on the VFB pin is higher than the V_{RECH} threshold AND the charge current is less than the I_{TERM} threshold, as calculated in Equation 5:

$$I_{TERM} = \frac{V_{ISET2}}{100 \times R_{SR}} \tag{5}$$

The input voltage of ISET2 is between 0 V and 2 V. The minimum precharge/termination current is clamped to be around 125 mA with default 10-mΩ sensing resistor. As a safety backup, the bq24618 also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TTC pin and GND, and is given by Equation 6

$$t_{CHARGE} = C_{TTC} \times K_{TTC} \tag{6}$$

where C_{TTC} (range from 0.01µF to 0.11 µF to give 1-h to 10-h safety time) is the capacitor connected from the TTC pin to GND, and K_{TTC} is the constant multiplier (5.6 min/nF).

A new charge cycle is initiated and the safety timer is reset when any of the following conditions occurs:

- The battery voltage falls below the recharge threshold.
- A power-on-reset (POR) event occurs.
- CE is toggled.

The TTC pin may be taken LOW to disable termination and to disable the safety timer. If TTC is pulled to VREF, the bq24618 continues to allow termination but disable the safety timer. TTC taken low resets the safety timer. When ACOV, VCCLOWV, and SLEEP mode resume normal, the safety timer is reset.

Power Up

The bq24618 uses a SLEEP comparator to determine the source of power on the VCC pin, because VCC can be supplied either from the battery or the adapter. If the VCC voltage is greater than the SRN voltage, the bq24618 enables the ACFET and disables BATFET. If all other conditions are met for charging, the bq24618 then attempts to charge the battery (see *Enable and Disable Charging*). If the SRN voltage is greater than VCC, indicating that the battery is the power source, the bq24618 enables the BATFET and enters a low-quiescent-current (<15-µA) SLEEP mode to minimize current drain from the battery.

If VCC is below the UVLO threshold, the device is disabled, ACFET turns off, and BATFET turns on.

Enable and Disable Charging

The following conditions must be valid before charge is enabled:

- CE is HIGH.
- The device is not in undervoltage lockout (UVLO) and not in VCCLOWV mode.
- The device is not in SLEEP mode.
- The VCC voltage is lower than the ac overvoltage threshold (VCC < V_{ACOV}).
- 30-ms delay is complete after initial power up.
- The REGN LDO and VREF LDO voltages are at the correct levels.
- Thermal shut (TSHUT) is not valid.
- TS fault is not detected.

Any of the following conditions will stop ongoing charging:

- CE is LOW.
- Adapter is removed, causing the device to enter UVLO, VCCLOWV, or SLEEP mode.
- Adapter is over voltage.
- The REGN or VREF LDOs are overloaded.
- TSHUT IC temperature threshold is reached (145°C on rising edge with 15°C hysteresis).
- TS voltage goes out of range, indicating the battery temperature is too hot or too cold.
- TTC safety timer times out.

System Power Selector

The bq24618 automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or during SLEEP mode. The battery is disconnected from the system, and then the adapter is connected to the system 30 ms after exiting SLEEP. An automatic break-before-make logic prevents shoot-through currents when the selectors switch.

The $\overline{ACDRV}$ is used to drive a pair of back-to-back p-channel power MOSFETs between the adapter and ACP with sources connected together and to VCC. The FET connected to the adapter prevents reverse discharge from the battery to the adapter when turned off. The p-channel FET with the drain connected to the adapter input provides reverse battery discharge protection when off; and also minimizes system power dissipation with its low $r_{DS(on)}$, compared to a Schottky diode. The other p-channel FET connected to ACP separates the battery from the adapter and provides a limited dI/dt when connecting the adapter to the system by controlling the FET turnon time. The $\overline{BATDRV}$ controls a p-channel power MOSFET placed between BAT and the system.

When an adapter is not detected, the $\overline{ACDRV}$ is pulled to VCC to keep ACFET off, disconnecting the adapter from system. $\overline{BATDRV}$ stays at ACN-6V to connect the battery to the system.

Approximately 30 ms after the device comes out of SLEEP mode, the system begins to switch from battery to adapter. The break-before-make logic keeps both ACFET and BATFET off for 10 µs before ACFET turns on. This prevents shoot-through current or any large discharging current from going into the battery. $\overline{BATDRV}$ is pulled up to ACN and the $\overline{ACDRV}$ pin is set to VCC-6V by an internal regulator to turn on p-channel ACFET, connecting the adapter to the system.

When the adapter is removed, the system waits until VCC drops back to within 200 mV above SRN to switch from the adapter back to the battery. The break-before-make logic still keeps 10-µs dead time. The $\overline{ACDRV}$ is pulled up to VCC and the $\overline{BATDRV}$ pin is set to ACN-6V by an internal regulator to turn on p-channel BATFET, connecting the battery to the system.

Asymmetrical gate drive (fast turnoff and slow turnon) for the $\overline{\text{ACDRV}}$ and $\overline{\text{BATDRV}}$ drivers provides fast turn-off and slow turn-on of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turnon of either FET. The soft-start time can be further increased by putting a capacitor from the gate to the source of the p-channel power MOSFETs.

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger goes into fast-charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping up the charge regulation current in eight evenly divided steps up to the programmed charge current. Each step lasts around 1.6 ms, for a typical rise time of 12.8 ms. No external components are needed for this function.

Converter Operation

The synchronous buck PWM converter uses a fixed-frequency voltage mode with a feed-forward control scheme. A type-III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected to give a resonant frequency of 12 kHz–17 kHz for the bq24618, where the resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} \tag{7}$$

An internal sawtooth ramp is compared to the internal EAO error control signal to vary the duty cycle of the converter. The ramp height is 7% of the input adapter voltage, making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage and simplifies the loop compensation. The ramp is offset by 300 mV in order to allow zero-percent duty cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the sawtooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate-drive logic allows achieving 99.5% duty cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.2 V for more than three cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the BTST-to-PH voltage is detected to fall low again due to leakage current discharging the BTST capacitor below 4.2 V, and the reset pulse is reissued.

The fixed-frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. Also see the *Application Information* section for selection of the inductor, capacitor, and MOSFET.

Synchronous and Non-Synchronous Operation

The charger operates in synchronous mode when the SRP-SRN voltage is above 5 mV (0.5-A inductor current for a 10-mΩ sense resistor). During synchronous mode, the internal gate-drive logic ensures there is break-before-make complementary switching to prevent shoot-through currents. During the 30-ns dead time where both FETs are off, the body diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn on keeps the power dissipation low and allows safely charging at high currents. During synchronous mode, the inductor current is always flowing and the converter operates in continuous-conduction mode (CCM), creating a fixed two-pole system.

The charger operates in non-synchronous mode when the SRP-SRN voltage is below 5 mV (0.5-A inductor current for a 10-mΩ sense resistor). The charger is forced into non-synchronous mode when battery voltage is lower than 2 V or when the average SRP-SRN voltage is lower than 1.25 mV.

During non-synchronous operation, the body diode of the low-side MOSFET can conduct the positive inductor current after the high-side n-channel power MOSFET turns off. When the load current decreases and the inductor current drops to zero, the body diode is naturally turned off and the inductor current becomes discontinuous. This mode is called discontinuous-conduction mode (DCM). During DCM, the low-side n-channel power MOSFET turns on for around 80 ns when the bootstrap capacitor voltage drops below 4.2 V. Then the low-side power MOSFET turns off and stays off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80-ns low-side MOSFET on-time is required to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80-ns low-side pulse pulls the PH node (the connection between high- and low-side MOSFETs) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring.

At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80-ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance. Whenever the converter goes into zero-percent duty cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (only 80-ns recharge pulse) either, and there is almost no discharge from the battery.

During the DCM mode, the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage.

Cycle-by-Cycle Charge Undercurrent Protection

If the SRP-SRN voltage decreases below 5 mV (the charger is also forced into non-synchronous mode when the average SRP-SRN voltage is lower than 1.25 mV), the low-side FET is turned off for the remainder of the switching cycle to prevent negative inductor current. During DCM, the low-side FET only turns on for around 80 ns when the bootstrap capacitor voltage drops below 4.2 V to provide refresh charge for the bootstrap capacitor. This is important to prevent negative inductor current from causing a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors and leads to an overvoltage stress on the VCC node, potentially causing damage to the system.

Input Overvoltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. Once the adapter voltage reaches the ACOV threshold, charge is disabled and the system is switched to the battery instead of the adapter.

Input Undervoltage Lockout (UVLO)

The system must have a minimum VCC voltage to allow proper operation. This VCC voltage could come from either the input adapter or the battery, because a conduction path exists from the battery to VCC through the high-side NMOS body diode. When VCC is below the UVLO threshold, all circuits on the IC are disabled, and the gate-drive bias to ACFET and BATFET is disabled.

Battery Overvoltage Protection

The converter does not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an overvoltage condition, such as occurs when the load is removed or the battery is disconnected. An 8-mA current sink from SRP to GND is on only during charge and allows discharging the stored output inductor energy that is transferred to the output capacitors. BATOVP also suspends the safety timer.

Cycle-by-Cycle Charge Overcurrent Protection

The charger has secondary cycle-to-cycle overcurrent protection. It monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold.

Thermal Shutdown Protection

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperature low. As an added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C; then the charger soft-starts again if all other charge enabling conditions are valid. Thermal shutdown also suspends the safety timer.

Temperature Qualification

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} and V_{HTF} thresholds. If battery temperature is outside of this range, the controller suspends charge and the safety timer and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. During the charge cycle, the battery temperature must be within the V_{LTF} and V_{TCO} thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. The controller suspends charge by turning off the PWM charge FETs. Figure 18 summarizes the operation.

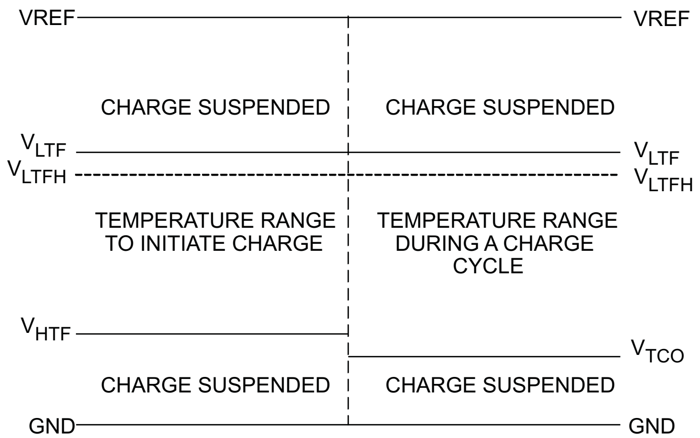


Figure 18. TS Pin, Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 1, the values of RT1 and RT2 can be determined by using the following equations:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1 \right)} \quad (8)$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (9)$$

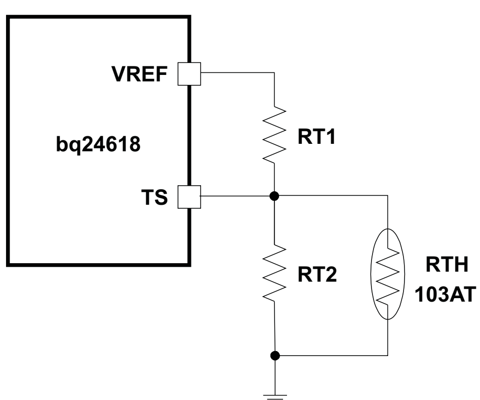


Figure 19. TS Resistor Network

For example, 103AT NTC thermistors are used to monitor the battery pack temperature. Selecting T_{COLD} = 0ºC and T_{CUT_OFF} = 45ºC gives R_{T2} = 430 kΩ and R_{T1} = 9.31 kΩ. A small RC filter is suggested to use for system-level ESD protection.

Timer Fault Recovery

The bq24618 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: The battery voltage is above the recharge threshold and a time-out fault occurs.

Recovery Method: The timer fault clears when the battery voltage falls below the recharge threshold, and battery detection begins. A POR condition or taking CE low also clears the fault.

Condition 2: The battery voltage is below the recharge threshold and a time-out fault occurs.

Recovery Method: Under this scenario, the bq24618 applies the I_{FAULT} current to the battery. This small current is used to detect a battery-removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the bq24618 disables the fault current and executes the recovery method described in Condition 1. A POR condition or taking CE low also clears the fault.

$\overline{\text{PG}}$ Output

The open-drain $\overline{\text{PG}}$ (power-good) output indicates whether the VCC voltage is valid or not. The open-drain FET turns on whenever the bq24618 has a valid VCC input (not in UVLO or ACOV or SLEEP mode). The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor.

CE (Charge Enable)

The CE digital input is used to disable or enable the charge process. A high-level signal on this pin enables charge, provided all the other conditions for charge are met (see *Enable and Disable Charging*). A high-to-low transition on this pin also resets all timers and fault conditions. There is an internal 1-MΩ pulldown resistor on the CE pin, so if CE is floated, the charge does not turn on.

Inductor, Capacitor, and Sense Resistor Selection Guidelines

The bq24618 provides internal loop compensation. With this scheme, best stability occurs when the LC resonant frequency, f_o, is approximately 12 kHz–17 kHz for the bq24618.

The following table provides a summary of typical LC components for various charge currents:

Table 2. Typical Inductor, Capacitor, and Sense Resistor Values as a Function of Charge Current for bq24618 (600-kHz Switching Frequency)

CHARGE CURRENT	2 A	4 A	6 A	8 A	10 A
Output inductor L_O	6.8 µH	6.8 µH	4.7 µH	3.3 µH	3.3 µH
Output capacitor C_O	20 µF	20 µF	30 µF	40 µF	40 µF
Sense resistor	10 mΩ	10 mΩ	10 mΩ	10 mΩ	10 mΩ

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 3. These status pins can be used to drive LEDs or communicate with the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 3. STAT Pin Definition for bq24618

CHARGE STATE	STAT1	STAT2
Charge in progress	ON	OFF
Charge complete	OFF	ON
Charge suspend, timer fault, overvoltage, sleep mode, battery absent	OFF	OFF

Battery Detection

For applications with removable battery packs, the bq24618 provides a battery-absent detection scheme to reliably detect insertion or removal of battery packs.

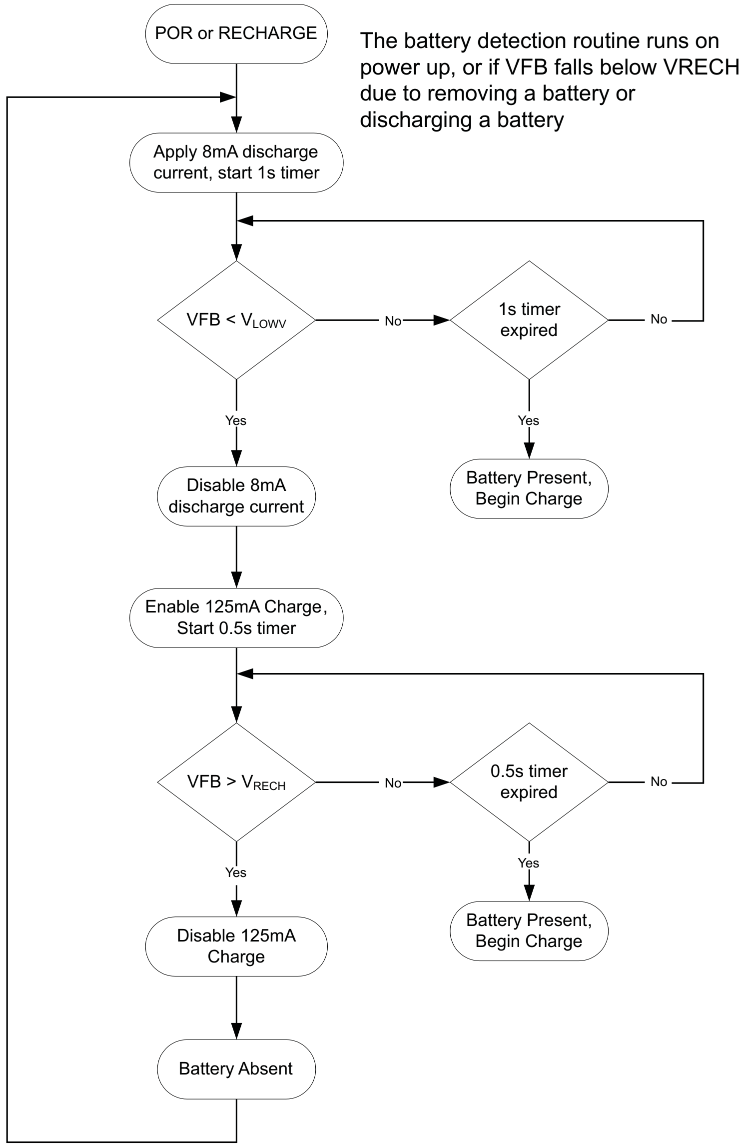


Figure 20. Battery-Detection Flowchart

Once the device has powered up, an 8-mA discharge current is applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125 mA). If the battery voltage rises above the recharge threshold within 500 ms, there is no battery present and the cycle restarts. If either the 500-ms or 1-second timer times out before its respective threshold is hit, a battery is detected and a charge cycle is initiated.

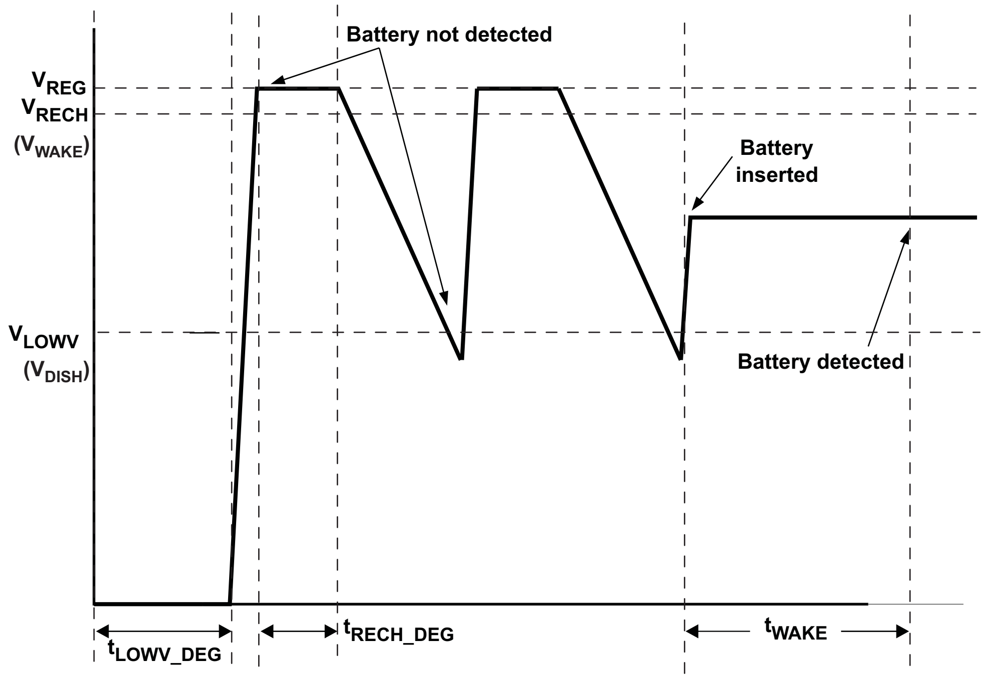


Figure 21. Battery-Detect Timing Diagram

Care must be taken that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the voltage below the LOWV threshold during the 1-second discharge time. The maximum output capacitance can be calculated as follows:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{0.5 \times \left[1 + \frac{R_2}{R_1}\right]} \quad (10)$$

where C_{MAX} is the maximum output capacitance, I_{DISCH} is the discharge current, t_{DISCH} is the discharge time, and R_2 and R_1 are the voltage feedback resistors from the battery to the VFB pin. The 0.5 factor is the difference between the RECHARGE and the LOWV thresholds at the VFB pin.

Example

For a three-cell Li+ charger, with R2 = 500 kΩ, R1 = 100 kΩ (giving 12.6 V for voltage regulation), I_{DISCH} = 8 mA, t_{DISCH} = 1 second,

$$C_{MAX} = \frac{8\text{mA} \times 1\text{sec}}{0.5 \times \left[1 + \frac{500\text{k}}{100\text{k}}\right]} = 2.7\ \text{mF} \quad (11)$$

Based on these calculations, no more than 2.7 mF should be allowed on the battery node for proper operation of the battery-detection circuit.

Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	2	P-channel MOSFET, –30 V, –35 A, PowerPAK 1212-8, Vishay-Siliconix, Si7617DN
Q4, Q5	2	N-channel MOSFET, 30 V, 12 A, PowerPAK 1212-8, Vishay-Siliconix, Sis412DN
D1	1	Diode, dual Schottky, 30 V, 200 mA, SOT23, Fairchild, BAT54C
D2, D3, D4	3	LED diode, green, 2.1 V, 20 mA, LTST-C190GKT
R_{AC}, R_{SR}	2	Sense resistor, 10 mΩ, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 6.8 µH, 5.5 A, Vishay-Dale IHLP2525CZ
C8, C9, C12, C13	4	Capacitor, ceramic, 10 µF, 35 V, 20%, X7R
C4, C5	2	Capacitor, ceramic, 1 µF, 16 V, 10%, X7R
C1, C3, C6, C11	4	Capacitor, ceramic, 0.1 µF, 16 V, 10%, X7R
C2, C10	2	Capacitor, ceramic, 0.1 µF, 50 V, 10%, X7R
C7	1	Capacitor, ceramic, 1 µF, 50 V, 10%, X7R
C14, C15 (Optional)	2	Capacitor, ceramic, 0.1 µF, 50 V, 10%, X7R
C16	1	Capacitor, ceramic, 2.2 µF, 35V, 10%, X7R
C_{ff}	1	Capacitor, ceramic, 22 pF, 25V, 10%, X7R
C_{TTC}	1	Capacitor, ceramic, 0.056 µF, 16V, 5%, X7R
R1, R3, R5, R7	4	Resistor, chip, 100 kΩ, 1/16 W, 0.5%
R2	1	Resistor, chip, 500 kΩ, 1/16 W, 0.5%
R4	1	Resistor, chip, 32.4 kΩ, 1/16 W, 0.5%
R6	1	Resistor, chip, 10 kΩ, 1/16 W, 0.5%
R8	1	Resistor, chip, 22.1 kΩ, 1/16 W, 0.5%
R9	1	Resistor, chip, 9.31 kΩ, 1/16 W, 1%
R10	1	Resistor, chip, 430 kΩ, 1/16 W, 1%
R11, R12, R13, R18, R19	5	Resistor, chip, 10 kΩ, 1/16 W, 5%
R14, R15 (optional)	2	Resistor, chip, 100 kΩ, 1/16 W, 5%
R16	1	Resistor, chip, 100 Ω, 1/16 W, 5%
R17	1	Resistor, chip, 10 Ω, 1/4 W, 5%
R20	1	Resistor, chip, 2 Ω, 1 W, 5%

APPLICATION INFORMATION

Inductor Selection

The bq24618 has a 600-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{12}$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \tag{13}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for a three-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is a four-cell battery, where the battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of 20%–40% of maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The bq24618 has cycle-by-cycle charge undercurrent protection (UCP) by monitoring the charge current-sensing resistor to prevent negative inductor current. The typical UCP threshold is 5 mV falling edge, corresponding to 0.5 A falling edge for a 10-mΩ charge current-sensing resistor.

Input Capacitor

The input capacitor should have enough ripple-current rating to absorb the input-switching ripple current. The worst-case rms ripple current is half of the charging current when the duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst-case capacitor rms current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{14}$$

A low-ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25-V rating or higher capacitor is preferred for 20-V input voltage. A 10-μF to 20-μF capacitor is suggested for typical 3-A to 4-A charging current.

Output Capacitor

The output capacitor also should have enough ripple-current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{15}$$

The output-capacitor voltage ripple can be calculated as follows:

$$\Delta V_o = \frac{1}{8LCf_s^2}\left(V_{BAT} - \frac{V_{BAT}^2}{V_{IN}}\right) \tag{16}$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The bq24618 has an internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 12 kHz and 17 kHz. The preferred ceramic capacitor is 25-V or higher rating, X7R or X5R for four-cell applications.

Power MOSFET Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6 V of gate drive voltage. MOSFETs of 30-V or higher voltage rating are preferred for 20-V input voltage and 40-V or higher rating MOSFETs are preferred for 20-V to 28-V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper the MOSFET, based on a trade-off between the conduction loss and switching loss. For a top-side MOSFET, FOM is defined as the product of a MOSFET on-resistance, $r_{DS(on)}$, and the gate-to-drain charge, Q_{GD}. For a bottom-side MOSFET, FOM is defined as the product of the MOSFET on-resistance, $r_{DS(on)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD} \qquad FOM_{bottom} = R_{DS(on)} \times Q_G \tag{17}$$

The lower the FOM value, the lower the total power loss. Usually, lower $r_{DS(on)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle (D = V_{OUT}/V_{IN}), charging current (I_{CHG}), MOSFET on-resistance $r_{DS(on)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times \left(t_{on} + t_{off}\right) \times f_S \tag{18}$$

The first item represents the conduction loss. Usually MOSFET $r_{DS(on)}$ increases by 50% with a 100ºC junction-temperature rise. The second term represents the switching loss. The MOSFET turnon and turnoff times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}},\ t_{off} = \frac{Q_{SW}}{I_{off}} \tag{19}$$

where Q_{sw} is the switching charge, I_{on} is the turnon gate-drive current, and I_{off} is the turnoff gate-drive current. If the switching charge is not given in the MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{20}$$

Total gate-drive current can be estimated by the REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turnon gate resistance (R_{on}) and turnoff gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}},\ I_{off} = \frac{V_{plt}}{R_{off}} \tag{21}$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous-conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \tag{22}$$

If the SRP-SRN voltage decreases below 5 mV (the charger is also forced into non-synchronous mode when the average SRP-SRN voltage is lower than 1.25 mV), the low-side FET is turned off for the remainder of the switching cycle to prevent negative inductor current.

As a result, all the freewheeling current goes through the body diode of the bottom-side MOSFET. The maximum charging current in non-synchronous mode can be up to 0.9 A (0.5 A typ.) for a 10-mΩ charging current-sensing resistor, considering IC tolerance. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

MOSFET gate-driver power loss contributes to the dominant losses on the controller IC when the buck converter is switching. Choosing a MOSFET with a small Q_{g_total} reduces the IC power loss to avoid thermal shutdown.

$$P_{ICLoss\_driver} = V_{IN} \cdot Q_{g\_total} \cdot f_s \tag{23}$$

where Q_{g_total} is the total gate charge for both upper and lower MOSFET at 6V V_{REGN}

Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second-order system. The voltage spike at the VCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an overvoltage event on the VCC pin. The ACP/ACN pin must be placed after the input ACFET in order to avoid overvoltage stress on these pins during hot-plug-in.

There are several methods to damping or limiting the overvoltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the overvoltage spike well below the IC maximum pin-voltage rating. A high-current-capability TVS Zener diode can also limit the overvoltage level to an IC-safe level. However, these two solutions may not have low cost or small size.

A cost-effective and small-size solution is shown in Figure 22. R1 and C1 comprise a damping RC network to damp the hot plug-in oscillation. As a result, the overvoltage spike is limited to a safe level. D1 is used for reverse voltage protection for the VCC pin (it can be the body diode of the input ACFET). C2 is a VCC pin decoupling capacitor, and it should be placed as close as possible to the VCC pin. R2 and C2 form a damping RC network to further protect the IC from high-dv/dt and high-voltage spikes. The C2 value should be less than the C1 value so R1 can be dominant over the ESR orf C1 to get enough damping effect for hot plug-in. The R1 and R2 packages must be sized to handle the inrush-current power loss according to the resistor manufacturer's datasheet. The filter component values always must be verified with the real application, and minor adjustments may be needed to fit in the real application circuit.

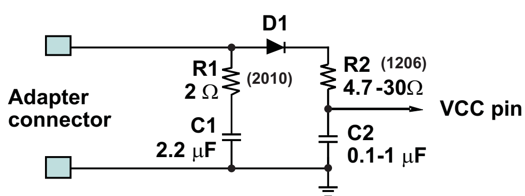


Figure 22. Input Filter

PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize the high-frequency current-path loop (see Figure 23) is important to prevent electrical and magnetic field radiation and high-frequency resonance problems. Here is a PCB layout priority list for proper layout. Layout of the PCB according to this specific order is essential.

1. Place the input capacitor as close as possible to the switching MOSFET supply and ground connections, and use the shortest-possible copper trace connection. These parts should be placed on the same layer of PCB, instead of on different layers using vias to make the connection.
2. The IC should be placed close to the switching MOSFET gate terminals to keep the gate-drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB from the switching MOSFETs.
3. Place the inductor input terminal as close as possible to the switching MOSFET output terminal. Minimize the copper area of this trace to lower electrical and magnetic field radiation, but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging-current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in the same layer, close to each other (minimize loop area), and do not route the sense leads through a high-current path (see Figure 24 for the Kelvin connection for best current accuracy). Place decoupling capacitors on these traces next to the IC.
5. Place the output capacitor next to the sensing resistor output and ground.
6. The output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.

7. Route the analog ground separately from the power ground and use a single ground connection to tie the charger power ground to the charger analog ground. Just beneath the IC, use the copper pour for analog ground, but avoid the power pins to reduce inductive and capacitive noise coupling. Connect the analog ground to GND. Connect the analog ground and power ground together using the thermal pad as the single ground connection point. Alternatively, use a 0-Ω resistor to tie the analog ground to power ground (the thermal pad should tie to analog ground in this case). A star-connection under the thermal pad is highly recommended.
8. It is critical that the exposed thermal pad on the back side of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC connecting to the ground plane on the other layers.
9. Place decoupling capacitors next to the IC pins, and make the trace connection as short as possible.
10. All via sizes and numbers should be adequate for a given current path.

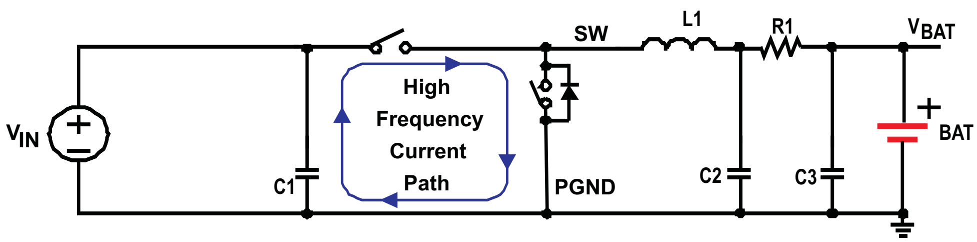


Figure 23. High Frequency Current Path

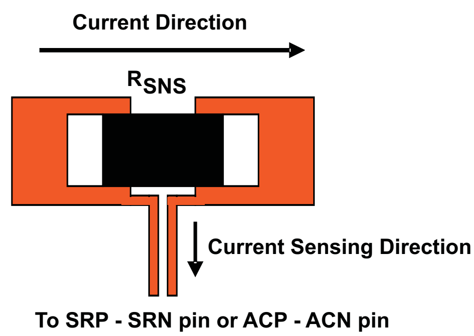


Figure 24. Sensing Resistor PCB Layout

See the EVM design (SLUU396) for recommended component placement with trace and via locations.

For QFN information, see SCBA017 and SLUA271.

REVISION HISTORY

Changes from Revision Original (October 2010) to Revision A	Page
• Changed descriptions for PH and BTST pins	13
• Corrected Equation 8	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ24618RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24618RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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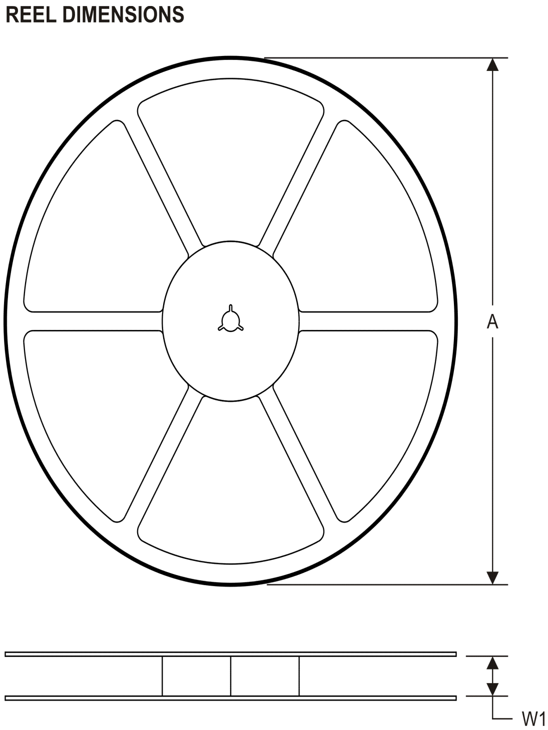
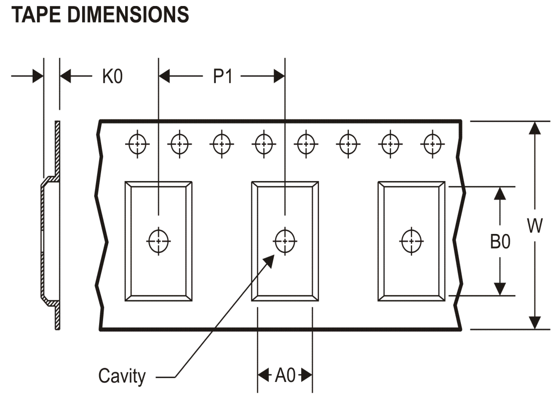
TAPE AND REEL INFORMATION





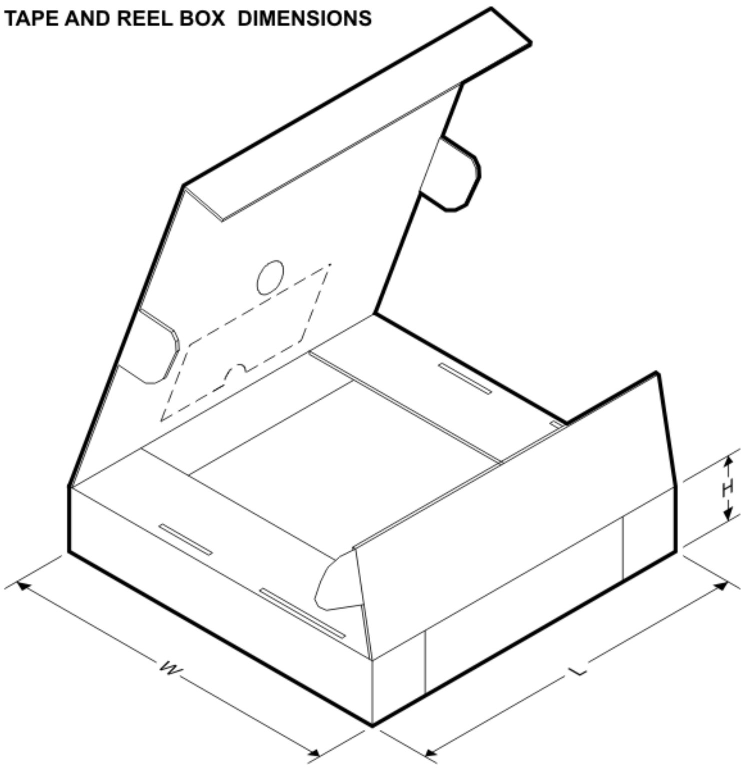
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24618RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24618RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24618RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24618RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

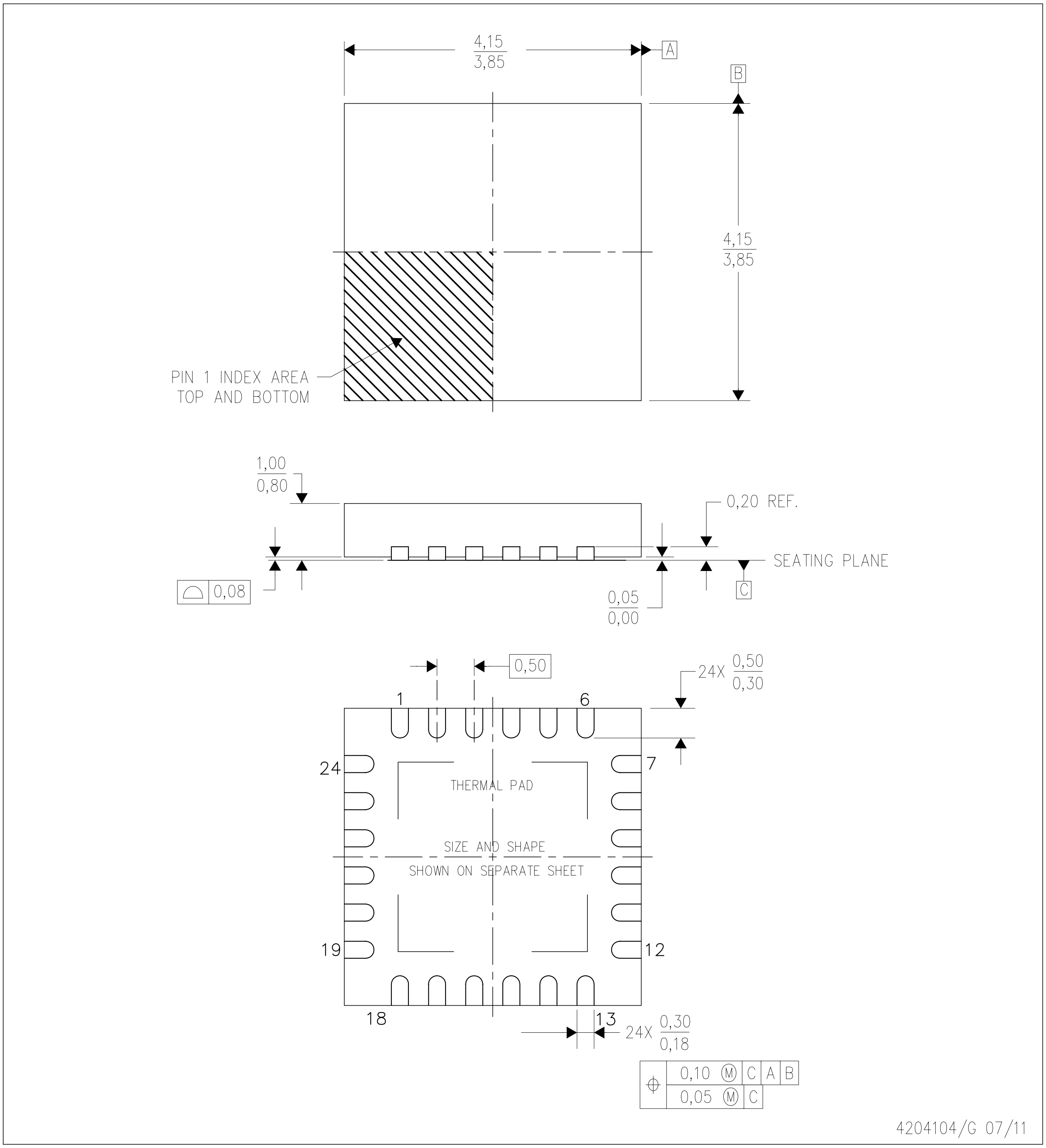
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24618RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24618RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24618RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24618RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

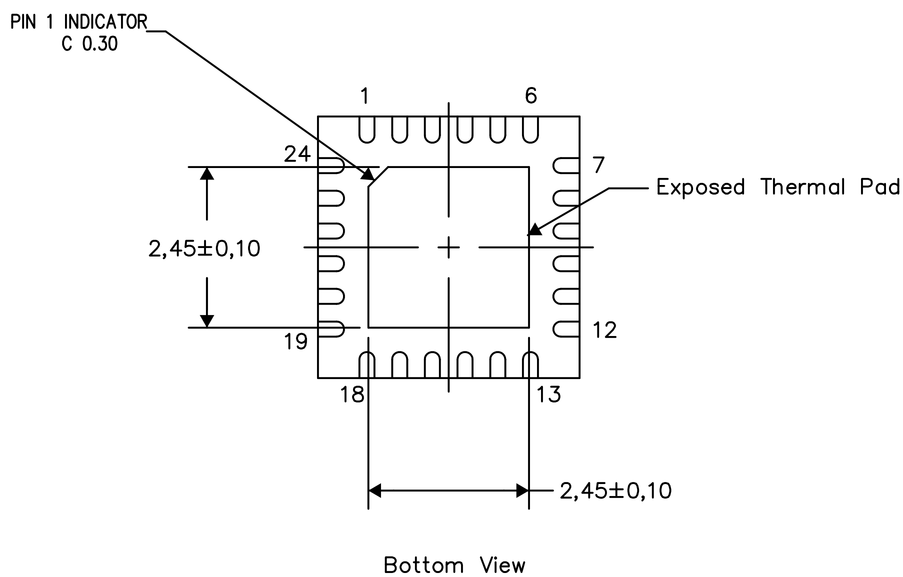
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

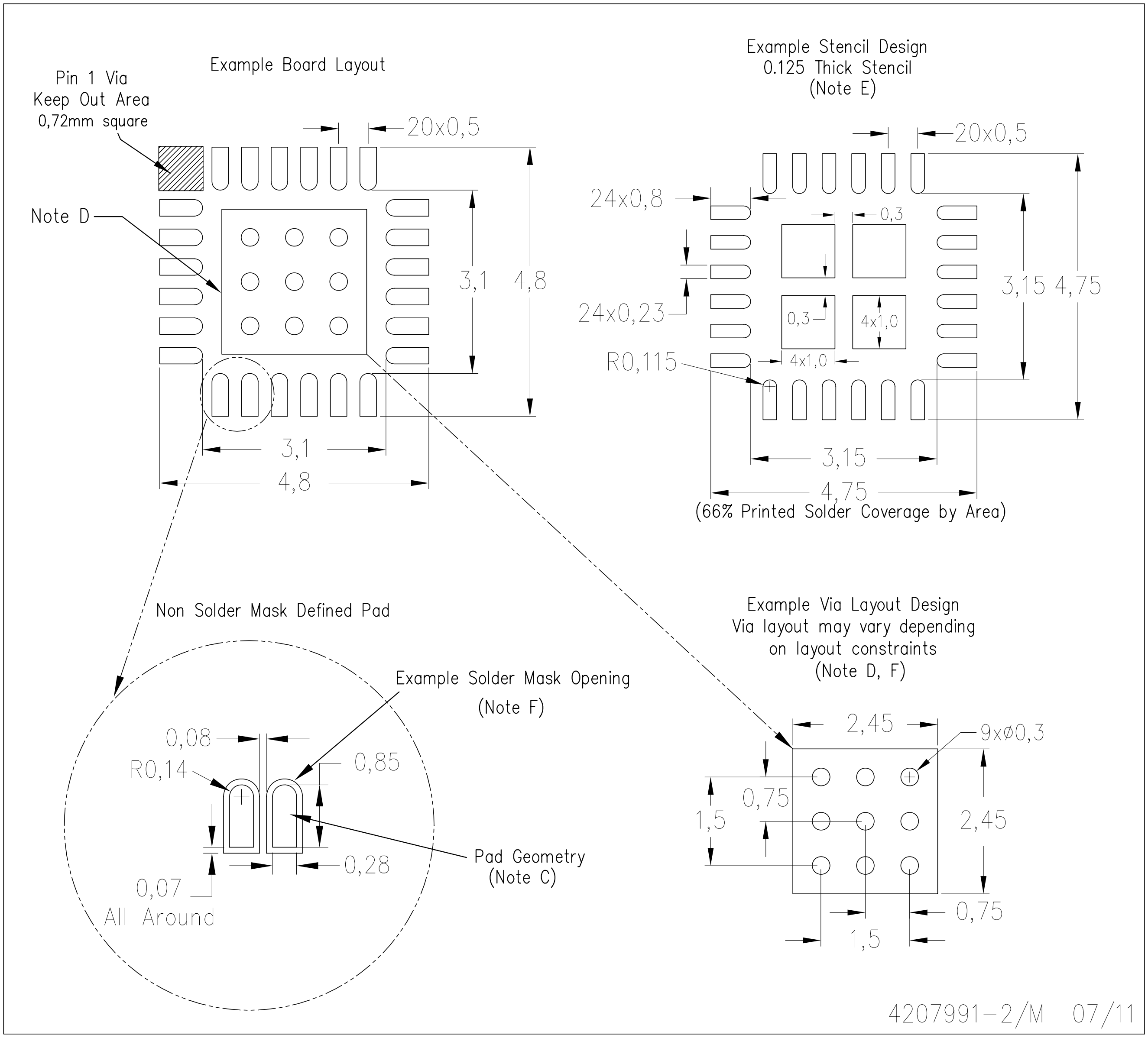


Exposed Thermal Pad Dimensions

4206344-3/AA 04/12

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.