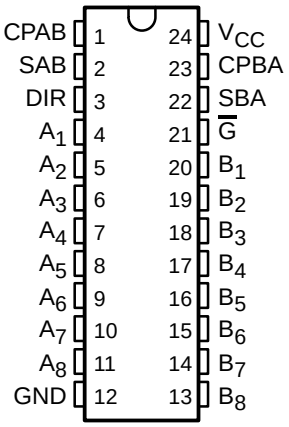
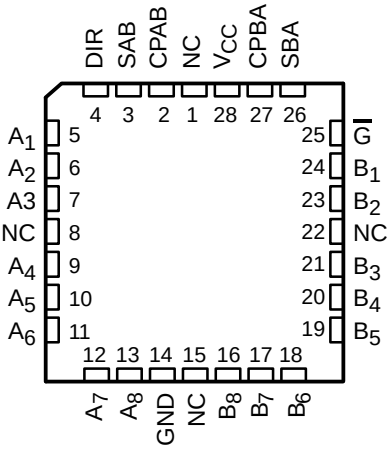
- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Independent Register for A and B Buses**
- **CY54FCT646T**
  - **48-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT646T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**
- **3-State Outputs**

CY54FCT646T . . . D PACKAGE
CY74FCT646T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT646T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’FCT646T devices consist of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers as the appropriate clock pin goes to a high logic level. Output-enable ($\overline{G}$) and direction (DIR) inputs control the transceiver function. In the transceiver mode,data present at the high-impedance port can be stored in either the A or B register, or in both. Select controls (SAB, SBA) can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{G}$ is low. In the isolation mode ($\overline{G}$ is high), A data can be stored in the B register and/or B data can be stored in the A register.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
A	Data register A inputs, data register B outputs
B	Data register B inputs, data register A outputs
CPAB, CPBA	Clock-pulse inputs
SAB, SBA	Output data-source-select inputs
DIR, $\overline{G}$	Output-enable inputs

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.4	CY74FCT646CTQCT	FCT646C
	SOIC – SO	Tube	5.4	CY74FCT646CTSOC	FCT646C
		Tape and reel	5.4	CY74FCT646CTSOCT	
	QSOP – Q	Tape and reel	6.3	CY74FCT646ATQCT	FCT646A
	SOIC – SO	Tube	6.3	CY74FCT646ATSOC	FCT646A
		Tape and reel	6.3	CY74FCT646ATSOCT	
	QSOP – Q	Tape and reel	9	CY74FCT646TQCT	FCT646
	SOIC – SO	Tube	9	CY74FCT646TSOC	FCT646
		Tape and reel	9	CY74FCT646TSOCT	
–55°C to 125°C	LCC – L	Tube	6	CY54FCT646CTLMB	
	CDIP – D	Tube	7.7	CY54FCT646ATDMB	
	LCC – L	Tube	7.7	CY54FCT646ATLMB	
		Tube	11	CY54FCT646TLMB	

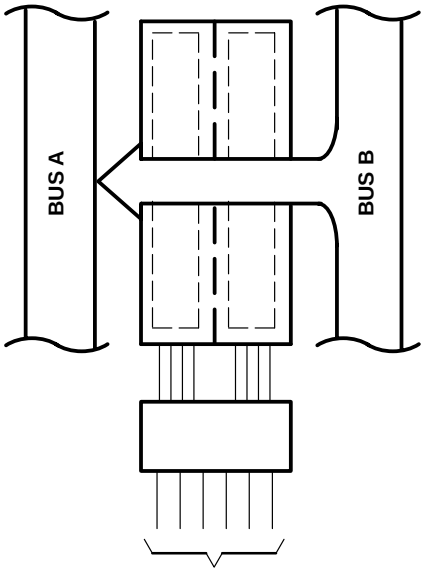
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS						DATA I/O‡		OPERATION OR FUNCTION
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1–A_8	B_1–B_8	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

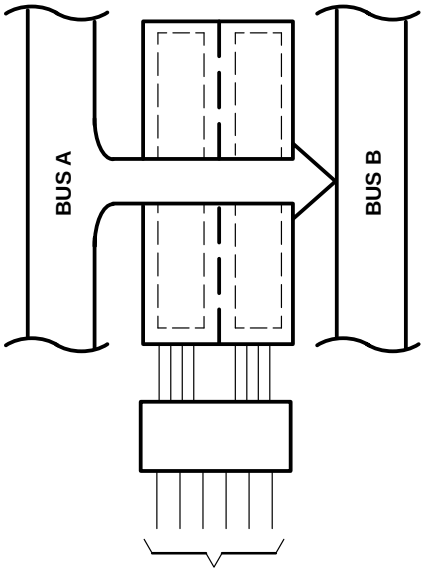
H = High logic level, L = Low logic level, ↑ = Low-to-high transition, X = Don't care

‡ The data output functions can be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



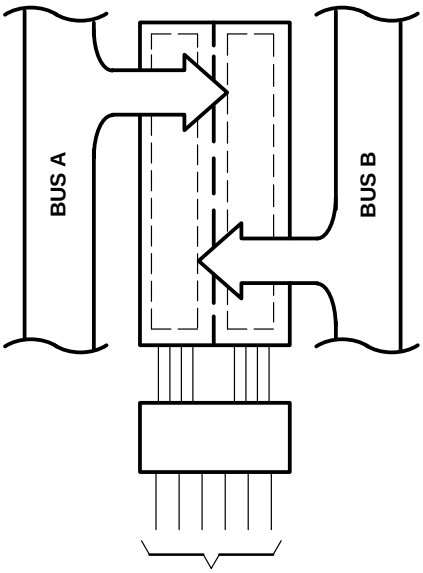
21	3	1	23	2	22
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



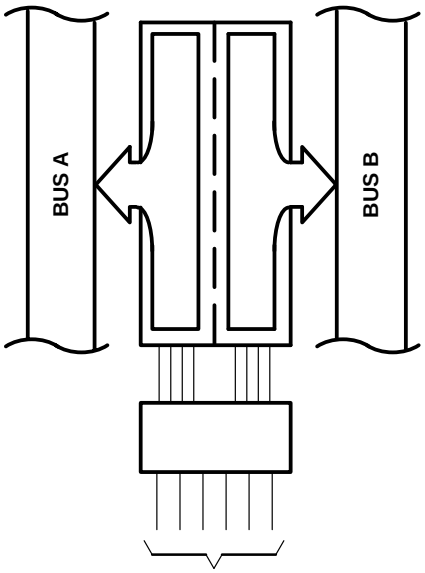
21	3	1	23	2	22
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21	3	1	23	2	22
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A AND/OR B



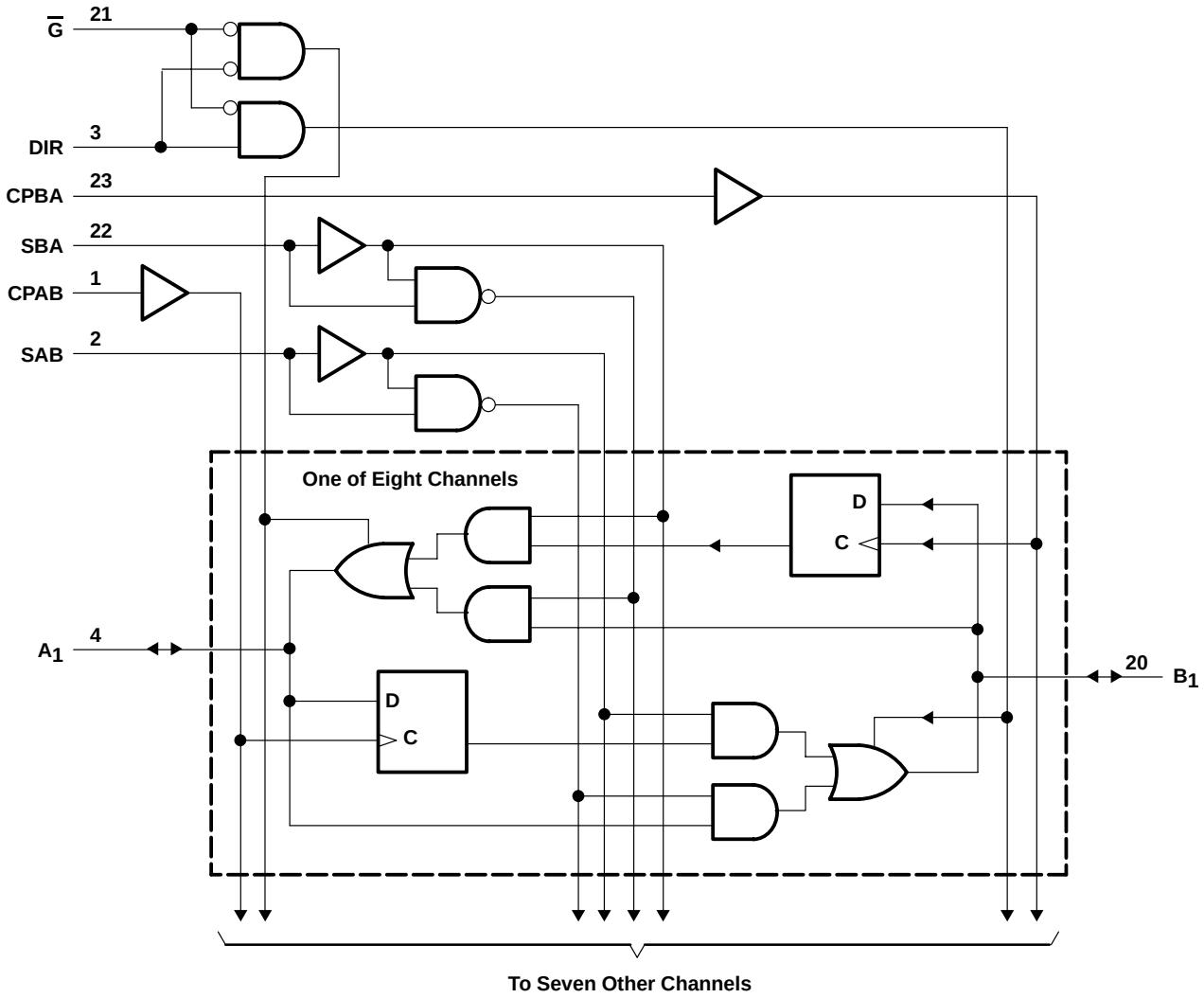
21	3	1	23	2	22
$\overline{G}$	DIR†	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

† Cannot transfer data to A bus and B bus simultaneously.

Figure 1. Bus-Management Functions

logic diagram (positive logic)



Pin numbers shown are for the Q and SO packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	61°C/W
SO package	46°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		CY54FCT646T			CY74FCT646T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY54FCT646T			CY74FCT646T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = –18 mA		–0.7	–1.2				V
	V_{CC} = 4.75 V,	I_{IN} = –18 mA					–0.7	–1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –12 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = –32 mA				2			
		I_{OH} = –15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V			10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V						10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V			–10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V						–10	
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V	–60	–120	–225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				–60	–120	–225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	µA
I_{CC}	V_{CC} = 5.5 V,	V_{IN} ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open			0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open						0.5	2	
I_{CCD}¶	V_{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{G}$ = DIR = GND, SAB = $\overline{SBA}$ = GND, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V			0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{G}$ = DIR = GND, SAB = $\overline{SBA}$ = GND, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V						0.06	0.12	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT646T			CY74FCT646T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_C#	V_{CC} = 5.5 V, f_0 = 10 MHz, Outputs open, $\overline{G}$ = DIR = GND, SAB = $\overline{SBA}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		2.8	5.6‖				
			V_{IN} = 3.4 V or GND		5.1	14.6‖				
	V_{CC} = 5.25 V, f_0 = 10 MHz, Outputs open, $\overline{G}$ = DIR = GND, SAB = $\overline{SBA}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					0.7	1.4	mA
			V_{IN} = 3.4 V or GND					1.2	3.4	
		Eight bits switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					2.8	5.6‖	
			V_{IN} = 3.4 V or GND					5.1	14.6‖	
C_i					6	10		6	10	pF
C_o					8	12		8	12	pF

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD}(f_0/2 + f_1 \times N_1)$
Where:
I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1
All currents are in milliamperes and all frequencies are in megahertz.
‖ Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		CY54FCT646T		CY54FCT646AT		CY54FCT646CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	6		5		5		ns
t_{su}	Setup time, data before CPAB↑ or CPBA↑	4.5		2		2		ns
t_h	Hold time, data after CPAB↑ or CPBA↑	2		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		CY74FCT646T		CY74FCT646AT		CY74FCT646CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	6		5		5		ns
t_{su}	Setup time, data before CPAB↑ or CPBA↑	4		2		2		ns
t_h	Hold time, data after CPAB↑ or CPBA↑	2		1.5		1.5		ns

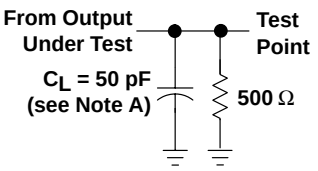
switching characteristics over operating free-air temperature range (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT646T		CY54FCT646AT		CY54FCT646CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	11	2	7.7	1.5	6	ns
t_{PHL}			2	11	2	7.7	1.5	6	
t_{PZH}	DIR	A or B	2	15	2	10.5	1.5	8.9	ns
t_{PZL}			2	15	2	10.5	1.5	8.9	
t_{PHZ}	$\overline{G}$ and DIR	A or B	2	11	2	7.7	1.5	7.7	ns
t_{PLZ}			2	11	2	7.7	1.5	7.7	
t_{PLH}	CPAB or CPBA	A or B	2	10	2	7	1.5	6.3	ns
t_{PHL}			2	10	2	7	1.5	6.3	
t_{PLH}	SBA or SAB	A or B	2	12	2	8.4	1.5	7	ns
t_{PHL}			2	12	2	8.4	1.5	7	

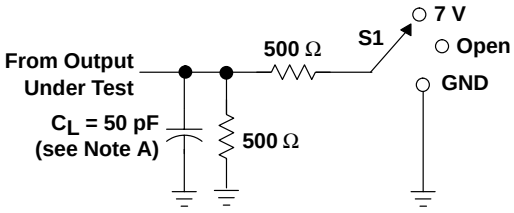
switching characteristics over operating free-air temperature range (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT646T		CY74FCT646AT		CY74FCT646CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	9	1.5	6.3	1.5	5.4	ns
t_{PHL}			1.5	9	1.5	6.3	1.5	5.4	
t_{PZH}	DIR	A or B	1.5	14	1.5	9.8	1.5	7.8	ns
t_{PZL}			1.5	14	1.5	9.8	1.5	7.8	
t_{PHZ}	$\overline{G}$ and DIR	A or B	1.5	9	1.5	6.3	1.5	6.3	ns
t_{PLZ}			1.5	9	1.5	6.3	1.5	6.3	
t_{PLH}	CPAB or CPBA	A or B	1.5	9	1.5	6.3	1.5	5.7	ns
t_{PHL}			1.5	9	1.5	6.3	1.5	5.7	
t_{PLH}	SBA or SAB	A or B	1.5	11	1.5	7.7	1.5	6.2	ns
t_{PHL}			1.5	11	1.5	7.7	1.5	6.2	

PARAMETER MEASUREMENT INFORMATION

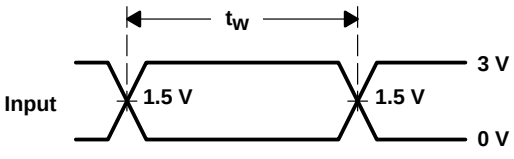


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

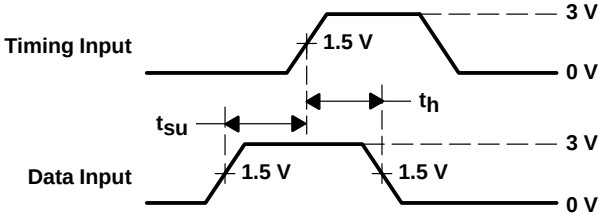


LOAD CIRCUIT FOR
3-STATE OUTPUTS

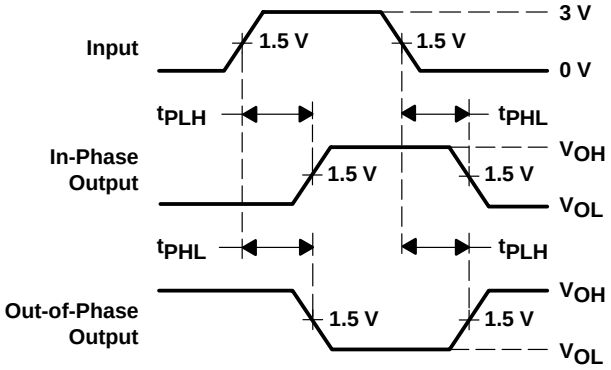
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



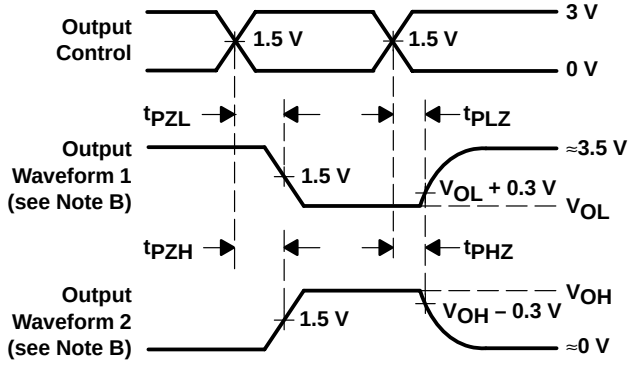
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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