Texas Instruments

DAC8564

16-Bit, Quad Channel, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTER with 2.5V, 2ppm/°C Internal Reference

Check for Samples: DAC8564

FEATURES

- **Relative Accuracy: 4LSB**
- **Glitch Energy: 0.15nV-s**
- **Internal Reference:**
  - **2.5V Reference Voltage (enabled by default)**
  - **0.004% Initial Accuracy (typ)**
  - **2ppm/°C Temperature Drift (typ)**
  - **5ppm/°C Temperature Drift (max)**
  - **20mA Sink/Source Capability**
- **Power-On Reset to Zero-Scale**
- **Ultra-Low Power Operation: 1mA at 5V**
- **Wide Power Supply Range: +2.7V to +5.5V**
- **16-Bit Monotonic Over Temperature Range**
- **Settling Time: 10μs to ±0.003% Full-Scale Range (FSR)**
- **Low-Power Serial Interface with Schmitt-Triggered Inputs: Up to 50MHz**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **1.8V to 5.5V Logic Compatibility**
- **Temperature Range: –40°C to +105°C**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control, PLCs**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

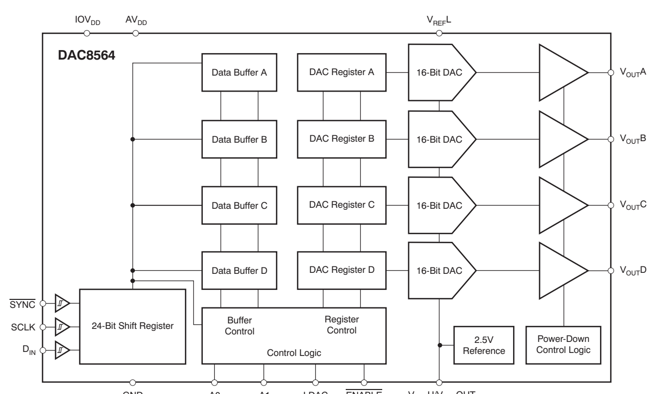
RELATED DEVICES	16-BIT	14-BIT	12-BIT
Pin and Functionally Compatible	DAC8564	DAC8164	DAC7564
Functionally Compatible	DAC8565	DAC8165	DAC7565

DESCRIPTION

The DAC8564 is a low-power, voltage-output, four-channel, 16-bit digital-to-analog converter (DAC). The device includes a 2.5V, 2ppm/°C internal reference (enabled by default), giving a full-scale output voltage range of 2.5V. The internal reference has an initial accuracy of 0.004% and can source up to 20mA at the $V_{REF}H/V_{REF}OUT$ pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch). The DAC8564 uses a versatile 3-wire serial interface that operates at clock rates up to 50MHz. The interface is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

The DAC8564 incorporates a power-on-reset circuit that ensures the DAC output powers up at zero-scale and remains there until a valid code is written to the device. The device contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 1.3μA at 5V. Power consumption is 2.9mW at 3V, reducing to 1.5μW in power-down mode. The low-power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment.

The DAC8564 is drop-in and functionally compatible with the DAC7564 and DAC8164, and functionally compatible with the DAC7565, DAC8165, and DAC8565. All these devices are available in a TSSOP-16 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	REFERENCE DRIFT (ppm/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8564A	±12	±1	25	TSSOP-16	PW	–40°C to +105°C	DAC8564
DAC8564B	±8	±1	25	TSSOP-16	PW	–40°C to +105°C	DAC8564B
DAC8564C	±12	±1	5	TSSOP-16	PW	–40°C to +105°C	DAC8564
DAC8564D	±8	±1	5	TSSOP-16	PW	–40°C to +105°C	DAC8564D

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		DAC8564	UNIT
AV_{DD} to GND		–0.3 to +6	V
Digital input voltage to GND		–0.3 to $+V_{DD}$ + 0.3	V
V_{OUT} to GND		–0.3 to $+V_{DD}$ + 0.3	V
V_{REF} to GND		–0.3 to $+V_{DD}$ + 0.3	V
Operating temperature range		–40 to +125	°C
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+150	°C
Power dissipation		$(T_J \text{ max} - T_A)/\theta_{JA}$	W
Thermal impedance, θ_{JA}		+118	°C/W
Thermal impedance, θ_{JC}		+29	°C/W
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1500	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

PARAMETER	TEST CONDITIONS		DAC8564 MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
Resolution			16			Bits
Relative accuracy	Measured by the line passing through codes 485 and 64714	DAC8564A, DAC8564C		±4	±12	LSB
		DAC8564B, DAC8564D		±4	±8	LSB
Differential nonlinearity	16-bit monotonic			±0.5	±1	LSB
Offset error	Measured by the line passing through codes 485 and 64714			±5	±8	mV
Offset error drift				±1		µV/°C
Full-scale error				±0.2	±0.5	% of FSR
Gain error				±0.05	±0.2	% of FSR
Gain temperature coefficient	AV_{DD} = 5V			±1		ppm of FSR/°C
	AV_{DD} = 2.7V			±2		
PSRR Power-supply rejection ratio	Output unloaded			1		mV/V
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		V_{REF}	V
Output voltage settling time	To ±0.003% FSR, 0200h to FD00h, R_L = 2kΩ, 0pF < C_L < 200pF			8	10	µs
	R_L = 2kΩ, C_L = 500pF			12		
Slew rate				2.2		V/µs
Capacitive load stability	R_L = ∞			470		pF
	R_L = 2kΩ			1000		
Code change glitch impulse	1LSB change around major carry			0.15		nV-s
Digital feedthrough	SCLK toggling, $\overline{SYNC}$ high			0.15		nV-s
Channel-to-channel dc crosstalk	Full-scale swing on adjacent channel			0.25		LSB
Channel-to-channel ac crosstalk	1kHz full-scale sine wave, outputs unloaded			–100		dB
DC output impedance	At mid-code input			1		Ω
Short-circuit current				50		mA
Power-up time	Coming out of power-down mode, AV_{DD} = 5V			2.5		µs
	Coming out of power-down mode, AV_{DD} = 3V			5		
AC PERFORMANCE(2)						
SNR	T_A = +25°C, BW = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz. First 19 harmonics removed for SNR calculation.			90		dB
THD				–77		dB
SFDR				78		dB
SINAD				77		dB
DAC output noise density	T_A = +25°C, at mid-code input, f_{OUT} = 1kHz			120		nV/√Hz
DAC output noise	T_A = +25°C, at mid-code input, 0.1Hz to 10Hz			6		μV_{PP}
REFERENCE						
Internal reference current consumption	AV_{DD} = 5.5V			360		µA
	AV_{DD} = 3.6V			348		µA
External reference current	External V_{REF} = 2.5V, if internal reference is disabled, all four channels active			80		µA
Reference input range $V_{REF}H$ voltage	$V_{REF}L < V_{REF}H$, $AV_{DD} - (V_{REF}H + V_{REF}L)/2 > 1.2V$		0		AV_{DD}	V
Reference input range $V_{REF}L$ voltage	$V_{REF}L < V_{REF}H$, $AV_{DD} - (V_{REF}H + V_{REF}L)/2 > 1.2V$		0		$AV_{DD}/2$	V
Reference input impedance				31		kΩ

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design or characterization; not production tested.

ELECTRICAL CHARACTERISTICS (continued)

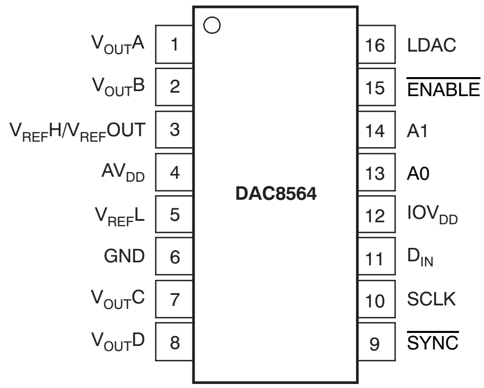
At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	DAC8564 MIN	TYP	MAX	UNIT
REFERENCE OUTPUT						
Output voltage		T_A = +25°C	2.4975	2.5	2.5025	V
Initial accuracy		T_A = +25°C	–0.1	±0.004	0.1	%
Output voltage temperature drift		DAC8564A, DAC8564B[3]		5	25	ppm/°C
		DAC8564C, DAC8564D[4]		2	5	
Output voltage noise		f = 0.1Hz to 10Hz		12		μV_{PP}
Output voltage noise density (high-frequency noise)		T_A = +25°C, f = 1MHz, C_L = 0µF		50		nV/√Hz
		T_A = +25°C, f = 1MHz, C_L = 1µF		20		
		T_A = +25°C, f = 1MHz, C_L = 4µF		16		
Load regulation, sourcing[5]		T_A = +25°C		30		µV/mA
Load regulation, sinking[5]		T_A = +25°C		15		µV/mA
Output current load capability[6]				±20		mA
Line regulation		T_A = +25°C		10		µV/V
Long-term stability/drift (aging)[5]		T_A = +25°C, time = 0 to 1900 hours		50		ppm
Thermal hysteresis[5]		First cycle		100		ppm
		Additional cycles		25		
LOGIC INPUTS[6]						
Input current				±1		µA
$V_{IN}L$	Logic input LOW voltage	2.7V ≤ IOV_{DD} ≤ 5.5V			0.3 × IOV_{DD}	V
		1.8V ≤ IOV_{DD} ≤ 2.7V			0.1 × IOV_{DD}	
$V_{IN}H$	Logic input HIGH voltage	2.7V ≤ IOV_{DD} ≤ 5.5V	0.7 × IOV_{DD}			V
		1.8V ≤ IOV_{DD} ≤ 2.7V	0.95 × IOV_{DD}			
Pin capacitance					3	pF
POWER REQUIREMENTS						
AV_{DD}			2.7		5.5	V
IOV_{DD}			1.8		5.5	V
IOI_{DD} [6]				10	20	µA
I_{DD} [7]	Normal mode	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1	1.6	mA
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		0.95	1.5	
	All power-down modes	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1.3	3.5	µA
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		0.5	2.5	
Power Dissipation [7]	Normal mode	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		3.6	8.8	mW
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		2.6	5.4	
	All power-down modes	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		4.7	19	µW
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1.4	9	
TEMPERATURE RANGE						
Specified performance			–40		+105	°C

(3) Reference is trimmed and tested at room temperature, and is characterized from –40°C to +120°C.
(4) Reference is trimmed and tested at two temperatures (+25°C and +105°C), and is characterized from –40°C to +120°C.
(5) Explained in more detail in the *Application Information* section of this data sheet.
(6) Ensured by design or characterization; not production tested.
(7) Input code = 32768, reference current included, no load.

PIN CONFIGURATIONS

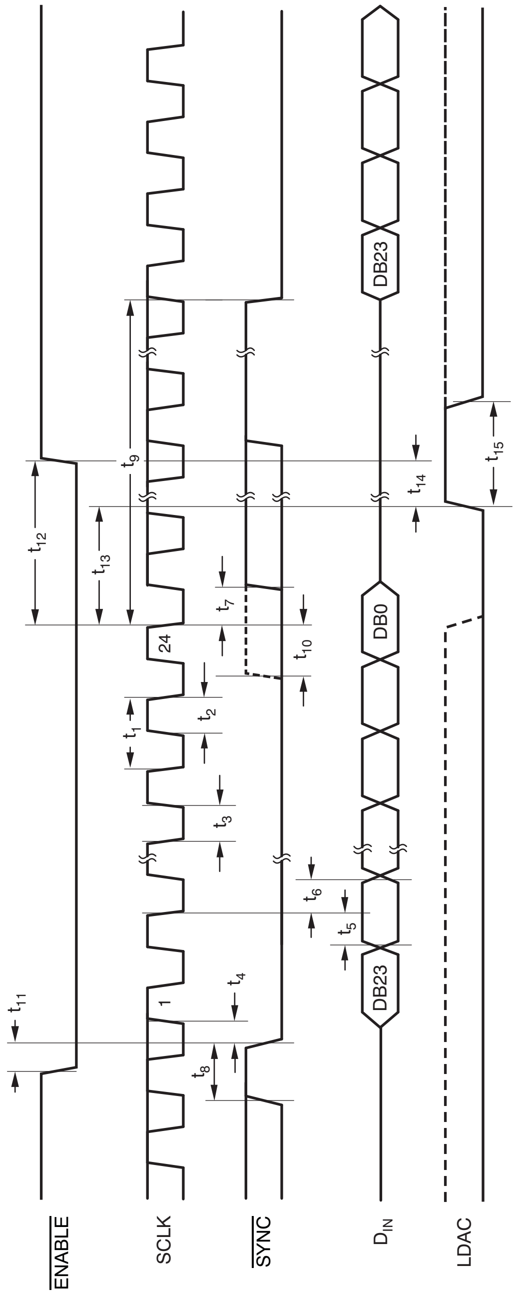
PW PACKAGE
TSSOP-16
(Top View)



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{OUT}A	Analog output voltage from DAC A
2	V_{OUT}B	Analog output voltage from DAC B
3	V_{REF}H/ V_{REF}OUT	Positive reference input / reference output 2.5V if internal reference used.
4	AV_{DD}	Power-supply input, 2.7V to 5.5V
5	V_{REF}L	Negative reference input
6	GND	Ground reference point for all circuitry on the part
7	V_{OUT}C	Analog output voltage from DAC C
8	V_{OUT}D	Analog output voltage from DAC D
9	$\overline{\text{SYNC}}$	Level-triggered control input (active low). This input is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24th clock. If $\overline{\text{SYNC}}$ is taken high before the 24th clock edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC8564. Schmitt-Trigger logic input.
10	SCLK	Serial clock input. Data can be transferred at rates up to 50MHz. Schmitt-Trigger logic input.
11	D_{IN}	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
12	IOV_{DD}	Digital input-output power supply
13	A0	Address 0—sets device address; see Table 5.
14	A1	Address 1—sets device address; see Table 5.
15	$\overline{\text{ENABLE}}$	The enable pin (active low) connects the SPI interface to the serial port
16	LDAC	Load DACs; rising edge triggered, loads all DAC registers

SERIAL WRITE OPERATION



TIMING REQUIREMENTS(1) (2)

At AV_{DD} = IOV_{DD}= 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	DAC8564 MIN	TYP	MAX	UNIT
t_1 (3)	SCLK cycle time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	40			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
t_2	SCLK HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_3	SCLK LOW time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_4	$\overline{SYNC}$ to SCLK rising edge setup time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
t_5	Data setup time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	5			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	5			
t_6	Data hold time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	4.5			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	4.5			
t_7	SCLK falling edge to $\overline{SYNC}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	40			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
t_9	24th SCLK falling edge to $\overline{SYNC}$ falling edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	130			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	130			
t_{10}	$\overline{SYNC}$ rising edge to 24th SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	15			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	15			
t_{11}	$\overline{ENABLE}$ falling edge to $\overline{SYNC}$ falling edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	15			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	15			
t_{12}	24th SCLK falling edge to $\overline{ENABLE}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_{13}	24th SCLK falling edge to LDAC rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	50			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	50			
t_{14}	LDAC rising edge to $\overline{ENABLE}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_{15}	LDAC HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			

(1) All input signals are specified with t_R = t_F = 3ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See the *Serial Write Operation* timing diagram.
(3) Maximum SCLK frequency is 50MHz at IOV_{DD} = V_{DD} = 3.6V to 5.5V and 25MHz at IOV_{DD} = AV_{DD} = 2.7V to 3.6V.

TYPICAL CHARACTERISTICS: Internal Reference

At T_A = +25°C, unless otherwise noted.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (Grades C and D)

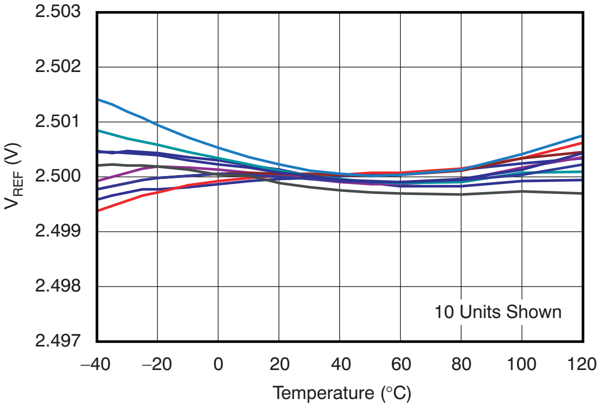


Figure 1.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (Grades A and B)

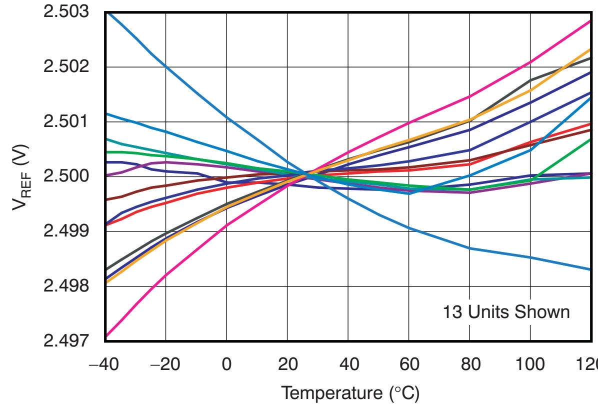


Figure 2.

REFERENCE OUTPUT TEMPERATURE DRIFT (–40°C to +120°C, Grades C and D)

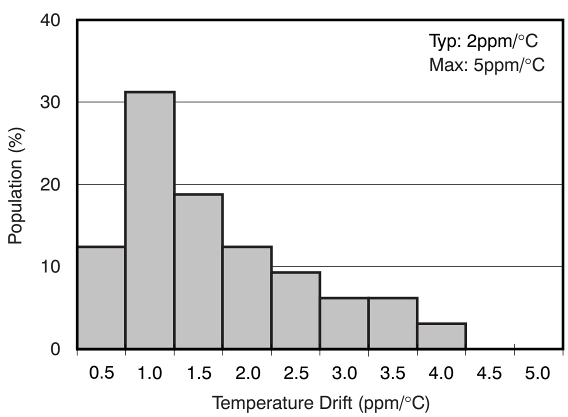


Figure 3.

REFERENCE OUTPUT TEMPERATURE DRIFT (–40°C to +120°, Grades A and B)

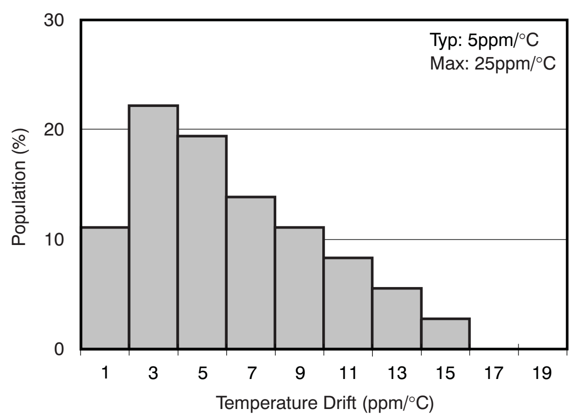


Figure 4.

REFERENCE OUTPUT TEMPERATURE DRIFT (0°C to +120°C, Grades C and D)

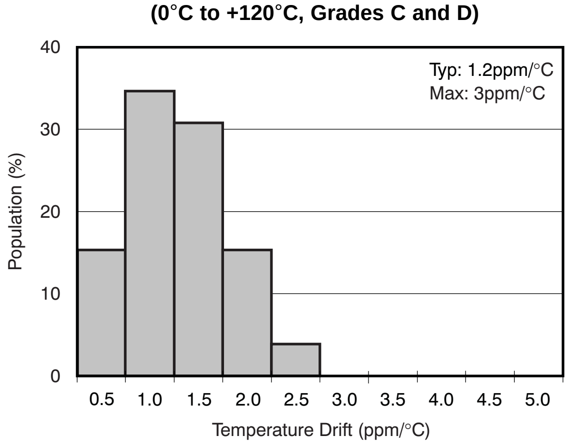


Figure 5.

LONG-TERM STABILITY/DRIFT (1)

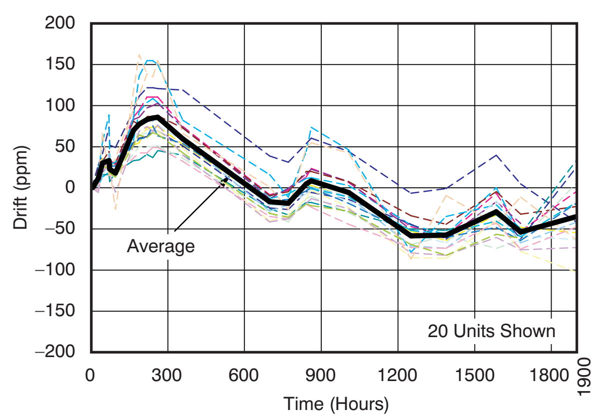


Figure 6.

(1) Explained in more detail in the *Application Information* section of this data sheet.

TYPICAL CHARACTERISTICS: Internal Reference (continued)

At T_A = +25°C, unless otherwise noted.

INTERNAL REFERENCE NOISE DENSITY vs FREQUENCY

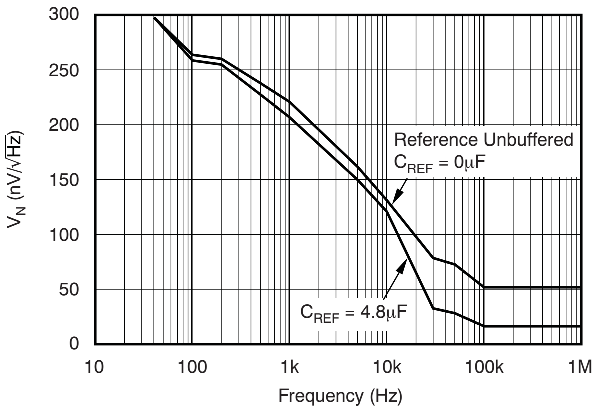


Figure 7.

INTERNAL REFERENCE NOISE 0.1Hz TO 10Hz

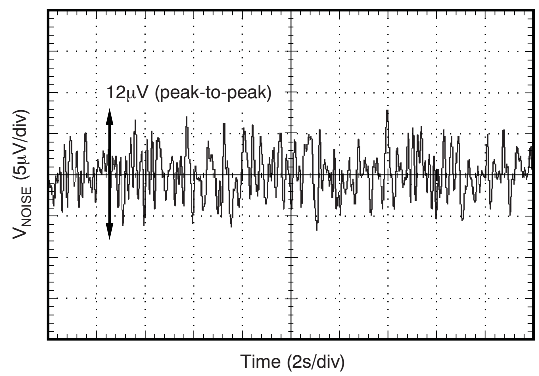


Figure 8.

INTERNAL REFERENCE VOLTAGE vs LOAD CURRENT (Grades C and D)

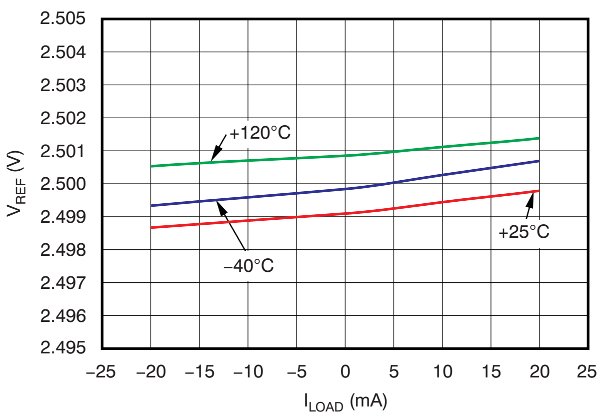


Figure 9.

INTERNAL REFERENCE VOLTAGE vs LOAD CURRENT (Grades A and B)

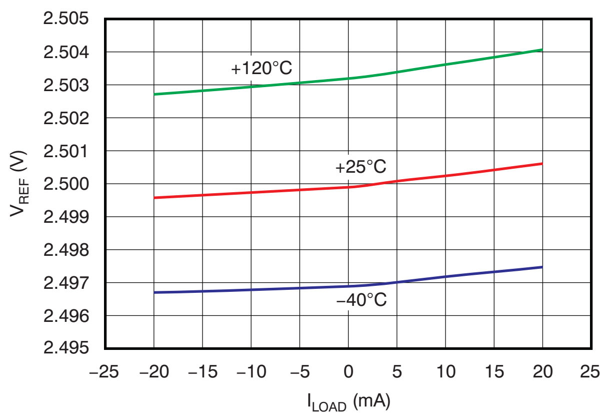


Figure 10.

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE (Grades C and D)

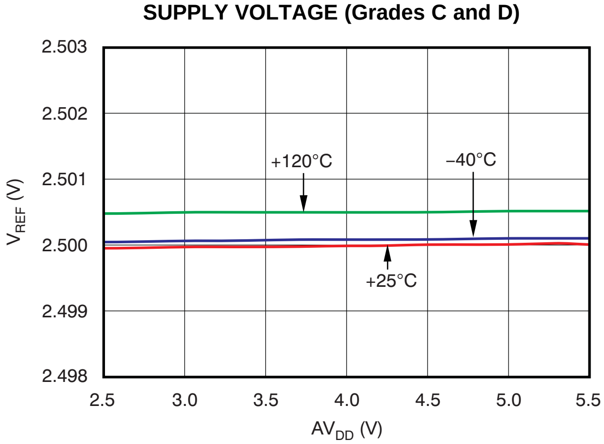


Figure 11.

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE (Grades A and B)

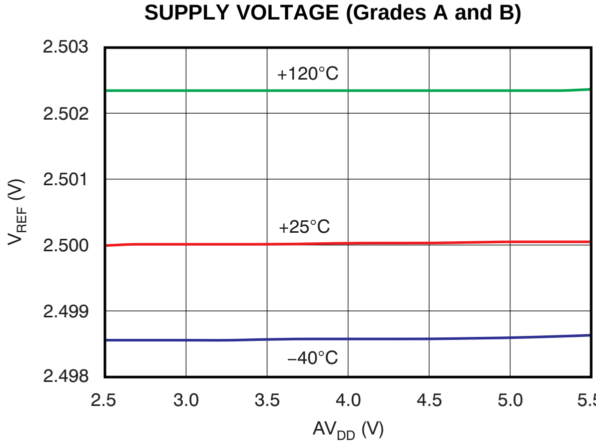


Figure 12.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

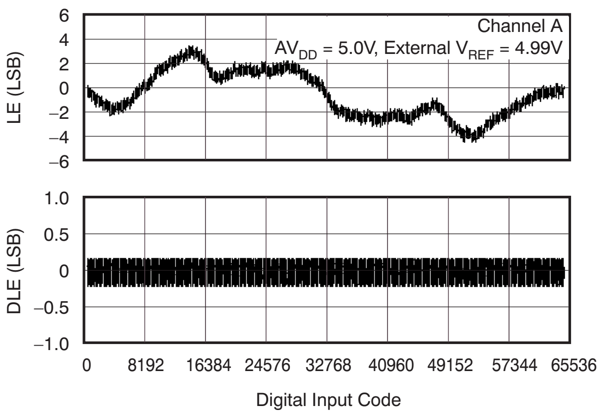


Figure 13.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

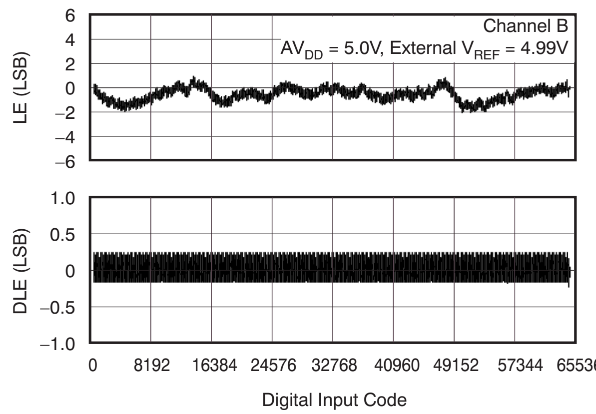


Figure 14.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

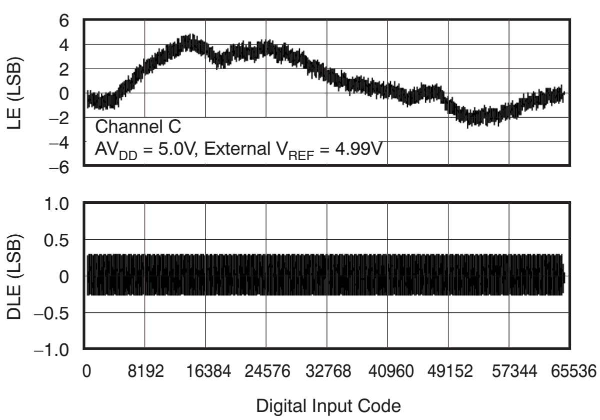


Figure 15.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

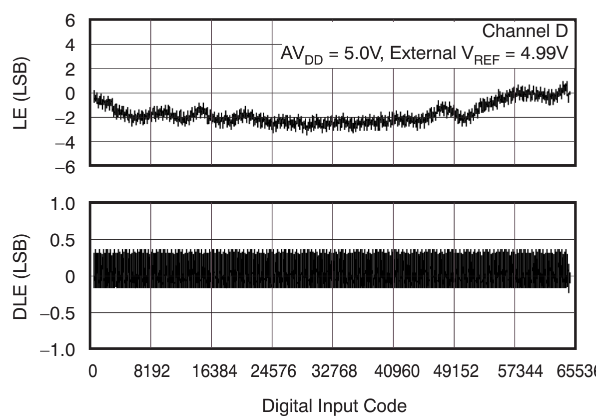


Figure 16.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

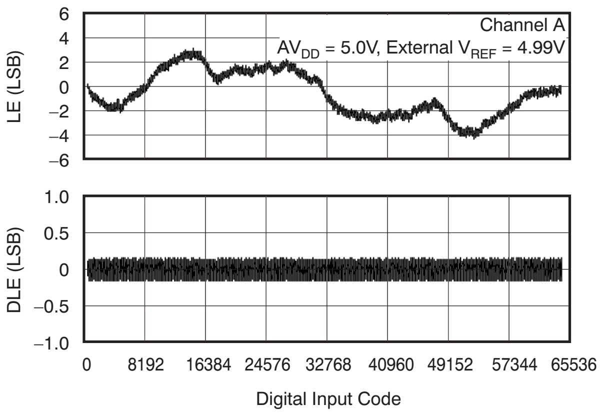


Figure 17.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

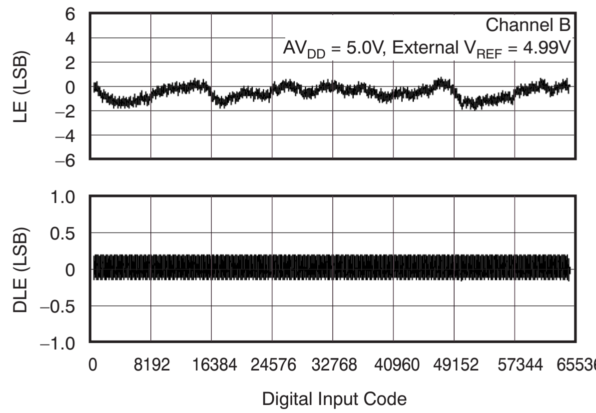


Figure 18.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

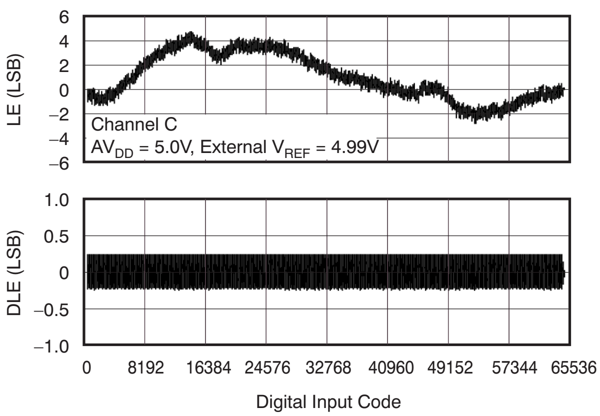


Figure 19.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

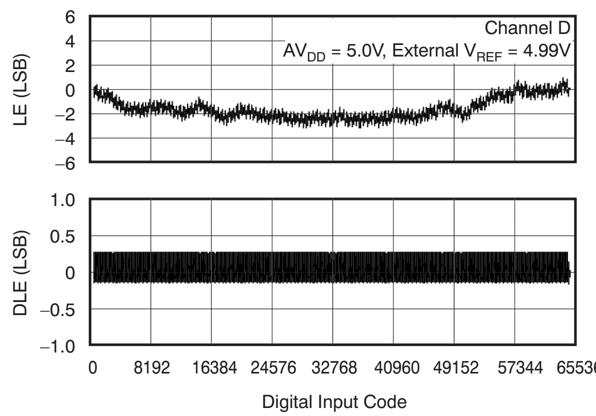


Figure 20.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

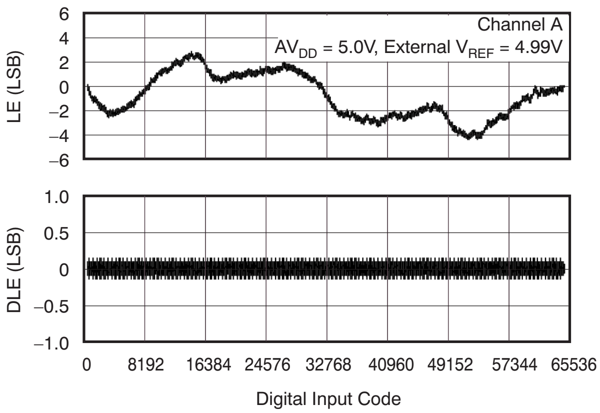


Figure 21.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

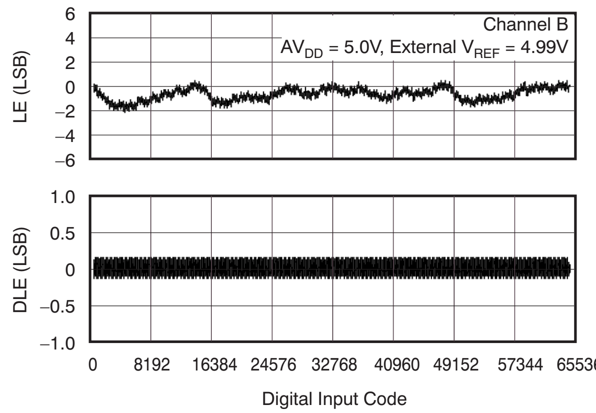


Figure 22.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

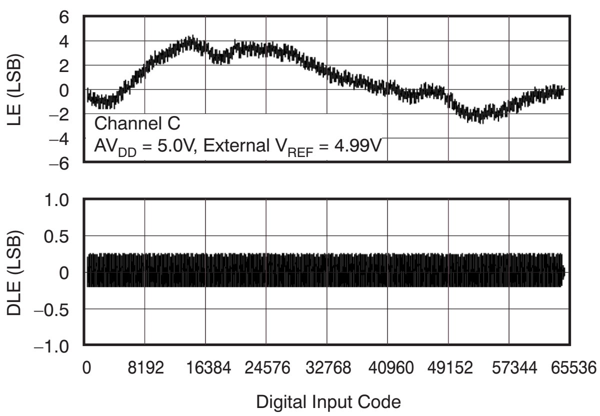


Figure 23.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

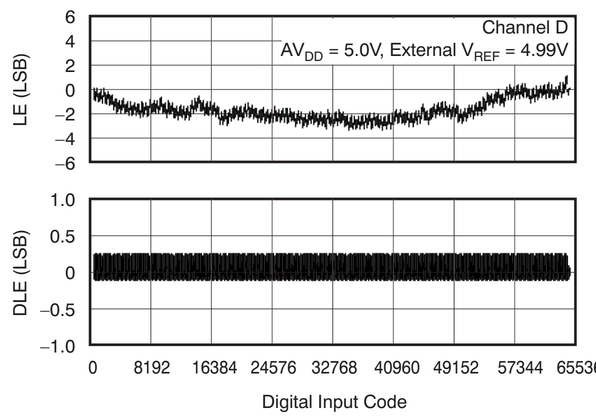


Figure 24.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

OFFSET ERROR vs TEMPERATURE

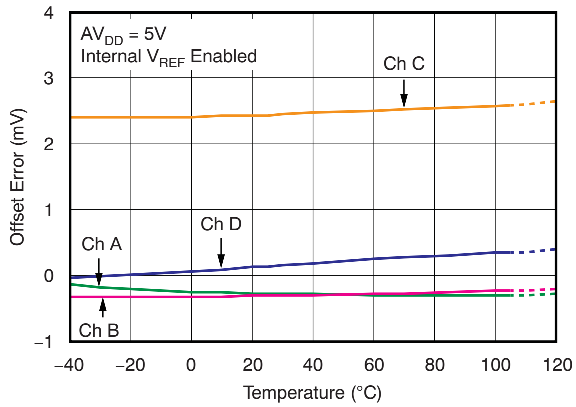


Figure 25.

FULL-SCALE ERROR vs TEMPERATURE

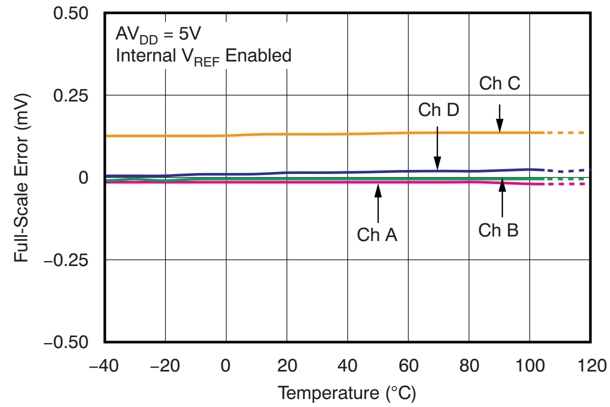


Figure 26.

SOURCE AND SINK CURRENT CAPABILITY

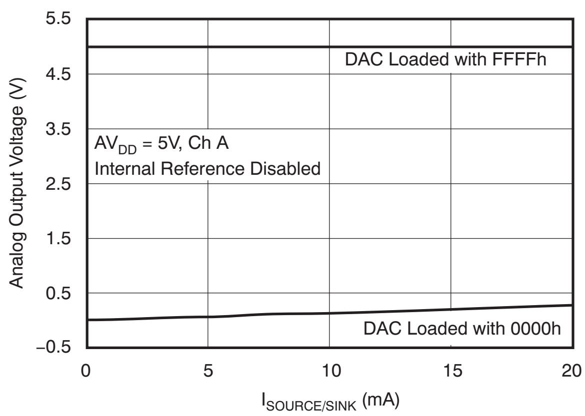


Figure 27.

SOURCE AND SINK CURRENT CAPABILITY

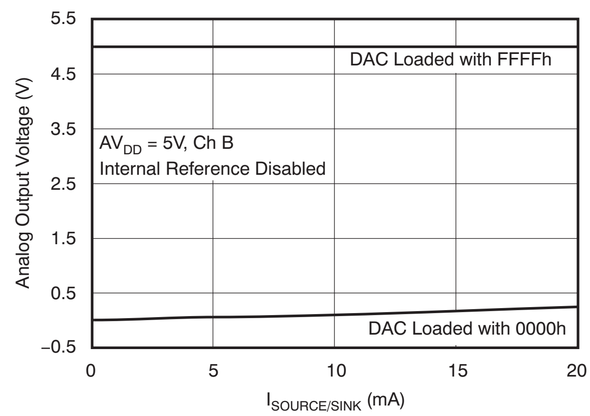


Figure 28.

SOURCE AND SINK CURRENT CAPABILITY

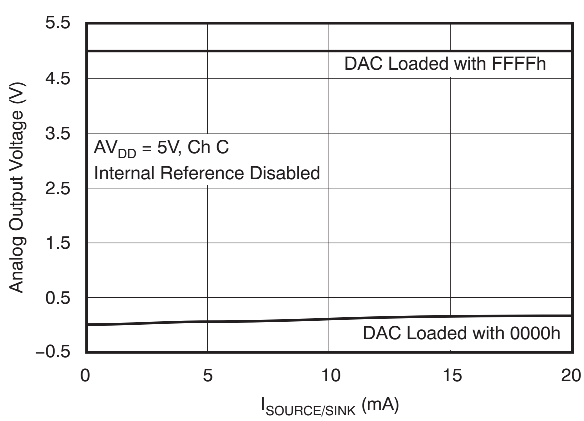


Figure 29.

SOURCE AND SINK CURRENT CAPABILITY

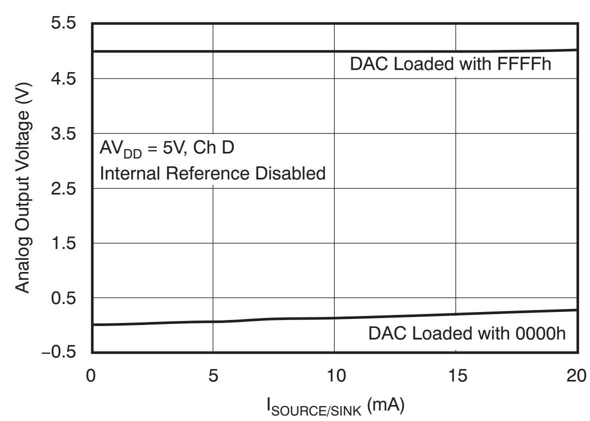


Figure 30.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

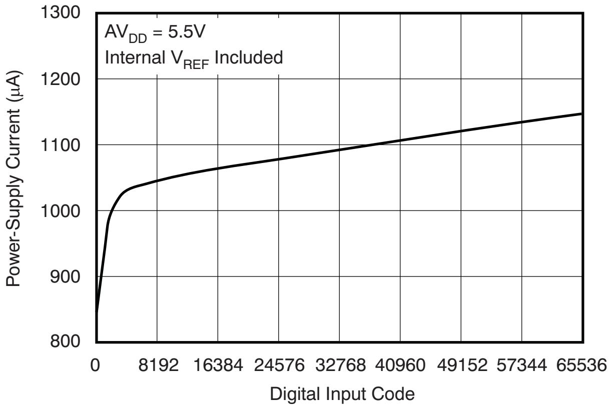


Figure 31.

POWER-SUPPLY CURRENT vs TEMPERATURE

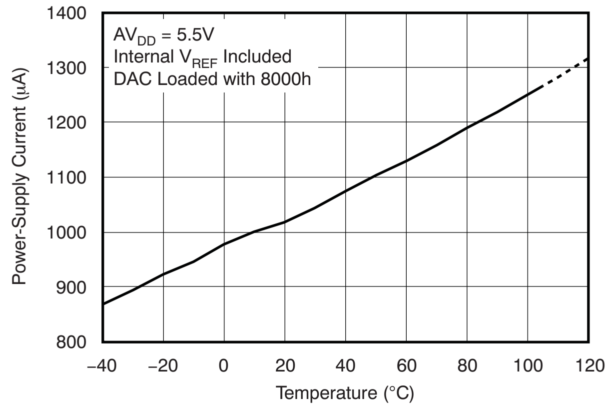


Figure 32.

POWER-SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

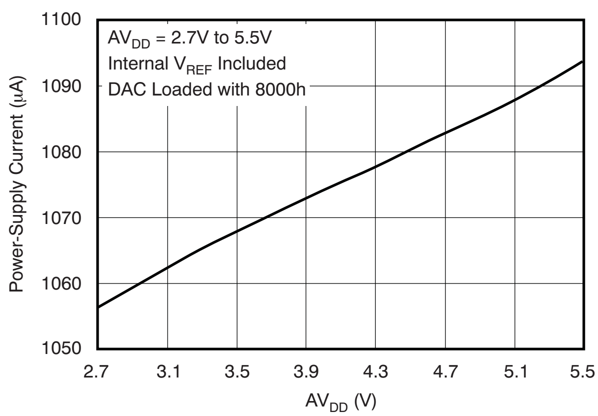


Figure 33.

POWER-DOWN CURRENT vs POWER-SUPPLY VOLTAGE

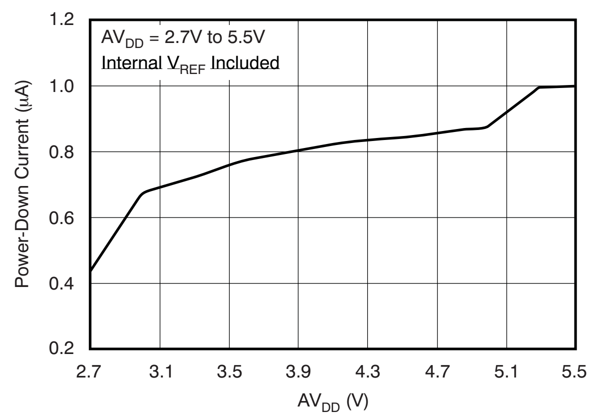


Figure 34.

POWER-DOWN CURRENT vs TEMPERATURE

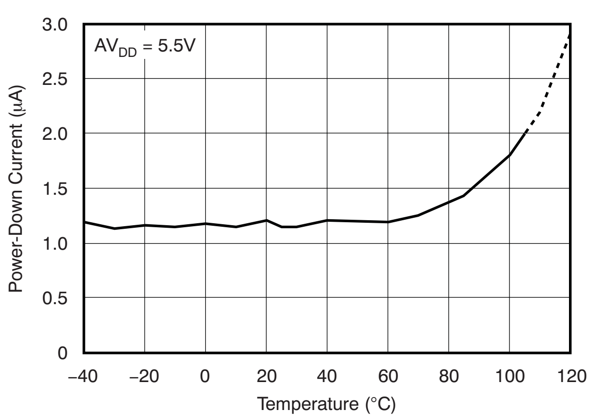


Figure 35.

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

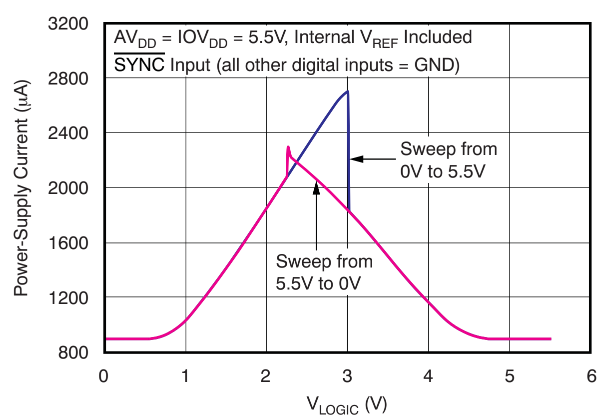


Figure 36.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

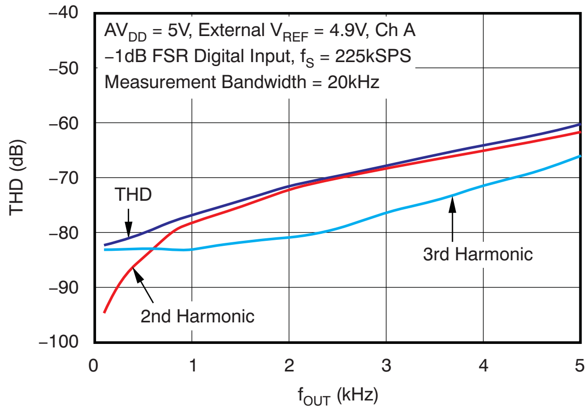


Figure 37.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

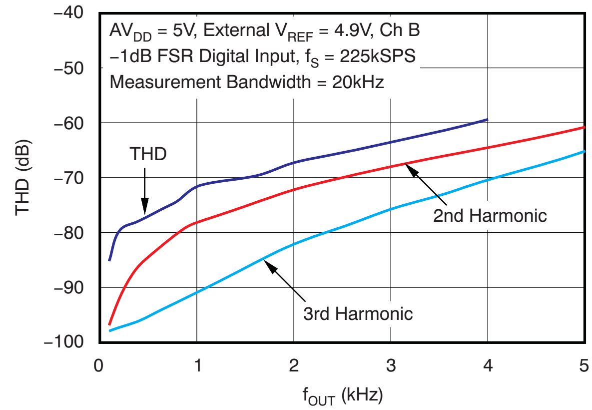


Figure 38.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

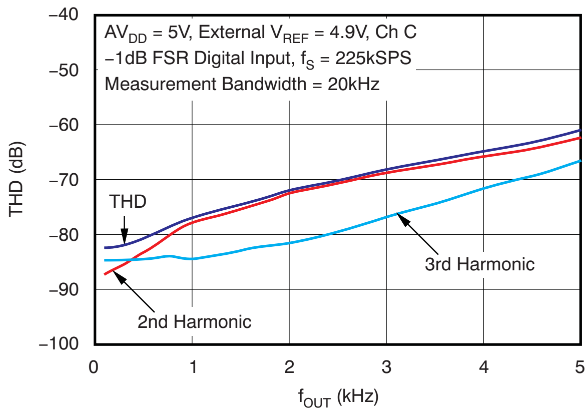


Figure 39.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

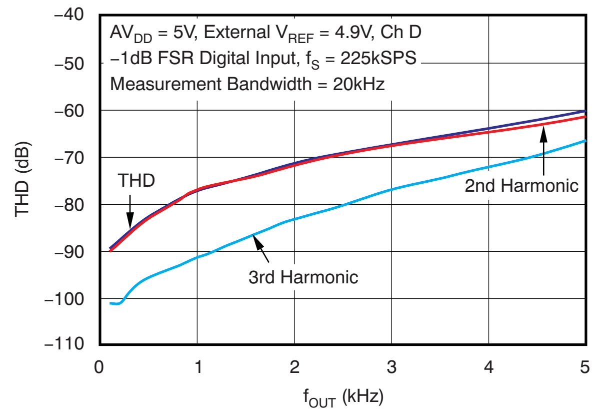


Figure 40.

POWER-SUPPLY CURRENT HISTOGRAM

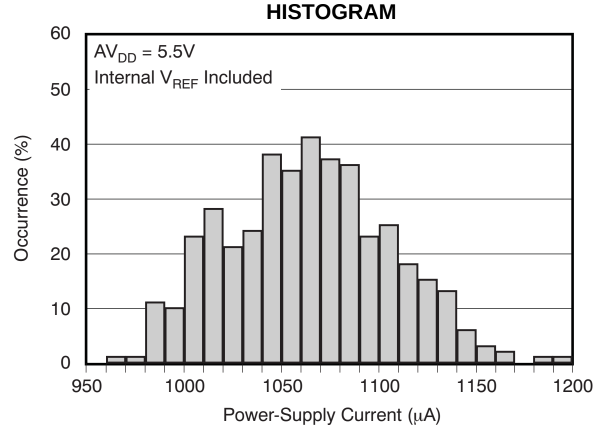


Figure 41.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

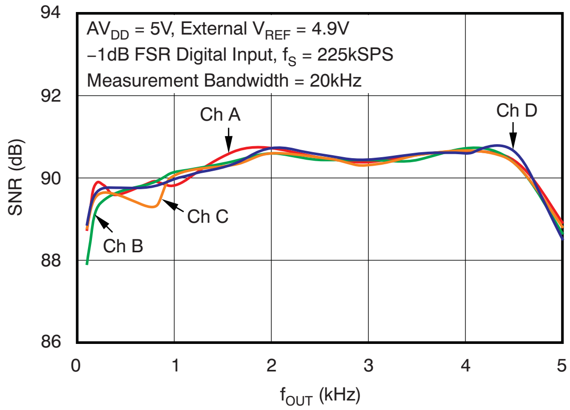


Figure 42.

POWER SPECTRAL DENSITY

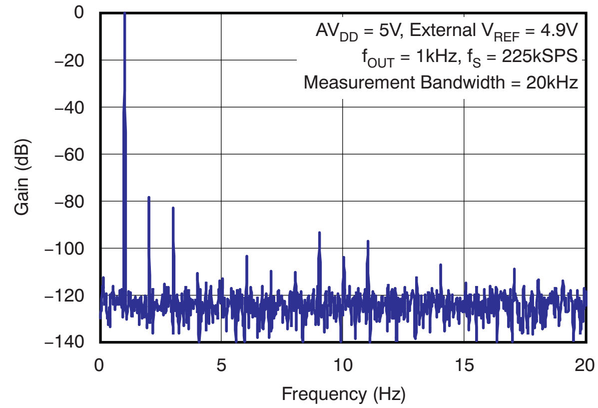


Figure 43.

FULL-SCALE SETTLING TIME: 5V RISING EDGE

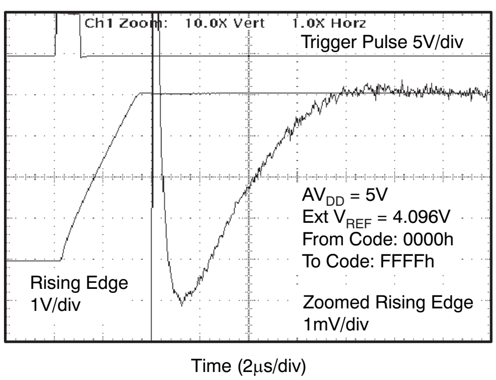


Figure 44.

FULL-SCALE SETTLING TIME: 5V FALLING EDGE

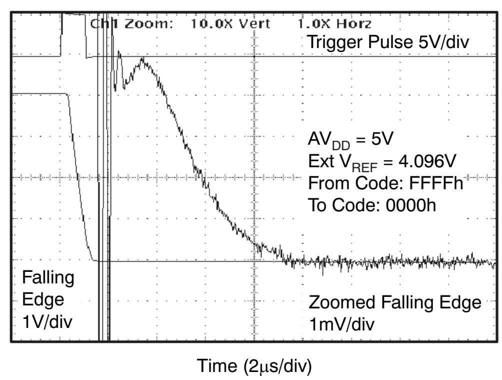


Figure 45.

HALF-SCALE SETTLING TIME: 5V RISING EDGE

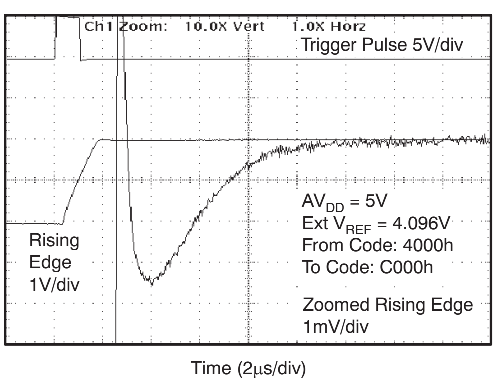


Figure 46.

HALF-SCALE SETTLING TIME: 5V FALLING EDGE

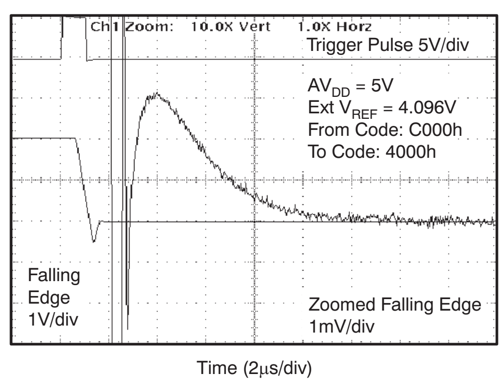


Figure 47.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

GLITCH ENERGY: 5V, 1LSB STEP, RISING EDGE

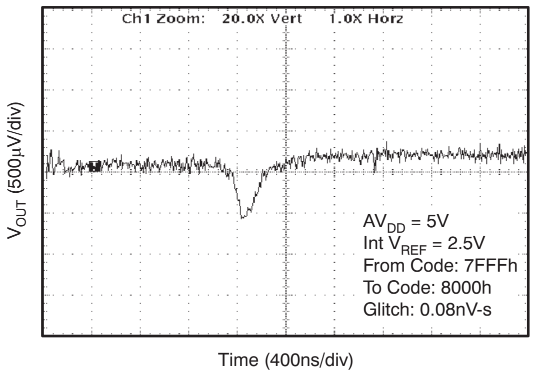


Figure 48.

GLITCH ENERGY: 5V, 1LSB STEP, FALLING EDGE

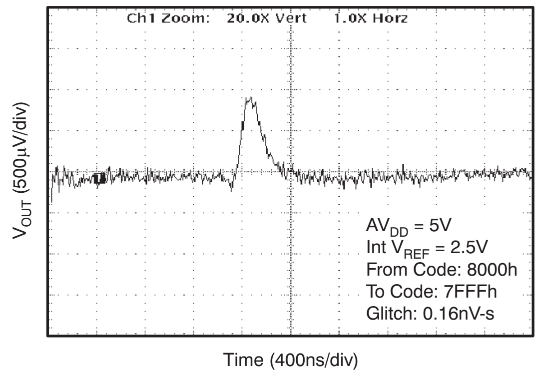


Figure 49.

GLITCH ENERGY: 5V, 16LSB STEP, RISING EDGE

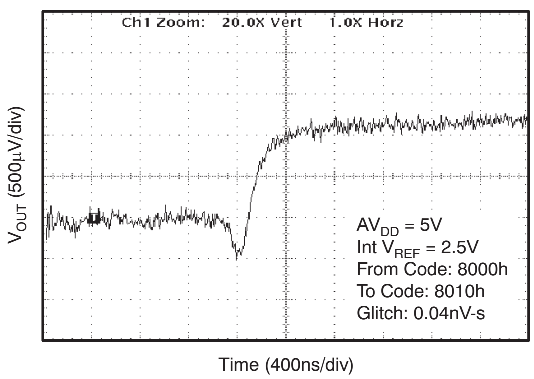


Figure 50.

GLITCH ENERGY: 5V, 16LSB STEP, FALLING EDGE

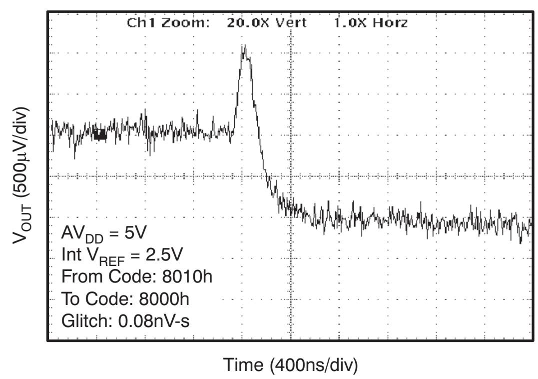


Figure 51.

GLITCH ENERGY: 5V, 256LSB STEP, RISING EDGE

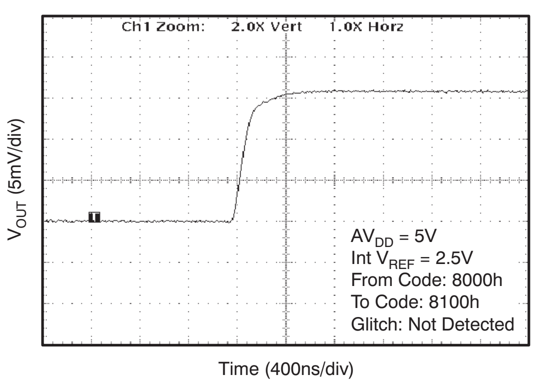


Figure 52.

GLITCH ENERGY: 5V, 256LSB STEP, FALLING EDGE

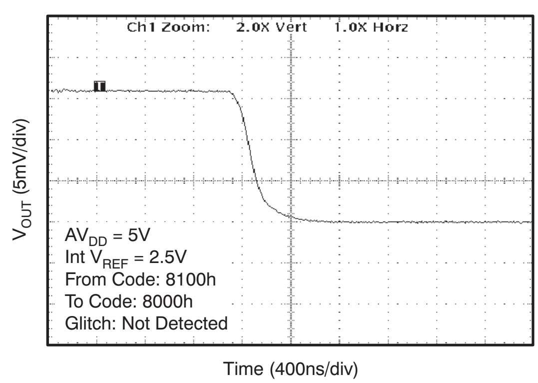


Figure 53.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

DAC OUTPUT NOISE DENSITY vs FREQUENCY[(1)]

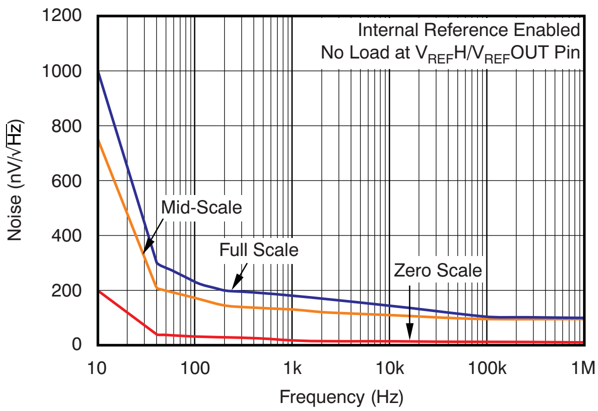


Figure 54.

DAC OUTPUT NOISE DENSITY vs FREQUENCY[(2)]

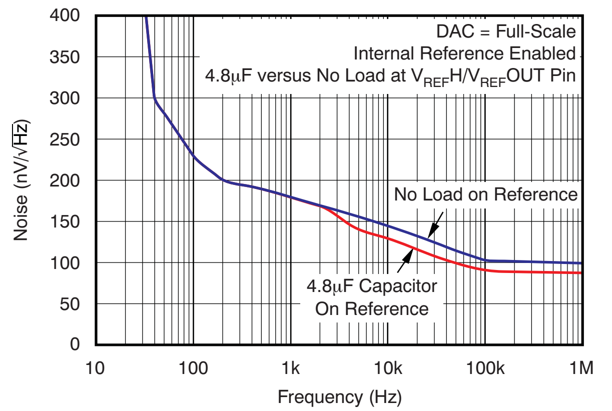


Figure 55.

DAC OUTPUT NOISE 0.1Hz TO 10Hz

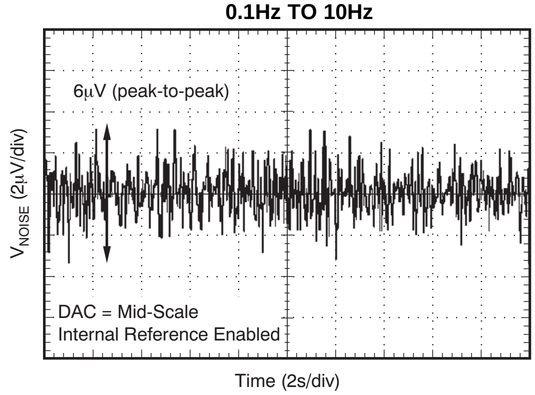


Figure 56.

(1) Explained in more detail in the *Application Information* section of this data sheet.
(2) See the *Application Information* section for more information.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 3.6V

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

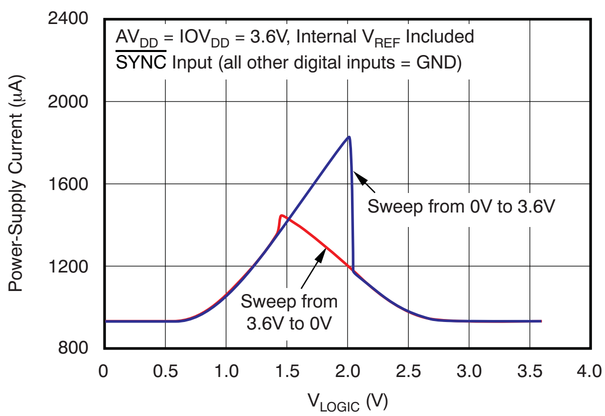


Figure 57.

POWER-SUPPLY CURRENT vs TEMPERATURE

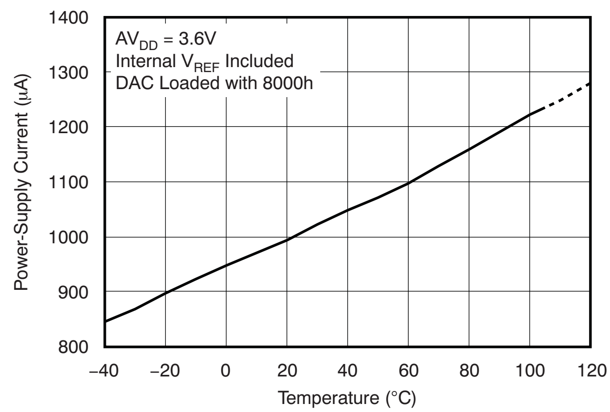


Figure 58.

POWER-SUPPLY CURRENT HISTOGRAM

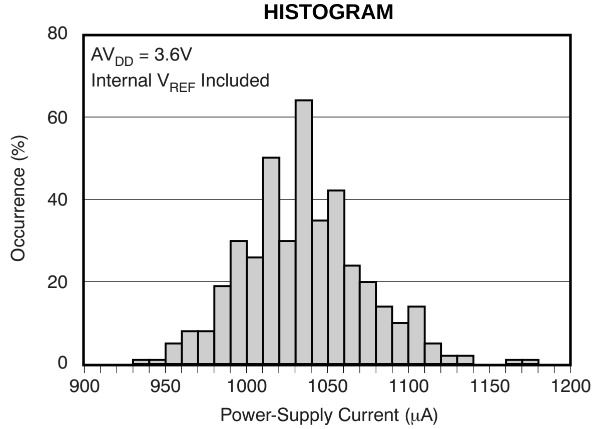


Figure 59.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

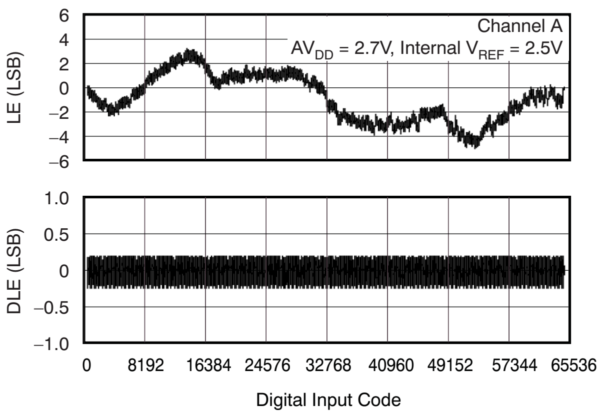


Figure 60.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

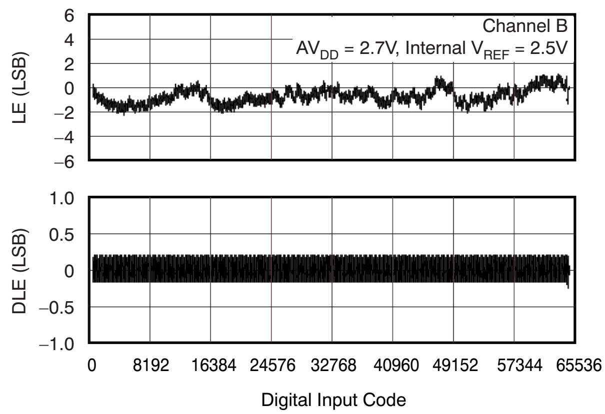


Figure 61.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

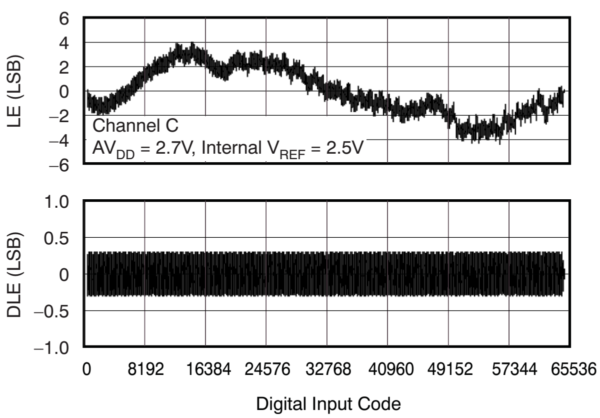


Figure 62.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

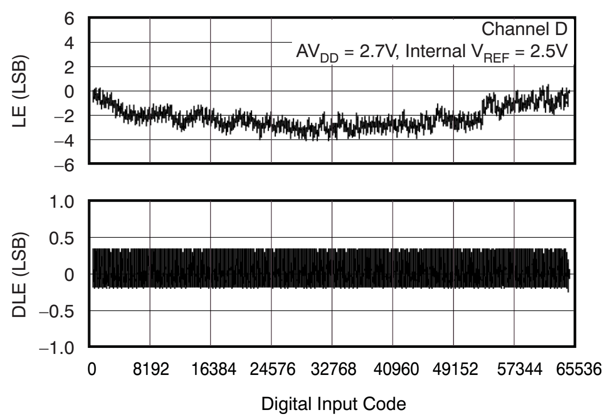


Figure 63.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

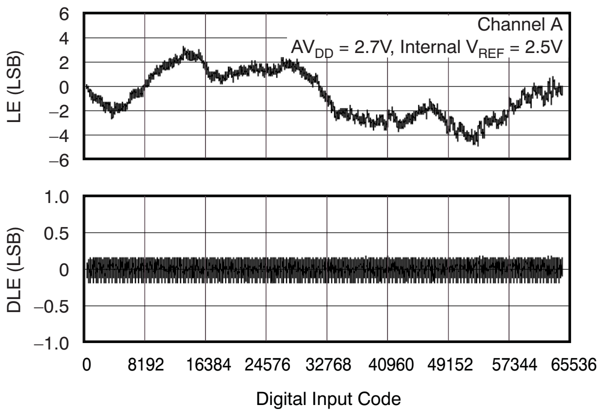


Figure 64.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

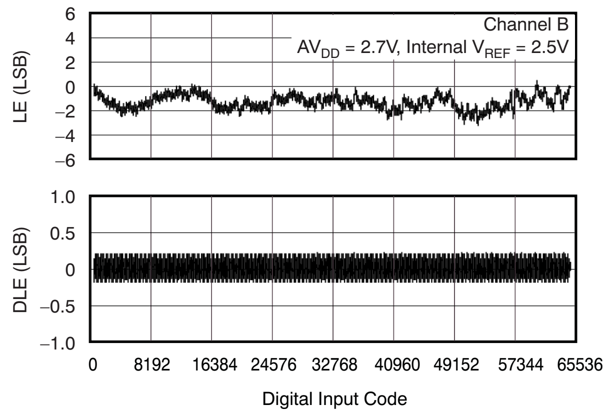


Figure 65.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

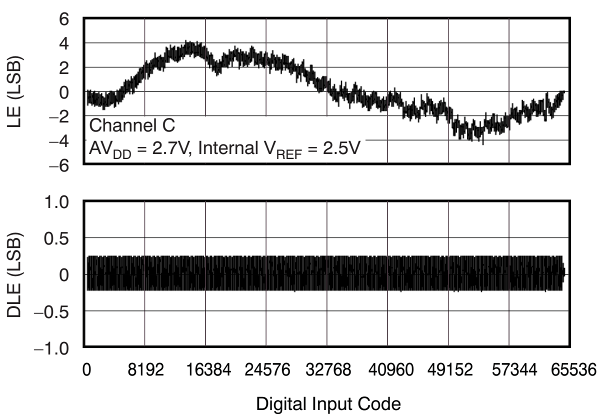


Figure 66.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

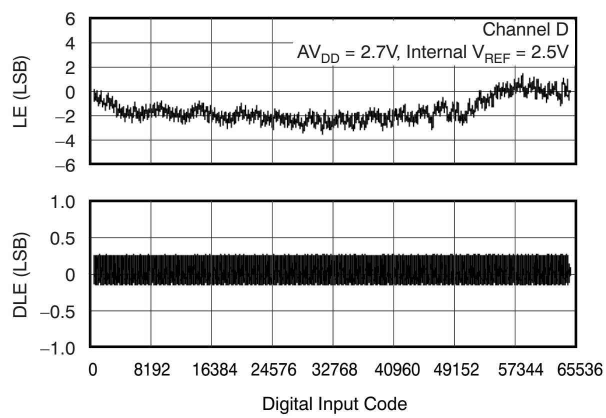


Figure 67.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

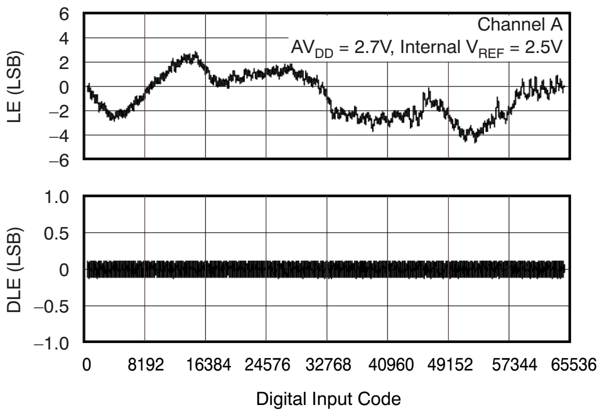


Figure 68.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

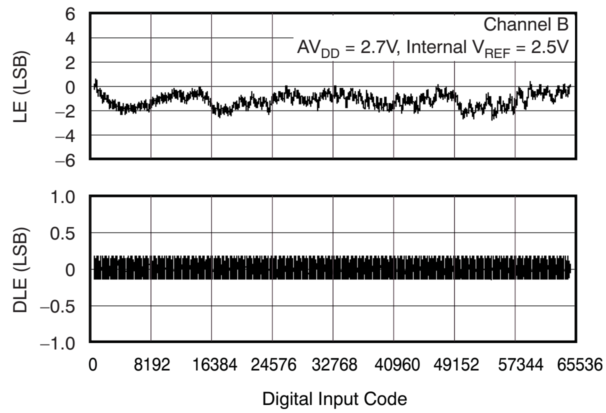


Figure 69.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

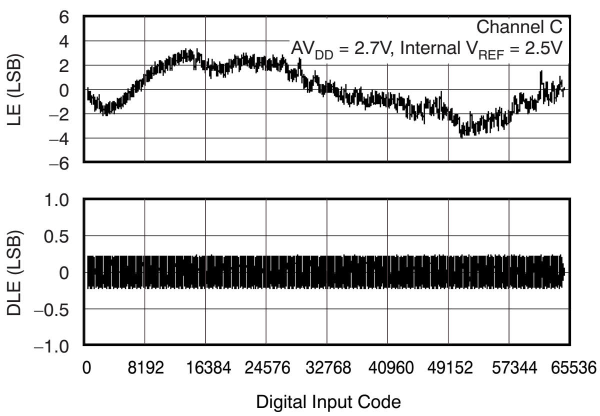


Figure 70.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

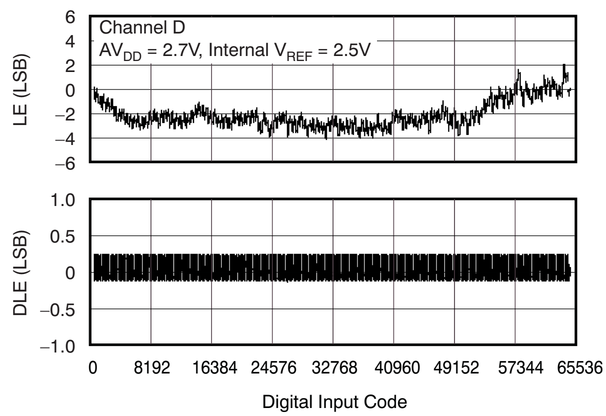


Figure 71.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

OFFSET ERROR vs TEMPERATURE

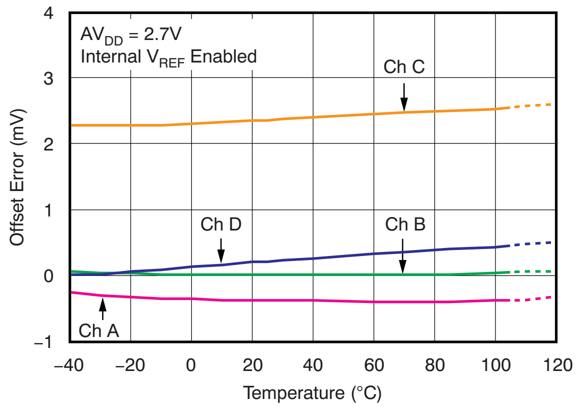


Figure 72.

FULL-SCALE ERROR vs TEMPERATURE

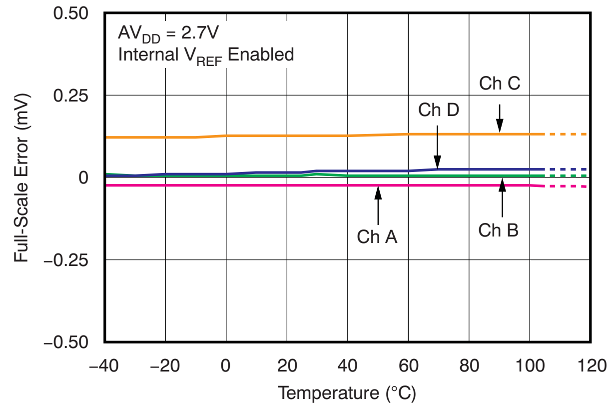


Figure 73.

SOURCE AND SINK CURRENT CAPABILITY

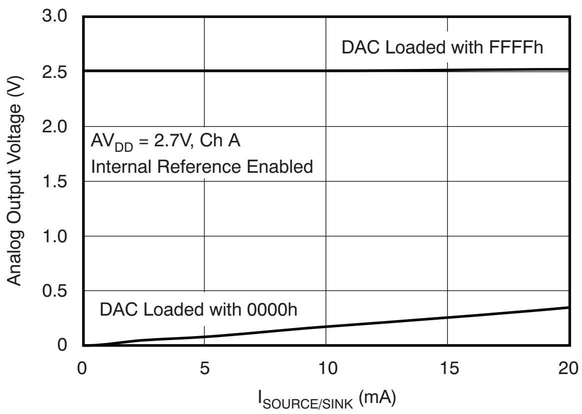


Figure 74.

SOURCE AND SINK CURRENT CAPABILITY

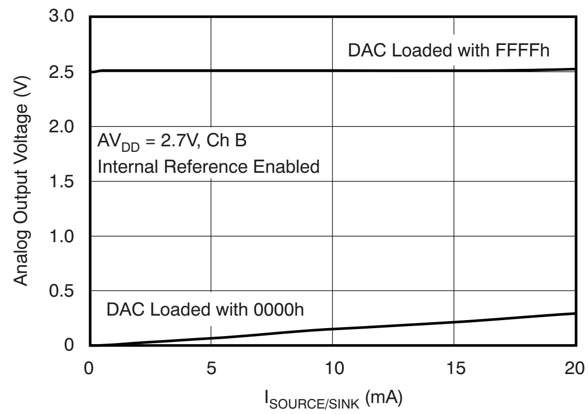


Figure 75.

SOURCE AND SINK CURRENT CAPABILITY

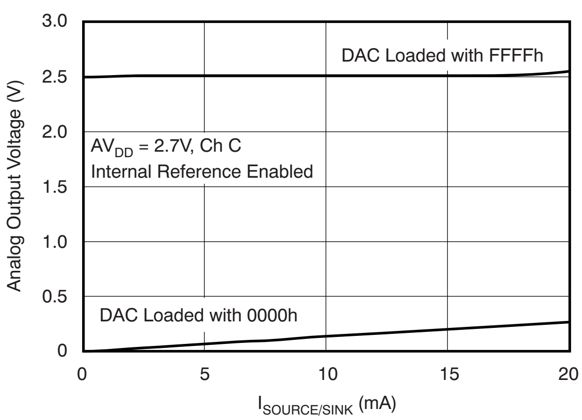


Figure 76.

SOURCE AND SINK CURRENT CAPABILITY

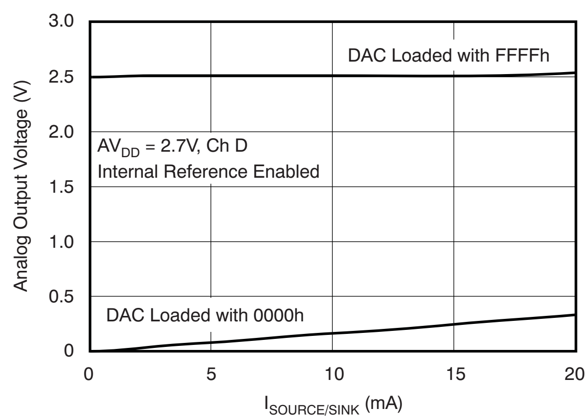


Figure 77.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

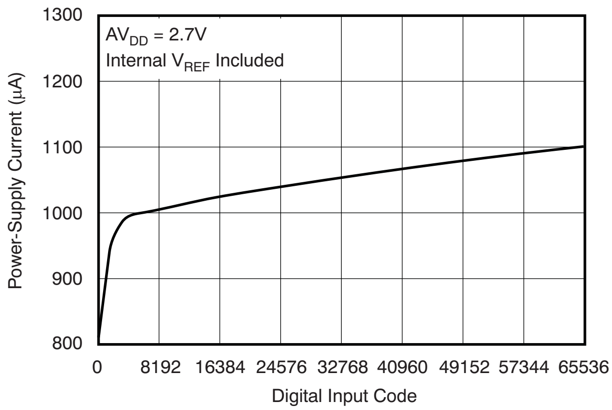


Figure 78.

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

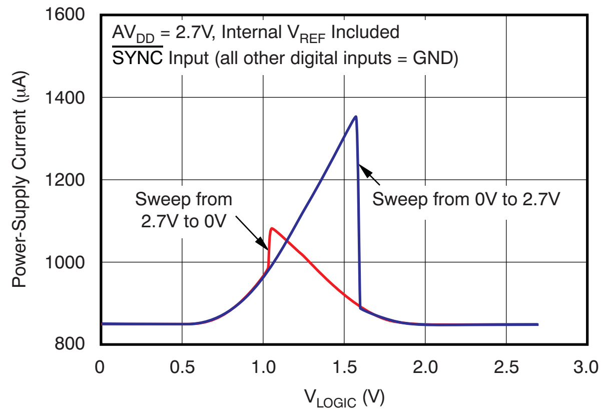


Figure 79.

FULL-SCALE SETTLING TIME: 2.7V RISING EDGE

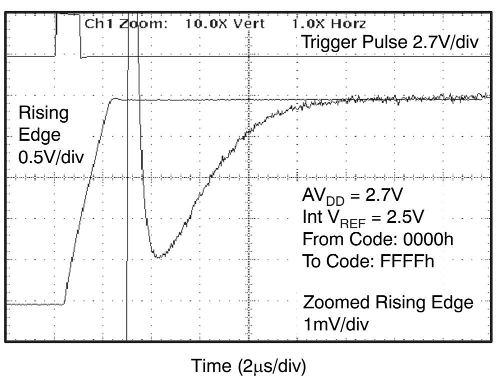


Figure 80.

FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

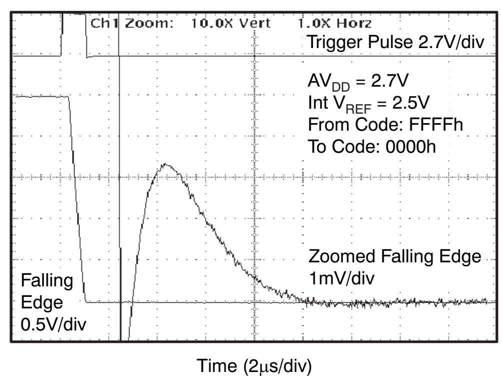


Figure 81.

HALF-SCALE SETTLING TIME: 2.7V RISING EDGE

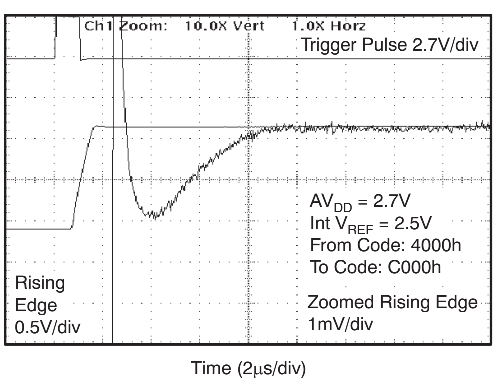


Figure 82.

HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE

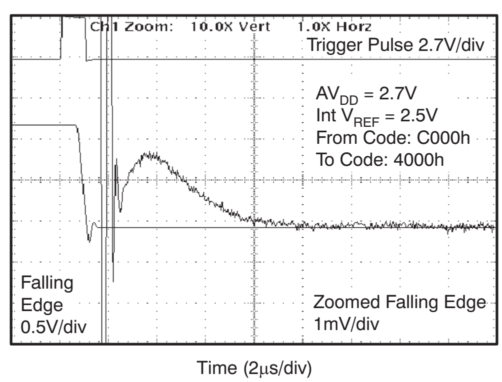


Figure 83.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

GLITCH ENERGY:
2.7V, 1LSB STEP, RISING EDGE

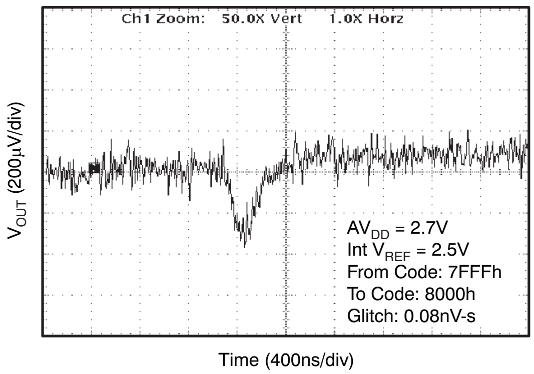


Figure 84.

GLITCH ENERGY:
2.7V, 1LSB STEP, FALLING EDGE

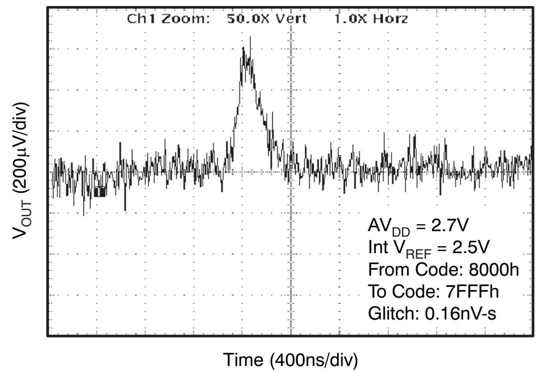


Figure 85.

GLITCH ENERGY:
2.7V, 16LSB STEP, RISING EDGE

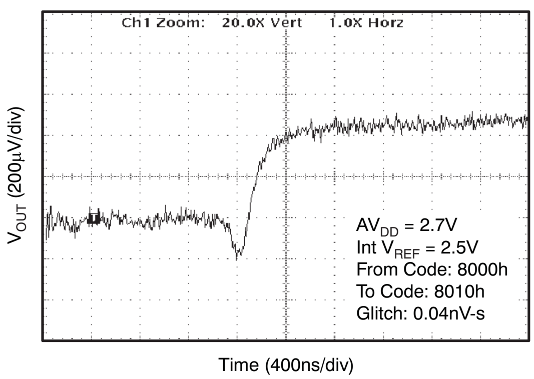


Figure 86.

GLITCH ENERGY:
2.7V, 16LSB STEP, FALLING EDGE

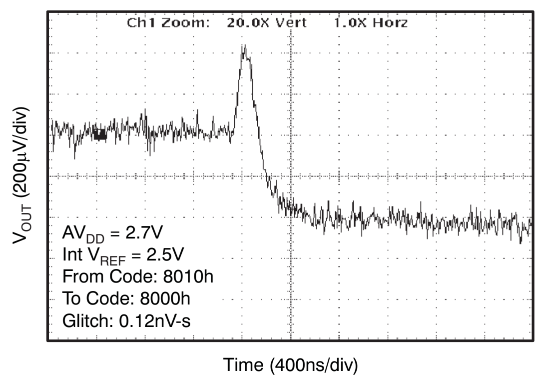


Figure 87.

GLITCH ENERGY:
2.7V, 256LSB STEP, RISING EDGE

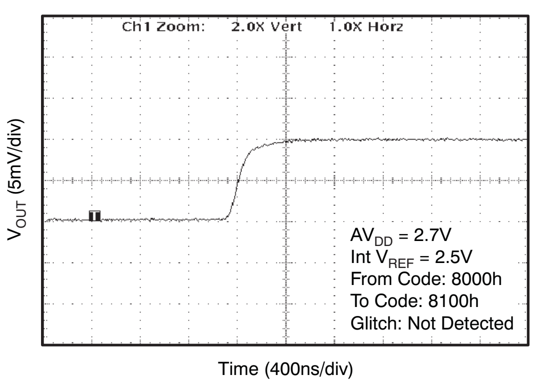


Figure 88.

GLITCH ENERGY:
2.7V, 256LSB STEP, FALLING EDGE

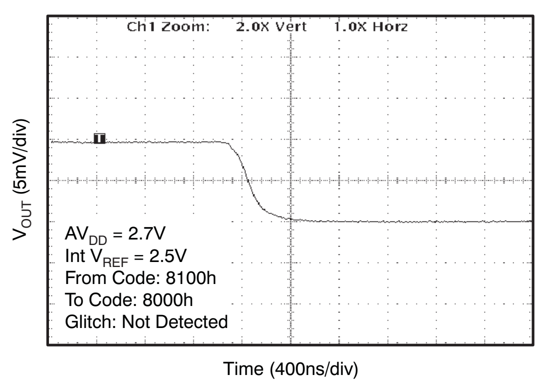


Figure 89.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

POWER-SUPPLY CURRENT vs TEMPERATURE

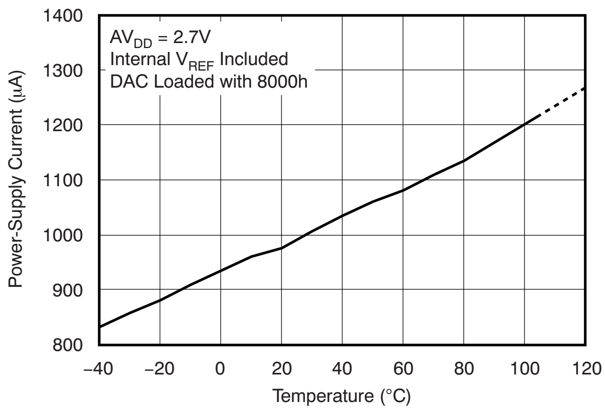


Figure 90.

POWER-DOWN CURRENT vs TEMPERATURE

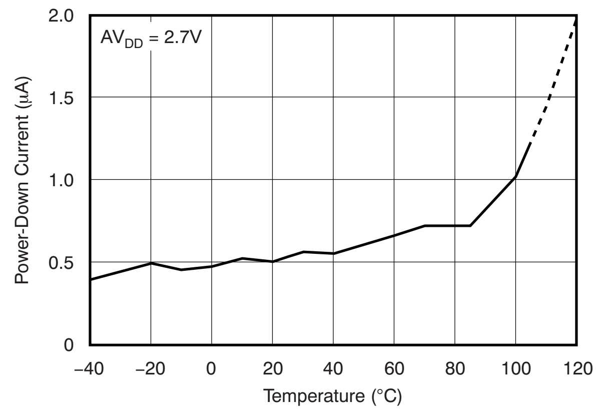


Figure 91.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC8564 architecture consists of a string DAC followed by an output buffer amplifier. Figure 92 shows a block diagram of the DAC architecture.

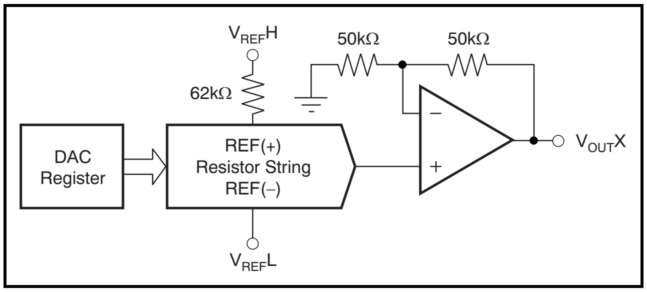


Figure 92. DAC8564 Architecture

The input coding to the DAC8564 is straight binary, so the ideal output voltage is given by Equation 1.

$$V_{OUT}X = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times \frac{D_{IN}}{65536} \quad (1)$$

where D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535. X represents channel A, B, C, or D.

RESISTOR STRING

The resistor string section is shown in Figure 93. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors.

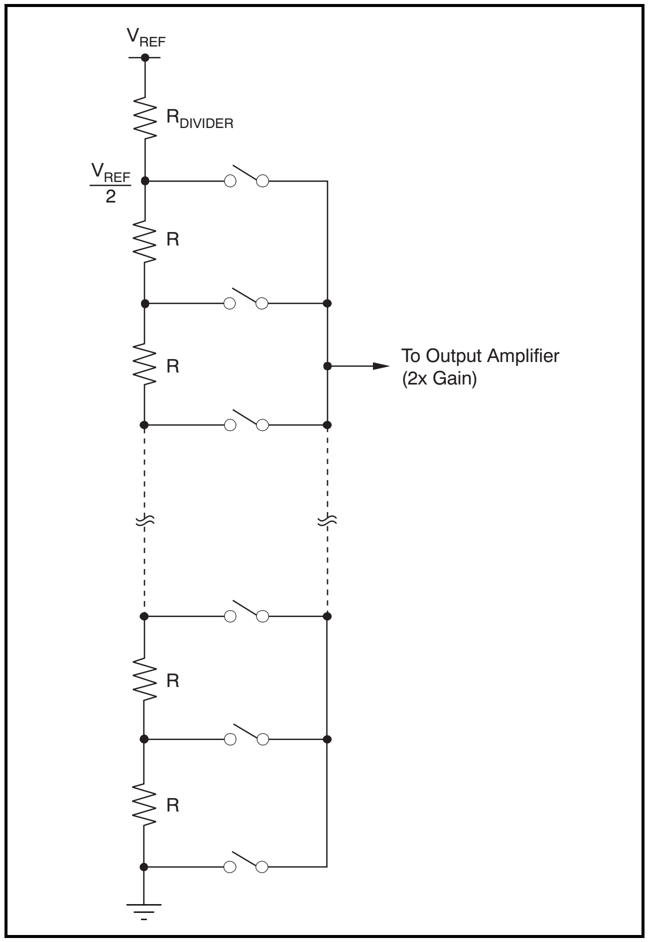


Figure 93. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 2.2V/μs, with a full-scale settling time of 8μs with the output unloaded.

INTERNAL REFERENCE

The DAC8564 includes a 2.5V internal reference that is enabled by default. The internal reference is externally available at the $V_{REF}H/V_{REF}OUT$ pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC8564 is a bipolar transistor-based, precision bandgap voltage reference. Figure 94 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($V_{BE1} - V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is gained up and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

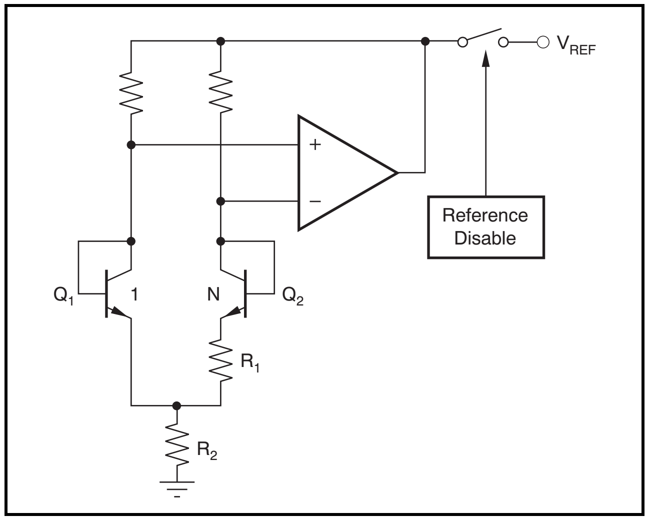


Figure 94. Simplified Schematic of the Bandgap Reference

Enable/Disable Internal Reference

The internal reference in the DAC8564 is enabled by default and operates in automatic mode; however, the reference can be disabled for debugging, evaluation purposes, or when using an external reference. A serial command that requires a 24-bit write sequence (see the *Serial Interface* section) must be used to disable the internal reference, as shown in Table 1. During the time that the internal reference is disabled, the DAC functions normally using an external reference. At this point, the internal reference is disconnected from the $V_{REF}H/V_{REF}OUT$ pin (3-state output). Do not attempt to drive the $V_{REF}H/V_{REF}OUT$ pin externally and internally at the same time indefinitely.

To then enable the internal reference, either perform a power-cycle to reset the device, or write the 24-bit serial command shown in Table 2. These actions put the internal reference back into the default mode. In the default mode, the internal reference powers down automatically when all DACs power down in any of the power-down modes (see the *Power-Down Modes* section); the internal reference powers up automatically when any DAC is powered up.

The DAC8564 also provides the option of keeping the internal reference powered on all the time, regardless of the DAC(s) state (powered up or down). To keep the internal reference powered on, regardless of the DAC(s) state, write the 24-bit serial command shown in Table 3.

Table 1. Write Sequence for Disabling Internal Reference (internal reference always powered down—012000h)

DB23							DB16			DB13													DB0
0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

|——— Data Bits ———| (DB15–DB0)

Table 2. Write Sequence for Enabling Internal Reference (internal reference powered up to default mode—010000h)

DB23							DB16																DB0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

|——— Data Bits ———| (DB15–DB0)

Table 3. Write Sequence for Enabling Internal Reference (internal reference always powered up—011000h)

DB23							DB16				DB12												DB0
0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

|——— Data Bits ———| (DB15–DB0)

SERIAL INTERFACE

The DAC8564 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The DAC8564 input shift register is 24 bits wide, consisting of eight control bits (DB23 to DB16) and 16 data bits (DB15 to DB0). All 24 bits of data are loaded into the DAC under the control of the serial clock input, SCLK. DB23 (MSB) is the first bit that is loaded into the DAC shift register, and is followed by the rest of the 24-bit word pattern, left-aligned. This configuration means that the first 24 bits of data are latched into the shift register and any further clocking of data is ignored. The DAC8564 receives all 24 bits of data and decodes the first eight bits to determine the DAC operating/control mode. The 16 bits of data that follow are decoded by the DAC to determine the equivalent analog output. The data format is straight binary with all '0's corresponding to 0V output and all '1's corresponding to full-scale output (that is, V_{REF} – 1 LSB).

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC8564 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data. Once 24 bits are locked into the shift register, the eight MSBs are used as control bits and the 16 LSBs are used as data. After receiving the 24th falling clock edge, the DAC8564 decodes the eight control bits and 16 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new write sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs. After the 24th falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. Refer to the Typical Characteristics section for Figure 36, Figure 57, and Figure 79 (*Supply Current vs Logic Input Voltage*).

IOV_{DD} AND VOLTAGE TRANSLATORS

The IOV_{DD} pin powers the digital input structures of the DAC8564. For single-supply operation, it can be tied to AV_{DD}. For dual-supply operation, the IOV_{DD} pin provides interface flexibility with various CMOS logic families and should be connected to the logic supply of the system. Analog circuits and internal logic of the DAC8564 use AV_{DD} as the supply voltage. The external logic high inputs translate to AV_{DD} by level shifters. These level shifters use the IOV_{DD} voltage as a reference to shift the incoming logic HIGH levels to AV_{DD}. IOV_{DD} is ensured to operate from 2.7V to 5.5V regardless of the AV_{DD} voltage, assuring compatibility with various logic families. Although specified down to 2.7V, IOV_{DD} operates at as low as 1.8V with degraded timing and temperature performance. For lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND voltages.

INPUT SHIFT REGISTER

The input shift register (SR) of the DAC8564 is 24 bits wide, as shown in Table 4, and consists of eight control bits (DB23 and DB16) and 16 data bits (DB15 to DB0). The first two control bits (DB23 and DB22) are the address match bits. The DAC8564 offers hardware-enabled addressing capability, allowing a single host to talk to up to four DAC8564s through a single SPI bus without any glue logic, enabling up to 16-channel operation. The state of DB23 should match the state of pin A1; similarly, the state of DB22 should match the state of pin A0. If there is no match, the control command and the data (DB21...DB0) are ignored by the DAC8564. That is, if there is no match, the DAC8564 is not addressed. Address matching can be overridden by the broadcast update.

Table 4. Data Input Register Format

DB23											DB12
A1	A0	LD1	LD0	0	DAC Select 1	DAC Select 0	PD0	D15	D14	D13	D12
DB11											DB0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

LD1 (DB21) and LD0 (DB20) control the loading of each analog output with the specified 16-bit data value or power-down command. Bit DB19 must always be '0'. The DAC channel select bits (DB18, DB17) control the destination of the data (or power-down command) from DAC A through DAC D. The final control bit, PD0 (DB16), selects the power-down mode of the DAC8564 channels as well as the power-down mode of the internal reference.

The DAC8564 supports a number of different load commands. The load commands include broadcast commands to address all the DAC8564s on an SPI bus. The load commands are summarized as follows:

DB21 = 0 and DB20 = 0: Single-channel store. The data buffer corresponding to a DAC selected by DB18 and DB17 updates with the contents of SR data (or power-down).

DB21 = 0 and DB20 = 1: Single-channel update. The data buffer and DAC register corresponding to a DAC selected by DB18 and DB17 update with the contents of SR data (or power-down).

DB21 = 1 and DB20 = 0: Simultaneous update. A channel selected by DB18 and DB17 updates with the SR data; simultaneously, all the other channels update with previously stored data (or power-down) from data buffers.

DB21 = 1 and DB20 = 1: Broadcast update. All the DAC8564s on the SPI bus respond, regardless of address matching. If DB18 = 0, SR data are ignored and any channels from all DAC8564s update with previously stored data (or power-down). If DB18 = 1, SR data (or power-down) update any channels of all DAC8564s in the system. This broadcast update feature allows the simultaneous update of up to 16 channels.

Refer to Table 5 for more information.

Table 5. Control Matrix for the DAC8564

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13-DB0	
A1	**A0**	**LD 1**	**LD 0**	**0**	**DAC Sel 1**	**DAC Sel 0**	**PD0**	**MSB**	**MSB-1**	**MSB-2...LSB**	
(Address Select)											**DESCRIPTION**
0/1	0/1	See Below									This address selects one of four possible devices on a single SPI data bus based on the address pin(s) state of each device.
A0 and A1 should correspond to the package address set via pins 13 and 14		0	0	0	0	0	0	Data			Write to buffer A with data
		0	0	0	0	1	0	Data			Write to buffer B with data
		0	0	0	1	0	0	Data			Write to buffer C with data
		0	0	0	1	1	0	Data			Write to buffer D with data
		0	0	0	(00, 01, 10, or 11)		1	See Table 6		0	Write to buffer (selected by DB17 and DB18) with power-down command
		0	1	0	(00, 01, 10, or 11)		0	Data			Write to buffer with data and load DAC (selected by DB17 and DB18)
		0	1	0	(00, 01, 10, or 11)		1	See Table 6		0	Write to buffer with power-down command and load DAC (selected by DB17 and DB18)
		1	0	0	(00, 01, 10, or 11)		0	Data			Write to buffer with data (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers
		1	0	0	(00, 01, 10, or 11)		1	See Table 6		0	Write to buffer with power-down command (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers
Broadcast Modes											
X	X	1	1	0	0	X	X	X			Simultaneously update all channels of all DAC8564 devices in the system with data stored in each channels data buffer
X	X	1	1	0	1	X	0	Data			Write to all devices and load all DACs with SR data
X	X	1	1	0	1	X	1	See Table 6		0	Write to all devices and load all DACs with power-down command in SR

SYNC INTERRUPT

In a normal write sequence, the SYNC line stays low for at least 24 falling edges of SCLK and the addressed DAC register updates on the 24th falling edge. However, if SYNC is brought high before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 95).

POWER-ON RESET TO ZERO-SCALE

The DAC8564 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain that way until a valid write sequence and load command are made to the respective DAC channel. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up.

No device pin should be brought high before power is applied to the device. The internal reference is powered on by default and remains that way until a valid reference-change command is executed.

LDAC FUNCTIONALITY

The DAC8564 offers both a software and hardware simultaneous update function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

DAC8564 data updates are *synchronized* with the falling edge of the 24th SCLK cycle, which follows a falling edge of SYNC. For such *synchronous* updates, the LDAC pin is not required and it must be connected to GND permanently. The LDAC pin is used as a positive edge triggered timing signal for *asynchronous* DAC updates. To do an LDAC operation, single-channel store(s) should be done (loading DAC buffers) by setting LD0 and LD1 to '0'. Multiple single-channel updates can be done in order to set different channel buffers to desired values and then make a rising edge on LDAC. Data buffers of all channels must be loaded with desired data before an LDAC rising edge. After a low-to-high LDAC transition, all DACs are simultaneously updated with the contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output remains unchanged after the LDAC trigger.

ENABLE PIN

For normal operation, the enable pin must be driven to a logic low. If the enable pin is driven high, the DAC8564 stops listening to the serial port. However, SCLK, SYNC, and D_{IN} must not be kept floating, but must be at some logic level. This feature can be useful for applications that share the same serial port.

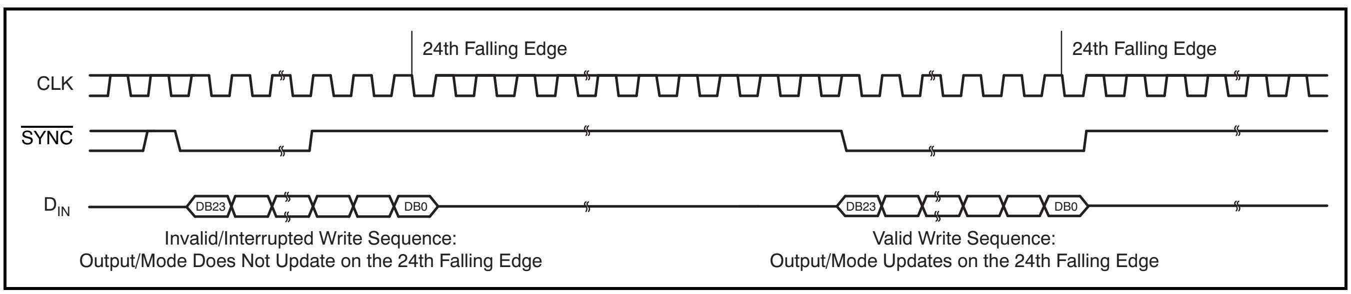


Figure 95. SYNC Interrupt Facility

POWER-DOWN MODES

The DAC8564 has two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. For more information on powering down the reference, see the *Enable/Disable Internal Reference* section.

DAC Power-Down Commands

The DAC8564 uses four modes of operation. These modes are accessed by setting three bits (PD2, PD1, and PD0) in the shift register. Table 6 shows how to control the operating mode with data bits PD0 (DB16), PD1 (DB15), and PD2 (DB14).

Table 6. DAC Operating Modes

PD0 (DB16)	PD1 (DB15)	PD2 (DB14)	DAC OPERATING MODES
0	X	X	Normal operation
1	0	1	Output typically 1kΩ to GND
1	1	0	Output typically 100 kΩ to GND
1	1	1	Output high-impedance

The DAC8564 treats the power-down condition as data; all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC8564s in a system; it is also possible to simultaneously power-down a channel while updating data on other channels.

When the PD0 bit is set to '0', the device works normally with its typical current consumption of 1mA at 5.5V with an input code = 32768. The reference current is included with the operation of all four DACs. However, for the three power-down modes, the supply current falls to 1.3μA at 5.5V (0.5μA at 3.6V). Not only does the supply current fall, but the output stage also switches internally from the output of the amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 6, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open circuited (High-Z). The output stage is shown in Figure 96. In other words, DB16, DB15, and DB14 = '111' represent a power-down condition with Hi-Z output impedance for a selected channel. '101' represents a power-down condition with 1kΩ output impedance, and '110' represents a power-down condition with 100kΩ output impedance.

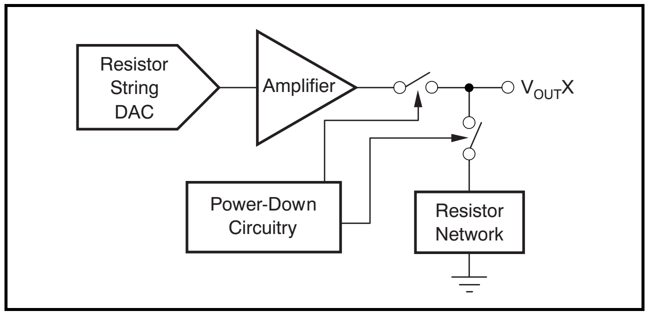


Figure 96. Output Stage During Power-Down

All analog channel circuitries are shut down when the power-down mode is exercised. However, the contents of the DAC register are unaffected when in power down. The time required to exit power-down is typically 2.5μs for V_{DD} = 5V, and 5μs for V_{DD} = 3V. See the Typical Characteristics for more information.

OPERATING EXAMPLES: DAC8564

For the following examples, ensure that DAC pins A0 and A1 are both connected to ground. Pins A0 and A1 must always match data bits DB22 and DB23 within the SPI write sequence/protocol. X = *don't care*. Value can be either '0' or '1'.

Example 1: Write to Data Buffer A Through Buffer D; Load DAC A Through DAC D Simultaneously

- 1st: Write to data buffer A:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	0	0	D15	D14	D13	D12	D11–D0

- 2nd: Write to data buffer B:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	1	0	D15	D14	D13	D12	D11–D0

- 3rd: Write to data buffer C:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	1	0	0	D15	D14	D13	D12	D11–D0

- 4th: Write to data buffer D and simultaneously update all DACs:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	1	0	0	1	1	0	D15	D14	D13	D12	D11–D0

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the fourth write cycle).

Example 2: Load New Data to DAC A Through DAC D Sequentially

- 1st: Write to data buffer A and load DAC A: DAC A output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	0	0	0	D15	D14	D13	D12	D11–D0

- 2nd: Write to data buffer B and load DAC B: DAC B output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	0	1	0	D15	D14	D13	D12	D11–D0

- 3rd: Write to data buffer C and load DAC C: DAC C output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	1	0	0	D15	D14	D13	D12	D11–D0

- 4th: Write to data buffer D and load DAC D: DAC D output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	1	1	0	D15	D14	D13	D12	D11–D0

After completion of each write cycle, DAC analog output settles to the voltage specified.

Example 3: Power-Down DAC A and DAC B to 1kΩ and Power-Down DAC C and DAC D to 100kΩ Simultaneously

- 1st: Write power-down command to data buffer A: DAC A to 1kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	0	1	0	1	X	X	X

- 2nd: Write power-down command to data buffer B: DAC B to 1kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	1	1	0	1	X	X	X

- 3rd: Write power-down command to data buffer C: DAC C to 100kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	1	0	1	1	0	X	X	X

- 4th: Write power-down command to data buffer D: DAC D to 100kΩ and simultaneously update all DACs.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	1	0	0	1	1	1	1	0	X	X	X

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously power-down to each respective specified mode upon completion of the fourth write sequence.

Example 4: Power-Down DAC A Through DAC D to High-Impedance Sequentially

- 1st: Write power-down command to data buffer A and load DAC A: DAC A output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	0	0	1	1	1	X	X	X

- 2nd: Write power-down command to data buffer B and load DAC B: DAC B output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	0	1	1	1	1	X	X	X

- 3rd: Write power-down command to data buffer C and load DAC C: DAC C output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	1	0	1	1	1	X	X	X

- 4th: Write power-down command to data buffer D and load DAC D: DAC D output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	1	1	1	1	1	X	X	X

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the first, second, third, and fourth write sequences, respectively.

Example 5: Power-Down All Channels Simultaneously while Reference is Always Powered Up

- 1st: Write sequence for enabling the DAC8564 internal reference all the time:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	0	1	0	0	0	1	X

- 2nd: Write sequence to power-down all DACs to high-impedance:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	1	1	0	1	0	1	1	1	X	X	X

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the first and second write sequences, respectively.

Example 6: Write a Specific Value to All DACs while Reference is Always Powered Down

- 1st: Write sequence for disabling the DAC8564 internal reference all the time (after this sequence, the DAC8564 requires an external reference source to function):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	0	1	0	0	1	0	X

- 2nd: Write sequence to write specified data to all DACs:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	1	1	0	1	0	0	D15	D14	D13	D12	D11–D0

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the fourth write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the fourth write cycle). Reference is always powered-down.

Example 7: Write a Specific Value to DAC A, while Reference is Placed in Default Mode and All Other DACs are Powered Down to High-Impedance

- 1st: Write sequence for placing the DAC8564 internal reference into default mode. Alternately, this step can be replaced by performing a power-on reset (see the *Power-On Reset* section):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	0	0	0	0	1	0	0	0	0	X

- 2nd: Write sequence to power-down all DACs to high-impedance (after this sequence, the DAC8564 internal reference powers down automatically):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	1	1	0	1	0	1	1	1	X	X	X

- 3rd: Write sequence to power-up DAC A to a specified value (after this sequence, the DAC8564 internal reference powers up automatically):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11–DB0
0	0	0	1	0	0	0	0	D15	D14	D13	D12	D11–D0

The DAC B, DAC C, and DAC D analog outputs simultaneously power-down to high-impedance, and DAC A settles to the specified value upon completion.

APPLICATION INFORMATION

INTERNAL REFERENCE

The internal reference of the DAC8564 does not require an external load capacitor for stability because it is stable with any capacitive load. However, for improved noise performance, an external load capacitor of 150nF or larger connected to the $V_{REF}H/V_{REF}OUT$ output is recommended. Figure 97 shows the typical connections required for operation of the DAC8564 internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

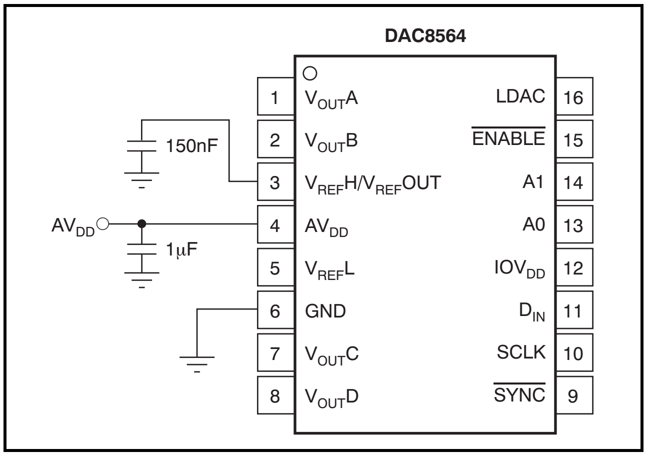


Figure 97. Typical Connections for Operating the DAC8564 Internal Reference

Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7V to 5.5V, the variation at $V_{REF}H/V_{REF}OUT$ is less than 10μV/V; see the Typical Characteristics.

Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the *box* method described by Equation 2:

$$\text{Drift Error} = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^6 \ (\text{ppm}/°\text{C}) \qquad (2)$$

Where:

V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.

V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.

V_{REF} = 2.5V, target value for reference output voltage.

The internal reference (grades C and D) features an exceptional typical drift coefficient of 2ppm/°C from –40°C to +120°C. Characterizing a large number of units, a maximum drift coefficient of 5ppm/°C (grades C and D) is observed. Temperature drift results are summarized in the Typical Characteristics.

Noise Performance

Typical 0.1Hz to 10Hz voltage noise can be seen in Figure 8, *Internal Reference Noise*. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at $V_{REF}H/V_{REF}OUT$ without any external components is depicted in Figure 7, *Internal Reference Noise Density vs Frequency*. Another noise density spectrum is also shown in Figure 7. This spectrum was obtained using a 4.8μF load capacitor at $V_{REF}H/V_{REF}OUT$ for noise filtering. Internal reference noise impacts the DAC output noise; see the *DAC Noise Performance* section for more details.

Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 98. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are summarized in the Typical Characteristics. Force and sense lines should be used for applications that require improved load regulation.

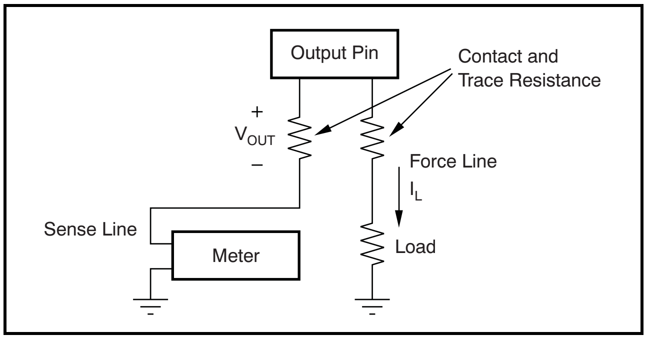


Figure 98. Accurate Load Regulation of the DAC8564 Internal Reference

Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses (see Figure 6, the typical long-term stability curve). The typical drift value for the internal reference is 50ppm from 0 hours to 1900 hours. This parameter is characterized by powering-up and measuring 20 units at regular intervals for a period of 1900 hours.

Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at +25°C, cycling the device through the operating temperature range, and returning to +25°C. Hysteresis is expressed by Equation 3:

$$V_{HYST} = \left(\frac{|V_{REF\_PRE} - V_{REF\_POST}|}{V_{REF\_NOM}} \right) \times 10^6 \text{ (ppm/°C)} \tag{3}$$

Where:

V_{HYST} = thermal hysteresis.

V_{REF_PRE} = output voltage measured at +25°C pre-temperature cycling.

V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to +120°C, and returns to +25°C.

DAC NOISE PERFORMANCE

Typical noise performance for the DAC8564 with the internal reference enabled is shown in Figure 54 to Figure 56. Output noise spectral density at the V_{OUT} pin versus frequency is depicted in Figure 54 for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is $120nV/\sqrt{Hz}$ at 1kHz and $100nV/\sqrt{Hz}$ at 1MHz. High-frequency noise can be improved by filtering the reference noise as shown in Figure 55, where a 4.8μF load capacitor is connected to the $V_{REF}H/V_{REF}OUT$ pin and compared to the no-load condition. Integrated output noise between 0.1Hz and 10Hz is close to $6\mu V_{PP}$ (midscale), as shown in Figure 56.

BIPOLAR OPERATION USING THE DAC8564

The DAC8564 is designed for single-supply operation, but a bipolar output range is also possible using the circuit in either Figure 99 or Figure 100. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated with Equation 4:

$$V_O = \left[V_{REF} \times \left(\frac{D}{65536} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_2}{R_1} \right) \right] \quad (4)$$

where *D* represents the input code in decimal (0–65535).

With $V_{REF}H = 5V$, $R_1 = R_2 = 10k\Omega$.

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5V \quad (5)$$

This result has an output voltage range of ±5V with 0000h corresponding to a –5V output and FFFFh corresponding to a +5V output, as shown in Figure 99. Similarly, using the internal reference, a ±2.5V output voltage range can be achieved, as Figure 100 shows.

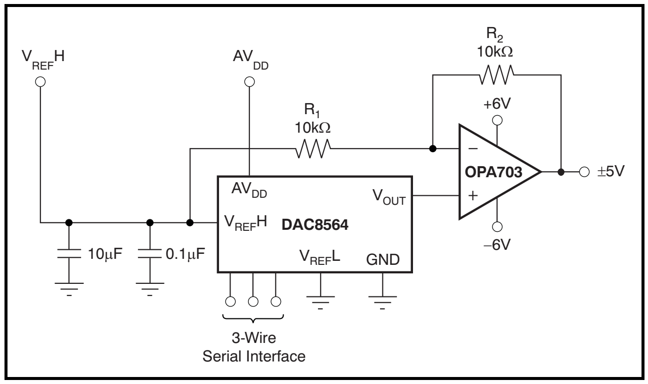


Figure 99. Bipolar Output Range Using External Reference at 5V

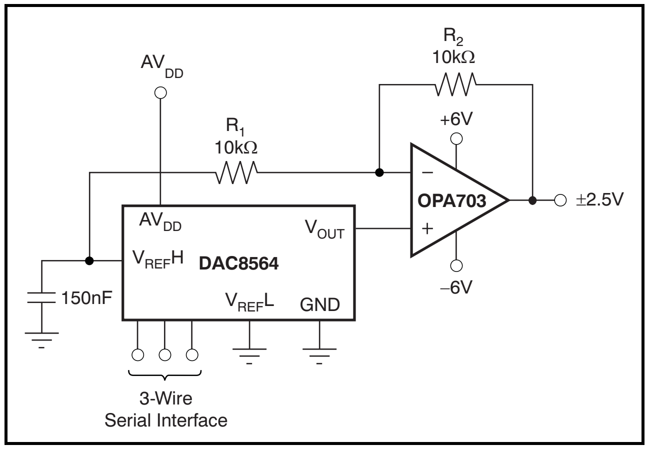


Figure 100. Bipolar Output Range Using Internal Reference

MICROPROCESSOR INTERFACING

DAC SPI Interfacing

Care must be taken with the digital control signals that are applied directly to the DAC, especially with the SYNC pin. The SYNC pin must not be toggled without having a full SCLK pulse in between. If this condition is violated, the SPI interface locks up in an erroneous state, causing the DAC to behave incorrectly and have errors. The DAC can be recovered from this faulty state by writing a valid SPI command or using the SYNC pin correctly; communication will then be restored. Avoid glitches and transients on the SYNC line to ensure proper operation.

DAC8564 to an 8051 Interface

Figure 101 shows a serial interface between the DAC8564 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8564, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051; in this case, port line P3.3 is used. When data are to be transmitted to the DAC8564, P3.3 is taken low. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC8564 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this requirement into account, and *mirror* the data as needed.

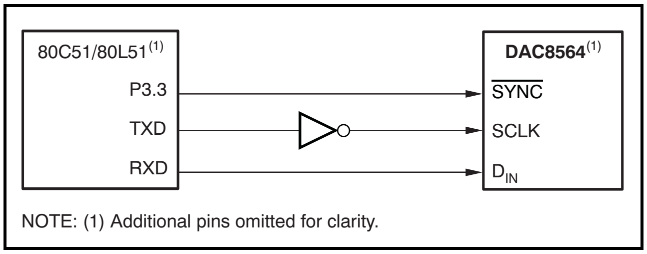


Figure 101. DAC8564 to 80C51/80L51 Interface

DAC8564 to Microwire Interface

Figure 102 shows an interface between the DAC8564 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DAC8564 on the rising edge of the SK signal.

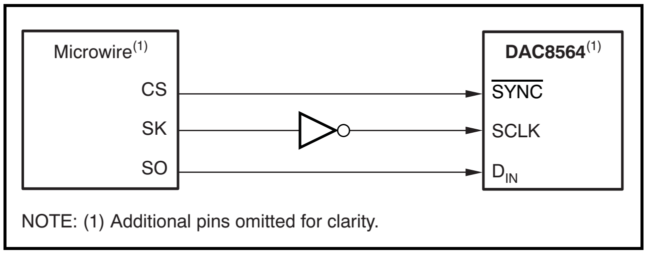


Figure 102. DAC8564 to Microwire Interface

DAC8564 to 68HC11 Interface

Figure 103 shows a serial interface between the DAC8564 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8564, while the MOSI output drives the serial data line of the DAC. The SYNC signal derives from a port line (PC7), similar to the 8051 diagram.

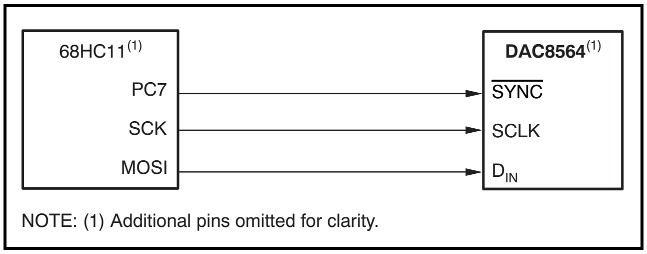


Figure 103. DAC8564 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is held low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC8564, PC7 is left low after the first eight bits are transferred; then, a second and third serial write operation are performed to the DAC. PC7 is taken high at the end of this procedure.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8564 offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

As a result of the single ground pin of the DAC8564, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to V_{DD} should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1μF to 10μF capacitor and 0.1μF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100μF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply and remove the high-frequency noise.

PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

Least Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by 2^n, where *n* is the resolution of the converter.

Most Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. DNL is measured in LSBs.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is less than 1LSB, the DAC is said to be monotonic.

Full-Scale Error

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code (0xFFFF). Ideally, the output should be V_{DD} – 1 LSB. The full-scale error is expressed in percent of full-scale range (%FSR).

Offset Error

The offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes (code 485 and 64714). Since the offset error is defined by a straight line, it can have a negative or positive value. Offset error is measured in mV.

Zero-Code Error

The zero-code error is defined as the DAC output voltage, when all '0's are loaded into the DAC register. Zero-scale error is a measure of the difference between actual output voltage and ideal output voltage (0V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

Gain Error

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (%FSR).

Full-Scale Error Drift

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of %FSR/°C.

Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in μV/°C.

Zero-Code Error Drift

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in μV/°C.

Gain Temperature Coefficient

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains at least constant for each step increase (or decrease) in the input code.

DYNAMIC PERFORMANCE

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

Slew Rate

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left(\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right)$$

Where $\Delta V_{OUT}(t)$ is the output produced by the amplifier as a function of time *t*.

Output Voltage Settling Time

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within ±0.003% (or whatever value is specified) of full-scale range (FSR).

Code Change/Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolts-second (nV-s), and is measured when the digital input code is changed by 1LSB at the major carry transition.

Digital Feedthrough

Digital feedthrough is defined as impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all '0's to all '1's and vice versa.

Channel-to-Channel DC Crosstalk

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel while monitoring another DAC channel remains at midscale. It is expressed in LSB.

Channel-to-Channel AC Crosstalk

AC crosstalk in a multi-channel DAC is defined as the amount of ac interference experienced on the output of a channel at a frequency (f) (and its harmonics), when the output of an adjacent channel changes its value at the rate of frequency (f). It is measured with one channel output oscillating with a sine wave of 1kHz frequency, while monitoring the amplitude of 1kHz harmonics on an adjacent DAC channel output (kept at zero scale). It is expressed in dB.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is defined as the ratio of the root mean-squared (RMS) value of the output signal divided by the RMS values of the sum of all other spectral components below one-half the output frequency, not including harmonics or dc. SNR is measured in dB.

Total Harmonic Distortion (THD)

Total harmonic distortion + noise is defined as the ratio of the RMS values of the harmonics and noise to the value of the fundamental frequency. It is expressed in a percentage of the fundamental frequency amplitude at sampling rate f_S.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from dc to the full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. SFDR is specified in decibels relative to the carrier (dBc).

Signal-to-Noise plus Distortion (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing any internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DAC Output Noise Density

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density ($nV/\sqrt{Hz}$). It is measured by loading the DAC to midscale and measuring noise at the output.

DAC Output Noise

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at midscale while filtering the output voltage within a band of 0.1Hz to 10Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage (V_{pp}).

Full-Scale Range (FSR)

Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an *n*-bit DAC, these values are usually given as the values matching with code 0 and 2^n.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2010) to Revision D **Page**

- Changed Output Voltage parameter min/max values from 2.4995 and 2.5005 to 2.4975 and 2.5025, respectively 4
- Changed Initial Accuracy parameter min/max values from –0.02 and 0.02 to –0.1 and 0.1, respectively 4

Changes from Revision B (March 2008) to Revision C **Page**

- Changed t_2 minimum values in the *Timing Requirements* table 7
- Added *DAC SPI Interfacing* subsection to *Microprocessor Interfacing* section 39

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8564IAPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564	Samples
DAC8564IAPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564	Samples
DAC8564IBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564 B	Samples
DAC8564ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564	Samples
DAC8564ICPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564	Samples
DAC8564ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564	Samples
DAC8564IDPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564 D	Samples
DAC8564IDPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564 D	Samples
DAC8564IDPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	DAC 8564 D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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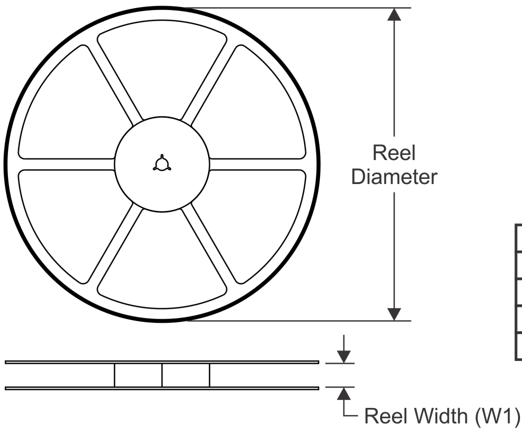
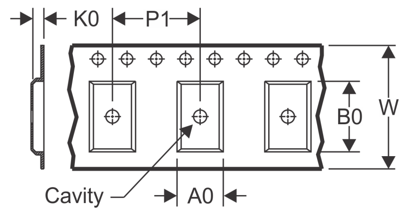
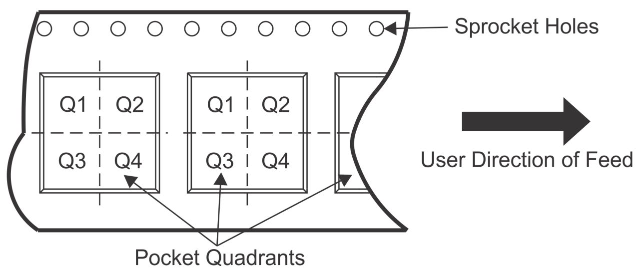
TAPE AND REEL INFORMATION





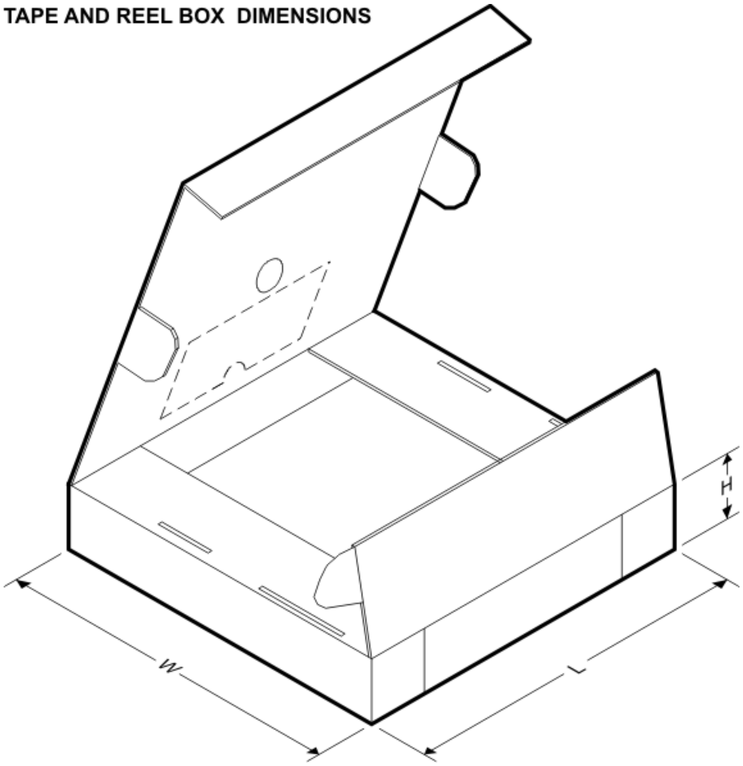
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8564IAPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8564ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8564IDPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

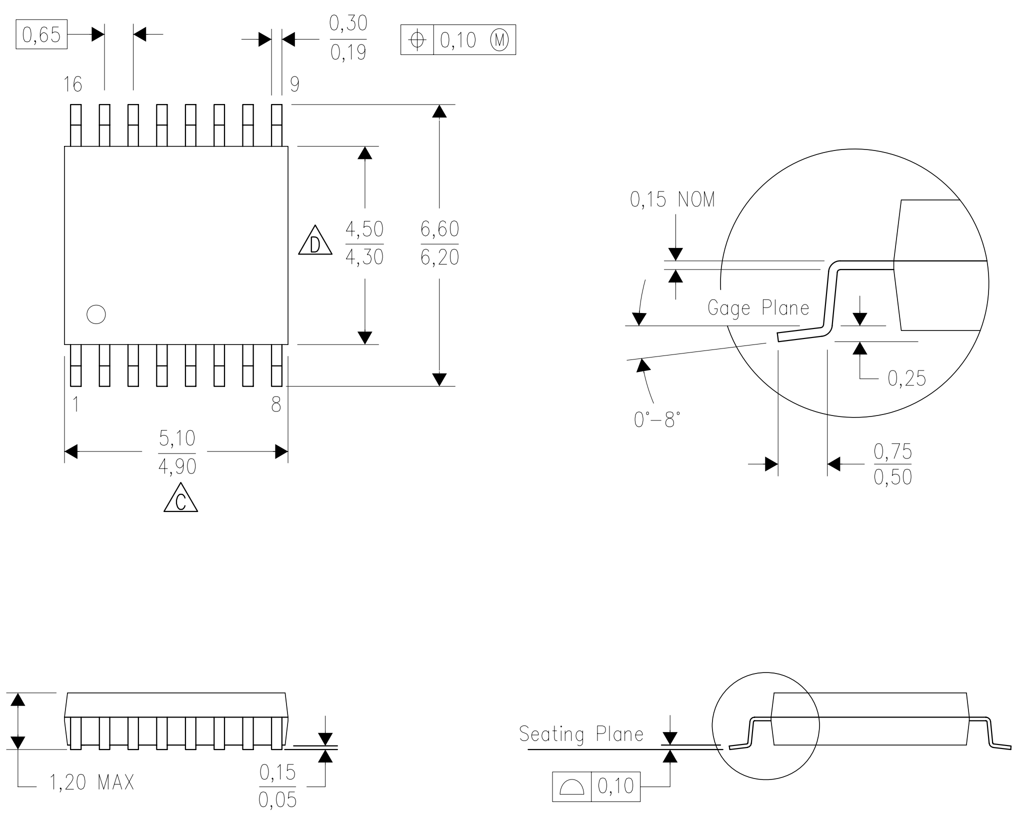
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8564IAPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
DAC8564ICPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
DAC8564IDPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

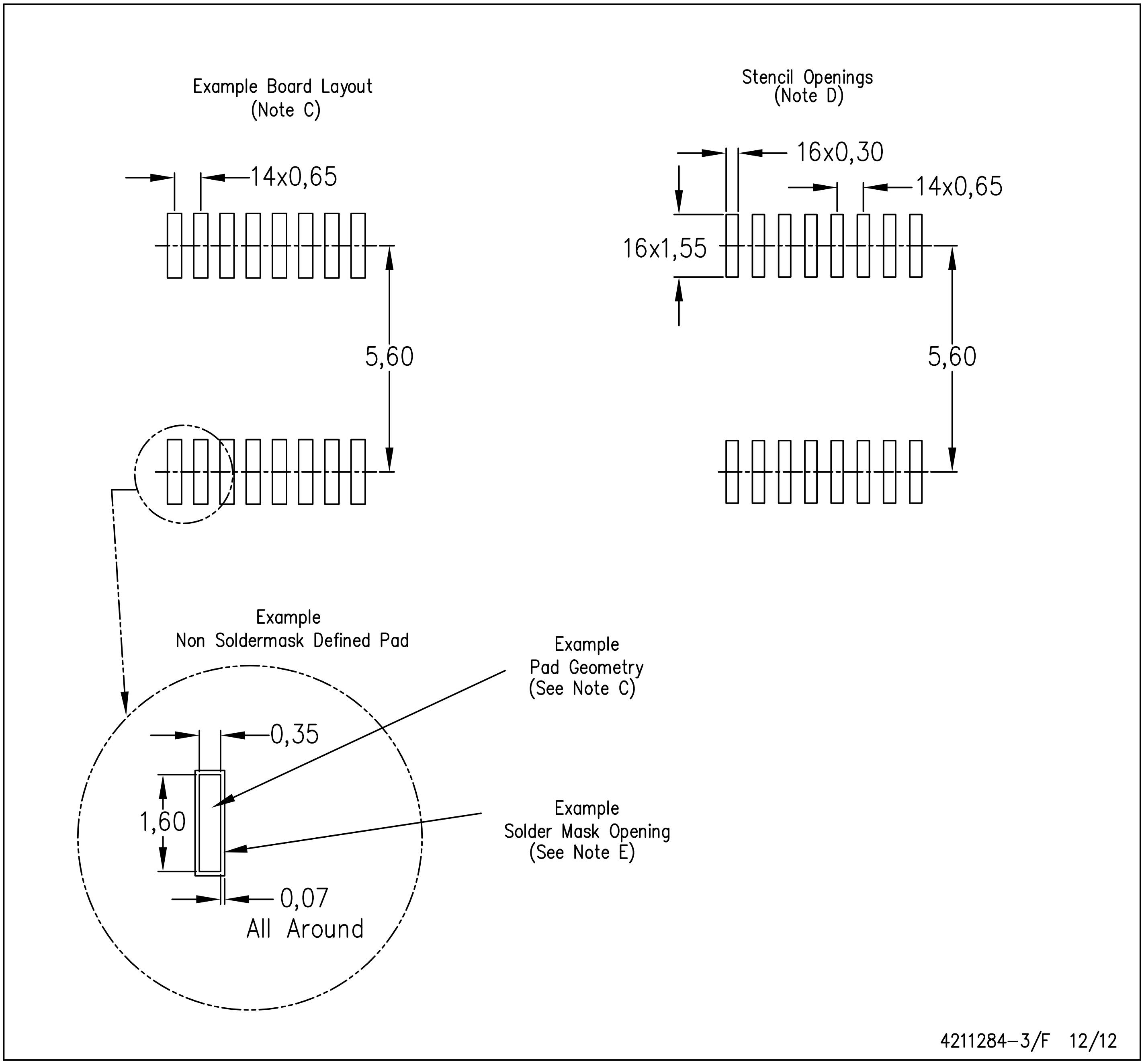
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.