LF412QML

LF412QML Low Offset, Low Drift Dual JFET Input Operational Amplifier

Literature Number: SNOSAO7

National Semiconductor

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LF412QML

Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and guaranteed input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Input offset voltage drift: 20 µV/°C (max)
- Low input bias current: 50 pA (Typ)
- Low input noise current: 0.01 $pA/\sqrt{Hz}$ (Typ)
- Wide gain bandwidth: 2.7 MHz (min)
- High slew rate: 8V/µs (min)
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion <0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

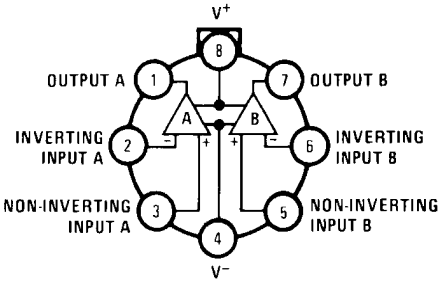
Ordering Information

NS Part Number	Part Number	NS Package Number	Package Description
LF412MH/883		H08A	8LD Metal Can
LF412MJ/883		J08A	8LD CERDIP
LF412 MD8		(*Note 1*)	Bare Die

Note 1: FOR ADDITIONAL DIE INFORMATION, PLEASE VISIT THE HI REL WEB SITE AT: www.national.com/analog/space/level_die

Connection Diagrams

Metal Can Package



Note. Pin 4 connected to case.

TOP VIEW

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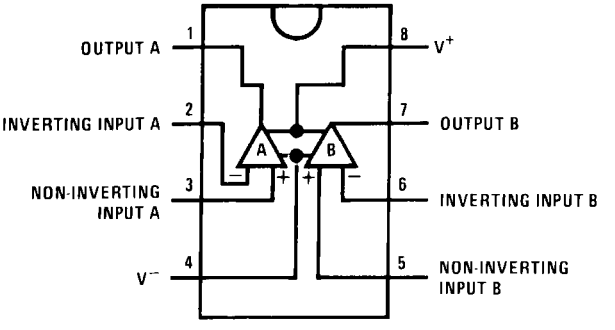
See NS Package Number H08A

Dual-In-Line Package



TOP VIEW

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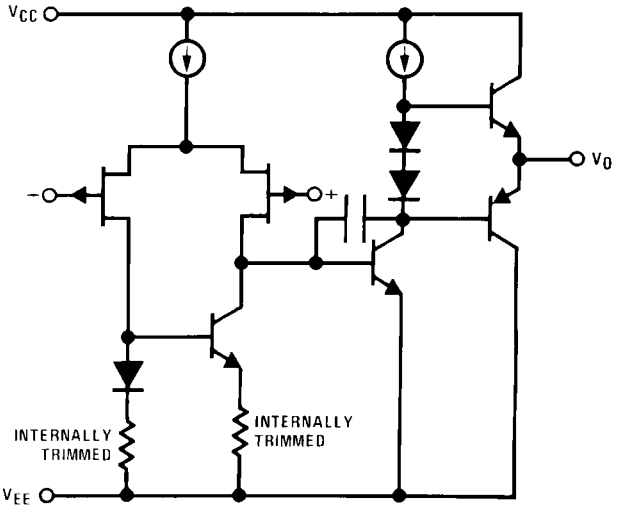
See NS Package Number J08A

BI-FET II™ is a trademark of National Semiconductor Corporation.

Simplified Schematic

1/2 Dual



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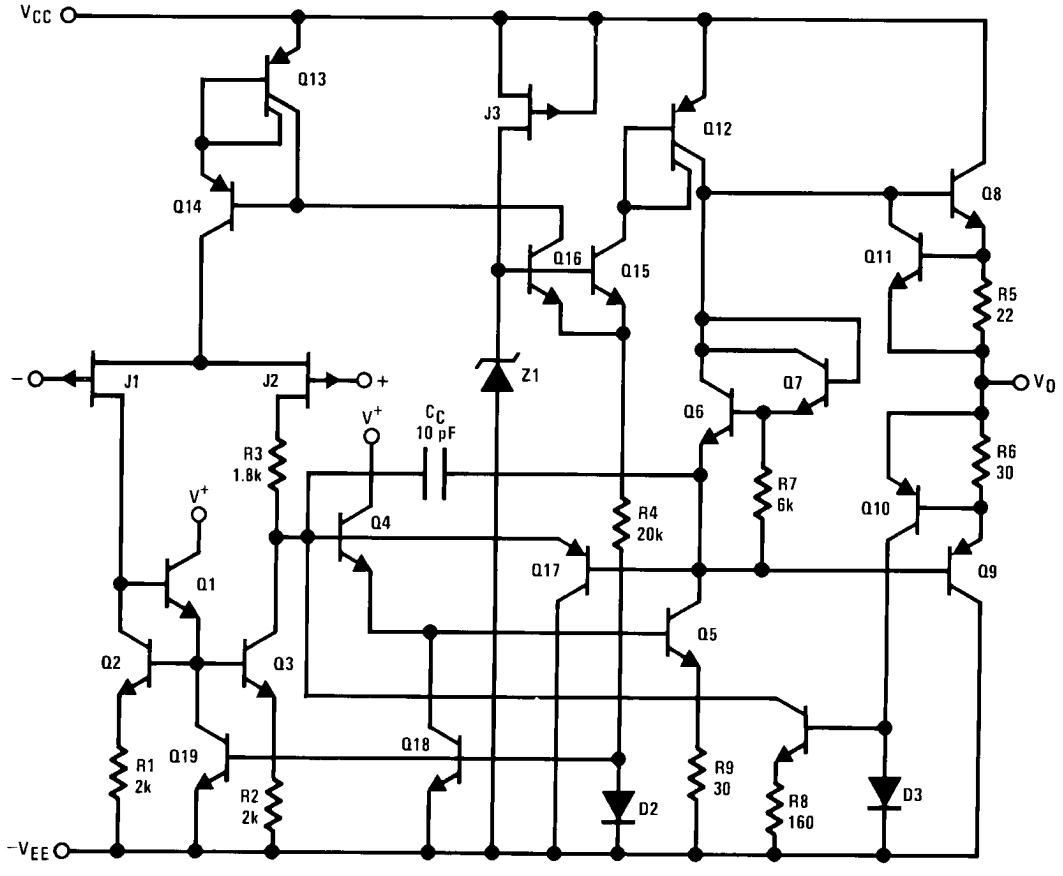
Detailed Schematic



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Absolute Maximum Ratings (*Note 2*)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input voltage Range(*Note 4*)	±15V
Output Short Circuit Duration (*Note 5*)	Continuous
Power Dissipation(*Note 3*)	
Metal Can Package	800mW
CERDIP Package	800mW
T_{Jmax}	150°C
Thermal Resistance	
θ_{JA}	
Metal Can Package (Still Air)	160°C/W
Metal Can Package (500 LF/Min Air Flow)	83°C/W
CERDIP Package (Still Air)	122°C/W
CERDIP Package (500 LF/Min Air Flow)	66°C/W
θ_{JC}	
Metal Can Package	38°C/W
CERDIP Package	15°C/W
Supply voltage Range	±5V to ±15V
Operating Temperature Range	$-55°C \leq T_A \leq 125°C$
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$
Lead Temperature Soldering (10 Sec)	260°C
ESD Tolerance(*Note 6*)	1,700V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

Electrical Characteristics

DC parameters

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
V_{IO}	Input offset Voltage	R_S = 10KΩ		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
ΔV_{IO} / ΔT	Temperature Coefficient of Input Offset Voltage	R_S = 10KΩ, 25°C ≤ T_A ≤ 125°C	(*Note 8*)	-20	20	µV/°C	2
		R_S = 10KΩ, -55°C ≤ T_A ≤ 25°C	(*Note 8*)	-20	20	µV/°C	3
I_{IO}	Input Offset Current		(*Note 10*)	-0.1	0.1	nA	1
				-25	25	nA	2
±I_{IB}	Input Bias Current		(*Note 10*)		0.2	nA	1
					50	nA	2
CMRR	Common Mode Rejection Ratio	R_S ≤ 10KΩ, V_{CM} = ±11V		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	6V ≤ +V_{CC} ≤ 15V, -V_{CC} = -15V		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	+V_{CC} = 15V, -15V ≤ -V_{CC} ≤ -6V		70		dB	1, 2, 3
I_S	Supply Current				6.5	mA	1, 2, 3
-I_{OS}	Output Short Circuit Current			13	45	mA	1
				6.0	45	mA	2, 3
+I_{OS}	Output Short Circuit Current			-45	-13	mA	1
				-45	-6.0	mA	2, 3
+A_{VS}	Large Signal Voltage Gain	V_O = 0 to 10V, R_L = 2KΩ	(*Note 9*)	25		V/mV	4
				15		V/mV	5, 6
-A_{VS}	Large Signal Voltage Gain	V_O = 0 to -10V, R_L = 2KΩ	(*Note 9*)	25		V/mV	4
				15		V/mV	5, 6
+V_O	Output Voltage Swing	R_L = 10KΩ, +V_I = 11V, -V_I = -11V		12		V	4, 5, 6
-V_O	Output Voltage Swing	R_L = 10KΩ, +V_I = -11V, -V_I = 11V			-12	V	4, 5, 6
V_{CM}	Input Common Mode Voltage Range		(*Note 7*)	–11	11	V	1, 2, 3

AC Parameters

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
SR+	Slew Rate	V_O = -5V to 5V		8.0		V/µs	7
SR-	Slew Rate	V_O = 5V to -5V		8.0		V/µs	7
GBW	Gain Bandwidth Product			2.7		MHz	7

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 4: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 5: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

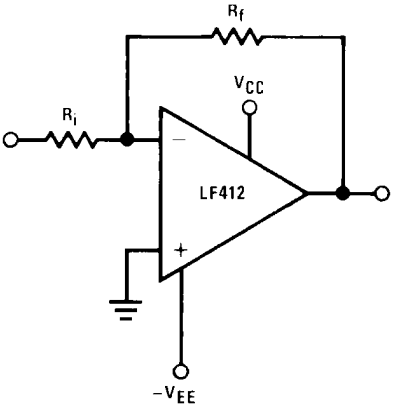
Note 7: Guaranteed by CMRR.

Note 8: Guaranteed parameter, not tested.

Note 9: Datalog reading in K = V/mV.

Note 10: R_S = 10KΩ @ +125°C

Typical Connection



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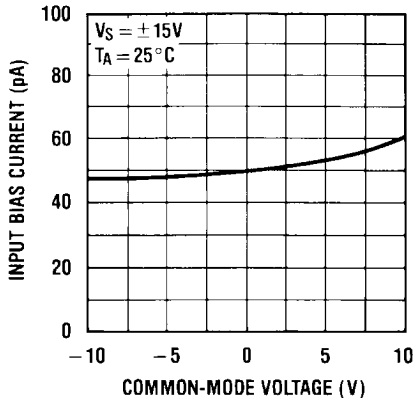
Typical Performance Characteristics

Input Bias Current



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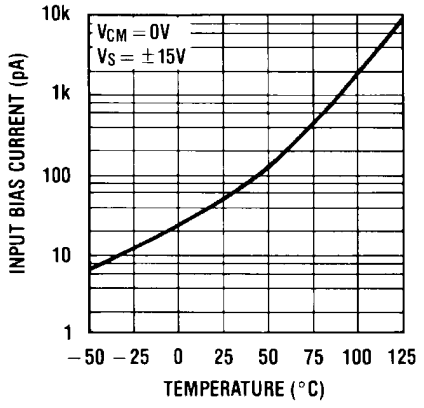
Input Bias Current



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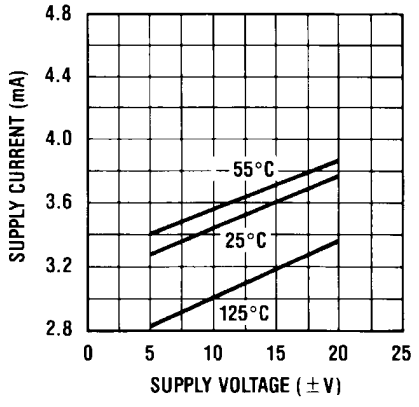
Supply Current



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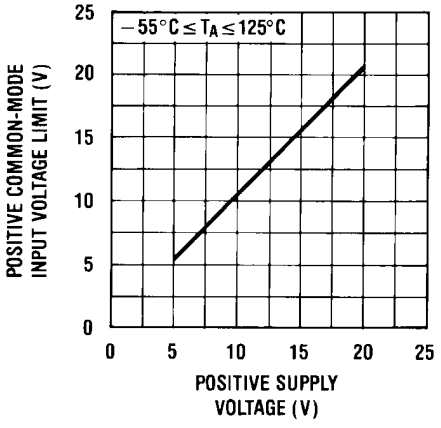
Positive Common-Mode Input Voltage Limit



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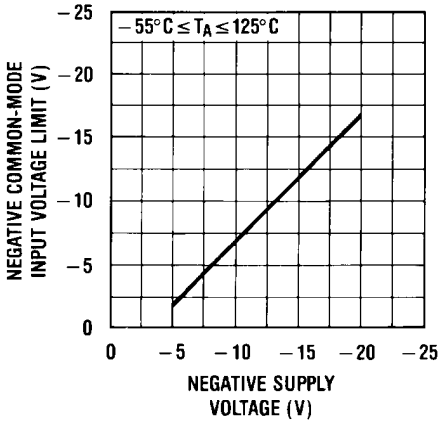
Negative Common-Mode Input Voltage Limit



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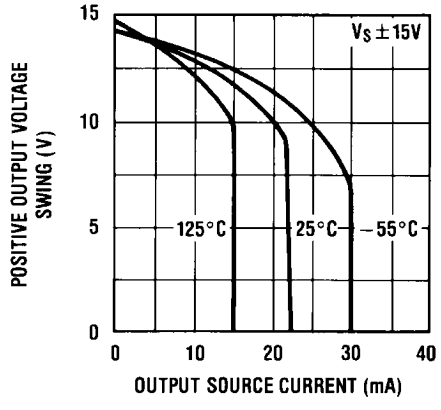
Positive Current Limit



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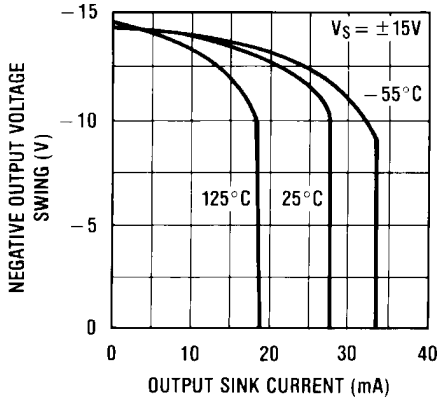
Negative Current Limit



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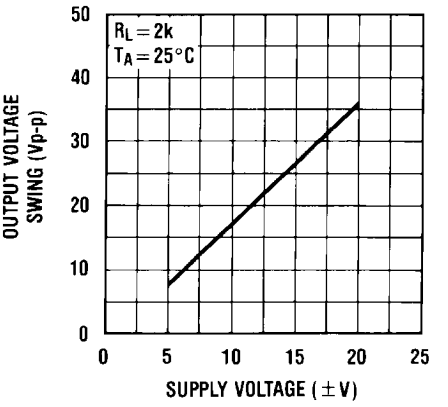
Output Voltage Swing



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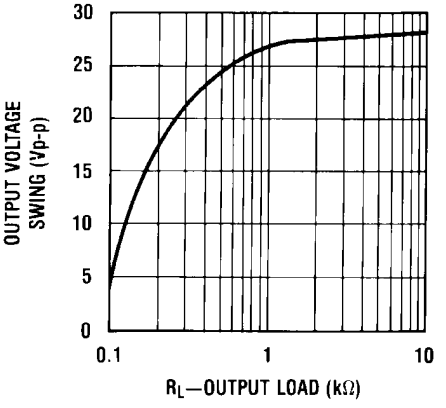
Output Voltage Swing



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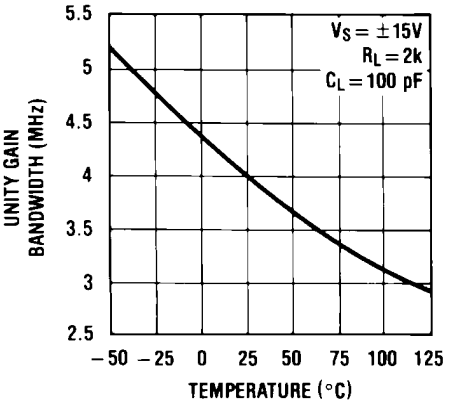
Gain Bandwidth



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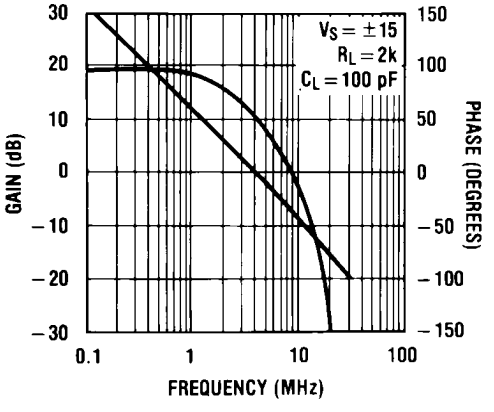
Bode Plot



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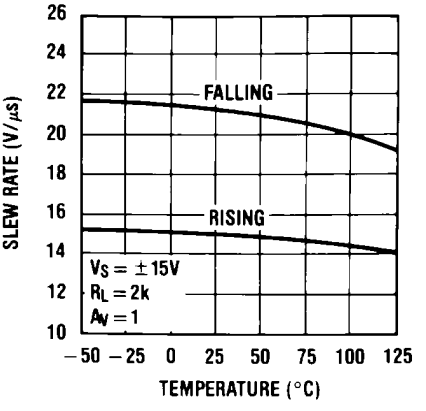
Slew Rate



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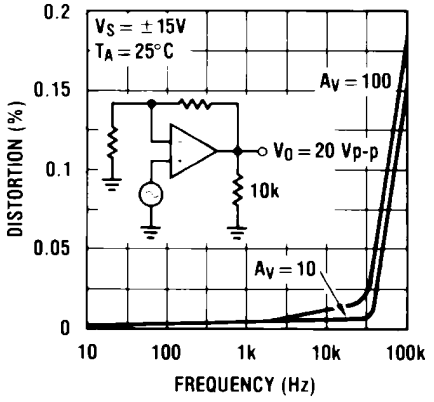
Distortion vs Frequency



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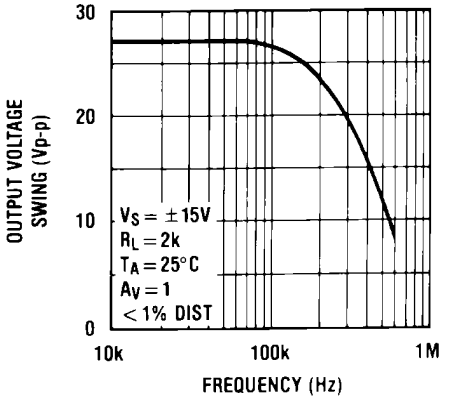
Undistorted Output Voltage Swing



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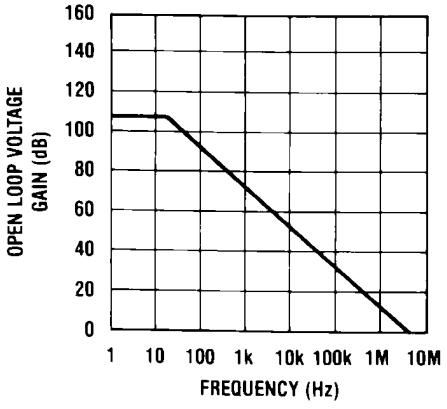
Open Loop Frequency Response



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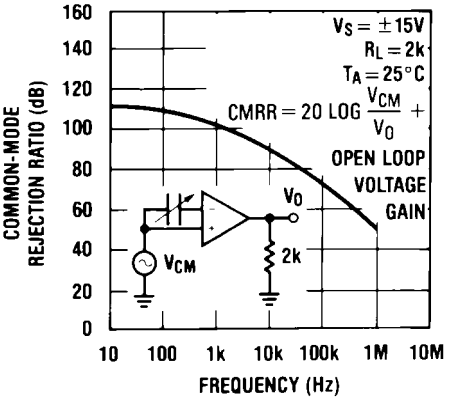
Common-Mode Rejection Ratio



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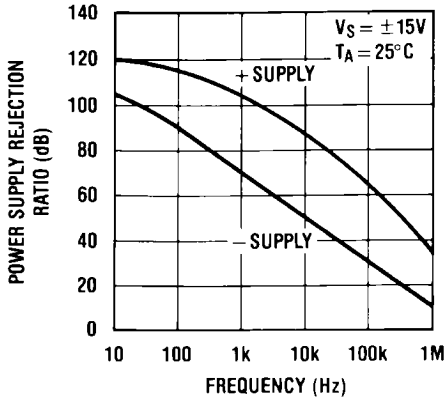
Power Supply Rejection Ratio



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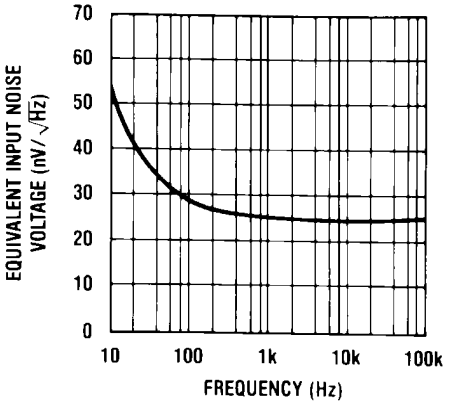
Equivalent Input Noise Voltage



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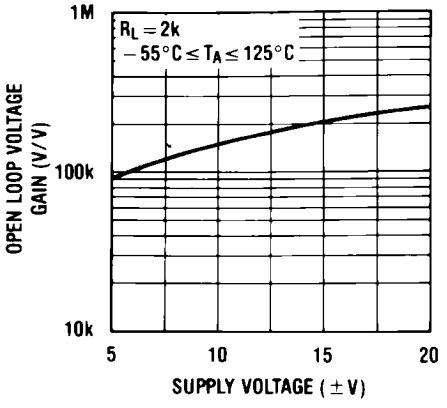
Open Loop Voltage Gain



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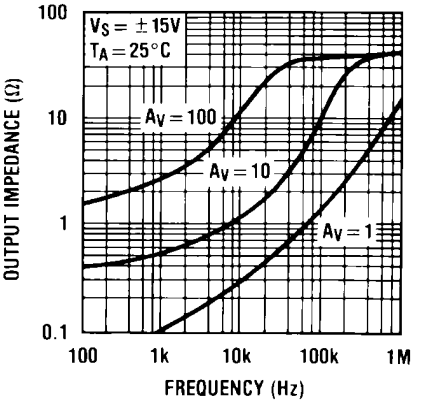
Output Impedance



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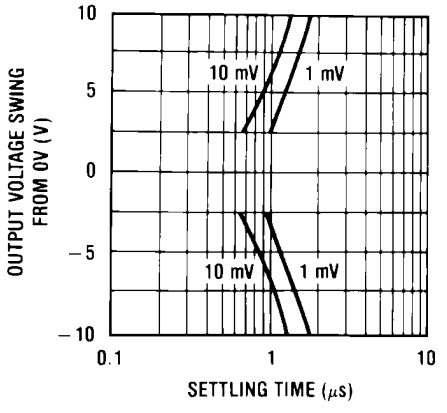
Inverter Settling Time



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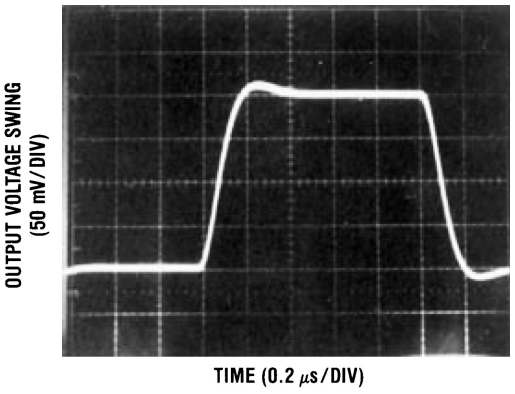
Pulse Response

R_L=2 kΩ, C_L=10 pF

Small Signal Inverting



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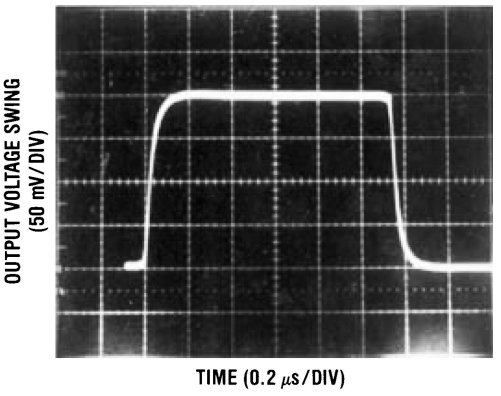
Small Signal Non-Inverting



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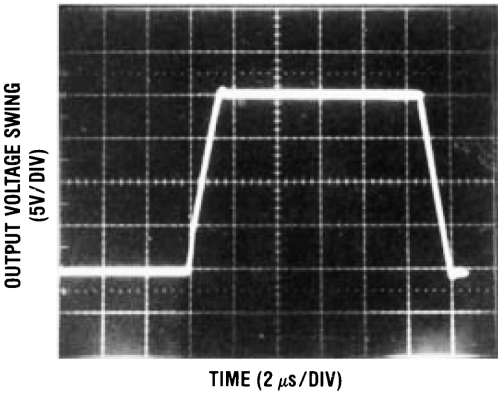
Large Signal Inverting



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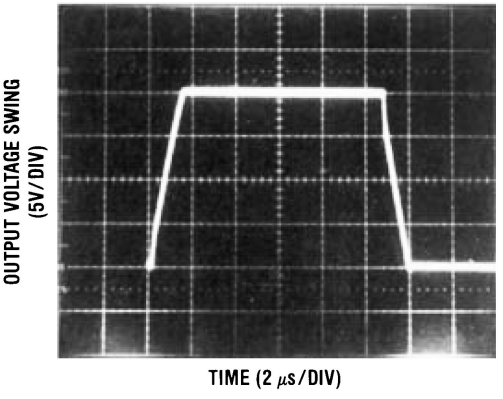
Large Signal Non-Inverting



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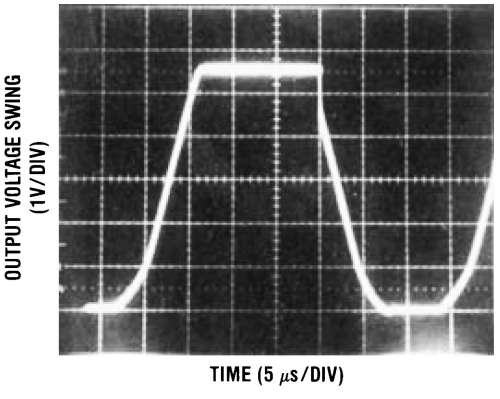
Current Limit (R_L=100Ω)



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Application Hints

The LF412 JFET input dual op amp is internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

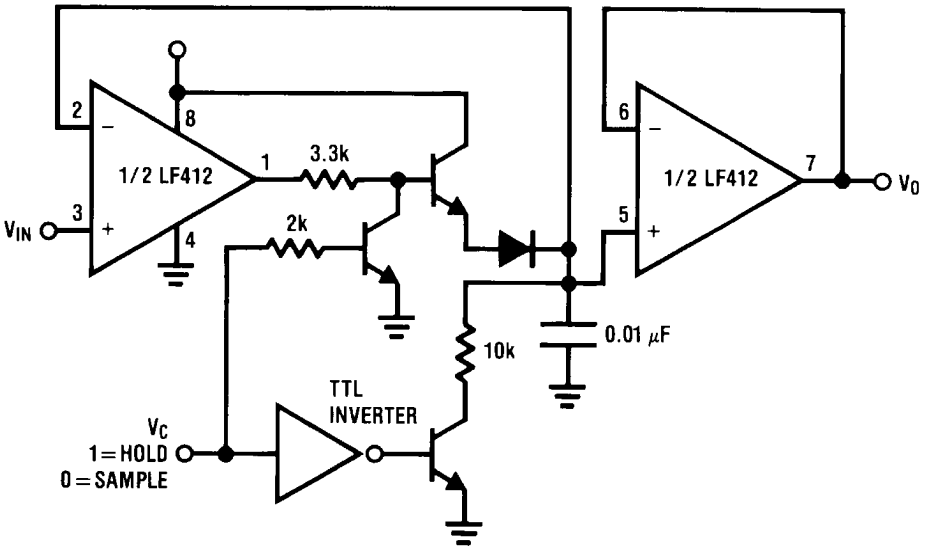
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold



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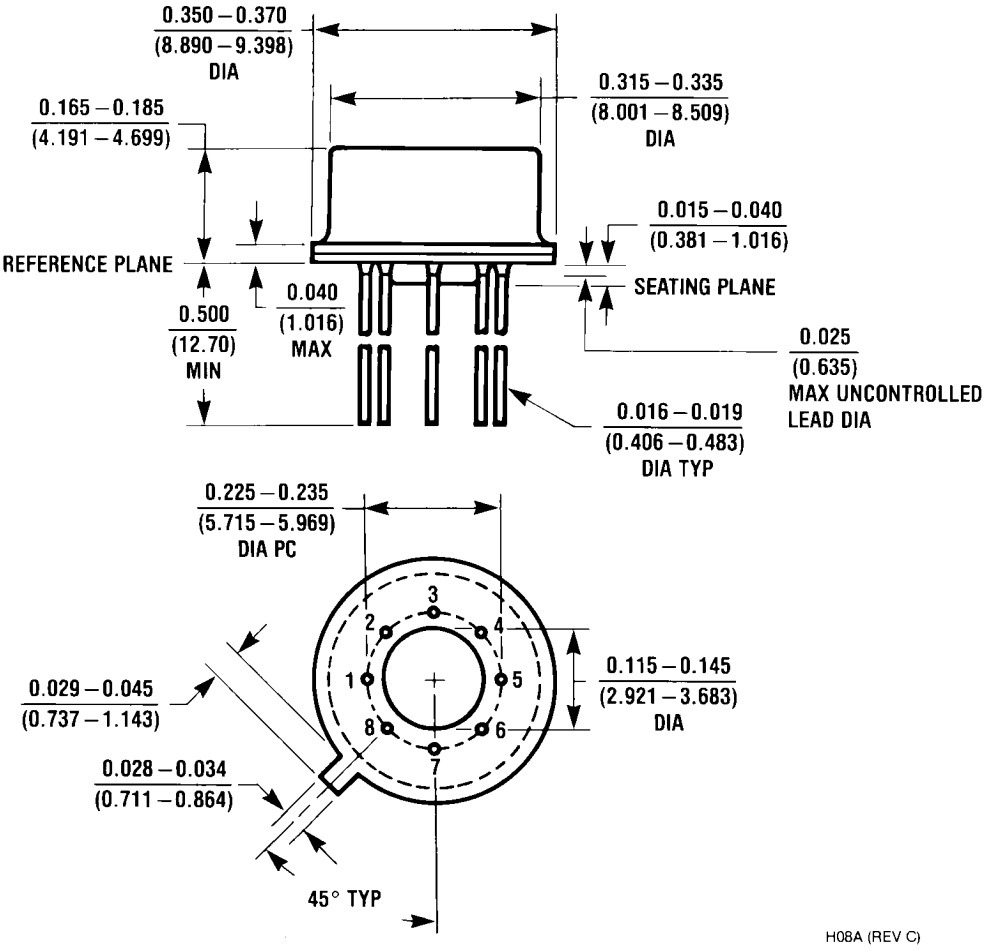
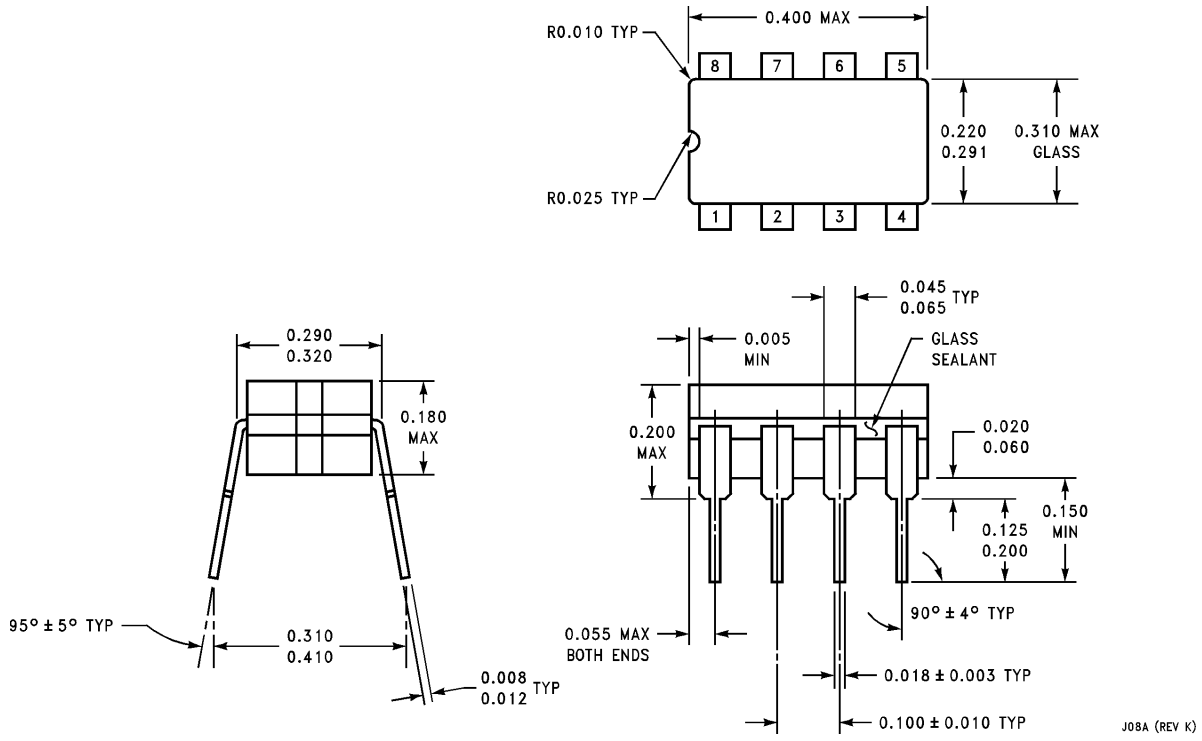
Revision History

Date Released	Revision	Section	Changes
12/08/2010	A	New Release to Corporate format	1 MDS datasheet converted into Corporate datasheet format. MNLF412-X Rev 0C1 will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08A



Dual-In-Line Package (J)
NS Package Number J08A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
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